1Gb E-die gDDR2 SDRAM

84 FBGA with Lead-Free & Halogen-Free (RoHS Compliant)

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- Target Spec	Sep. 2008	-	K.A.Kim
0.9	- Added current data(IDD) for 1000Mbps and 800Mbps speed bin - Added thermal characteristics table	Sep. 2008	-	K.A.Kim
1.0	- Added thermal characteristics values	Oct. 2008	-	K.A.Kim
1.1	- Add clock jitter spec table	Nov. 2008	-	S.H.Kim
1.2	- Correct package size	Dec. 2008	-	S.H.Kim
1.3	- Added tFAW value in timing parameter table on page12	Dec. 2008	-	S.H.Kim
1.31	- Corrected package dimension	Aug. 2009	-	S.H.Kim
1.32	- Changed layout	Feb. 2010	-	S.H.Kim
1.33	- Corrected Typo.	Apr. 2010	-	S.H.Kim

Table Of Contents

1Gb E-die gDDR2 SDRAM

1. FEATURES

- 1.8V ± 0.1V power supply for device operation
- 1.8V ± 0.1V power supply for I/O interface
- 8 Banks operation
- Posted $\overline{CAS}$
- Programmable $\overline{CAS}$ Letency : 5, 6, 7
- Programmable Additive Latency : 0, 1, 2, 3, 4, 5
- Write Latency (WL) = Read Latency (RL) -1
- Burst Legth : 4 and 8 (Interleave/nibble sequential)
  Programmable Sequential/ Interleave Burst Mode
- Bi-directional Differential Data-Strobe
  (Single-ended data-strobe is an optional feature)
- Off-chip Driver (OCD) Impedance Adjustment
- On Die Termination
- Refresh and Self Refresh
  Average Refresh Period : 7.8us at lower than T_{CASE} 85 °C,
  3.9us at 85 °C < T_{CASE} ≤ 95 °C

Lead Free & Halogen Free 84 ball FBGA(RoHS compliant)

2. ORDERING INFORMATION

Part NO.	Max Freq.	Max Data Rate	V_{DD}/V_{DDQ}	Package
K4N1G164QE-HC20	500MHz	1000Mbps/pin	1.8V ± 0.1V	84 Ball FBGA
K4N1G164QE-HC25	400MHz	800Mbps/pin		

3. GENERAL DESCRIPTION

FOR 8M x 16Bit x 8 Bank gDDR2 SDRAM

The 1Gb gDDR2 SDRAM chip is organized as 8Mbit x 16 I/O x 8banks banks device. This synchronous device achieve high speed graphic double-data-rate transfer rates of up to 500MHz for general applications. The chip is designed to comply with the following key gDDR2 SDRAM features such as posted CAS with additive latency, write latency = read latency - 1, Off-Chip Driver(OCD) impedance adjustment and On Die Termination. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and $\overline{DQS}$) in a source synchronous fashion. A thirteen bit address bus is used to convey row, column, and bank address information in a $\overline{RAS}/\overline{CAS}$ multiplexing style. For example, 1Gb(x16) device receive 13/10/3 addressing. The 1Gb gDDR2 devices are available in 84ball FBGAs(x16).

NOTE : The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

4. PINCONFIGURATION

4.1 Normal Package (Top view)

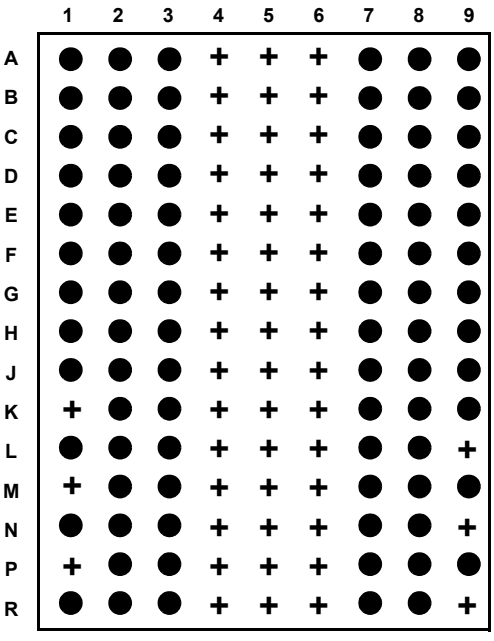
1	2	3		7	8	9
VDD	NC	VSS	A	VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM	B	UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ	C	VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11	D	DQ10	VSSQ	DQ13
VDD	NC	VSS	E	VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM	F	LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ	G	VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3	H	DQ2	VSSQ	DQ5
VDDL	VREF	VSS	J	VSSDL	CK	VDD
	CKE	$\overline{\text{WE}}$	K	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1	L	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1	M	A2	A0	VDD
VSS	A3	A5	N	A6	A4	
	A7	A9	P	A11	A8	VSS
VDD	A12	NC	R	NC	NC	

NOTE :
1. VDDL and VSSDL are power and ground for the DLL.
2. In case of only 8 DQs out of 16 DQs are used, LDQS, LDQSB and DQ0~7 must be used.

Ball Locations (x16)

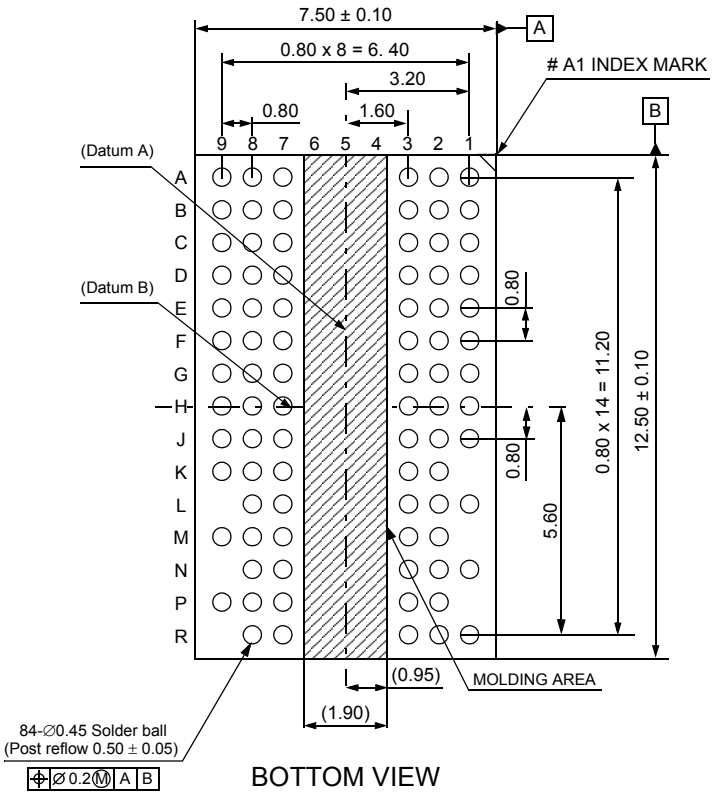
● : **Populated Ball**
+ : **Depopulated Ball**

Top View
(See the balls through the Package)

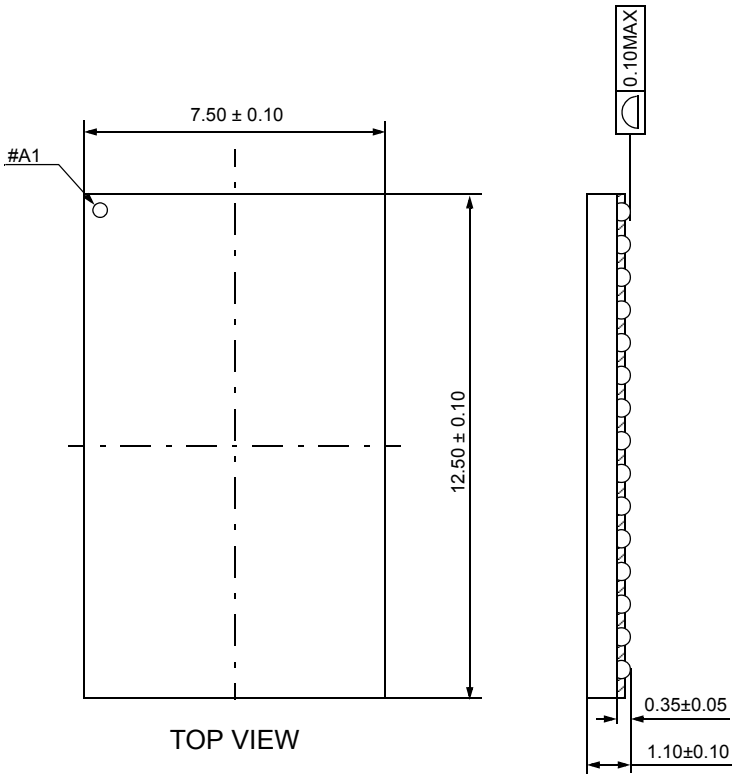


5. PACKAGE DIMENSIONS (84 Ball FBGA)

Units : Millimeters



BOTTOM VIEW



TOP VIEW

6. Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. CMD, ADD inputs are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the gDDR2 SDRAM. When enabled, ODT is only applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, UDM, and LDM signal for x16 configurations. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
(L)UDM	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
BA0 - BA2	Input	**Bank Address Inputs:** BA0,BA1 and BA2 define to which bank an Actove, Read, Write or Precharge command is being applied. BA0 also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A12	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/ Output	**Data Input/ Output:** Bi-directional data bus.
LDQS,($\overline{LDQS}$) UDQS,($\overline{UDQS}$)	Input/ Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. The data strobes LDQS and UDQS may be used in single ended mode or paired with optional complementary signals $\overline{LDQS}$ and $\overline{UDQS}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.
NC/RFU		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply**
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply**
V_{SSL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply**
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

7. ABSOLUTE MAXIMUM DC RATINGS

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	- 1.0 V ~ 2.3 V	V	1
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
VDDL	Voltage on VDDL pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.5 V ~ 2.3 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

NOTE :
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

8. AC & DC OPERATING CONDITIONS

8.1 Recommended DC Operating Conditions (SSTL - 1.8)

Symbol	Parameter	Rating			Units	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	4
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	4
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	1,2
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	3

NOTE : There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak AC noise on VREF may not exceed +/-2% VREF(DC).
3. VTT of transmitting device must track VREF of receiving device.
4. AC parameters are measured with VDD, VDDQ and VDDL tied together.

8.2 Operating Temperature Condition

Symbol	Parameter	Rating	Units	NOTE
TOPER	Operating Temperature	0 to 95	°C	1, 2, 3

NOTE :
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
2. At 0 - 85 °C, operation temperature range are the temperature which all DRAM specification will be supported.
3. At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

8.3 Input DC & AC Logic Level

Input DC Logic Level

Symbol	Parameter	Min.	Max.	Units	NOTE
V_{IH}(DC)	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V	
V_{IL}(DC)	DC input logic low	- 0.3	V_{REF} - 0.125	V	

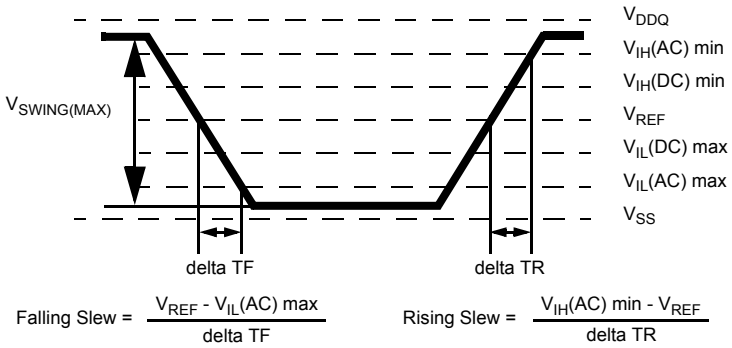
Input AC Logic Level

Symbol	Parameter	Min.	Max.	Units	NOTE
V_{IH}(AC)	AC input logic high	V_{REF} + 0.250	-	V	
V_{IL}(AC)	AC input logic low	-	V_{REF} - 0.250	V	

8.4 AC Input Test Conditions

Symbol	Condition	Value	Units	NOTE
V_{REF}	Input reference voltage	0.5 * V_{DDQ}	V	1
$V_{SWING(MAX)}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum slew rate	1.0	V/ns	2, 3

NOTE :
1. Input waveform timing is referenced to the input signal crossing through the $V_{IH/IL}$(AC) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from V_{REF} to V_{IH}(AC) min for rising edges and the range from V_{REF} to V_{IL}(AC) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from V_{IL}(AC) to V_{IH}(AC) on the positive transitions and V_{IH}(AC) to V_{IL}(AC) on the negative transitions.

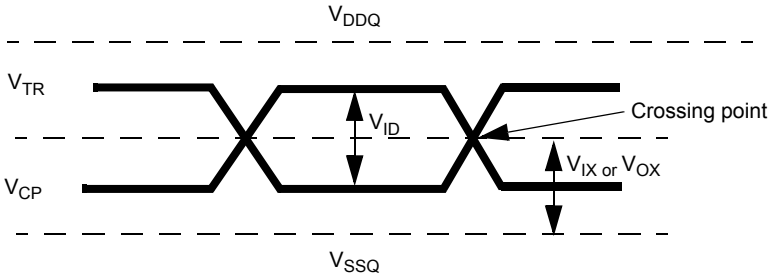


< AC Input Test Signal Waveform >

8.5 Differential input AC logic Level

Symbol	Parameter	Min.	Max.	Units	NOTE
V_{ID}(AC)	AC differential input voltage	0.5	V_{DDQ} + 0.6	V	1
V_{IX}(AC)	AC differential cross point voltage	0.5 * V_{DDQ} - 0.175	0.5 * V_{DDQ} + 0.175	V	2

NOTE :
1. VID(AC) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CK, DQS, LDQS or UDQS) and VCP is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to VIH(AC) - VIL(AC).
2. The typical value of VIX(AC) is expected to be about 0.5 * VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ . VIX(AC) indicates the voltage at which differential input signals must cross.



< Differential signal levels >

8.6 Differential AC output parameters

Symbol	Parameter	Min.	Max.	Units	NOTE
V_{OX}(AC)	AC differential cross point voltage	0.5 * V_{DDQ} - 0.125	0.5 * V_{DDQ} + 0.125	V	1

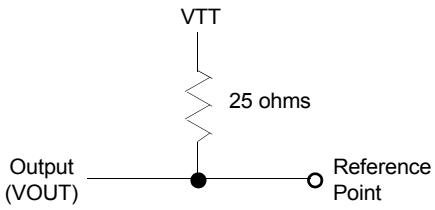
NOTE :
1. The typical value of VOX(AC) is expected to be about 0.5 * VDDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ . VOX(AC) indicates the voltage at which differential output signals must cross.

8.7 OCD default characteristics

Description	Parameter	Min	Nom	Max	Unit	NOTE
Output impedance		Normal 18ohms See full strength default driver characteristics			ohms	1,2
Output impedance step size for OCD calibration		0		1.5	ohms	6
Pull-up and pull-down mismatch		0		4	ohms	1,2,3
Output slew rate	Sout	1.5		5	V/ns	1,4,5,6,7,8

NOTE :
1. Absolute Specifications ($0°C \le T_{CASE} \le +95°C$; V_{DD}/V_{DDQ} = 1.8V ± 0.1V)
2. Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.
3. Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.
4. Slew rate measured from V_{IL}(AC) to V_{IH}(AC).
5. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
6. This represents the step size when the OCD is near 18 ohms at nominal conditions across all process and represents only the DRAM uncertainty.

Output slew rate load :



7. DRAM output slew rate specification applies to 400MHz and 500MHz speed bins.
8. Timing skew due to DRAM output slew rate mis-match between DQS / $\overline{DQS}$ and associated DQs is included in tDQSQ and tQHS specification.

8.8 DC characteristics

(Recommended operating conditions unless otherwise noted, 0°C ≤ Tc ≤85°C)

Parameter	Symbol	Test Condition		Version		Unit
				-20	-25	
Operating Current (One Bank Active)	ICC1	Burst Length=4 tRC ≥ tRC(min). IOL=0mA, tCC= tCC(min). DQ,DM,DQS inputs changing twice per clock cycle. Address and control inputs changing once per clock cycle		80	75	mA
Precharge Standby Current in Power-down mode	ICC2P	CKE ≤ VIL(max), tCC= tCC(min)		15	10	mA
Precharge Standby Current in Non Power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min),tCC= tCC(min) Address and control inputs changing once per clock cycle		32	32	mA
Active Standby Current power-down mode	ICC3P	CKE ≤ VIL(max), tCC= tCC(min)	Fast PDN Exit MRS(12) = 0mA	30	28	mA
			Slow PDN Exit MRS(12) = 1mA	15	15	
Active Standby Current in in Non Power-down mode	ICC3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCC= tCC(min) DQ,DM,DQS inputs changing twice per clock cycle. Address and control inputs changing once per clock cycle		43	40	mA
Operating Current (Burst Mode)	ICC4	IOL=0mA ,tCC= tCC(min), Page Burst, All Banks activated. DQ,DM,DQS inputs changing twice per clock cycle. Address and control inputs changing once per clock.		160	125	mA
Refresh Current	ICC5	tRC≥ tRFC		116	115	mA
Self Refresh Current	ICC6	CKE ≤ 0.2V		15	10	mA
Operating Current (4Bank interleaving)	ICC7	Burst Length=4 tRC ≥ tRC(min). IOL=0mA, tCC= tCC(min). DQ,DM,DQS inputs changing twice per clock cycle. Address and control inputs changing once per clock cycle		215	200	mA

NOTE :
1. Measured with outputs open and ODT off

8.9 Input/Output capacitance

Parameter	Symbol	-20		- 25		Units
		Min	Max	Min	Max	
Input capacitance, CK and $\overline{CK}$	CCK	1.0	2.0	1.0	2.0	pF
Input capacitance delta, CK and $\overline{CK}$	CDCK	x	0.25	x	0.25	pF
Input capacitance, all other input-only pins	CI	1.0	2.0	1.0	2.0	pF
Input capacitance delta, all other input-only pins	CDI	x	0.25	x	0.25	pF
Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	CIO	2.5	3.5	2.5	3.5	pF
Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	CDIO	x	0.5	x	0.5	pF

9. Electrical Characteristics & AC Timing

($0\ °C \leq T_{CASE} \leq 95\ °C$; $V_{DD}/V_{DDQ} = 1.8V \pm 0.1V$)

9.1 Refresh Parameters

Parameter	Symbol		1Gb	Units
Refresh to active/Refresh command time	tRFC		127.5	ns
Average periodic refresh interval	tREFI	$0\ °C \leq T_{CASE} \leq 85°C$	7.8	µs
		$85\ °C < T_{CASE} \leq 95°C$	3.9	µs

9.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS

SPEED	-20	-25	Units
Bin (CL-tRCD-tRP)	7-7-7	6-6-6	
Parameter	**min**	**min**	
CAS LATENCY	7	6	tCK
tCK	2.0	2.5	ns
tRCD	7	6	tCK
tRP	7	6	tCK
tRC	28	24	tCK
tRAS	21	18	tCK

9.3 Thermal Characteristics(500/400Mhz at VDD=1.8V ± 0.1V, VDDQ=1.8V ± 0.1V)

Parameter	Description	Value	Units	NOTE
Theta_JA	Thermal resistance junction to ambient	33.7	°C/W	Thermal measurement : 1,2,3,5
Max_Tj	Maximum operating junction temperature	38.8 37.9	°C	500Mhz@ Max1.9V : 4(Pd=0.41W) 400Mhz@ Max1.9V : 4(Pd=0.38W)
Max_Tc	Maximum operating case temperature	36.3 35.5	°C	500Mhz@ Max 1.9V : 4 400Mhz@ Max 1.9V : 4
Theta_Jc	Thermal resistance junction to case	6.25	°C/W	Thermal measurement : 1, 6
Theta_JB	Thermal resistance junction to board	16.7	°C/W	Thermal simulation : 1, 2, 6

NOTE

1.Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standard.
2. Theta_JA and Theta_JB must be measured with the high effective thermal conductivity test board defined in JESD51-7
3. Airflow information must be documented for Theta JA.
4. Max_Tj and Max_Tc are documented for normal operation in this table. These are not intended to reflect reliablility limits.
5. Theta_JA should only be used for comparing the thermal performance of single packages and not for system related junction.
6. Theta_JB and Theta_JC are derived through a package thermal simulation and measurement.

9.4 Timing Parameters by Speed Grade

(Refer to notes for informations related to this table at the bottom)

Parameter	Symbol	- 20		- 25		Units	NOTE
		min	max	min	max		
DQ output access time from CK/$\overline{CK}$	tAC	-350	+350	-400	+400	ps	
DQS output access time from CK/$\overline{CK}$	tDQSCK	-300	+300	-350	+350	ps	
CK high-level width	tCH	0.45	0.55	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	0.45	0.55	tCK	
CK half period	tHP	min(tCL, tCH)	-	min(tCL, tCH)	-	ps	20,21
Clock cycle time, CL= x	tCK	2.0	8.0	2.5	8.0	ns	24
DQ and DM input hold time	tDH	125	-	125	-	ps	15,16, 17
DQ and DM input setup time	tDS	50	-	50	-	ps	15,16, 17
Control & Address input pulse width for each input	tIPW	0.6	-	0.6	-	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	-	0.35	-	tCK	
Data-out high-impedance time from CK/$\overline{CK}$	tHZ	-	tAC max	-	tAC max	ps	
DQS low-impedance time from CK/$\overline{CK}$	tLZ (DQS)	tAC min	tAC max	tAC min	tAC max	ps	27
DQ low-impedance time from CK/$\overline{CK}$	tLZ(DQ)	2*tAC min	tAC max	2*tAC min	tAC max	ps	27
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	280	-	280	ps	22
DQ hold skew factor	tQHS	-	380	-	380	ps	21
DQ/DQS output hold time from DQS	tQH	tHP - tQHS	-	tHP - tQHS	-	ps	
Write command to first DQS latching transition	tDQSS	WL -0.25	WL +0.25	WL -0.25	WL +0.25	tCK	
DQS input high pulse width	tDQSH	0.35	-	0.35	-	tCK	
DQS input low pulse width	tDQSL	0.35	-	0.35	-	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	0.2	-	tCK	
Mode register set command cycle time	tMRD	2	-	2	-	tCK	
Write postamble	tWPST	0.4	0.6	0.4	0.6	tCK	19
Write preamble	tWPRE	0.35	-	0.35	-	tCK	
Address and control input hold time	tIH	200	-	250	-	ps	14,16, 18
Address and control input setup time	tIS	150	-	175	-	ps	14,16, 18
Read preamble	tRPRE	0.9	1.1	0.9	1.1	tCK	28
Read postamble	tRPST	0.4	0.6	0.4	0.6	tCK	28
Active to active command period	tRRD	7.5	-	7.5	-	ns	12

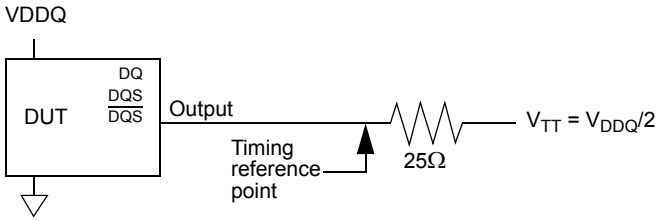
Parameter	Symbol	- 20		-25		Units	NOTE
		min	max	min	max		
Four Activate Window for 1KB page size products	tFAW	35	-	35	-	ns	
Four Activate Window for 2KB page size products	tFAW	45	-	45	-	ns	
$\overline{CAS}$ to $\overline{CAS}$ command delay	tCCD	2	-	2	-	tCK	
Write recovery time	tWR	6	-	6	-	tCK	
Auto precharge write recovery + precharge time	tDAL	tWR +tRP	-	tWR +tRP	-	tCK	23
Internal write to read command delay	tWTR	4	-	3	-	tCK	
Internal read to precharge command delay	tRTP	4	-	3	-	tCK	11
Exit self refresh to a non-read command	tXSNR	tRFC + 10	-	tRFC + 10	-	ns	
Exit self refresh to a read command	tXSRD	200	-	200	-	tCK	
Exit precharge power down to any non-read command	tXP	2	-	2	-	tCK	
Exit active power down to read command	tXARD	2	-	2	-	tCK	9
Exit active power down to read command (Slow exit, Lower power)	tXARDS	6 - AL	-	6 - AL	-	tCK	9, 10
CKE minimum pulse width (high and low pulse width)	tCKE	3	-	3	-	tCK	
ODT turn-on delay	tAOND	2	2	2	2	tCK	
ODT turn-on	tAON	tAC (min)	tAC(max)+0.7	tAC (min)	tAC(max)+0.7	ns	13, 25
ODT turn-on(Power-Down mode)	tAONPD	tAC (min)+2	2tCK +tAC (max)+1	tAC (min)+2	2tCK +tAC (max)+1	ns	
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK	
ODT turn-off	tAOF	tAC (min)	tAC(max)+ 0.6	tAC (min)	tAC(max)+ 0.6	ns	26
ODT turn-off (Power-Down mode)	tAOFPD	tAC (min)+2	2.5tCK+ tAC(max)+1	tAC (min)+2	2.5tCK+ tAC(max)+1	ns	
ODT to power down entry latency	tANPD	3	-	3	-	tCK	
ODT power down exit latency	tAXPD	8	-	8	-	tCK	
OCD drive mode output delay	tOIT	0	12	0	12	ns	
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK +tIH	-	tIS+tCK +tIH	-	ns	24

NOTE : General notes, which may apply for all AC parameters

1. Slew Rate Measurement Levels
   a. Output slew rate for falling and rising edges is measured between VTT - 250 mV and VTT + 250 mV for single ended signals. For differential signals (e.g. DQS - $\overline{DQS}$) output slew rate is measured between DQS - $\overline{DQS}$ = -500 mV and DQS - $\overline{DQS}$ = +500mV. Output slew rate is guaranteed by design, but is not necessarily tested on each device.
   b. Input slew rate for single ended signals is measured from dc-level to ac-level: from VREF - 125 mV to VREF + 250 mV for rising edges and from VREF + 125 mV and VREF - 250 mV for falling edges. For differential signals (e.g. CK - $\overline{CK}$) slew rate for rising edges is measured from CK - $\overline{CK}$ = -250 mV to CK - $\overline{CK}$ = +500 mV (250mV to -500 mV for falling egdes).
   c. VID is the magnitude of the difference between the input voltage on CK and the input voltage on $\overline{CK}$, or between DQS and $\overline{DQS}$ for differential strobe.

2. gDDR2 SDRAM AC timing reference load

Following figure represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

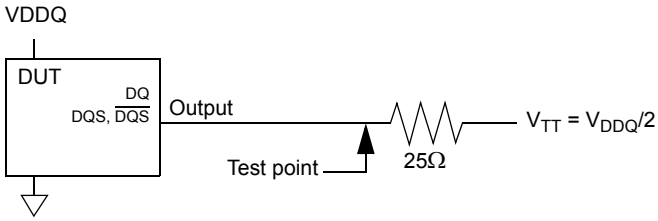


<AC Timing Reference Load>

The output timing reference voltage level for single ended signals is the crosspoint with VTT. The output timing reference voltage level for differential signals is the crosspoint of the true (e.g. DQS) and the complement (e.g. DQS) signal.

3. gDDR2 SDRAM output slew rate test load

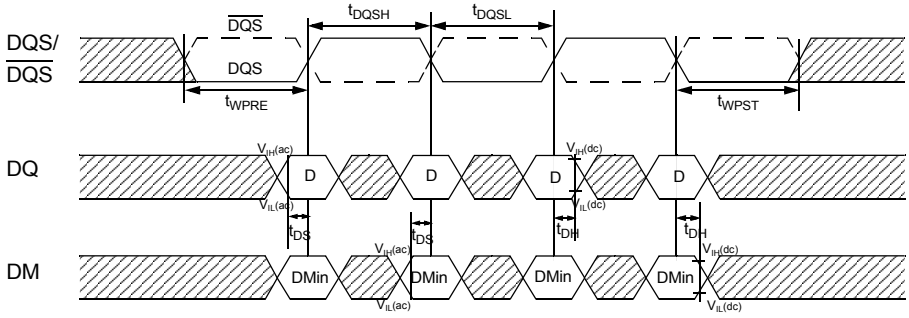
Output slew rate is characterized under the test conditions as shown in the following figure.



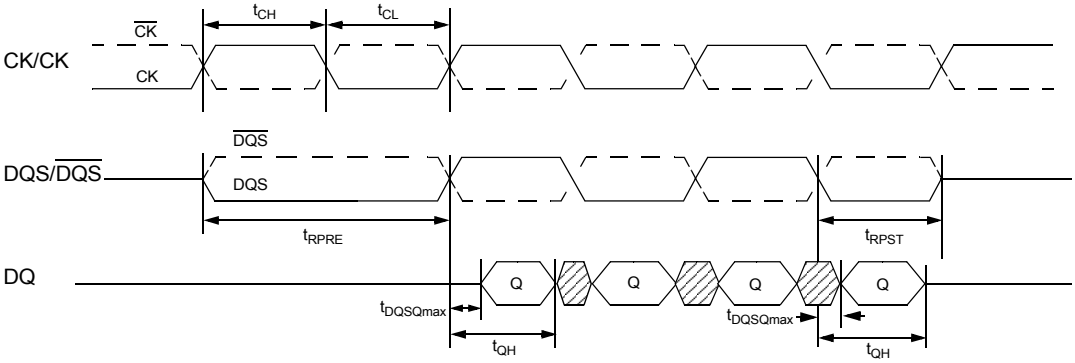
<Slew Rate Test Load>

4. Differential data strobe

gDDR2 SDRAM pin timings are specified for either single ended mode or differential mode depending on the setting of the EMRS “Enable DQS” mode bit; timing advantages of differential mode are realized in system design. The method by which the gDDR2 SDRAM pin timings are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF. In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, DQS. This distinction in timing methods is guaranteed by design and characterization. Note that when differential data strobe mode is disabled via the EMRS, the complementary pin, DQS, must be tied externally to VSS through a 20 ohm to 10 K ohm resisor to insure proper operation.



<Data input(write) timing>



<Data output(read) timing>

5. AC timings are for linear signal transitions.

6. These parameters guarantee device behavior, but they are not necessarily tested on each device.
They may be guaranteed by device design or tester correlation.

7. All voltages are referenced to VSS.

8. Tests for AC timing, IDD, and electrical (AC and DC) characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.

: Specific Notes for dedicated AC parameters

9. User can choose which active power down exit timing to use via MRS(bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.

10. AL = Additive Latency

11. This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing the tRTP and tRAS(min) have been satisfied.

12. A minimum of two clocks (2 * tCK) is required irrespective of operating frequency

13. Timings are guaranteed with command/address input slew rate of 1.0 V/ns.

14. These parameters guarantee device behavior, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.

15. Timings are guaranteed with data, mask, and (DQS in singled ended mode) input slew rate of 1.0 V/ns.

16. Timings are guaranteed with CK/$\overline{CK}$ differential slew rate of 2.0 V/ns. Timings are guaranteed for DQS signals with a differential slew rate of 2.0 V/ns in differential strobe mode and a slew rate of 1V/ns in single ended mode.

17. tDS and tDH (data setup and hold) derating
1) Input waveform timing is referenced from the input signal crossing at the V_{IH}(AC) level for a rising signal and V_{IL}(AC) for a falling signal applied to the device under test.
2) Input waveform timing is referenced from the input signal crossing at the V_{IH}(DC) level for a rising signal and V_{IL}(DC) for a falling signal applied to the device under test.

ΔtDS, ΔtDH Derating Values (ALL units in 'ps', Note 1 applies to entire Table)

		DQS,$\overline{DQS}$ Differential Slew Rate																	
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns		0.8V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	100	45	100	45	100	45	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	67	21	67	21	67	21	79	33	-	-	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	12	12	24	24	-	-	-	-	-	-	-	-
	0.9	-	-	-5	-14	-5	-14	7	-2	19	10	31	22	-	-	-	-	-	-
	0.8	-	-	-	-	-13	-31	-1	-19	11	-7	23	5	35	17	-	-	-	-
	0.7	-	-	-	-	-	-	-10	-42	2	-30	14	-18	26	-6	38	6	-	-
	0.6	-	-	-	-	-	-	-	-	-10	-59	2	-47	14	-35	26	-23	38	-11
	0.5	-	-	-	-	-	-	-	-	-	-	-24	-89	-12	-77	0	-65	12	-53
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-52	-140	-40	-128	-28	-116

For all input signals the total tDS (setup time) and tDH(hold time) required is calculated by adding the datasheet tDS(base) and tDH(base) value to the delta tDS and delta tDH derating value respectively. Example : tDS (total setup time) = tDS(base) + delta tDS.

ΔtDS1, ΔtDH1 Derating Values for gDDR2-700Mbps (All units in 'ps'; the note applies to the entire table)

		DQS Single-ended Slew Rate																	
		2.0 V/ns		1.5 V/ns		1.0 V/ns		0.9 V/ns		0.8 V/ns		0.7 V/ns		0.6 V/ns		0.5 V/ns		0.4 V/ns	
		ΔtDS 1	ΔtDH 1	ΔtDS 1	ΔtDH 1	ΔtDS 1	ΔtDH 1	ΔtDS 1	ΔtDH 1	ΔtDS 1	ΔtDH 1	ΔtDS 1	ΔtDH 1	ΔtDS 1	ΔtDH 1	ΔtDS 1	ΔtDH 1	ΔtDS 1	ΔtDH 1
DQ Slew rate V/ns	2.0	188	188	167	146	125	63	-	-	-	-	-	-	-	-	-	-	-	-
	1.5	146	167	125	125	83	42	81	43	-	-	-	-	-	-	-	-	-	-
	1.0	63	125	42	83	0	0	-2	1	-7	-13	-	-	-	-	-	-	-	-
	0.9	-	-	31	69	-11	-14	-13	-13	-18	-27	-29	-45	-	-	-	-	-	-
	0.8	-	-	-	-	-25	-31	-27	-30	-32	-44	-43	-62	-60	-86	-	-	-	-
	0.7	-	-	-	-	-	-	-45	-53	-50	-67	-61	-85	-78	-109	-108	-152	-	-
	0.6	-	-	-	-	-	-	-	-	-74	-96	-85	-114	-102	-138	-138	-181	-183	-246
	0.5	-	-	-	-	-	-	-	-	-	-	-128	-156	-145	-180	-175	-223	-226	-288
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-210	-243	-240	-286	-291	-351

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ΔtDS and ΔtDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.

18. tIS and tIH (input setup and hold) derating

1) Input waveform timing is referenced from the input signal crossing at the V_{IH}(AC) level for a rising signal and V_{IL}(AC) for a falling signal applied to the device under test.

2) Input waveform timing is referenced from the input signal crossing at the V_{IH}(DC) level for a rising signal and V_{IL}(DC) for a falling signal applied to the device under test.

		ΔtIS and ΔtIH Derating Values						Units	NOTE
		CK,$\overline{CK}$ Differential Slew Rate							
		2.0 V/ns		1.5 V/ns		1.0 V/ns			
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH		
Command /Adress Slew rate(V/ns)	4.0	+150	+94	+180	+124	+210	+154	ps	1
	3.5	+143	+89	+173	+119	+203	+149	ps	1
	3.0	+133	+83	+163	+113	+193	+143	ps	1
	2.5	+120	+75	+150	+105	+180	+135	ps	1
	2.0	+100	+45	+130	+75	+160	+105	ps	1
	1.5	+67	+21	+97	+51	+127	+81	ps	1
	1.0	0	0	+30	+30	+60	+60	ps	1
	0.9	-5	-14	+25	+16	+55	+46	ps	1
	0.8	-13	-31	+17	-1	+47	29	ps	1
	0.7	-22	-54	+8	-24	+38	+6	ps	1
	0.6	-34	-83	-4	-53	+26	-23	ps	1
	0.5	-60	-125	-30	-95	0	-65	ps	1
	0.4	-100	-188	-70	-158	-40	-128	ps	1
	0.3	-168	-292	-138	-262	-108	-232	ps	1
	0.25	-200	-375	-170	-345	-140	-315	ps	1
	0.2	-325	-500	-295	-470	-265	-440	ps	1
	0.15	-517	-708	-487	-678	-457	-648	ps	1
	0.1	-1000	-1125	-970	-1095	-940	-1065		

19. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.

20. MIN (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH). For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.

21. tQH = tHP – tQHS, where:
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL).
tQHS accounts for:
1) The pulse duration distortion of on-chip clock circuits; and
2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

22. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{\text{DQS}}$ and associated DQ in any given cycle.

23. tDAL = (nWR) + (tRP/tCK) :
For each of the terms above, if not already an integer, round to the next highest integer. tCK refers to the application clock period. nWR refers to the tWR parameter stored in the MRS.
Example: For gDDR800 at t CK = 2.5 ns with tWR programmed to 6 clocks. tDAL = 6 + (15 ns / 2.5 ns) clocks =6 +(6)clocks=12clocks.

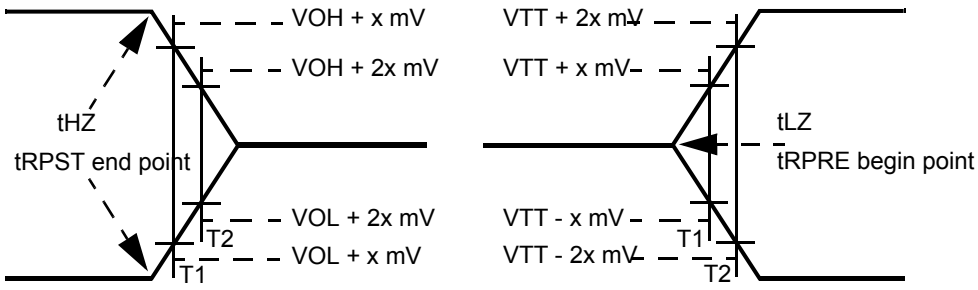
24. The clock frequency is allowed to change during self–refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in gDDR2 device operation

25. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

26. ODT turn off time min is when the device starts to turn off ODT resistance.
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

27. tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (tHZ), or begins driving (tLZ) . Following figure shows a method to calculate the point when device is no longer driving (tHZ), or begins driving (tLZ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

28. tRPST end point and tRPRE begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (tRPST), or begins driving (tRPRE). Following figure shows a method to calculate these points when the device is no longer driving (tRPST), or begins driving (tRPRE) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. These notes are referenced to the “Timing parameters by speed grade” tables for gDDR2-350/400/450MHz and gDDR2-500MHz.



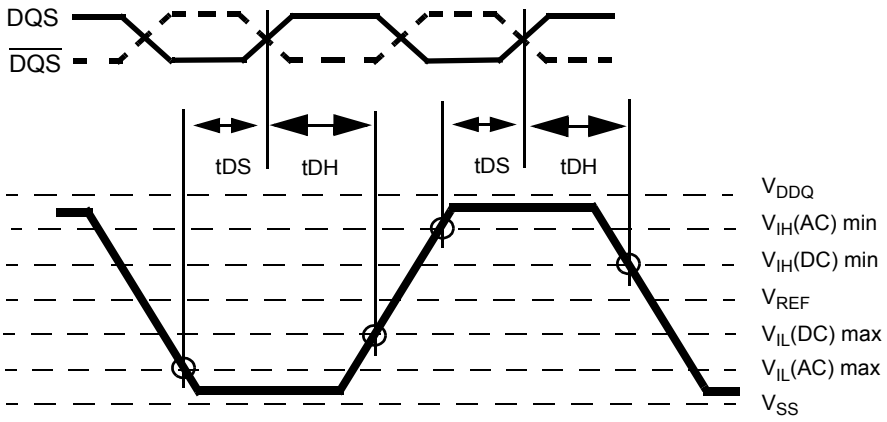
tHZ,tRPST end point = 2*T1-T2 tLZ,tRPRE begin point = 2*T1-T2

<Test method for tLZ, tHZ, tRPRE and tRPST>

29. Input waveform timing with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH(ac)}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL(ac)}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test.

30. Input waveform timing with differential data strobe enabled MR[bit10]=0, is referenced from the input signal crossing at the $V_{IH(dc)}$ level to the differential data strobe crosspoint for a rising signal and $V_{IL(dc)}$ to the differential data strobe crosspoint for a falling signal applied to the device under test.

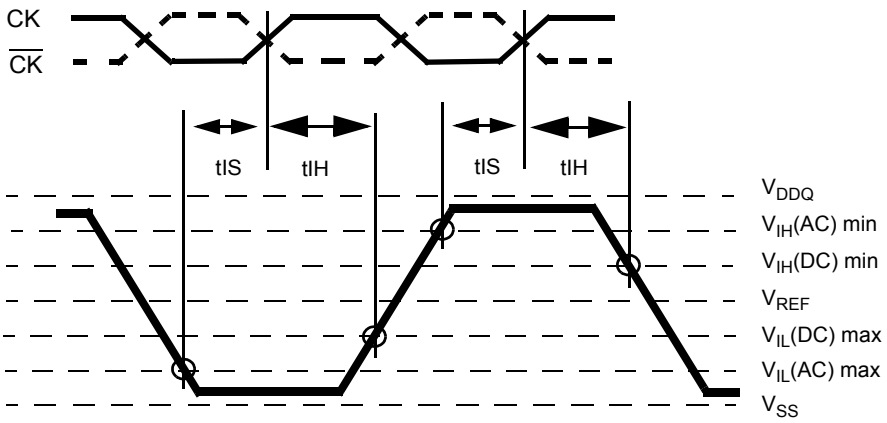
Differential Input waveform timing



<Data setup/hold timing>

31. Input waveform timing is referenced from the input signal crossing at the VIH(ac) level for a rising signal and VIL(ac) for a falling signal applied to the device under test.

32. Input waveform timing is referenced from the input signal crossing at the VIL(dc) level for a rising signal and VIH(dc) for a falling signal applied to the device under test.



<Input setup/hold timing>

33. tWTR is at lease two clocks (2 * tCK) independent of operation frequency.

34. Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the VIH(ac) level to the single-ended data strobe crossing VIH/L(dc) at the start of its transition for a rising signal, and from the input signal crossing at the VIL(ac) level to the single-ended data strobe crossing VIH/L(dc) at the start of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

35. Input waveform timing with single-ended data strobe enabled MR[bit10] = 1, is referenced from the input signal crossing at the VIH(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a rising signal, and from the input signal crossing at the VIL(dc) level to the single-ended data strobe crossing VIH/L(ac) at the end of its transition for a falling signal applied to the device under test. The DQS signal must be monotonic between Vil(dc)max and Vih(dc)min.

36. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registeration. Thus, after any cKE transition, CKE may not transitioin from its valid level during the time period of tIS + 2*tCK + tIH.

37. Input clock jitter spec parameter. These parameters and the ones in the table below are referred to as 'input clock jitter spec parameters' and these parameters apply to and 400MHz and 500MHz. The jitter specified is a random jitter meeting a Gaussian distribution.

Parameter	Symbol	-25		-20		units
		Min	Max	Min	Max	
Clock period jitter	tJIT(per)	-100	100	-80	80	ps
Clock period jitter during DLL locking period	tJIT(per,lck)	-80	80	-64	64	ps
Cycle to cycle clock period jitter	tJIT(cc)	-200	200	-160	160	ps
Cycle to cycle clock period jitter during DLL locking period	tJIT(cc,lck)	-160	160	-128	128	ps
Cumulative error across 2 cycles	tERR(2per)	-150	150	-120	120	ps
Cumulative error across 3 cycles	tERR(3per)	-175	175	-140	140	ps
Cumulative error across 4 cycles	tERR(4per)	-200	200	-160	160	ps
Cumulative error across 5 cycles	tERR(5per)	-200	200	-160	160	ps
Cumulative error across n cycles, n = 6 ... 10, inclusive	tERR(6-10per)	-300	300	-240	240	ps
Cumulative error across n cycles, n = 11 ... 50, inclusive	tERR(11-50per)	-450	450	-360	360	ps
Duty cycle jitter	tJIT(duty)	-100	100	-80	80	ps

Definitions :

- tCK(avg)
  tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) /N$$

where $N = 200$

- tCH(avg) and tCL(avg)
  tCH(avg) is defined as the average HIGH pulse width, as calculated across any consecutive 200 HIGH pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) /(N \times tCK(avg))$$

where $N = 200$

- tCL(avg) is defined as the average LOW pulse width, as calculated across any consecutive 200 LOW pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) /(N \times tCK(avg))$$

where $N = 200$

- tJIT(duty)
  tJIT(duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH(avg). tCL jitter is the largest deviation of any single tCL from tCL(avg).

  tJIT(duty) = Min/max of {tJIT(CH), tJIT(CL)}
  where,
  tJIT(CH) = {tCHi- tCH(avg) where i=1 to 200}
  tJIT(CL) = {tCLi- tCL(avg) where i=1 to 200}

- tJIT(per), tJIT(per,lck)
  tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg).
  tJIT(per) = Min/max of {tCKi- tCK(avg) where i=1 to 200}

  tJIT(per) defines the single period jitter when the DLL is already locked.
  tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
  tJIT(per) and tJIT(per,lck) are not guaranteed through final production testing.

- tJIT(cc), tJIT(cc,lck)
  tJIT(cc) is defined as the difference in clock period between two consecutive clock cycles : tJIT(cc) = Max of $|tCK_{i+1} - tCKi|$
  tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
  tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
  tJIT(cc) and tJIT(cc,lck) are not guaranteed through final production testing.

- tERR(2per), tERR (3per), tERR (4per), tERR (5per), tERR (6-10per) and tERR (11-50per)
  tERR is defined as the cumulative error across multiple consecutive cycles from tCK(avg).

$$tERR(nper) = \left(\sum_{j=1}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

where
$n = 2$ *for* tERR(2per)
$n = 3$ *for* tERR(3per)
$n = 4$ *for* tERR(4per)
$n = 5$ *for* tERR(5per)
$6 \le n \le 10$ *for* tERR(6-10per)
$11 \le n \le 50$ *for* tERR(11-50per)