128Mb I-die SDRAM Specification

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Rev. 1.1 May 2006

Revision History

Revision	Month	Year	History
1.0	October	2005	- Final spec release.
1.1	May	2006	- Added 5ns speed bin for x16

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8M x 4Bit x 4 Banks / 4M x 8Bit x 4 Banks / 2M x 16Bit x 4 Banks SDRAM

FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- DQM (x4,x8) & L(U)DQM (x16) for masking
- Auto & self refresh
- 64ms refresh period (4K Cycle)
- RoHS compliant for Pb-free Package

GENERAL DESCRIPTION

The K4S280432I / K4S280832I / K4S281632I is 134,217,728 bits synchronous high data rate Dynamic RAM organized as 4 x 8,388,608 words by 4 bits / 4 x 4,194,304 words by 8 bits / 4 x 2,097,152 words by 16 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Ordering Information

Part No.	Orgainization	Max Freq.	Interface	Package
K4S280432I-T(U)C/L75	32Mb x 4	133MHz (CL=3)	LVTTL	54pin TSOP(II)
K4S280832I-T(U)C/L75	16Mb x 8	133MHz (CL=3)		
K4S281632I-T(U)C/L50	8Mb x 16	200MHz (CL=3)		
K4S281632I-T(U)C/L60	8Mb x 16	166MHz (CL=3)		
K4S281632I-T(U)C/L75	8Mb x 16	133MHz (CL=3)		

Organization	Row Address	Column Address
32Mx4	A0~A11	A0-A9, A11
16Mx8	A0~A11	A0-A9
8Mx16	A0~A11	A0-A8

Row & Column address configuration

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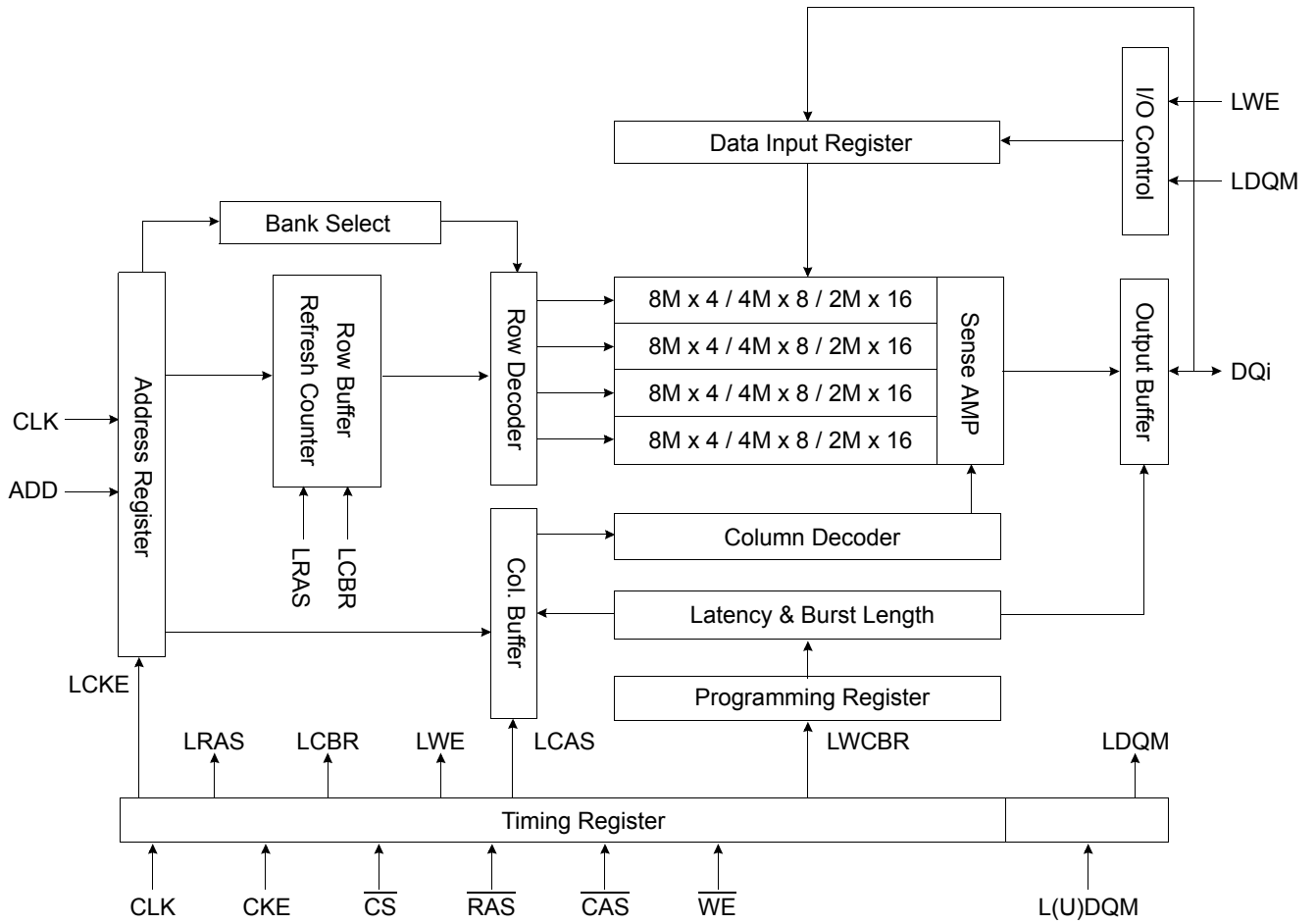
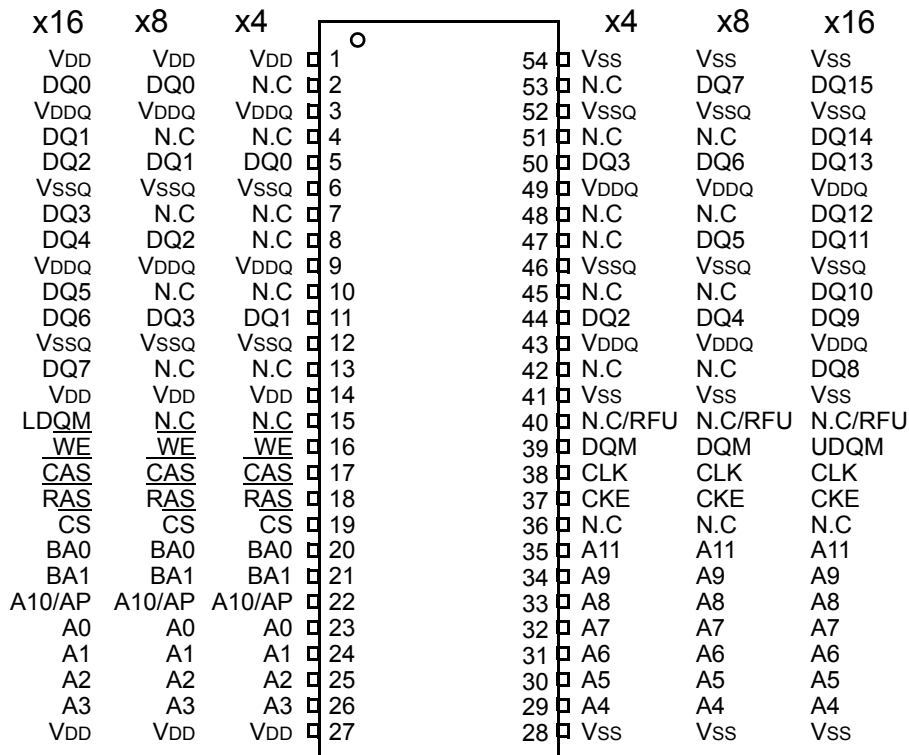## Package Physical Dimension
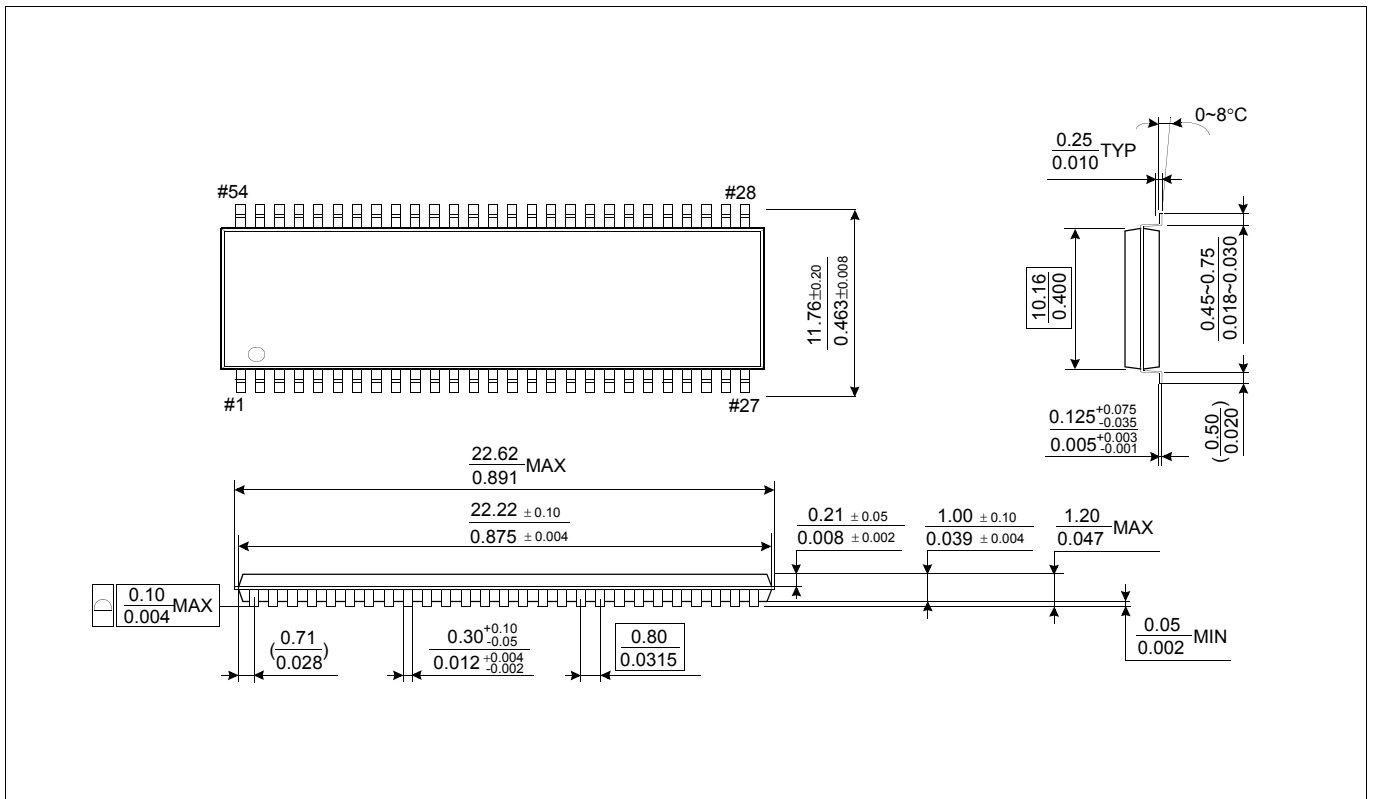
54Pin TSOP(II) Package Dimension

FUNCTIONAL BLOCK DIAGRAM

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PIN CONFIGURATION (Top view)

x16	x8	x4	Pin		Pin	x4	x8	x16
VDD	VDD	VDD	1		54	VSS	VSS	VSS
DQ0	DQ0	N.C	2		53	N.C	DQ7	DQ15
VDDQ	VDDQ	VDDQ	3		52	VSSQ	VSSQ	VSSQ
DQ1	N.C	N.C	4		51	N.C	N.C	DQ14
DQ2	DQ1	DQ0	5		50	DQ3	DQ6	DQ13
VSSQ	VSSQ	VSSQ	6		49	VDDQ	VDDQ	VDDQ
DQ3	N.C	N.C	7		48	N.C	N.C	DQ12
DQ4	DQ2	N.C	8		47	N.C	DQ5	DQ11
VDDQ	VDDQ	VDDQ	9		46	VSSQ	VSSQ	VSSQ
DQ5	N.C	N.C	10		45	N.C	N.C	DQ10
DQ6	DQ3	DQ1	11		44	DQ2	DQ4	DQ9
VSSQ	VSSQ	VSSQ	12		43	VDDQ	VDDQ	VDDQ
DQ7	N.C	N.C	13		42	N.C	N.C	DQ8
VDD	VDD	VDD	14		41	VSS	VSS	VSS
LDQM	N.C	N.C	15		40	N.C/RFU	N.C/RFU	N.C/RFU
WE	WE	WE	16		39	DQM	DQM	UDQM
CAS	CAS	CAS	17		38	CLK	CLK	CLK
RAS	RAS	RAS	18		37	CKE	CKE	CKE
CS	CS	CS	19		36	N.C	N.C	N.C
BA0	BA0	BA0	20		35	A11	A11	A11
BA1	BA1	BA1	21		34	A9	A9	A9
A10/AP	A10/AP	A10/AP	22		33	A8	A8	A8
A0	A0	A0	23		32	A7	A7	A7
A1	A1	A1	24		31	A6	A6	A6
A2	A2	A2	25		30	A5	A5	A5
A3	A3	A3	26		29	A4	A4	A4
VDD	VDD	VDD	27		28	VSS	VSS	VSS

54Pin TSOP
(400mil x 875mil)
(0.8 mm Pin pitch)

PIN FUNCTION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
$A_0 \sim A_{11}$	*Address*	Row/column addresses are multiplexed on the same pins. Row address : $RA_0 \sim RA_{11}$, Column address : (x4 : $CA_0 \sim CA_9, CA_{11}$), (x8 : $CA_0 \sim CA_9$), (x16 : $CA_0 \sim CA_8$)
$BA_0 \sim BA_1$	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active.
$DQ_0 \sim N$	*Data input/output*	Data inputs/outputs are multiplexed on the same pins. (x4 : $DQ_0 \sim 3$), (x8 : $DQ_0 \sim 7$), (x16 : $DQ_0 \sim 15$)
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}, V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{DD}+0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

CAPACITANCE (V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	C_{CLK}	2.5	3.5	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	C_{IN}	2.5	3.8	pF
Address	C_{ADD}	2.5	3.8	pF
(x4 : DQ_0 ~ DQ_3), (x8 : DQ_0 ~ DQ_7), (x16 : DQ_0 ~ DQ_{15})	C_{OUT}	4.0	6.0	pF

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DC CHARACTERISTICS (x4, x8)

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition		Version 75	Unit	Note
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		90	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		2	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		2		
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		20	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		10		
Active standby current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns		5	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞		5		
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns		30	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable		25	mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst		110	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		200	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	C	2	mA	3
			L	800	uA	4

Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S2804(08)32I-T(U)C
4. K4S2804(08)32I-T(U)L
5. Unless otherwise noted, input swing level is CMOS(V_{IH} /V_{IL}=V_{DDQ}/V_{SSQ})

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DC CHARACTERISTICS (x16)

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

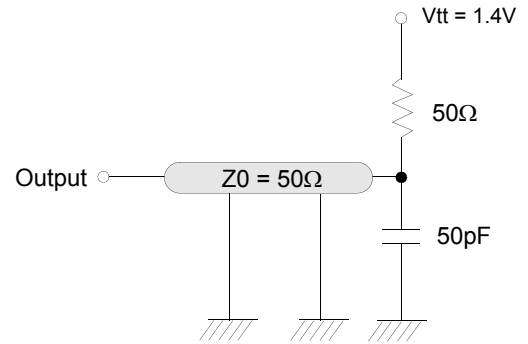| Parameter	Symbol	Test Condition		Version			Unit	Note
				50	60	75		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA		140	130	100	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE $\leq V_{IL}$(max), t_{CC} = 10ns		2			mA	
	I_{CC2PS}	CKE & CLK $\leq V_{IL}$(max), t_{CC} = ∞		2				
Precharge standby current in non power-down mode	I_{CC2N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 10ns Input signals are changed one time during 20ns		20			mA	
	I_{CC2NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), t_{CC} = ∞ Input signals are stable		10				
Active standby current in power-down mode	I_{CC3P}	CKE $\leq V_{IL}$(max), t_{CC} = 10ns		5			mA	
	I_{CC3PS}	CKE & CLK $\leq V_{IL}$(max), t_{CC} = ∞		5				
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE $\geq V_{IH}$(min), $\overline{CS} \geq V_{IH}$(min), t_{CC} = 10ns Input signals are changed one time during 20ns		30			mA	
	I_{CC3NS}	CKE $\geq V_{IH}$(min), CLK $\leq V_{IL}$(max), t_{CC} = ∞ Input signals are stable		25			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs		160	150	140	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)		230	220	200	mA	2
Self refresh current	I_{CC6}	CKE $\leq$ 0.2V	C	2			mA	3
			L	800			uA	4

Notes : 1. Measured with outputs open.

2. Refresh period is 64ms.

3. K4S281632I-T(U)C

4. K4S281632I-T(U)L

5. Unless otherwise noted, input swing level is CMOS($V_{IH} / V_{IL} = V_{DDQ}/V_{SSQ}$)

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AC OPERATING TEST CONDITIONS (VDD = 3.3V ± 0.3V, TA = 0 to 70°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	

(Fig. 1) DC output load circuit

VOH (DC) = 2.4V, IOH = -2mA
VOL (DC) = 0.4V, IOL = 2mA
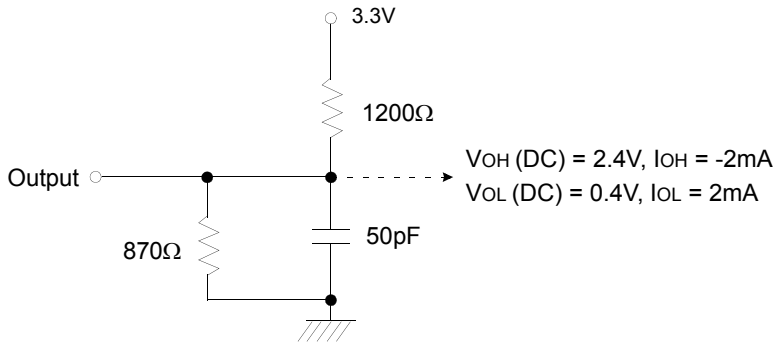
(Fig. 2) AC output load circuit

OPERATING AC PARAMETER
(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version			Unit	Note
			50	60 (x16	75		
Row active to row active delay		tRRD(min)	10	12	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	15	18	20	ns	1
Row precharge time		tRP(min)	15	18	20	ns	1
Row active time		tRAS(min)	40	42	45	ns	1
		tRAS(max)	100			us	
Row cycle time		tRC(min)	55	60	65	ns	1,6
Last data in to row precharge		tRDL(min)	2			CLK	2,5,6
Last data in to Active delay		tDAL(min)	2 CLK + tRP			-	5
Last data in to new col. address delay		tCDL(min)	1			CLK	2
Last data in to burst stop		tBDL(min)	1			CLK	2
Col. address to col. address delay		tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3		2			ea	4
	CAS latency=2		-		1		

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.

3. All parts allow every cycle column address change.

4. In case of row precharge interrupt, auto precharge and read burst stop.

5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.

6. tRC =tRFC, tRDL = tWR.

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AC CHARACTERISTICS (AC operating conditions unless otherwise noted)

Parameter		Symbol	50		60 (x16 only)		75		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	5	1000	6	1000	7.5	1000	ns	1
	CAS latency=2		-		-		10			
CLK to valid output delay	CAS latency=3	tSAC	-	4.5		5		5.4	ns	1,2
	CAS latency=2		-	-		-		6		
Output data hold time	CAS latency=3	tOH	2	-	2.5		3		ns	2
	CAS latency=2		-	-	-		3			
CLK high pulse width		tCH	2	-	2.5		2.5		ns	3
CLK low pulse width		tCL	2	-	2.5		2.5		ns	3
Input setup time		tSS	1.5	-	1.5		1.5		ns	3,4
Input hold time		tSH	1	-	1		0.8		ns	3,4
CLK to output in Low-Z		tSLZ	1	-	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	4.5		5		5.4	ns	
	CAS latency=2		-	-		-		6		

Notes : 1. Parameters depend on programmed CAS latency.

2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.

3. Assumed input rise and fall time (tr & tf) = 1ns.

   If tr & tf is longer than 1ns, transient time compensation should be considered,

   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

4. tSS applies for address setup time, clock enable setup time, commend setup time and data setup time

   tSH applies for address holde time, clock enable hold time, commend hold time and data hold time

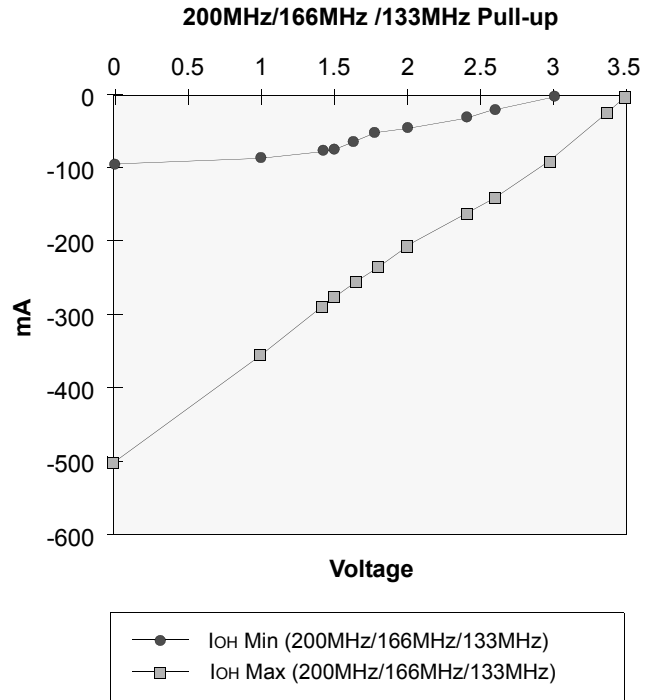## DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Notes
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

Notes : 1. Rise time specification based on 0pF + 50 Ω to VSS, use these values to design to.

2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.

3. Measured into 50pF only, use these values to characterize to.

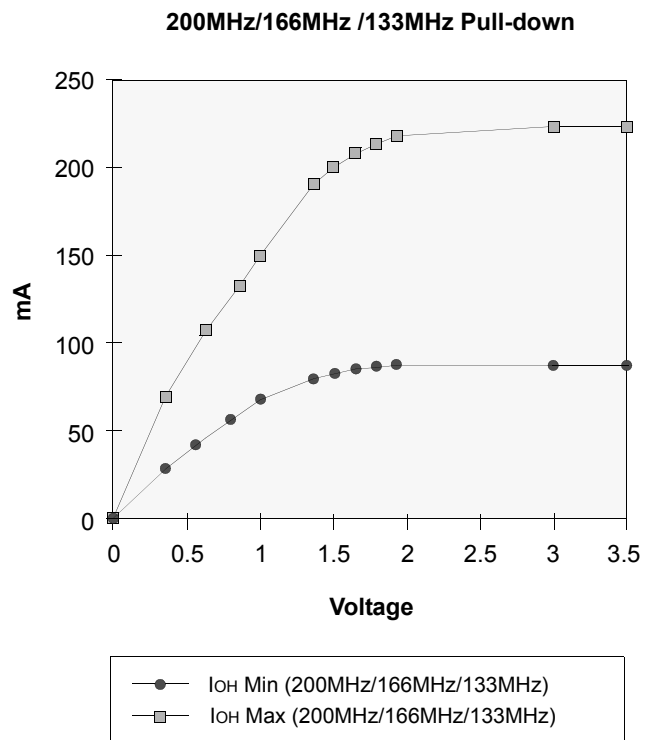4. All measurements done with respect to VSS.

IBIS SPECIFICATION

I$_{OH}$ Characteristics (Pull-up)

Voltage	200MHz 166MHz 133MHz Min	200MHz 166MHz 133MHz Max
(V)	I (mA)	I (mA)
3.45		-2.4
3.3		-27.3
3.0	0.0	-74.1
2.6	-21.1	-129.2
2.4	-34.1	-153.3
2.0	-58.7	-197.0
1.8	-67.3	-226.2
1.65	-73.0	-248.0
1.5	-77.9	-269.7
1.4	-80.8	-284.3
1.0	-88.6	-344.5
0.0	-93.0	-502.4

200MHz/166MHz /133MHz Pull-up

- ● I$_{OH}$ Min (200MHz/166MHz/133MHz)
- ■ I$_{OH}$ Max (200MHz/166MHz/133MHz)

I$_{OL}$ Characteristics (Pull-down)

Voltage	200MHz 166MHz 133MHz Min	200MHz 166MHz 133MHz Max
(V)	I (mA)	I (mA)
0.0	0.0	0.0
0.4	27.5	70.2
0.65	41.8	107.5
0.85	51.6	133.8
1.0	58.0	151.2
1.4	70.7	187.7
1.5	72.9	194.4
1.65	75.4	202.5
1.8	77.0	208.6
1.95	77.6	212.0
3.0	80.3	219.6
3.45	81.4	222.6

200MHz/166MHz /133MHz Pull-down

- ● I$_{OH}$ Min (200MHz/166MHz/133MHz)
- ■ I$_{OH}$ Max (200MHz/166MHz/133MHz)

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V_{DD} Clamp @ CLK, CKE, C̄S̄, DQM & DQ

V_{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

**Minimum V_{DD} clamp current
(Referenced to V_{DD})**
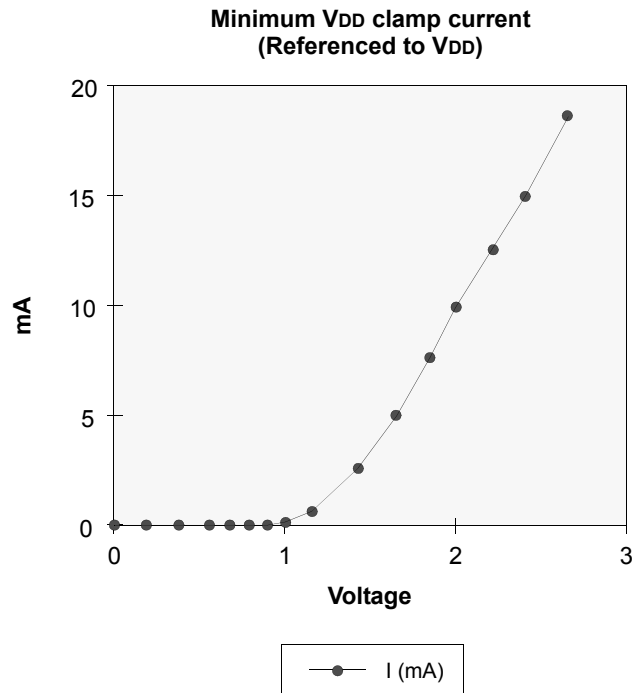
Vss Clamp @ CLK, CKE, C̄S̄, DQM & DQ

Vss (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

Minimum Vss clamp current

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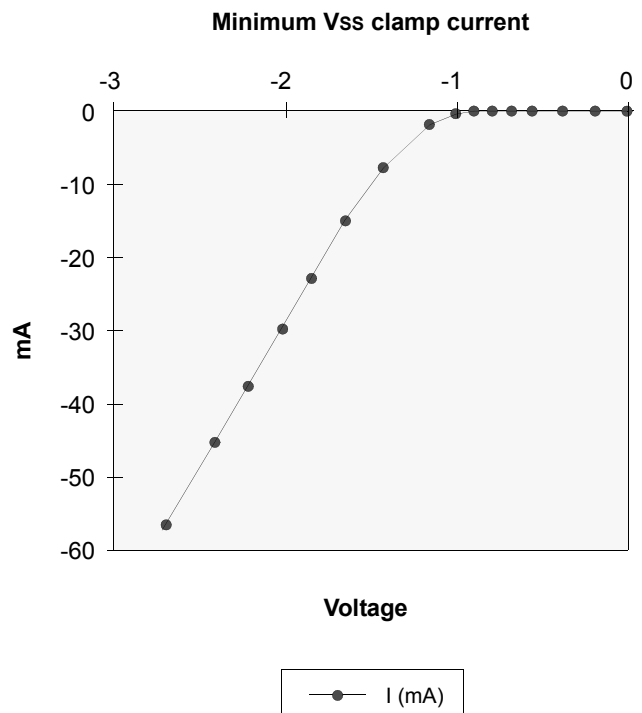
SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A0 ~ A9, A11,	Note
Register	Mode register set	H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh	H	H	L	L	L	H	X	X			3
	Self refresh Entry		L									3
	Self refresh Exit	L	H	L	H	H	H	X	X			3
				H	X	X	X					3
Bank active & row addr.		H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable	H	X	L	H	L	H	X	V	L	Column address	4
	Auto precharge enable									H		4,5
Write & column address	Auto precharge disable	H	X	L	H	L	L	X	V	L	Column address	4
	Auto precharge enable									H		4,5
Burst stop		H	X	L	H	H	L	X	X			6
Precharge	Bank selection	H	X	L	L	H	L	X	V	L	X	
	All banks								X	H		
Clock suspend or active power down	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X	X	X	X	X	X			
Precharge power down mode	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X	X			
				L	V	V	V					
DQM		H		X				V	X			7
No operation command		H	X	H	X	X	X	X	X			
				L	H	H	H					

Notes :

1. OP Code : Operand code

   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)

2. MRS can be issued only at all banks precharge state.

   A new command can be issued after 2 CLK cycles of MRS.

3. Auto refresh functions are as same as CBR refresh of DRAM.

   The automatical precharge without row precharge command is meant by "Auto".

   Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.

5. During burst read or write with auto precharge, new read/write command can not be issued.

   Another bank read/write command can be issued after the end of burst.

   New row active of the associated bank can be issued at tRP after the end of burst.

6. Burst stop command is valid at every burst length.

7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),

   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

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