1Gb gDDR3 SDRAM E-die

96 FBGA with Lead-Free & Halogen-Free
(RoHS Compliant)

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Revision History

Revision	Month	Year	History
0.0	July	2008	- First release
0.9	October	2008	- Correction ball configuration on page 4. - Changed ordering Infomation
0.9	November	2008	- Correction package size on page 5.
0.91	December	2008	- Added thermal characteristics table - Added speed bin 1066Mbps
0.92	February	2009	- Corrected tFAW value on page 44 - Corrected Package Dimension on page - Corrected Package pinout on page 4
1.0	February	2009	- Added thermal characteristics values (speed bin 1066/1333/1600Mbps) on page 14. - Added IDD SPEC values (speed bin 1066/1333/1600Mbps) on page 36. - Added note for lower frequencies supportabilty on page 3.
1.1	April	2009	- Added CWL and CL conditions (speed bin 1333/1600Mbps) on page 39,40
1.2	July	2009	- Corrected thermal Max_Tj, Max_Tc values (speed bin 1333/1600Mbps) on page 14. - Added thermal characteristics values (speed bin 1800/2000Mbps) on page 14. - Added IDD SPEC values (speed bin 1800/2000Mbps) on page 36. - Added CIO value (speed bin 1800/2000Mbps) on page 36.

1.0 Ordering Information

[Table 1] Samsung gDDR3 ordering information table

Organization	gDDR3-1066(7-7-7)	gDDR3-1333(9-9-9)	gDDR3-1600(11-11-11)	gDDR3-1800(12-12-12)	gDDR3-2000(13-13-13)	Package
64Mx16	K4W1G1646E-HC19	K4W1G1646E-HC15	K4W1G1646E-HC12	K4W1G1646E-HC11	K4W1G1646E-HC1A	96 FBGA

Note :

1. Speed bin is in order of CL-tRCD-tRP.
2. x16 Package

Part NO.	Max Freq.	Max Data Rate	V_{DD}&V_{DDQ}	Package
K4W1G1646E-HC1A	1000MHz	2000Mbps/pin	1.5V±0.075V	96 Ball FBGA
K4W1G1646E-HC11	900MHz	1800Mbps/pin		
K4W1G1646E-HC12	800MHz	1600Mbps/pin		
K4W1G1646E-HC15	667MHz	1333Mbps/pin		
K4W1G1646E-HC19	533MHz	1066Mbps/pin		

2.0 Key Features

[Table 2] 1Gb gDDR3 E-die Speed bins

Speed	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	Unit
	7-7-7	9-9-9	11-11-11	12-12-12	13-13-13	
tCK(min)	1.875	1.5	1.25	1.1	1.0	ns
CAS Latency	7	9	11	12	13	tCK
tRCD(min)	13.125	13.5	13.75	13.2	13	ns
tRP(min)	13.125	13.5	13.75	13.2	13	ns
tRAS(min)	37.5	36	35	34	33	ns
tRC(min)	50.625	49.5	48.75	47.2	46	ns

- V_{DD}/V_{DDQ}= 1.5V ± 0.075V at 1066/1333/1600/1800/2000
- 533MHz f_{CK} for 1066Mb/sec/pin, 667MHz f_{CK} for 1333Mb/sec/pin, 800MHz f_{CK} for 1600Mb/sec/pin 900MHz f_{CK} for 1800Mb/sec/pin, 1000MHz f_{CK} for 2000Mb/sec/pin
- 8 Banks
- Posted CAS
- Programmable CAS Latency(posted CAS): 7,9,11,12,13
- Programmable Additive Latency: 0, CL-2 or CL-1 clock
- Programmable CAS Write Latency: (CWL) =6 (1066Mbps), 7(1333Mbps), 8(1600Mbps), 9(1800Mbps),10(2000Mbps)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data-Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period: 7.8us at lower than T_{CASE} 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95 °C
- Asynchronous Reset
- Package : 96 balls FBGA - x16
- All of Lead-Free products are compliant for RoHS
- All of products are Halogen-Free

The 1Gb gDDR3 SDRAM E-die is organized as 8Mbit x 16 I/Os x 8 banks device. This synchronous device achieves high speed double-data-rate transfer rates of up to 2000Mb/sec/pin (gDDR3-2000) for general applications.

The chip is designed to comply with the following key gDDR3 SDRAM features such as posted CAS, Programmable CWL, Internal (Self) Calibration, On Die Termination using ODT pin and Asynchronous Reset .

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the crosspoint of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a pair of bidirectional strobes (DQS and $\overline{DQS}$) in a source synchronous fashion. The address bus is used to convey row, column, and bank address information in a $\overline{RAS}/\overline{CAS}$ multiplexing style. The gDDR3 E-die device operates with a 1.5V ± 0.075V power supply and 1.5V ± 0.075V_{DDQ} based upon operation frequency.

The 1Gb gDDR3 E-die device is available in 96ball FBGA(x16)

Note 1. The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

2. Any gDDR3 speed bin also supports functional operation at lower frequencies as shown in the Table 2 if voltage rail is identical.

3.0 Package pinout/Mechanical Dimension & Addressing

3.1 x16 Package Pinout (Top view) : 96ball FBGA Package

	1	2	3	4	5	6	7	8	9	
A	V_{DDQ}	DQU5	DQU7				DQU4	V_{DDQ}	V_{SS}	A
B	V_{SSQ}	V_{DD}	V_{SS}				$\overline{\text{DQSU}}$	DQU6	V_{SSQ}	B
C	V_{DDQ}	DQU3	DQU1				DQSU	DQU2	V_{DDQ}	C
D	V_{SSQ}	V_{DDQ}	DMU				DQU0	V_{SSQ}	V_{DD}	D
E	V_{SS}	V_{SSQ}	DQL0				DML	V_{SSQ}	V_{DDQ}	E
F	V_{DDQ}	DQL2	DQSL				DQL1	DQL3	V_{SSQ}	F
G	V_{SSQ}	DQL6	$\overline{\text{DQSL}}$				V_{DD}	V_{SS}	V_{SSQ}	G
H	V_{REFDQ}	V_{DDQ}	DQL4				DQL7	DQL5	V_{DDQ}	H
J	NC	V_{SS}	$\overline{\text{RAS}}$				CK	V_{SS}	NC	J
K	ODT	V_{DD}	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	V_{DD}	CKE	K
L	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	L
M	V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}	M
N	V_{DD}	A3	A0				A12/$\overline{\text{BC}}$	BA1	V_{DD}	N
P	V_{SS}	A5	A2				A1	A4	V_{SS}	P
R	V_{DD}	A7	A9				A11	A6	V_{DD}	R
T	V_{SS}	$\overline{\text{RESET}}$	A13				NC	A8	V_{SS}	T

Ball Locations (x16)

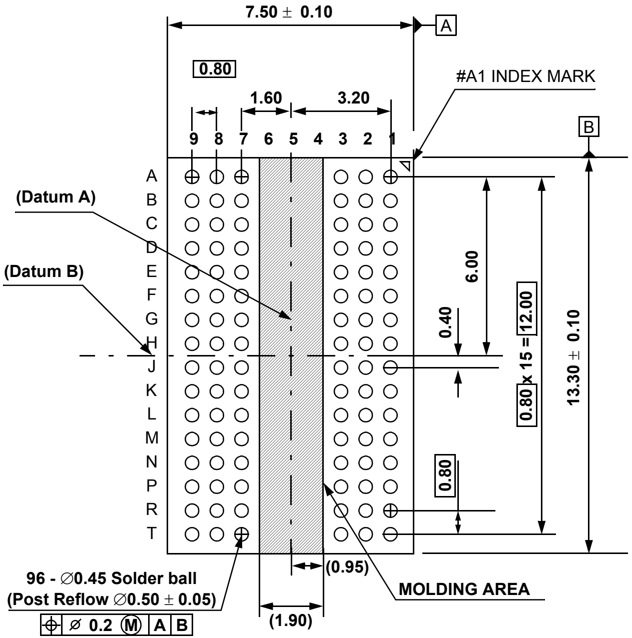
● Populated ball
+ Ball not populated

Top view
(See the balls through the package)

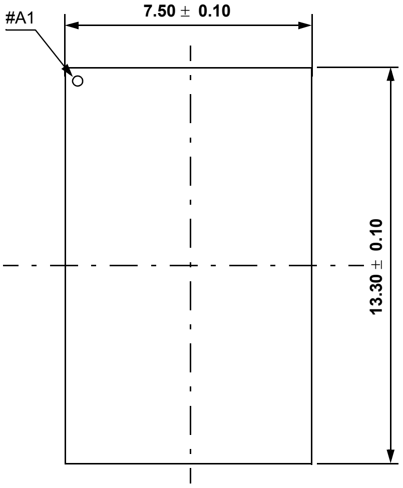
	1	2	3	4	5	6	7	8	9
A	●	●	●	+	+	+	●	●	●
B	●	●	●	+	+	+	●	●	●
C	●	●	●	+	+	+	●	●	●
D	●	●	●	+	+	+	●	●	●
E	●	●	●	+	+	+	●	●	●
F	●	●	●	+	+	+	●	●	●
G	●	●	●	+	+	+	●	●	●
H	●	●	●	+	+	+	●	●	●
J	●	●	●	+	+	+	●	●	●
K	●	●	●	+	+	+	●	●	●
L	●	●	●	+	+	+	●	●	●
M	●	●	●	+	+	+	●	●	●
N	●	●	●	+	+	+	●	●	●
P	●	●	●	+	+	+	●	●	●
R	●	●	●	+	+	+	●	●	●
T	●	●	●	+	+	+	●	●	●

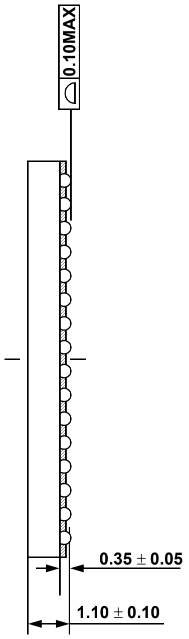
3.2 FBGA Package Dimension (x16)

Units : Millimeters


7.50 ± 0.10
A
0.80
1.60
3.20
#A1 INDEX MARK
B
9 8 7 6 5 4 3 2 1
A B C D E F G H J K L M N P R T
(Datum A)
(Datum B)
6.00
0.40
0.80 x 15 = 12.00
13.30 ± 0.10
0.80
(0.95)
MOLDING AREA
96 - ∅0.45 Solder ball
(Post Reflow ∅0.50 ± 0.05)
⌖ ∅ 0.2 Ⓜ A B
(1.90)

BOTTOM VIEW


#A1
7.50 ± 0.10
13.30 ± 0.10


0.10MAX
0.35 ± 0.05
1.10 ± 0.10

TOP VIEW

4.0 Input/Output Functional Description

[Table 3] Input/Output function description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (Row Active in any bank). CKE is asynchronous for self refresh exit. After VREFCA has become stable during the power on and initialization sequence, it must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self -Refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	**On Die Termination:** ODT (registered HIGH) enables termination resistance internal to the gDDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/$\overline{TDQS}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. The ODT pin will be ignored if the Mode Register (MR1) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (DMU), (DML)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/$\overline{TDQS}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A13	Input	**Address Inputs:** Provided the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional functions, see below) The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	**Autoprecharge:** A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH:Autoprecharge; LOW: No Autoprecharge) A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). if only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	**Burst Chop:**A12 is sampled during Read and Write commands to determine if burst chop(on-the-fly) will be performed. (HIGH : no burst chop, LOW : burst chopped). See command truth table for details
$\overline{RESET}$	Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is LOW, and inactive when $\overline{RESET}$ is HIGH. $\overline{RESET}$ must be HIGH during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDD, i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input/Output	**Data Input/ Output:** Bi-directional data bus.
DQS, ($\overline{DQS}$)	Input/Output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data, centered in write data.
TDQS, ($\overline{TDQS}$)	fout	**Termination Data Strobe:** TDQS/$\overline{TDQS}$ is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and $\overline{TDQS}$ is not used.
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.5V +/- 0.075V
V_{SSQ}	Supply	**DQ Ground**
V_{DD}	Supply	**Power Supply:** 1.5V +/- 0.075V
V_{SS}	Supply	**Ground**
V_{REFDQ}	Supply	**Reference voltage for DQ**
V_{REFCA}	Supply	**Reference voltage for CA**
ZQ	Supply	**Reference Pin for ZQ calibration**
Note : Input only pins (BA0-BA2, A0-A12, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT and $\overline{RESET}$) do not supply termination.		

5.0 gDDR3 SDRAM Addressing

1Gb

Configuration	64Mb x 16
# of Bank	8
Bank Address	BA0 - BA2
Auto precharge	A_{10}/AP
Row Address	A_0 - A_{12}
Column Address	A_0 - A_9
BC switch on the fly	$A_{12}/\overline{BC}$
Page size [*1]	2 KB

Note 1 : Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered.
Page size is per bank, calculated as follows: page size = $2^{COLBITS} * ORG \div 8$
where, COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

6.0 Absolute Maximum Ratings

6.1 Absolute Maximum DC Ratings

[Table 4] Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 V ~ 1.975 V	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note :

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times;and V_{REF} must be not greater than 0.6xV_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

6.2 DRAM Component Operating Temperature Range

[Table 5] Temperature Range

Symbol	Parameter	rating	Unit	Notes
T_{OPER}	Operating Temperature Range	0 to 95	°C	1, 2, 3

Note :

1. Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b)

7.0 AC & DC Operating Conditions

7.1 Recommended DC operating Conditions (SSTL_1.5)

[Table 6] Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

Note :

1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.

8.0 AC & DC Input Measurement Levels

8.1 AC and DC Logic input levels for single-ended signals

[Table 7] Single Ended AC and DC input levels for Command and Address

Symbol	Parameter	gDDR3-1066		gDDR3-1333/1600		gDDR3-1800/2000		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
$V_{IH.CA}$(DC)	DC input logic high	V_{REF} + 100	V_{DD}	V_{REF} + 100	V_{DD}	V_{REF} + 100	V_{DD}	mV	1
$V_{IL.CA}$(DC)	DC input logic low	V_{SS}	V_{REF} - 100	V_{SS}	V_{REF} - 100	V_{SS}	V_{REF} - 100	mV	1
$V_{IH.CA}$(AC)	AC input logic high	V_{REF} + 175	-	V_{REF} + 175	-	V_{REF} + 175	-	mV	1,2
$V_{IL.CA}$(AC)	AC input logic low	-	V_{REF} - 175	-	V_{REF} - 175	-	V_{REF} - 175	mV	1,2
$V_{IH.CA}$(AC150)	AC input logic high	-	-	V_{REF} + 150	-	V_{REF} + 150	-	mV	1,2
$V_{IL.CA}$(AC150)	AC input logic low	-	-	-	V_{REF} - 150	-	V_{REF} - 150	mV	1,2
VREFCA(DC)	Reference Voltage for ADD, CMD inuts	0.49*V_{DDQ}	0.51*V_{DDQ}	0.49*V_{DDQ}	0.51*V_{DDQ}	0.49*V_{DDQ}	0.51*V_{DDQ}	V	3,4

1. For DQ and DM, $V_{REF} = V_{REFDQ}$. For input only pins except $\overline{RESET}$, $V_{REF} = V_{REFCA}$ (DC)
2. See 9.6 "Overshoot and Undershoot specifications" on page 21.
3. The AC peak noise on V_{REF} may not allow V_{REF} to deviate from V_{REF}(DC) by more than ± 1% V_{DD} (for reference : approx. ± 15mV)
4. For reference : approx. $V_{DD/2}$ ± 15mV

The dc-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} and V_{REFDQ} are illustrate in Figure 1. It shows a valid reference voltage V_{REF}(t) as a function of time. (V_{REF} stands for V_{REFCA} and V_{REFDQ} likewise).

V_{REF}(DC) is the linear average of V_{REF}(t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requiremts in table 7. Furthermore V_{REF}(t) may temporarily deviate from V_{REF}(DC) by no more than ± 1% V_{DD}.

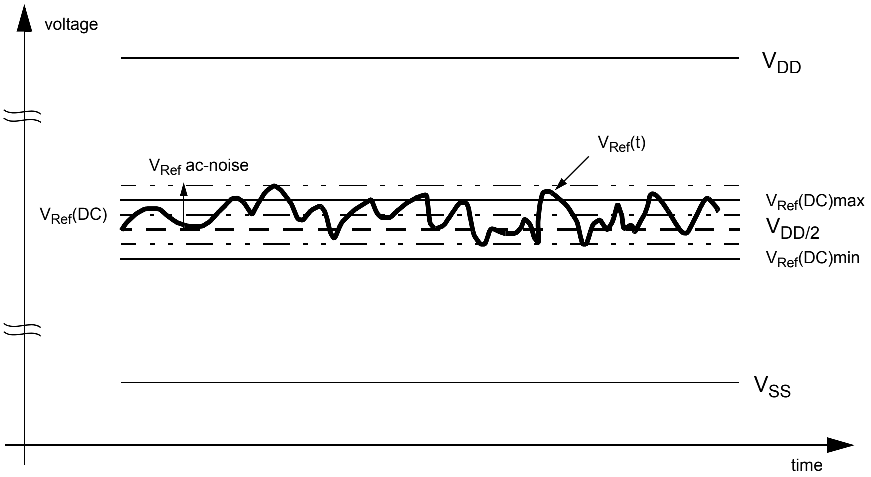


Figure 1. Illustration of V_{REF}(DC) tolerance and V_{REF} ac-noise limits

The voltage levels for setup and hold time measurements V_{IH}(AC), V_{IH}(DC), V_{IL}(AC) and V_{IL}(DC) are dependent on V_{REF}.

"V_{REF}" shall be understood as V_{REF}(DC), as defined in Figure 1.

This clarifies, that dc-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for V_{REF}(DC) deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} ac-noise. Timing and voltage effects due to ac-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

8.2 AC and DC Logic Input Levels for Ditterential Signals

8.2.1 Differential signal definitian

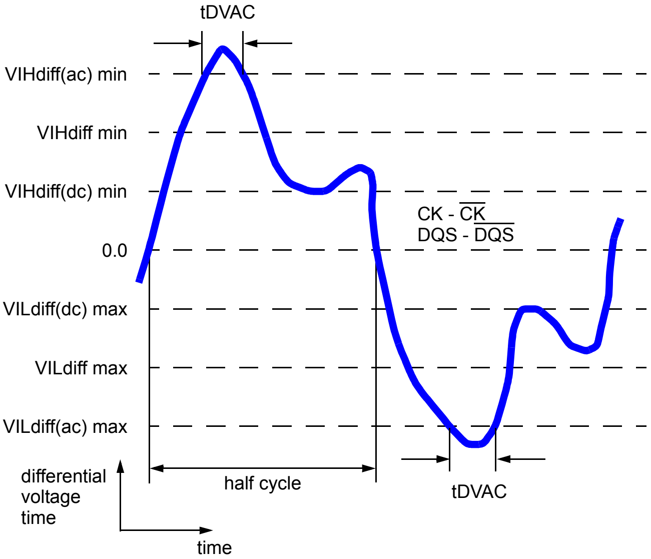

tDVAC
VIHdiff(ac) min
VIHdiff min
VIHdiff(dc) min
CK - $\overline{\text{CK}}$
DQS - $\overline{\text{DQS}}$
0.0
VILdiff(dc) max
VILdiff max
VILdiff(ac) max
differential
voltage
time
half cycle
tDVAC
time

Figure 2 : Definition of differential ac-swing and "time above ac level tDVAC

8.2.2 Differential swing requirement for clock (CK - $\overline{\text{CK}}$) and strobe (DQS - $\overline{\text{DQS}}$)

[Table 8] Differential AC and DC Input Levels

Symbol	Parameter	gDDR3-1066/1333/1600/1800/2000		unit	Note
		min	max		
VIHdiff	differential input high	+0.2	note 3	V	1
VILdiff	differential input low	note 3	-0.2	V	1
VIHdiff(ac)	differential input high ac	2 x (V_{IH}(ac)-Vref)	note 3	V	2
VILdiff(ac)	differential input low ac	note 3	2 x (Vref - VIL(ac))	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. for CK - $\overline{\text{CK}}$ use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - $\overline{\text{DQS}}$, DQSL - $\overline{\text{DQSL}}$, DQSU - $\overline{\text{DQSU}}$ use V_{IH}/V_{IL}(ac) of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however they single-ended signals CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$, DQSL, $\overline{\text{DQSL}}$, DQSU, $\overline{\text{DQSU}}$ need to be within the respective limits (V_{IH}(dc) max, V_{IL}(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Reter to "overshoot and Undersheet Specification " on page21.

[Table 9] Allowed time before ringback (tDVAC) for CLK - $\overline{\text{CLK}}$ and DQS - $\overline{\text{DQS}}$.

Slew Rate [V/ns]	tDVAC [ps] @ |VIH/Ldiff(ac)| = 350mV		tDVAC [ps] @ |VIH/Ldiff(ac)| = 300mV	
	min	max	min	max
> 4.0	75	-	175	-
4.0	57	-	170	-
3.0	50	-	167	-
2.0	38	-	163	-
1.8	34	-	162	-
1.6	29	-	161	-
1.4	22	-	159	-
1.2	13	-	155	-
1.0	0	-	150	-
< 1.0	0	-	150	-

8.2.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, or $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals.
CK and $\overline{CK}$ have to approximately reach V_{SEH}min / V_{SEL}max (approximately equal to the ac-levels (V_{IH}(ac) / V_{IL}(ac)) for ADD/CMD signals) in every half-cycle.
DQS, DQSL, DQSU, $\overline{DQS}$, $\overline{DQSL}$ have to reach V_{SEH}min / V_{SEL}max (approximately the ac-levels (V_{IH}(ac) / V_{IL}(ac)) for DQ signals) in every half-cycle preceeding and following a valid transition.
Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if V_{IH}150(ac)/V_{IL}150(ac) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$.

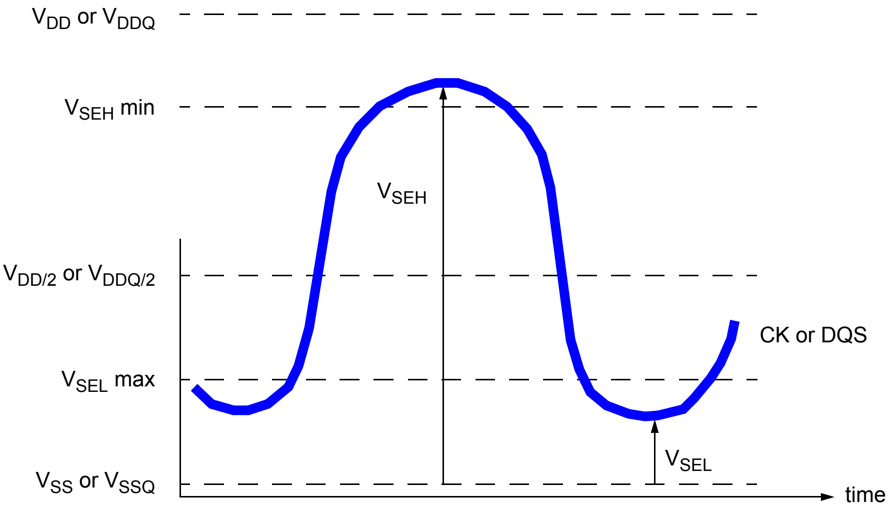


Figure 3 : Single-ended requirement for differential signals.

Note that while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to $V_{DD/2}$; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach V_{SEL}max, V_{SEH}min has no bearing on timing, but adds a restriction on the common mode charateristics of these signals.

[Table 10] Single ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

Symbol	Parameter	gDDR3-1066/1333/1600/1800/2000		Unit	Notes
		Min	Max		
V_{SEH}	Single-ended high-level for strobes	V_{IH}(ac)-V_{REFDQ}+V_{DDQ}/2	Note3	V	1, 2
	Single-ended high-level for CK, $\overline{CK}$	V_{IH}(ac)-V_{REFCA}+V_{DD}/2	Note3	V	1, 2
V_{SEL}	Single-ended low-level for strobes	Note3	V_{IL}(ac)+V_{REFDQ}-V_{DDQ}/2	V	1, 2
	Single-ended low-level for CK, $\overline{CK}$	Note3	V_{IL}(ac)+V_{REFCA}-V_{DD}/2	V	1, 2

Notes:
1. For CK, $\overline{CK}$ use V_{IH}/V_{IL}(ac) of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use V_{IH}/V_{IL}(ac) of DQs.
2. V_{IH}(ac)/V_{IL}(ac) for DQs is based on V_{REFDQ}; V_{IH}(ac)/V_{IL}(ac) for ADD/CMD is based on V_{REFCA}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
3. These values are not defined, however they single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (V_{IH}(dc) max, V_{IL}(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot.

8.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{\text{CK}}$ and DQS, $\overline{\text{DQS}}$) must meet the requirements in below table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signal to the mid level between of V_{DD} and V_{SS}.

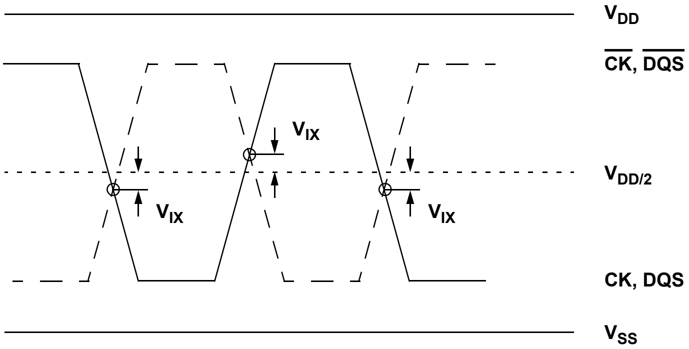


Figure 4. Vix Definition

[Table 12] Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	gDDR3-1066/1333/1600/1800/2000		Unit	Notes
		Min	Max		
V_{IX}	Differential input Cross point voltage relative to $V_{DD/2}$	-150	150	mV	

8.4 Slew Rate Definition for Single Ended Input Signals

8.4.1 Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of V_{IH}(AC)min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of V_{IL}(AC)max.

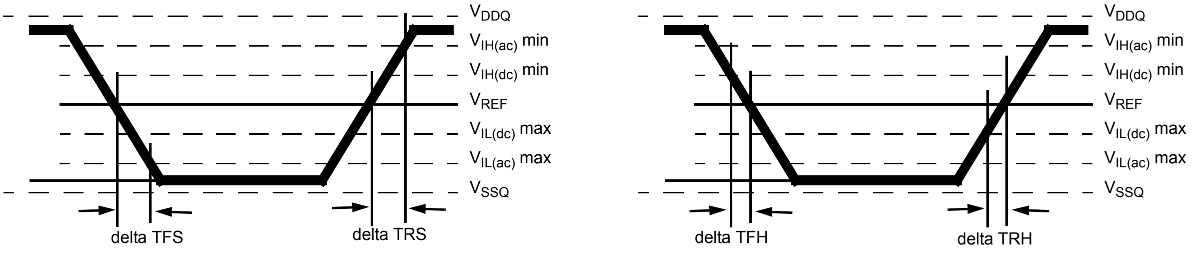
8.4.2 Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL}(DC)max and the first crossing of VRef. Hold (tIH & tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(DC)min and the first crossing of VRef

[Table 13] Single Ended Input Slew Rate definition

Description	Measured		Defined by	Applicable for
	From	To		
Input slew rate for rising edge	V_{REF}	V_{IH}(AC)min	$\frac{\text{VIH(AC)min-VREF}}{\text{Delta TRS}}$	Setup (tIS,tDS)
Input slew rate for falling edge	V_{REF}	V_{IL}(AC)max	$\frac{\text{VREF-VIL(AC)max}}{\text{Delta TFS}}$	
Input slew rate for rising edge	V_{IL}(DC)max	V_{REF}	$\frac{\text{VREF-VIL(DC)max}}{\text{Delta TRH}}$	Hold (tIH,tDH)
Input slew rate for falling edge	V_{IH}(DC)min	V_{REF}	$\frac{\text{VIH(DC)min-VREF}}{\text{Delta TFH}}$	

Notes: This nominal slew rate applies for linear signal waveforms.



< Figure : Input slew rate for setup>

< Figure : Input slew rate for Hold>

Figure 5. Input Nominal Slew Rate definition for Singel ended Signals

8.5 Slew rate definition for Differential Input Signals

[Table 14] Differential input slew rate definition

Description	Measured		Defined by
	From	To	
Differential input slew rate for rising edge (CK-$\overline{\text{CK}}$ and DQS-$\overline{\text{DQS}}$)	VILdiffmax	VIHdiffmin	$\frac{\text{VIHdiffmin - VILdiffmax}}{\text{Delta TRdiff}}$
Differential input slew rate for falling edge (CK-$\overline{\text{CK}}$ and DQS-$\overline{\text{DQS}}$)	VIHdiffmin	VILdiffmax	$\frac{\text{VIHdiffmin - VILdiffmax}}{\text{Delta TFdiff}}$

Note : The differential signal (i.e. CK - $\overline{\text{CK}}$ and DQS - $\overline{\text{DQS}}$) must be linear between these thresholds

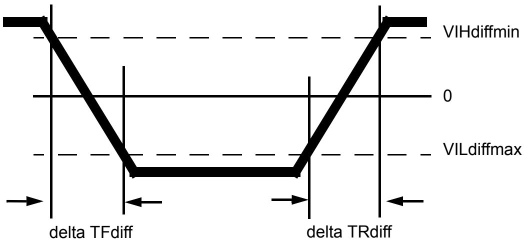


Figure 6. Differential Input Slew Rate definition for DQS, $\overline{\text{DQS}}$ and CK, $\overline{\text{CK}}$

9.0 AC and DC Output Measurement Levels

9.1 Single Ended AC and DC Output Levels

[Table 15] Single Ended AC and DC output levels

Symbol	Parameter	gDDR3-1066/1333/1600/1800/2000	Units	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Note :

1. The swing of +/-0.1xV_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 34ohms and an effective test load of 25ohms to V_{TT}=V_{DDQ}/2.

9.2 Differential AC and DC Output Levels

[Table 16] Differential AC and DC output levels

Symbol	Parameter	gDDR3-1066/1333/1600/1800/2000	Units	Notes
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+0.2 x V_{DDQ}	V	1
$V_{OLdiff(DC)}$	AC differential output low measurement level (for output SR)	-0.2 x V_{DDQ}	V	1

Note :

1. The swing of +/-0.2xV_{DDQ} is based on approximately 50% of the static singel ended output high or low swing with a driver impedance of 34ohms and an effective test load of 25ohms to V_{TT}=V_{DDQ}/2 at each of the differential outputs.

9.3 Thermal Characterstics(1.06/1.33/1.6/1.8/2.0Gbps at V_{DD}=1.5V $\pm$ 0.075V, V_{DDQ}=1.5V $\pm$ 0.075V)

Parameter	Description	Value	Units	Note
Theta_JA	Thermal resistance junction to ambient	34.3	°C/W	Thermal measurement : 1,2,3,5
Max_Tj	Maximum operating junction temperature	41.7 41.2 40.7 38.0 35.8	°C	2.0Gbps@Max1.575V (Pd=0.488W) 1.8Gbps@Max1.575V (Pd=0.473W) 1.6Gbps@Max1.575V (Pd=0.456W) 1.33Gbps@Max1.575V (Pd=0.378W) 1.06Gbps@Max1.575V (Pd=0.315W)
Max_Tc	Maximum operating case temperature	39.4 38.9 38.5 36.1 34.3	°C	2.0Gbps@Max1.575V 1.8Gbps@Max1.575V 1.6Gbps@Max1.575V 1.33Gbps@Max1.575V 1.06Gbps@Max1.575V
Theta_Jc	Thermal resistance junction to case	4.8	°C/W	Thermal simulation :1, 2, 6
Theta_JB	Thermal resistance junction to board	14.9	°C/W	Thermal simulation :1, 2, 6

Note :

1. Measurement procedures for each parameter must follow standard procedures defined in the current JEDEC JESD-51 standard.
2. Theta_JA and Theta_JB must be measured with the high effective thermal conductivity test board defined in JESD51-7
3. Airflow information must be documented for Theta JA.
4. Max_Tj and Max_Tc are documented for normal operation in this table. These are not intended to reflect reliablility limits.
5. Theta_JA should only be used for comparing the thermal performance of single packages and not for system related junction.
6. Theta_JB and Theta_JC are derived through a package thermal simulation and measurement.

9.4.Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between V_{OL}(AC) and V_{OH}(AC) for single ended signals as shown in Table 17 and figure 7.

[Table 17] Single Ended Output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	VOH(AC)-VOL(AC) Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	VOH(AC)-VOL(AC) Delta TFse

[Table 18] Single Ended Output slew rate

Parameter	Symbol	gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1800		gDDR3-2000		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	2.5	5	2.5	5	2.5	5	2.5	5	TBD	TBD	V/ns

Note : Output slew rate is verified by design and characterization, and may not be subject to production test.
For Ron=RZQ/7 setting

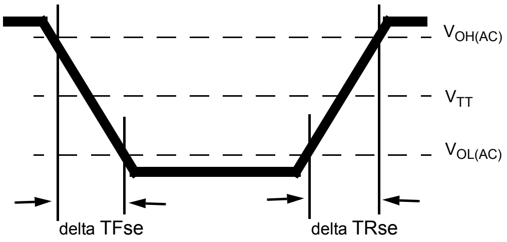


Figure 7. Single Ended Output Slew Rate definition

9.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown inTable 19 and figure 8.

[Table 19] Differential Output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	VOHdiff(AC)-VOLdiff(AC) Delta TRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	VOHdiff(AC)-VOLdiff(AC) Delta TFdiff

[Table 20] Differential Output slew rate

Parameter	Symbol	gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1800		gDDR3-2000		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	5	10	5	10	5	10	5	10	TBD	TBD	V/ns

Note : Output slew rate is verified by design and characterization, and may not be subject to production test.
For Ron=RZQ/7 setting

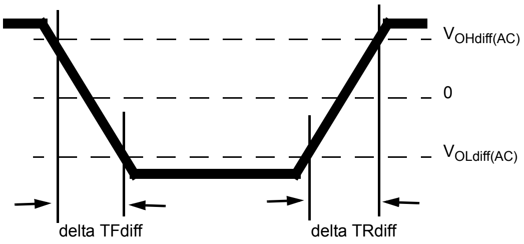


Figure 8. Differential Output Slew Rate definition

9.6 Reference Load for AC Timing and Output Slew Rate

Figure 9 represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment of a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

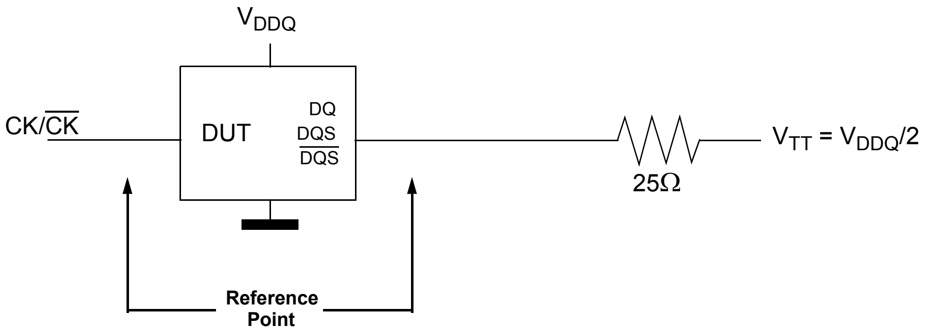


Figure 9. Reference Load for AC Timing and Output Slew Rate

9.7 Overshoot/Undershoot Specification

9.7.1 Address and Control Overshoot and Undershoot specifications

[Table 21] AC overshoot/undershoot specification for Address and Control pins (A0-A12, BA0-BA2, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, ODT)

Parameter	Specification					Unit
	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	
Maximum peak amplitude allowed for overshoot area (See Figure 10)	0.4V	0.4V	0.4V	0.4V	0.4V	V
Maximum peak amplitude allowed for undershoot area (See Figure 10)	0.4V	0.4V	0.4V	0.4V	0.4V	V
Maximum overshoot area above V_{DD} (See Figure 10)	0.5V-ns	0.4V-ns	0.33V-ns	0.28V-ns	0.23V-ns	V-ns
Maximum undershoot area below V_{SS} (See Figure 10)	0.5V-ns	0.4V-ns	0.33V-ns	0.28V-ns	0.23V -ns	V -ns

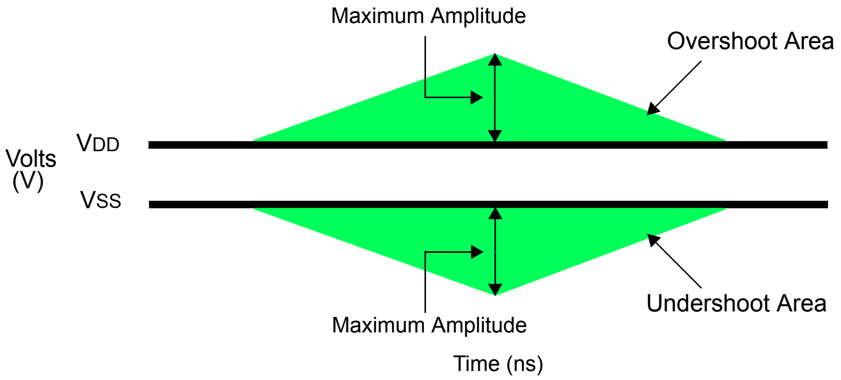

Maximum Amplitude
Overshoot Area
Volts (V)
VDD
VSS
Maximum Amplitude
Undershoot Area
Time (ns)

Figure 10. Address and Control Overshoot and Undershoot definition

9.7.2 Clock, Data, Strobe and Mask Overshoot and Undershoot specifications

[Table 22] AC overshoot/undershoot specification for Clock, Data, Strobe and Mask (DQ, DQS, $\overline{DQS}$, DM, CK, $\overline{CK}$)

Parameter	Specification					Unit
	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	
Maximum peak amplitude allowed for overshoot area (See Figure 11)	0.4V	0.4V	0.4V	0.4V	0.4V	V
Maximum peak amplitude allowed for undershoot area (See Figure 11)	0.4V	0.4V	0.4V	0.4V	0.4V	V
Maximum overshoot area above V_{DDQ} (See Figure 11)	0.19V-ns	0.15V-ns	0.13V-ns	0.11V -ns	0.09V -ns	V -ns
Maximum undershoot area below V_{SSQ} (See Figure 11)	0.19V-ns	0.15V-ns	0.13V-ns	0.11V -ns	0.09V -ns	V -ns

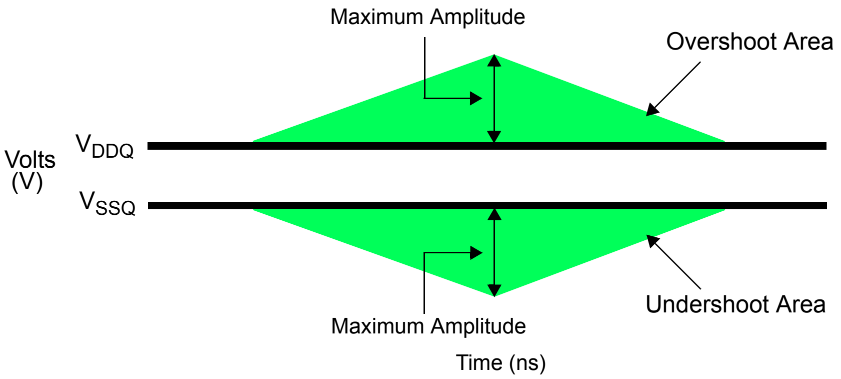

Maximum Amplitude
Overshoot Area
Volts (V)
VDDQ
VSSQ
Maximum Amplitude
Undershoot Area
Time (ns)

Figure 11. Clock, Data, Strobe and Mask Overshoot and Undershoot definition

9.8 34 ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown below. Output driver impedance RON is defined by the value of external reference resistor RZQ as follows:

RON_{34} = RZQ/7 (Nominal 34ohms +/- 10% with nominal RZQ=240ohm)
RON_{40} = RZQ/6 (Nominal 40ohms +/- 10% with nominal RZQ=240ohm)

The individual Pull-up and Pull-down resistors (RONpu and RONpd) are defined as follows

$$RONpu = \frac{V_{DDQ}\text{-}Vout}{|\,Iout\,|} \quad \text{under the condition that RONpd is turned off}$$

$$RONpd = \frac{Vout}{|\,Iout\,|} \quad \text{under the condition that RONpu is turned off}$$

Output Driver : Definition of Voltages and Currents

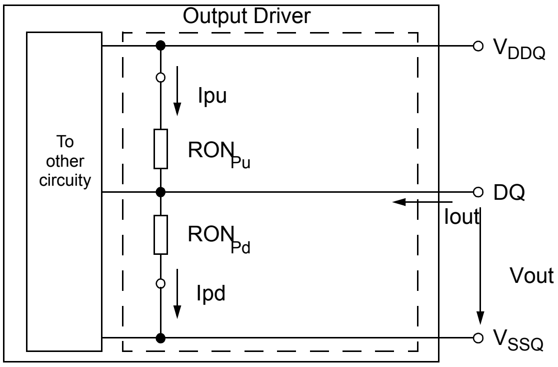


Figure 12. Output Driver : Definition of Voltages and Currents

[Table 23] Output Driver DC Electrical Characteristics, assuming RZQ=240 ohms ; entire operating temperature range; after proper ZQ calibration

RONnom	Resistor	Vout	Min	Nom	Max	Units	Notes
34Ohms	RON34pd	V_{OL}dc = 0.2 x V_{DDQ}	0.6	1.0	1.1	RZQ/7	1,2,3
		V_{OM}dc = 0.5 x V_{DDQ}	0.9	1.0	1.1		1,2,3
		V_{OH}dc = 0.8 x V_{DDQ}	0.9	1.0	1.4		1,2,3
	RON34pu	V_{OL}dc = 0.2 x V_{DDQ}	0.9	1.0	1.4		1,2,3
		V_{OM}dc = 0.5 x V_{DDQ}	0.9	1.0	1.1		1,2,3
		V_{OH}dc = 0.8 x V_{DDQ}	0.6	1.0	1.1		1,2,3
40Ohms	RON40pd	V_{OL}dc = 0.2 x V_{DDQ}	0.6	1.0	1.1	RZQ/6	1,2,3
		V_{OM}dc = 0.5 x V_{DDQ}	0.9	1.0	1.1		1,2,3
		V_{OH}dc = 0.8 x V_{DDQ}	0.9	1.0	1.4		1,2,3
	RON40pu	V_{OL}dc = 0.2 x V_{DDQ}	0.9	1.0	1.4		1,2,3
		V_{OM}dc = 0.5 x V_{DDQ}	0.9	1.0	1.1		1,2,3
		V_{OH}dc = 0.8 x V_{DDQ}	0.6	1.0	1.1		1,2,3
Mismatch between Pull-up and Pull-down, MMpupd		V_{OM}dc = 0.5 x V_{DDQ}	-10		10	%	1,2,4

Note :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$
3. Pull-down and pull-up output driver impedance are recommended to be calibrated at 0.5 X V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 X V_{DDQ} and 0.8 X V_{DDQ}
4. Measurement definition for mismatch between pull-up and pull-down, MMpupd: Measure RONpu and RONpd. both at 0.5 X V_{DDQ}:

$$MMpupd = \frac{RONpu - RONpd}{RONnom} \times 100$$

9.8.1 Output Drive Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to table 24 and 25.
ΔT = T - T(@calibration); $\Delta V = V_{DDQ} - V_{DDQ}$ (@calibration); $V_{DD} = V_{DDQ}$

*$dR_{ON}dT$ and $dR_{ON}dV$ are not subject to production test but are verified by design and characterization

[Table 24] Output Driver Sensitivity Definition

	Min	Max	Units
RONPU@V_{OHDC}	0.6 - $dR_{ON}dTH$ * $\lvert\Delta T\rvert$ - $dR_{ON}dVH$ * $\lvert\Delta V\rvert$	1.1 + $dR_{ON}dTH$ * $\lvert\Delta T\rvert$ + $dR_{ON}dVH$ * $\lvert\Delta V\rvert$	RZQ/7
RON@V_{OMDC}	0.9 - $dR_{ON}dTM$ * $\lvert\Delta T\rvert$ - $dR_{ON}dVM$ * $\lvert\Delta V\rvert$	1.1 + $dR_{ON}dTM$ * $\lvert\Delta T\rvert$ + $dR_{ON}dVM$ * $\lvert\Delta V\rvert$	RZQ/7
RONPD@$_{VOLDC}$	0.6 - $dR_{ON}dTL$ * $\lvert\Delta T\rvert$ - $dR_{ON}dVL$ * $\lvert\Delta V\rvert$	1.1 + $dR_{ON}dTL$ * $\lvert\Delta T\rvert$ + $dR_{ON}dVL$ * $\lvert\Delta V\rvert$	RZQ/7

[Table 25] Output Driver Voltage and Temperature Sensitivity

Speed Bin	gDDR3-1066/1333/1600		gDDR3-1800/2000		Units
	Min	Max	Min	Max	
$dR_{ON}dTM$	0	1.5	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	0	0.13	%/mV
$dR_{ON}dTL$	0	1.5	0	1.5	%/°C
$dR_{ON}dVL$	0	0.15	0	0.13	%/mV
$dR_{ON}dTH$	0	1.5	0	1.5	%/°C
$dR_{ON}dVH$	0	0.15	0	0.13	%/mV

9.9 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of MR1 register.
ODT is applied to the DQ,DQ, DQS/$\overline{\text{DQS}}$ and TDQS,$\overline{\text{TDQS}}$ (x8 devices only) pins.
A functional representation of the on-die termination is shown below. The individual pull-up and pull-down resistors (RTTpu and RTTpd) are defined as follows :

$$RTTpu = \frac{V_{DDQ}\text{-}Vout}{\lvert Iout \rvert}$$ under the condition that RTTpd is turned off

$$RTTpd = \frac{Vout}{\lvert Iout \rvert}$$ under the condition that RTTpu is turned off

On-Die Termination : Definition of Voltages and Currents

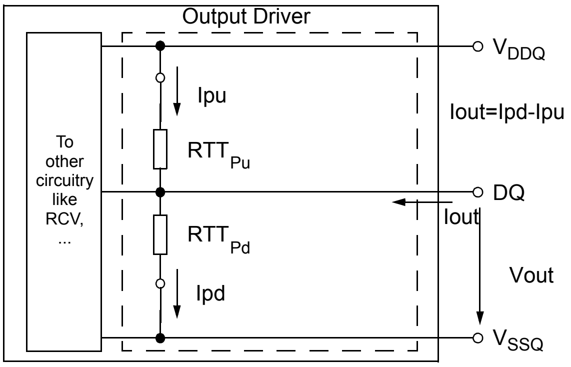


Figure 13. On-Die Termination : Definitionof Voltages and Currents

9.9.1 ODT DC electrical characteristics

Table 26 provides and overview of the ODT DC electrical characteristics. They values for RTT$_{60pd120}$, RTT$_{60pu120}$, RTT$_{120pd240}$, RTT$_{120pu240}$, RTT$_{40pd80}$, RTT$_{40pu80}$, RTT$_{30pd60}$, RTT$_{30pu60}$, RTT$_{20pd40}$, RTT$_{20pu40}$ are not specification requirements, but can be used as design guide lines:

[Table 26] ODT DC Electrical characteristics, assuming RZQ=240 ohm +/- 1% entire operating temperature range; after proper ZQ calibration.

MR1 (A9,A6,A2)	RTT	RESISTOR	Vout	Min	Nom	Max	Unit	Notes
(0,1,0)	120 ohm	RTT$_{120pd240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}	1,2,3,4
		RTT$_{120pu240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}	1,2,3,4
		RTT$_{120}$	$V_{IL(AC)}$ TO $V_{IH(AC)}$	0.9	1.0	1.6	R_{ZQ}/2	1,2,5
(0,0,1)	60 ohm	RTT$_{60pd240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}/2	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}/2	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}/2	1,2,3,4
		RTT$_{60pu240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}/2	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}/2	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}/2	1,2,3,4
		RTT$_{60}$	$V_{IL(AC)}$ TO $V_{IH(AC)}$	0.9	1.0	1.6	R_{ZQ}/4	1,2,5
(0,1,1)	40 ohm	RTT$_{40pd240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}/3	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}/3	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}/3	1,2,3,4
		RTT$_{40pu240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}/3	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}/3	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}/3	1,2,3,4
		RTT$_{40}$	$V_{IL(AC)}$ TO $V_{IH(AC)}$	0.9	1.0	1.6	R_{ZQ}/6	1,2,5
(1,0,1)	30 ohm	RTT$_{60pd240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}/4	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}/4	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}/4	1,2,3,4
		RTT$_{60pu240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}/4	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}/4	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}/4	1,2,3,4
		RTT$_{60}$	$V_{IL(AC)}$ TO $V_{IH(AC)}$	0.9	1.0	1.6	R_{ZQ}/8	1,2,5
(1,0,0)	20 ohm	RTT$_{60pd240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}/6	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}/6	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}/6	1,2,3,4
		RTT$_{60pu240}$	V_{OL}(DC) 0.2XV_{DDQ}	0.9	1.0	1.4	R_{ZQ}/6	1,2,3,4
			0.5XV_{DDQ}	0.9	1.0	1.1	R_{ZQ}/6	1,2,3,4
			V_{OH}(DC) 0.8XV_{DDQ}	0.6	1.0	1.1	R_{ZQ}/6	1,2,3,4
		RTT$_{60}$	$V_{IL(AC)}$ TO $V_{IH(AC)}$	0.9	1.0	1.6	R_{ZQ}/12	1,2,5
Deviation of V_M w.r.t $V_{DDQ/2}$, ΔV_M				-5		5	%	1,2,5,6

Note :

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$
3. Pull-down and pull-up ODT resistors are recommended to be calibrated at $0.5XV_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2XV_{DDQ}$ and $0.8XV_{DDQ}$.
4. Not a specification requirement, but a design guide line
5. Measurement definition for RTT:
   Apply $V_{IH}(ac)$ to pin under test and measure current $I(V_{IH}(ac))$, then apply $V_{IL}(ac)$ to pin under test and measure current $I(V_{IL}(ac))$ perspectively

$$RTT = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

6. Measurement definition for V_M and ΔV_M : Measure voltage (V_M) at test pin (midpoint) with no load

$$\Delta V_M = \left(\frac{2 \times V_M}{V_{DDQ}} - 1 \right) \times 100$$

9.9.2 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to table below

$\Delta T = T - T(@calibration)$; $\Delta V = V_{DDQ} - V_{DDQ}(@calibration)$; $V_{DD} = V_{DDQ}$

[Table 27] ODT Sensitivity Definition

	Min	Max	Units
RTT	$0.9 - dR_{TT}dT * \|\Delta T\| - dR_{TT}dV * \|\Delta V\|$	$1.6 + dR_{TT}dT * \|\Delta T\| + dR_{TT}dV * \|\Delta V\|$	RZQ/2,4,6,8,12

[Table 28] ODT Voltage and Temperature Sensitivity

	Min	Max	Units
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

These parameters may not be subject to production test. They are verified by design and characterization.

9.10 ODT Timing Definitions

9.10.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 14.

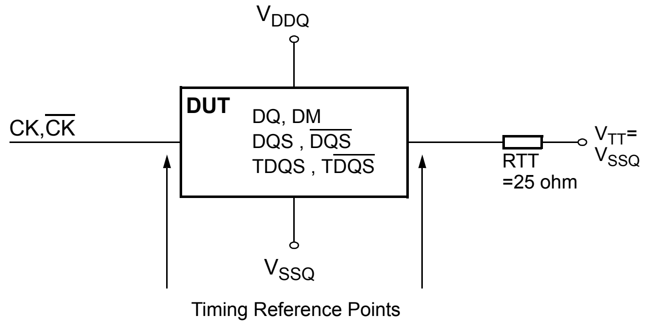


Figure 14. ODT Timing Reference Load

9.10.2 ODT Timing Definition

Definitions for t_{AON}, t_{AONPD}, t_{AOF}, t_{AOFPD} and t_{ADC} are provided in Table29 and subsequent figures. Measurement reference settings are provided in Table30.

[Table 29] ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figute
t_{AON}	Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLon	Extrapolated point at V_{SSQ}	Figure 15
t_{AONPD}	Rising edge of CK - $\overline{CK}$ with ODT being first registered high	Extrapolated point at V_{SSQ}	Figure 16
t_{AOF}	Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure 17
t_{AOFPD}	Rising edge of CK - $\overline{CK}$ with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure 18
t_{ADC}	Rising edge of CK - $\overline{CK}$ defined by the end point of ODTLcnw, ODTLcwn4 of ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively	Figure 19

[Table 30] Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V_{SW1}[V]	V_{SW2}[V]	Note
t_{AON}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AONPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOF}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOFPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{ADC}	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.30	

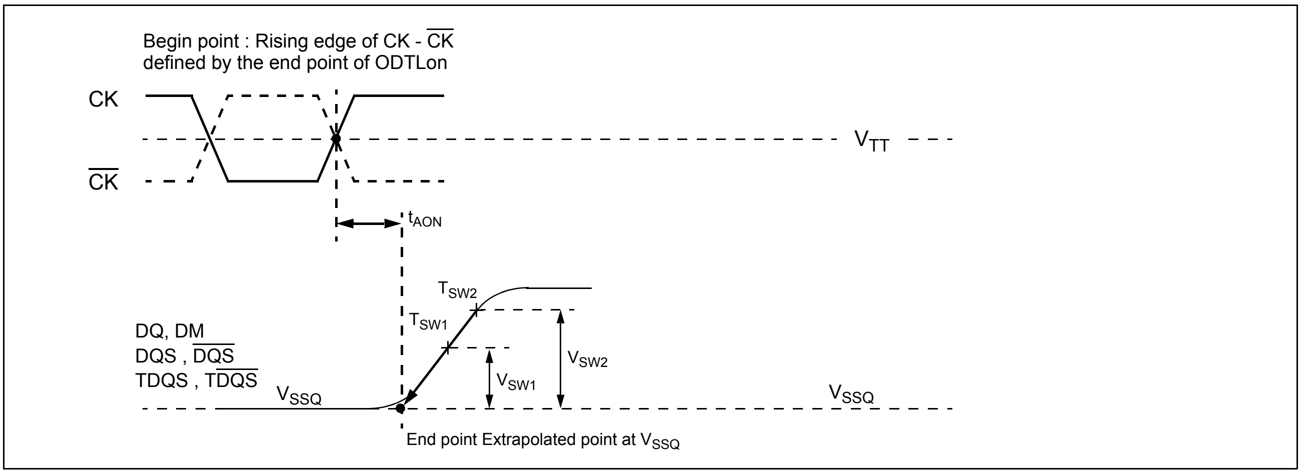

Begin point : Rising edge of CK - CK
defined by the end point of ODTLon
CK
CK
VTT
tAON
TSW2
TSW1
DQ, DM
DQS , DQS
TDQS , TDQS
VSSQ
VSW2
VSW1
VSSQ
End point Extrapolated point at VSSQ

Figure 15. Definition of tAON

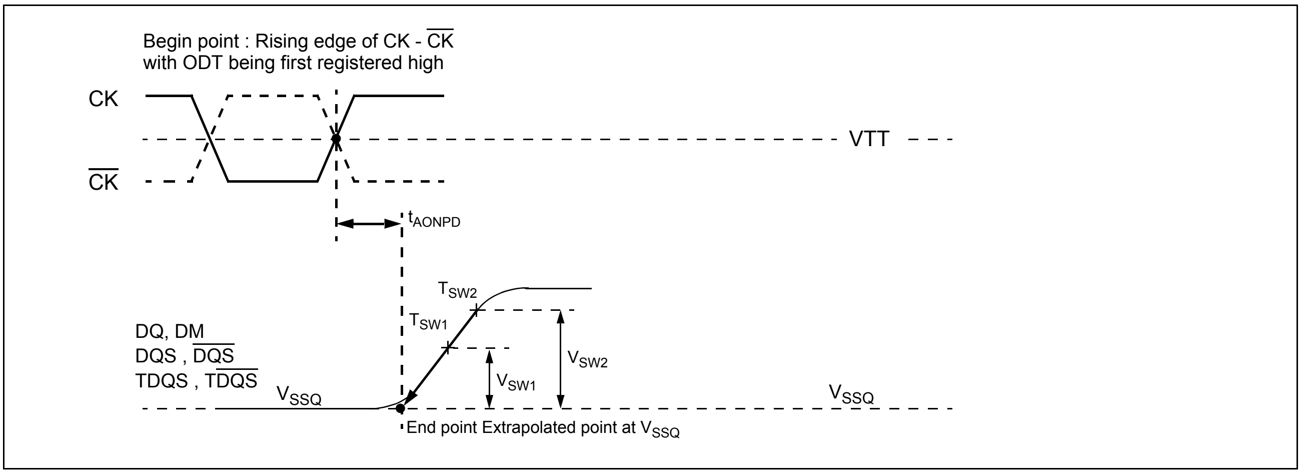

Begin point : Rising edge of CK - CK
with ODT being first registered high
CK
CK
VTT
tAONPD
TSW2
TSW1
DQ, DM
DQS , DQS
TDQS , TDQS
VSSQ
VSW2
VSW1
VSSQ
End point Extrapolated point at VSSQ

Figure 16. Definition of tAONPD

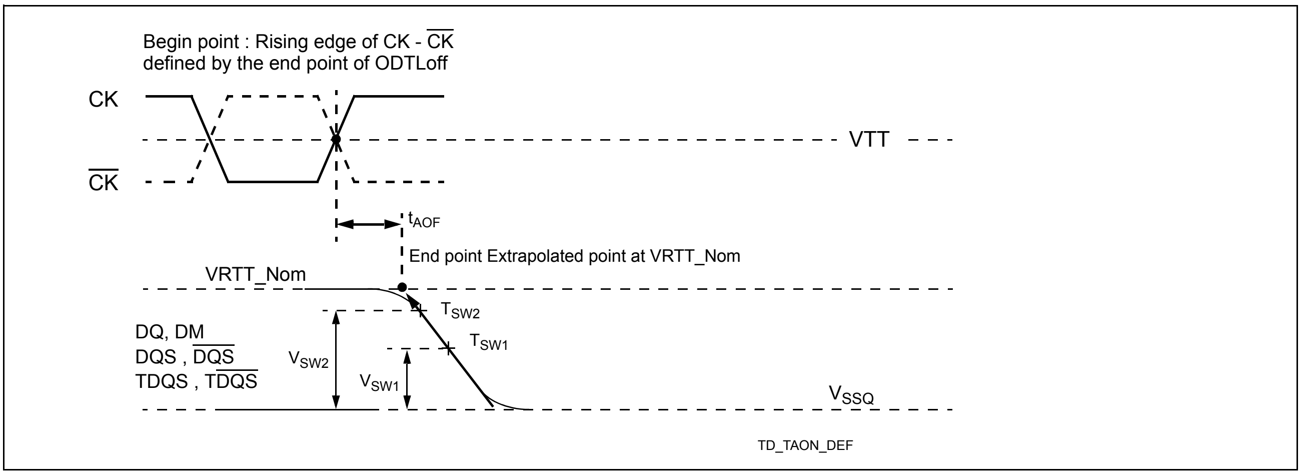

Begin point : Rising edge of CK - CK
defined by the end point of ODTLoff
CK
CK
VTT
tAOF
End point Extrapolated point at VRTT_Nom
VRTT_Nom
TSW2
TSW1
DQ, DM
DQS , DQS
TDQS , TDQS
VSW2
VSW1
VSSQ
TD_TAON_DEF

Figure 17. Definition of tAOF

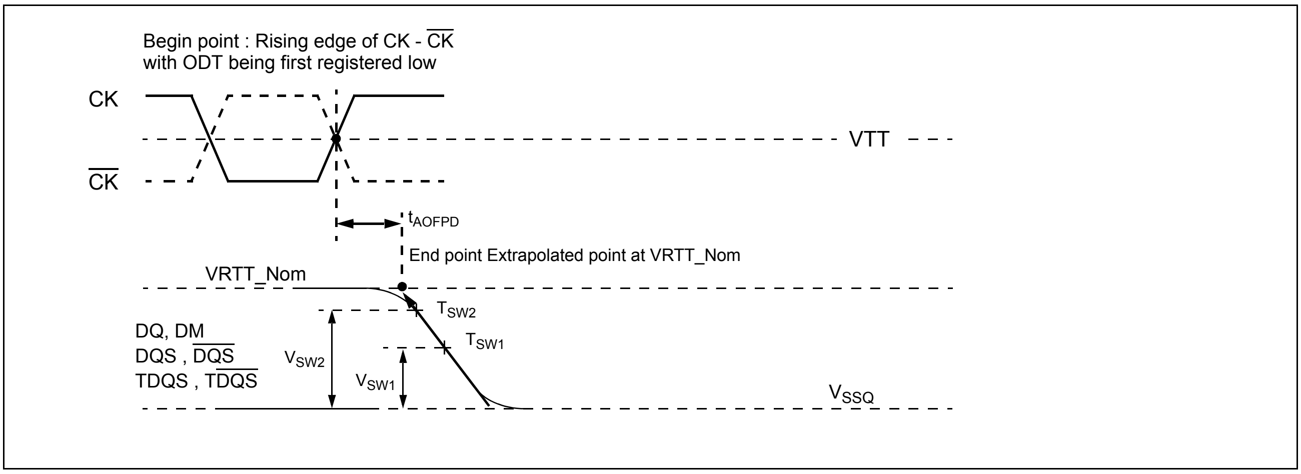

Begin point : Rising edge of CK - CK
with ODT being first registered low
CK
CK
VTT
tAOFPD
End point Extrapolated point at VRTT_Nom
VRTT_Nom
TSW2
TSW1
DQ, DM
DQS , DQS
TDQS , TDQS
VSW2
VSW1
VSSQ

Figure 18. Definition of tAOFPD

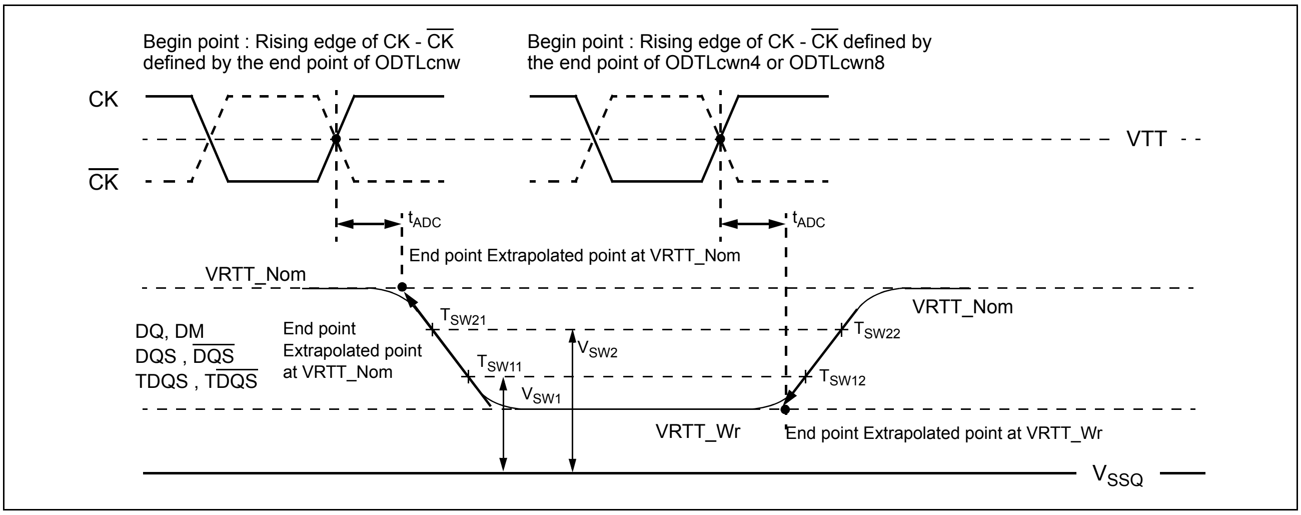

Begin point : Rising edge of CK - CK
defined by the end point of ODTLcnw
Begin point : Rising edge of CK - CK defined by
the end point of ODTLcwn4 or ODTLcwn8
CK
CK
VTT
tADC
tADC
End point Extrapolated point at VRTT_Nom
VRTT_Nom
VRTT_Nom
TSW21
TSW22
DQ, DM
DQS , DQS
TDQS , TDQS
End point
Extrapolated point
at VRTT_Nom
VSW2
TSW11
TSW12
VSW1
VRTT_Wr
End point Extrapolated point at VRTT_Wr
VSSQ

Figure 19. Definition of tADC

10.0 Idd Specification Parameters and Test Conditions

10.1 IDD Measurement Conditions

Within the tables provided further down, an overview about the IDD measurement conditions is provided as follows:

[Table 31] Overview of Tables providing IDD Measurement Conditions and DRAM Behavior

Table number	Measurement Conditions
Table 35	IDD0 and IDD1
Table 36	IDD2N, IDD2Q, IDD2P(0), IDD2P(1)
Table 37	IDD3N and IDD3P
Table 38	IDD4R, IDD4W, IDD7
Table 39	IDD7 for different speed grades and different tRRD, tFAW conditions
Table 40	IDD5B
Table 41	IDD6, IDD6ET

Within the tables about IDD measurement conditions, the following definitions are used:

- LOW is defined as $V_{IN} <= V_{ILAC}$(max.); HIGH is defined as $V_{IN} >= V_{IHAC}$(min.);
- STABLE is defined as inputs are stable at a HIGH or LOW level
- FLOATING is defined as inputs are $V_{REF} = V_{DDQ} / 2$
- SWITCHING is defined as described in the following 2 tables.

[Table 32] Definition of SWITCHING for Address and Command Input Signals

SWITCHING for Address (row, column) and Command Signals ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$) is defined as:	
Address (Row, Column):	If not otherwise mentioned the inputs are stable at HIGH or LOW during 4 clocks and change then to the opposite value (e.g. Ax Ax Ax Ax $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ Ax Ax Ax Ax ..... please see each IDDx definition for details
Bank address:	If not otherwise mentioned the bank addresses should be switched like the row/column addresses - please see each IDDx definition for details
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$):	Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } := {HIGH, LOW, LOW, LOW} Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ } := {HIGH, HIGH,HIGH,HIGH} Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ ... If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R) the Background Pattern Command is substituted by the respective $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ levels of the necessary command. See each IDDx definition for details and figures as examples.

[Table 33] Definition of SWITCHING for Data (DQ)

SWITCHING for Data (DQ) is defined as	
Data (DQ)	Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock; see each IDDx definition for exceptions from this rule and for further details. See figures as examples.
Data Masking (DM)	NO Switching; DM must be driven LOW all the time

Timing parameters are listed in the following table:

[Table 34] For IDD testing the following parameters are utilized.

Parameter Bin	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	Unit
	7-7-7	9-9-9	11-11-11	12-12-12	13-13-13	
t_{CKmin}(IDD)	1.875	1.5	1.25	1.1	1.0	ns
CL(IDD)	7	9	11	12	13	tCK
t_{RCDmin}(IDD)	13.125	13.5	13.75	13.2	13	ns
t_{RCmin}(IDD)	50.625	49.5	48.75	47.2	46	ns
t_{RASmin}(IDD)	37.5	36	35	34	33	ns
t_{RPmin}(IDD)	13.125	13.5	13.75	13.2	13	ns
t_{FAW}(IDD)	50.625	45	40	40	40	ns
t_{RRD}(IDD)	11.25	7.5	7.5	7.5	7.5	ns
t_{RFC}(IDD) - 1Gb	110	110	110	110	110	ns

The following conditions apply:

1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by AC Parametric test conditions.
3. IDD parameters are specified with ODT and output buffer disabled (MR1 Bit A12).

[Table 35] IDD Measurement Conditions for IDD0 and IDD1

Current	IDD0	IDD1
Name	Operating Current 0 -> One Bank Activate -> Precharge	Operating Current 1 -> One Bank Activate -> Read -> Precharge
Measurement Condition		
Timing Diagram Example		Figure 20
CKE	HIGH	HIGH
External Clock	on	on
t_{CK}	t_{CK}min(IDD)	t_{CK}min(IDD)
t_{RC}	t_{RC}min(IDD)	t_{RC}min(IDD)
t_{RAS}	t_{RAS}min(IDD)	t_{RAS}min(IDD)
t_{RCD}	n.a.	t_{RCD}min(IDD)
t_{RRD}	n.a.	n.a.
CL	n.a.	CL(IDD)
AL	n.a.	0
$\overline{CS}$	HIGH between. Activate and Precharge Commands	HIGH between Activate, Read and Precharge
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table 32; only exceptions are Activate and Precharge commands; example of IDD0 pattern: A0 D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ **P0** (gDDR3-1333: tRAS = 36ns between (A)ctivate and (P)recharge to bank 0 ; Definition of D and D: see Table 2) Definition of D and $\overline{D}$: See table ##.	SWITCHING as described in Table 32; only exceptions are Activate, Read and Precharge commands; example of IDD1 pattern: A0 D $\overline{D}$ $\overline{D}$ D R0 D $\overline{D}$ $\overline{D}$ DD $\overline{D}$ $\overline{D}$ DD $\overline{D}$ **P0** (gDDR3-1333 -9-9-9: tRCD = 13.5ns between (A)ctivate and (R)ead to bank 0 ; Definition of D and D: see Table 2) Definition of D and $\overline{D}$: See table ##.
Row, Column Addresses	Row addresses SWITCHING as described in Table 32; Address Input A10 must be LOW all the time!	Row addresses SWITCHING as described in Table 32; Address Input A10 must be LOW all the time!
Bank Addresses	bank address is fixed (bank 0)	bank address is fixed (bank 0)
Data I/O	SWITCHING as described in Table 33	Read Data: output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1". When there is no read data burst from DRAM the DQ I/O should be FLOATING.
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
Rtt_NOM, Rtt_WR	disabled	disabled
Burst length	n.a.	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	one ACT-PRE loop	one ACT-RD-PRE loop
Idle banks	all other	all other
Precharge Power Down Mode / Mode Register Bit 12	n.a.	n.a.

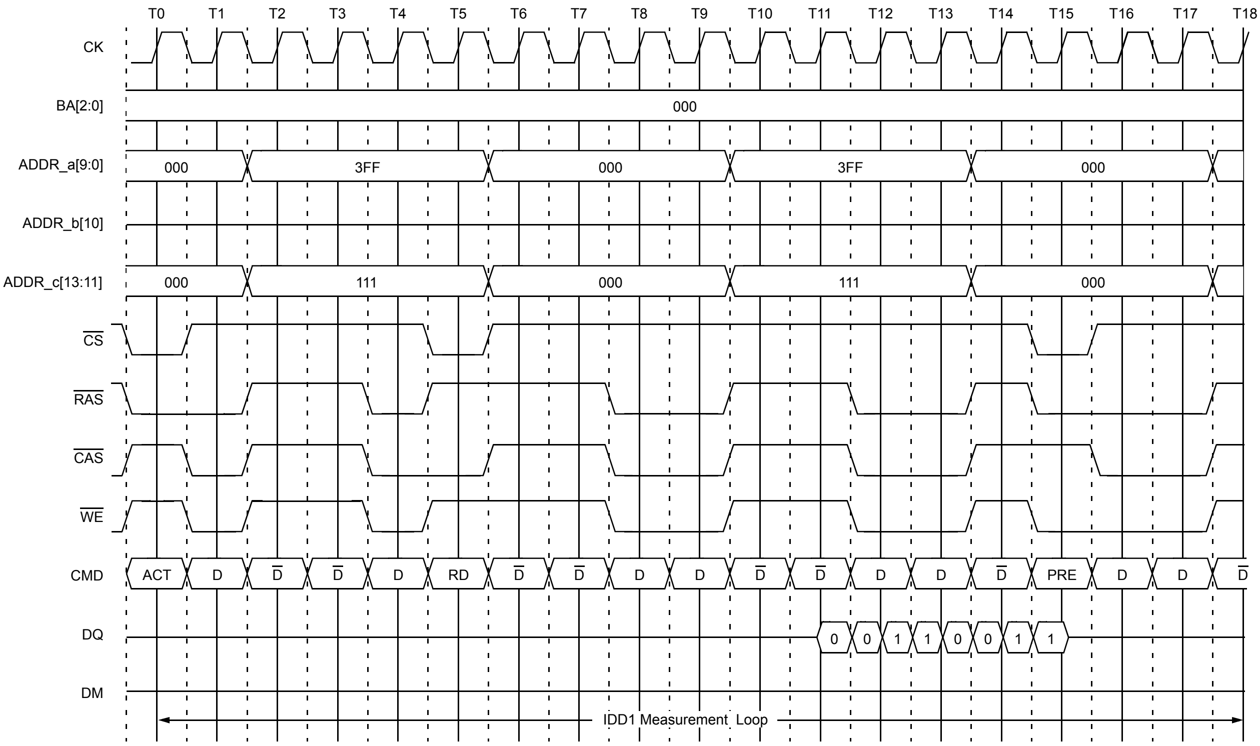

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
CK
BA[2:0]
000
ADDR_a[9:0]
000
3FF
000
3FF
000
ADDR_b[10]
ADDR_c[13:11]
000
111
000
111
000
CS
RAS
CAS
WE
CMD
ACT
D
D̄
D̄
D
RD
D̄
D̄
D
D
D̄
D̄
D
D
D̄
PRE
D
D
D̄
DQ
0
0
1
1
0
0
1
1
DM
IDD1 Measurement Loop

Figure 20.
IDD1 Example (gDDR3-1333-999, 1Gb x16): Data DQ is shown but the output buffer should be switched off (per MR1 Bit A12 ="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.

[Table 36] IDD Measurement Conditions for IDD2N, IDD2P(1), IDD2P(0) and IDD2Q

Current	IDD2N	IDD2P(1) a	IDD2P(0)	IDD2Q
Name	Precharge Standby Current	Precharge Power Down Current Fast Exit - MRS A12 Bit = 1	Precharge Power Down Current Slow Exit - MRS A12 Bit = 0	Precharge Quiet Standby Current
Measurement Condition				
Timing Diagram Example	Figure 21			
CKE	HIGH	LOW	LOW	LOW
External Clock	on	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	n.a.	n.a.
t_{RAS}	n.a.	n.a.	n.a.	n.a.
t_{RCD}	n.a.	n.a.	n.a.	n.a.
t_{RRD}	n.a.	n.a.	n.a.	n.a.
CL	n.a.	n.a.	n.a.	n.a.
AL	n.a.	n.a.	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE	HIGH	STABLE
Bank Address, Row Addr. and Command Inputs	SWITCHING as described in Table 32	STABLE	STABLE	STABLE
Data inputs	SWITCHING	FLOATING	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1	off / 1
Rtt_NOM, Rtt_WE	disabled	disabled	disabled	disabled
Burst length	n.a.	n.a.	n.a.	n.a.
Active banks	none	none	none	none
Idle banks	all	all	all	all
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	Fast Exit / 1 (any valid command after tXP[1])	Slow Exit / 0 Slow exit (RD and ODT commands must satisfy tXPDLL-AL)	n.a.

Note :

1. In gDDR3 the MRS Bit 12 defines DLL on/off behavior ONLY for precharge power down. There are 2 different Precharge Power Down states possible : one with DLL on (fast exit, bit 12 = 1) and one with DLL off (slow exit, bit 12 = 0).
2. Because it is an exit after precharge power down the valid commands are: Activate, Refresh, Mode-Register Set, Enter - Self Refresh.

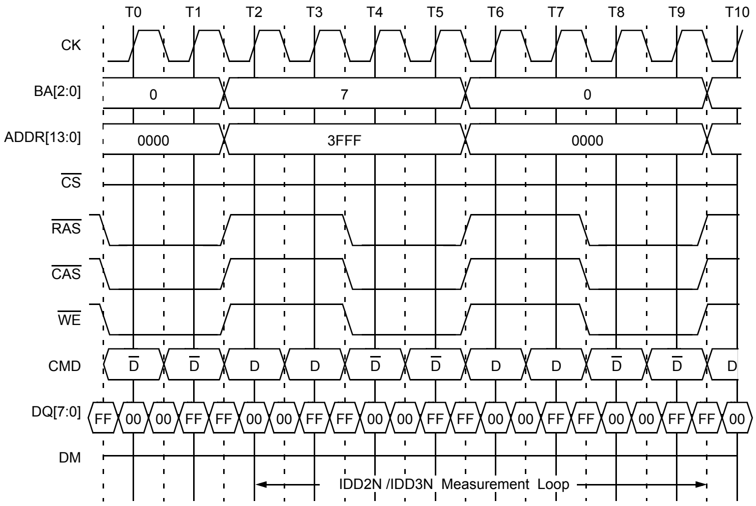

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CK
BA[2:0]
0
7
0
ADDR[13:0]
0000
3FFF
0000
$\overline{CS}$
$\overline{RAS}$
$\overline{CAS}$
$\overline{WE}$
CMD
$\overline{D}$
$\overline{D}$
D
D
$\overline{D}$
$\overline{D}$
D
D
$\overline{D}$
$\overline{D}$
D
DQ[7:0]
FF 00 00 FF FF 00 00 FF FF 00 00 FF FF 00 00 FF FF 00 00 FF FF 00
DM
IDD2N /IDD3N Measurement Loop

Figure 21. IDD2N /IDD3N Example

[Table37] IDD Measurement Conditions for IDD3N and IDD3P(fast exit)

Current	IDD3N	IDD3P
Name	Active Standby Current	Active Power-Down Current[a] Always Fast Exit
Measurement Condition		
Timing Diagram Example	Figure 21	
CKE	HIGH	LOW
External Clock	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	HIGH	STABLE
Addr. and cmd Inputs	SWITCHING as described in Table 32	STABLE
Data inputs	SWITCHING as described in Table 33	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
Rtt_NOM, Rtt_WE	disabled	disabled
Burst length	n.a.	n.a.
Active banks	all	all
Idle banks	none	none
Precharge Power Down Mode / Mode Register Bit [a]	n.a.	n.a. (Active Power Down Mode is always "Fast Exit" with DLL on

Note :

1. gDDR3 will offer only ONE active power down mode with DLL on (-> fast exit). MRS bit 12 will not be used for active power down. Instead bit A12 will be used to switch between two different precharge power down modes.

[Table 38] IDD Measurement Conditions for IDD4R, IDD4W and IDD7

Current	IDD4R	IDD4W	IDD7
Name	Operating Current Burst Read	Operating Current Burst Write	All Bank Interleave Read Current
Measurement Condition			
Timing Diagram Example	Figure 22		
CKE	HIGH	HIGH	HIGH
External Clock	on	on	on
t_{CK}	t_{CKmin}(IDD)	t_{CKmin}(IDD)	t_{CKmin}(IDD)
t_{RC}	n.a.	n.a.	t_{RCmin}(IDD)
t_{RAS}	n.a.	n.a.	t_{RASmin}(IDD)
t_{RCD}	n.a.	n.a.	t_{RCDmin}(IDD)
t_{RRD}	n.a.	n.a.	t_{RRDmin}(IDD)
CL	CL(IDD)	CL(IDD)	CL(IDD)
AL	0	0	t_{RCDmin}-1t_{CK}
$\overline{CS}$	HIGH btw. valid cmds	HIGH btw. valid cmds	HIGH btw. valid cmds
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	SWITCHING as described in Table 32; exceptions are Read commands => IDD4R Pattern: $R0D\overline{DD}R1D\overline{gDDR3}D\overline{gDDR3}D\overline{DD}R4$ ..... Rx = Read from bank x; Definition of D and D: see Table 32	SWITCHING as described in Table 32; exceptions are Write commands => IDD4W Pattern: $W0D\overline{DD}W1D\overline{DD}W2D\overline{DD}W3D\overline{DD}$ W4 ... Wx = Write to bank x; Definition of D and D: see Table 32	For patterns see Table 39
Row, Column Addresses	column addresses SWITCHING as described in Table 32; Address Input A10 must be LOW all the time!	column addresses SWITCHING as described in Table 32; Address Input A10 must be LOW all the time!	STABLE during DESELECTs
Bank Addresses	bank address cycling (0 ->1 -> 2 -> 3 ...)	bank address cycling (0 ->1 -> 2 -> 3 ...)	bank address cycling (0 ->1 -> 2 -> 3 ...), see pattern in Table 9
DQ I/O	Seamless Read Data Burst (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1".	Seamless Write Data Burst (BL8): input data switches every clock, which means that Write data is stable during one clock cycle. DM is low all the time.	Read Data (BL8): output data switches every clock, which means that Read data is stable during one clock cycle. To achieve Iout = 0mA the output buffer should be switched off by MR1 Bit A12 set to "1".
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1	off / 1
Rtt_NOM, Rtt_WE	disabled	disabled	disabled
Burst length	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}	8 fixed / MR0 Bits [A1, A0] = {0,0}
Active banks	all	all	all
Idle banks	none	none	none
Precharge Power Down Mode / Mode Register Bit	n.a.	n.a.	n.a.

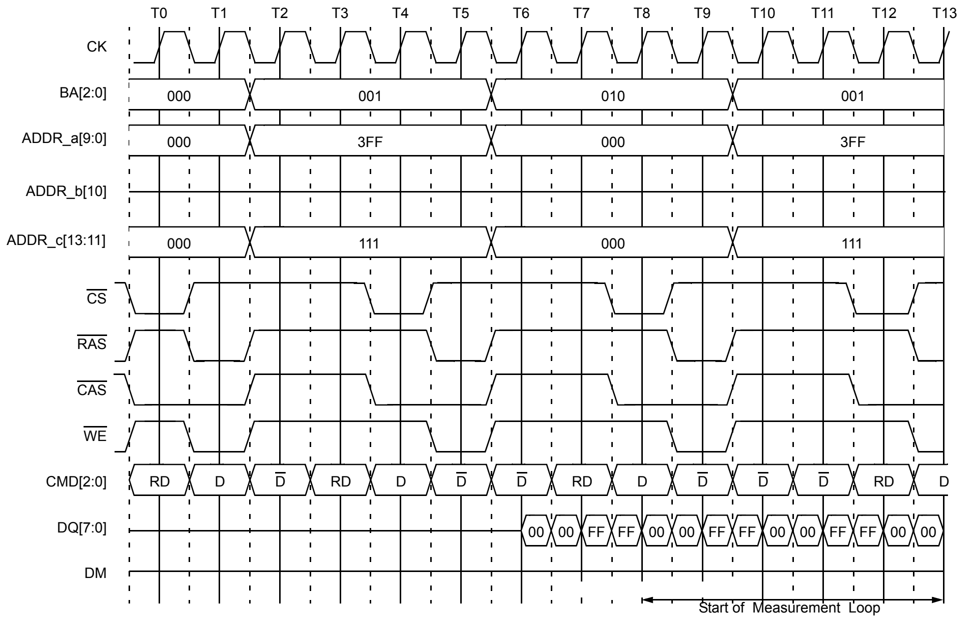

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
CK
BA[2:0]
000
001
010
001
ADDR_a[9:0]
000
3FF
000
3FF
ADDR_b[10]
ADDR_c[13:11]
000
111
000
111
CS
RAS
CAS
WE
CMD[2:0]
RD
D
D̄
RD
D
D̄
D̄
RD
D
D̄
D̄
D̄
RD
D
DQ[7:0]
00
00
FF
FF
00
00
FF
FF
00
00
FF
FF
00
00
DM
Start of Measurement Loop

Figure 22
IDD4R Example (gDDR3-1333(999)): data DQ is shown but the output buffer should be switched off (per MR1 Bit A12="1") to achieve Iout = 0mA. Address inputs are split into 3 parts.

[Table 39] IDD7 Pattern for different Speed Grades and different tRRD, tFAW conditions

Speed	Bin	tFAW	tFAW	tRRD	tRRD	IDD7 Pattern
Mb/s		[ns]	[CLK]	[ns]	[CLK]	
1333	all	45	30	7.5	5	A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3RA3 D D D D D D D D D D D D D A4 RA4 D D DA5 RA5 D D D A6 RA6 D D D A7 RA7 D D D DD D D D D D D D D
1600	all	40	32	7.5	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D DD D A3 RA3 D D D D D D D D D D D D A4 RA4D D D D A5 RA5 D D D D A6 RA6 D D D D A7RA7 D D D D D D D D D D D D
1800	all	40	32	7.5	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D DD D A3 RA3 D D D D D D D D D D D D A4 RA4D D D D A5 RA5 D D D D A6 RA6 D D D D A7RA7 D D D D D D D D D D D D
2000	all	40	32	7.5	6	A0 RA0 D D D D A1 RA1 D D D D A2 RA2 D DD D A3 RA3 D D D D D D D D D D D D A4 RA4D D D D A5 RA5 D D D D A6 RA6 D D D D A7RA7 D D D D D D D D D D D D

Note :
1. A0 = Activation of Bank 0; RA0 = Read with Auto-Precharge of Bank 0; D = Deselect

[Table 40] IDD Measurement Conditions for IDD5B

Current	IDD5B
Name	Burst Refresh Current
Measurement Condition	
CKE	HIGH
External Clock	on
t_{CK}	t_{CKmin}(IDD)
t_{RC}	n.a.
t_{RAS}	n.a.
t_{RCD}	n.a.
t_{RRD}	n.a.
t_{RFC}	t_{RFCmin}(IDD)
CL	n.a.
AL	n.a.
$\overline{CS}$	HIGH btw. valid cmds
Addr. and cmd Inputs	SWITCHING
Data inputs	SWITCHING
Output Buffer DQ,DQS / MR1 bit A12	off / 1
Rtt_NOM, Rtt_WE	disabled
Burst length	n.a.
Active banks	Refresh command every t_{RFC}=t_{RFC}min
Idle banks	none
Precharge Power Down Mode / Mode Register Bit	n.a.

[Table 41] IDD Measurement Conditions for IDD6 and IDD6ET

Current	IDD6	IDD6ET
Name	Self-Refresh Current Normal Temperature Range TCASE = 0 .. 85°C	Self-Refresh Current Extended Temperature Range a TCASE = 0 .. 95°C
Measurement Condition		
Temperature	TCASE = 85°C	TCASE = 95°C
Auto Self Refresh(ASR) / MR2 Bit A6	Disabled / "0"	Disabled / "0"
Self Refresh Temperature Range (SRT) / MR2 Bit A7	Normal / "0"	Enabled / "1"
CKE	LOW	LOW
External Clock	OFF; CK and $\overline{CK}$ at LOW	OFF; CK and $\overline{CK}$ at LOW
t_{CK}	n.a.	n.a.
t_{RC}	n.a.	n.a.
t_{RAS}	n.a.	n.a.
t_{RCD}	n.a.	n.a.
t_{RRD}	n.a.	n.a.
CL	n.a.	n.a.
AL	n.a.	n.a.
$\overline{CS}$	FLOATING	FLOATING
Command Inputs ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	FLOATING	FLOATING
Row, Column Addresses	FLOATING	FLOATING
Bank Addresses	FLOATING	FLOATING
Data I/O	FLOATING	FLOATING
Output Buffer DQ,DQS / MR1 bit A12	off / 1	off / 1
Rtt_NOM, Rtt_WR	disabled	disabled
Burst length	n.a.	n.a.
Active banks	all during self-refresh actions	all during self-refresh actions
Idle banks	all btw. Self-Refresh actions	all btw. Self-Refresh actions
Precharge Power Down Mode / Mode Register Bit 12	n.a.	n.a.

Note :
1 .Users should refer to the DRAM supplier datasheet and/or the DIMM SPD to determine if gDDR3 SDRAM devices support the following options referred to in this material

[Table 42] IDD6 current definition

Symbol	Parameter/Condition
IDD6	Normal Temperature Range Self-Refresh Current : CKE< 0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 setting A6=0 and A7=0.
IDD6ET	Extended Temperature Range SElf-Refresh Current: CKE<0.2V; external clock off, CK and $\overline{CK}$ at 0V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled. Applicable for MR2 settings A6=0 and A7=1.

10.2 IDD Specifications definition

[Table 43] IDD Specification

Symbol	Conditions	Units	Notes
IDD0	**Operating one bank active-precharge current**; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD1	**Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC (IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD2P	**Precharge power-down current**; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2Q	**Precharge quiet standby current**; All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD2N	**Precharge standby current**; All banks idle; tCK = tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD3P	**Active power-down current**; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	mA	
IDD3N	**Active standby current**; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD4W	**Operating burst write current**; All banks open, Continuous burst writes; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING;Data bus inputs are SWITCHING	mA	
IDD4R	**Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	mA	
IDD5B	**Burst refresh current**; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	mA	
IDD6	**Self refresh current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	mA	
IDD6ET	**Extended Temperature Range Self-Refresh Current**; CK and $\overline{CK}$ at 0V; CKE ≤ 0.2V; Other control and address inputs are FLOATING; Data Bus inputs are FLOATING, PASR disabled, Applicable for MR2 setting A6=0 and A7=1	mA	
IDD7	**Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 8, CL = CL(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R;	mA	

11.0 1Gb gDDR3 SDRAM E-die IDD Spec Table

[Table 44] IDD Specification for 1Gb gDDR3 E-die

Symbol	64Mx16 (K4W1G1646E)					Unit	Notes
	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000		
	7-7-7	9-9-9	11-11-11	12-12-12	13-13-13		
IDD0	65	70	80	85	90	mA	
IDD1	85	90	105	110	115	mA	
IDD2P-F	25	25	25	25	25	mA	
IDD2P-S	10	10	10	10	10	mA	
IDD2N	35	40	40	40	40	mA	
IDD2Q	35	40	40	40	40	mA	
IDD3P-F	30	35	35	40	40	mA	
IDD3N	45	50	55	58	60	mA	
IDD4R	130	160	200	205	210	mA	
IDD4W	130	155	195	200	205	mA	
IDD5	150	160	160	185	200	mA	
IDD6	10	10	10	10	10	mA	
IDD7	200	240	290	300	310	mA	

12.0 Input/Output Capacitance

[Table 45] Input / Output Capacitance

Parameter	Symbol	gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1800		gDDR3-2000		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CIO	1.5	2.7	1.5	2.5	1.5	2.3	1.4	2.2	1.4	2.1	pF	1,2,3
Input capacitance (CK and $\overline{CK}$)	CCK	0.8	1.6	0.8	1.4	0.8	1.4	TBD	TBD	TBD	TBD	pF	2,3
Input capacitance delta (CK and $\overline{CK}$)	CDCK	0	0.15	0	0.15	0	0.15	TBD	TBD	TBD	TBD	pF	2,3,4
Input capacitance (All other input-only pins)	CI	0.75	1.5	0.75	1.3	0.75	1.3	TBD	TBD	TBD	TBD	pF	2,3,6
Input capacitance delta (DQS and $\overline{DQS}$)	CDDQS	0	0.2	0	0.15	0	0.15	TBD	TBD	TBD	TBD	pF	2,3,5
Input capacitance delta (All control input-only pins)	CDI_CTRL	-0.5	0.3	-0.4	0.2	-0.4	0.2	TBD	TBD	TBD	TBD	pF	2,3,7,8
Input capacitance delta (all ADD and CMD input-onlypins)	CDI_ADD_CMD	-0.5	0.5	-0.4	0.4	-0.4	0.4	TBD	TBD	TBD	TBD	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	TBD	TBD	TBD	TBD	pF	2,3,11
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	TBD	TBD	TBD	TBD	pF	2, 3, 12

Note :

1. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins floating (except the pin under test, CKE, $\overline{RESET}$ and ODT as necessary). $V_{DD}=V_{DDQ}=1.5V$, $V_{BIAS}=V_{DD/2}$ and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of CCK-$\overline{CCK}$
5. Absolute value of CIO(DQS)-CIO($\overline{DQS}$)
6. CI applies to ODT, $\overline{CS}$, CKE, A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
7. CDI_CTRL applies to ODT, $\overline{CS}$ and CKE
8. CDI_CTRL=CI(CTRL)-0.5*(CI(CLK)+CI($\overline{CLK}$))
9. CDI_ADD_CMD applies to A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$
10. CDI_ADD_CMD=CI(ADD_CMD) - 0.5*(CI(CLK)+CI($\overline{CLK}$))
11. CDIO=CIO(DQ,DM) - 0.5*(CIO(DQS)+CIO($\overline{DQS}$))
12. Maximum external load capacitance on ZQ pin: 5pF

13.0 Electrical Characteristics and AC timing for gDDR3-1066 to gDDR3-2000

13.1 Clock specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the gDDR3 SDRAM device.

13.1.1 Definition for tCK (avg)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$\left(\sum_{j=1}^{N} tCKj \right) \Big/ N \qquad N=200$$

13.1.2 Definition for tCK (abs)

tCK(abs) is the absolute clock period, as measured from one rising edge to the next consecutive rising edge. tCK(abs) is not subject to production test.

13.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses:
tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses:

$$\left(\sum_{j=1}^{N} tCHj \right) \Big/ N \times tCK(avg) \qquad N=200 \qquad\qquad \left(\sum_{j=1}^{N} tCLj \right) \Big/ N \times tCK(avg) \qquad N=200$$

13.1.4 Definition for note for tJIT(per), tJIT(per,lck)

tJIT(per) is defined as the largest deviation of any single tCK from tCK(avg). tJIT(per) = min/max of {tCKi-tCK(avg) where i=1 to 200}
tJIT(per) defines the single period jitter when the DLL is already locked.
tJIT(per,lck) uses the same definition for single period jitter, during the DLL locking period only.
tJIT(per) and tJIT(per,lck) are not subject to production test.

13.1.5 Definition for tJIT(cc), tJIT(cc,lck)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles: tJIT(cc) = Max of {tCKi+1-tCKi}
tJIT(cc) defines the cycle to cycle jitter when the DLL is already locked.
tJIT(cc,lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only.
tJIT(cc) and tJIT(cc,lck) are not subject to production test.

13.1.6 Definition for tERR(nper)

tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg). tERR is not subject to production test.

13.2 Refresh Parameters by Device Density

[Table 46] Refresh parameters by device density

Parameter	Symbol		1Gb	Units
All Bank Refresh to active/refresh cmd time	tRFC		110	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	μs
		85 °C < T_{CASE} ≤ 95°C	3.9	μs

13.3 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin

gDDR3 SDRAM Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

[Table 44] DDR3-1066 Speed Bins

Speed			gDDR3-1066		Units	Note
CL-nRCD-nRP			7 - 7 - 7			
Parameter		Symbol	min	max		
Internal read command to first data		tAA	13.125	20	ns	
ACT to internal read or write delay time		tRCD	13.125	-	ns	
PRE command period		tRP	13.125	-	ns	
ACT to ACT or REF command period		tRC	50.625	-	ns	
ACT to PRE command period		tRAS	37.5	9*tREFI	ns	11
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	ns	1,2,3,6
	CWL = 6	tCK(AVG)	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3,4
CL = 8	CWL = 5	tCK(AVG)	Reserved		ns	4
	CWL = 6	tCK(AVG)	1.875	<2.5	ns	1,2,3
Supported CL Settings			6,7,8		nCK	
Supported CWL Settings			5,6		nCK	

[Table 47] gDDR3-1333 Speed Bins

Speed			**gDDR3-1333**		**Units**	**Note**
CL-nRCD-nRP			**9 -9 - 9**			
Parameter		**Symbol**	**min**	**max**		
Internal read command to first data		t_{AA}	13.5	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.5	-	ns	
PRE command period		t_{RP}	13.5	-	ns	
ACT to ACT or REF command period		t_{RC}	49.5	-	ns	
ACT to PRE command period		t_{RAS}	36	9*tREFI	ns	11
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 6,7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings			6,8,9,(10)		n_{CK}	
Supported CWL Settings			5,6,7		n_{CK}	

[Table 48] gDDR3-1600 Speed Bins

Speed			gDDR3-1600		Units	Note
CL-nRCD-nRP			11 -11 - 11			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.75	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.75	-	ns	
PRE command period		t_{RP}	13.75	-	ns	
ACT to ACT or REF command period		t_{RC}	48.75	-	ns	
ACT to PRE command period		t_{RAS}	35	9*tREFI	ns	11
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 7,8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	<2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1,2,3
Supported CL Settings			6,8,10,11		n_{CK}	
Supported CWL Settings			5,6,7,8		n_{CK}	

[Table 49] gDDR3-1800 Speed Bins

Speed			gDDR3-1800		Units	Note
CL-nRCD-nRP			12 -12 -12			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.2	20.0	ns	
ACT to internal read or write delay time		t_{RCD}	13.2	—	ns	
PRE command period		t_{RP}	13.2	—	ns	
ACT to ACT or REF command period		t_{RC}	47.2	—	ns	
ACT to PRE command period		t_{RAS}	34	9 x tREFI	ns	11
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4,9
	CWL = 6,7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 9
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 4, 9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 9
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4,9
	CWL = 8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 4, 9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4,9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	ns	1, 2, 3, 4, 9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	ns	1, 2, 3, 4
Supported CL Settings		Sup_CL	6, 7, 8, 9, 10, 11, 12		nCK	
Supported CWL Settings		Sup_CWL	5, 6, 7, 8, 9		nCK	

[Table 50] gDDR3-2000 Speed Bins

Speed Bin			gDDR3-2000		Unit	Note
CL - nRCD - nRP			13-13-13			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13	20.0	ns	
ACT to internal read or write delay time		t_{RCD}	13	—	ns	
PRE command period		t_{RP}	13	—	ns	
ACT to ACT or REF command period		t_{RC}	46	—	ns	
ACT to PRE command period		t_{RAS}	33	9 x tREFI	ns	11
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 4, 10
	CWL = 6,7,8,9,10	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3,10
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4,10
	CWL = 7,8,9,10	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 10
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 10
	CWL = 8,9,10	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3,10
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 10
	CWL = 8,9,10	$t_{CK(AVG)}$	Reserved		ns	4
CL = 9	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 10
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 10
	CWL = 9,10	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 10
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	ns	1, 2, 3, 4,10
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 10
	CWL = 10	$t_{CK(AVG)}$	Reserved		ns	4
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	< 1.5	ns	1, 2, 3, 10
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 10
	CWL = 10	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	ns	1, 2, 3, 4, 10
	CWL = 10	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 13	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	< 1.25	ns	1, 2, 3, 10
	CWL = 10	$t_{CK(AVG)}$	0.935	< 1.07	ns	1, 2, 3, 4
Supported CL Settings		Sup_CL	5, 6, 7, 8, 9, 10, 11, 12, 13		nCK	
Supported CWL Settings		Sup_CWL	5, 6, 7, 8, 9, 10		nCK	

Note :

Absolute Specification (T_{OPER};V_{DDQ}=V_{DD}=1.5V +/- 0.075V);

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfiled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CLSELECTED and round the resulting tCK(AVG) down to the next valid speed bin limit (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CLSELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any gDDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any gDDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any gDDR3-1800 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. Any gDDR3-2000 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
11. tREFI depends on T_{OPER}

13.3 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin

[Table 51] Timing Parameters by Speed Bin

Speed		gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1800		gDDR3-2000		Units	Note
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing													
Minimum Clock Cycle Time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	-	8	-	8	-	8	-	8	-	ns	6
Average Clock Period	$t_{CK(avg)}$											ps	
Clock Period	$t_{CK(abs)}$	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps	
Average high pulse width	$t_{CH(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	
Average low pulse width	$t_{CL(avg)}$	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	$t_{CK(avg)}$	
Clock Period Jitter	$tJIT_{(per)}$	-90	90	-80	80	-70	70	-60	60	-40	40	ps	
Clock Period Jitter during DLL locking period	$tJIT_{(per,\ lck)}$	-80	80	-70	70	-60	60	-50	50	-40	40	ps	
Cycle to Cycle Period Jitter	$tJIT_{(cc)}$	180		160		140		TBD		TBD		ps	
Cycle to Cycle Period Jitter during DLL locking period	$tJIT_{(cc,\ lck)}$	160		140		120		TBD		TBD		ps	
Cumulative error across 2 cycles	$t_{ERR(2per)}$	- 132	132	- 118	118	-103	103	TBD	TBD	TBD	TBD	ps	
Cumulative error across 3 cycles	$t_{ERR(3per)}$	- 157	157	- 140	140	-122	122	TBD	TBD	TBD	TBD	ps	
Cumulative error across 4 cycles	$t_{ERR(4per)}$	- 175	175	- 155	155	-136	136	TBD	TBD	TBD	TBD	ps	
Cumulative error across 5 cycles	$t_{ERR(5per)}$	- 188	188	- 168	168	-147	147	TBD	TBD	TBD	TBD	ps	
Cumulative error across 6 cycles	$t_{ERR(6per)}$	- 200	200	- 177	177	-155	155	TBD	TBD	TBD	TBD	ps	
Cumulative error across 7 cycles	$t_{ERR(7per)}$	- 209	209	- 186	186	-163	163	TBD	TBD	TBD	TBD	ps	
Cumulative error across 8 cycles	$t_{ERR(8per)}$	- 217	217	- 193	193	-169	169	TBD	TBD	TBD	TBD	ps	
Cumulative error across 9 cycles	$t_{ERR(9per)}$	- 224	224	- 200	200	-175	175	TBD	TBD	TBD	TBD	ps	
Cumulative error across 10 cycles	$t_{ERR(10per)}$	- 231	231	- 205	205	-180	180	TBD	TBD	TBD	TBD	ps	
Cumulative error across 11 cycles	$t_{ERR(11per)}$	- 237	237	- 210	210	-184	184	TBD	TBD	TBD	TBD	ps	
Cumulative error across 12 cycles	$t_{ERR(12per)}$	- 242	242	- 215	215	-188	188	TBD	TBD	TBD	TBD	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	$t_{ERR(nper)}$											ps	24
Absolute clock HIGH pulse width	$t_{CH(abs)}$	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	$t_{CK(avg)}$	25
Absolute clock Low pulse width	$t_{CL(abs)}$	0.43	-	0.43	-	0.43	-	0.43	-	0.43	-	$t_{CK(avg)}$	26
Data Timing													
DQS,$\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	150	-	125	-	100	-	86	-	75	ps	13
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.38	-	0.38	-	0.38	-	0.38	-	0.38	-	$t_{CK(avg)}$	13, g
DQ low-impedance time from CK, $\overline{CK}$	$t_{LZ(DQ)}$	-600	300	-500	250	-450	225	-390	195	-360	180	ps	13,14, f
DQ high-impedance time from CK, $\overline{CK}$	$t_{HZ(DQ)}$	-	300	-	250	-	225	-	195	-	180	ps	13,14, f
Data setup time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	$t_{DS(base)}$	25	-	30	-	10		0		-10		ps	d, 17
Data hold time to DQS, $\overline{DQS}$ referenced to Vih(ac)Vil(ac) levels	$t_{DH(base)}$	100	-	65	-	45		35		25		ps	d, 17
DQ and DM Input pulse width for each input	t_{DIPW}	490	-	400	-	360		320		280		ps	28
Data Strobe Timing													
DQS, $\overline{DQS}$ READ Preamble	t_{RPRE}	0.9	Note 19	0.9	Note 19	0.9	Note 19	0.9	Note 19	0.9	Note 19	t_{CK}	13, 19, g
DQS, $\overline{DQS}$ differential READ Postamble	t_{RPST}	0.3	Note 11	0.3	Note 11	0.3	Note 11	0.3	Note 11	0.3	Note 11	t_{CK}	11, 13, b
DQS, $\overline{DQS}$ output high time	t_{QSH}	0.38	-	0.4	-	0.4	-	0.4	-	0.4	-	$t_{CK(avg)}$	13, g
DQS, $\overline{DQS}$ output low time	t_{QSL}	0.38	-	0.4	-	0.4	-	0.4	-	0.4	-	$t_{CK(avg)}$	13, g
DQS, $\overline{DQS}$ WRITE Preamble	t_{WPRE}	0.9	-	0.9	-	0.9	-	0.9	-	0.9	-	t_{CK}	
DQS, $\overline{DQS}$ WRITE Postamble	t_{WPST}	0.3	-	0.3	-	0.3	-	0.3	-	0.3	-	t_{CK}	
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-300	300	-255	255	-225	225	-195	195	-180	180	ps	13,f
DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1)	$t_{LZ(DQS)}$	-600	300	-500	250	-450	225	-390	195	-360	180	ps	13,14,f
DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2)	$t_{HZ(DQS)}$	-	300	-	250	-	225	-	195	-	180	ps	12,13,14
DQS, $\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	28,30
DQS, $\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	29,30
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	t_{DQSS}	-0.25	0.25	-0.25	0.25	-0.27	0.27	-0.3	0.3	-0.3	0.3	$t_{CK(avg)}$	c
DQS,$\overline{DQS}$ faling edge setup time to CK, $\overline{CK}$ rising edge	t_{DSS}	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	$t_{CK(avg)}$	c,31
DQS,$\overline{DQS}$ faling edge hold time to CK, $\overline{CK}$ rising edge	t_{DSH}	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	$t_{CK(avg)}$	c,31

[Table 52] Timing Parameters by Speed Bin (Cont.)

Speed		gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1800		gDDR3-2000		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Command and Address Timing													
DLL locking time	t_{DLLK}	512	-	512	-	512	-	512	-	512	-	nCK	
internal READ Command to PRECHARGE Command delay	t_{RTP}	max (4nCK,7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-		e
Delay from start of internal write transaction to internal read command	t_{WTR}	max (4nCK,7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-		e,18
WRITE recovery time	t_{WR}	15	-	15	-	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	t_{MRD}	4	-	4	-	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	t_{MOD}	max (12nCK,15ns)	-	max (12t_{CK},15ns)	-	max (12t_{CK},15ns)	-	max (12t_{CK},15ns)	-	max (12t_{CK},15ns)	-		
$\overline{CAS}$ to $\overline{CAS}$ command delay	t_{CCD}	4	-	4	-	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	$t_{DAL(min)}$	WR + roundup (t_{RP} / $t_{CK(AVG)}$)										nCK	
Multi-Purpose Register Recovery Time	t_{MPRR}	1	-	1	-	1	-	1	-	1	-	nCK	
ACTIVE to PRECHARGE command period	t_{RAS}	37.5	9*tRFI	36	9*tRFI	35	9*tRFI	34	9*tRFI	33	9*tRFI	ns	e
ACTIVE to ACTIVE command period for 2KB page size	t_{RRD}	max (4nCK,7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-	max (4t_{CK},7.5ns)	-		e
Four activate window for 2KB page size	t_{FAW}	50	-	45	-	40	-	40	-	40	-	ns	e
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	$t_{IS(base)}$	125	-	65	-	45	-	35	-	25	-	ps	b,16
Command and Address hold time from CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	$t_{IH(base)}$	200	-	140	-	120	-	110	-	100	-	ps	b,16
Command and Address setup time to CK, $\overline{CK}$ referenced to Vih(ac) / Vil(ac) levels	$t_{IS(base)}$ AC150	125+150	-	-	-	45+125	-	35+125	-	25+125	-	ps	b,16,27
Control & Address Input pulse width for each input	t_{IPW}	780	-	620	-	560	-	535	-	470	-	ps	28
Calibration Timing	-												
Power-up and RESET calibration time	$t_{ZQinitl}$	512	-	512	-	512	-	512	-	512	-	t_{CK}	
Normal operation Full calibration time	t_{ZQoper}	256	-	256	-	256	-	256	-	256	-	t_{CK}	
Normal operation short calibration time	t_{ZQCS}	64	-	64	-	64	-	64	-	64	-	t_{CK}	23
Reset Timing	-												
Exit Reset from CKE HIGH to a valid command	t_{XPR}	max(5t_{CK}, t_{RFC} + 10ns)	-	max(5t_{CK}, t_{RFC} + 10ns)	-	max(5t_{CK}, t_{RFC} + 10ns)	-	max(5t_{CK}, t_{RFC} + 10ns)	-	max(5t_{CK}, t_{RFC} + 10ns)	-		
Self Refresh Timing													
Exit Self Refresh to commands not requiring a locked DLL	t_{XS}	max(5nCK, tRFC + 10ns)	-	max(5t_{CK},t_{RFC} + 10ns)	-	max(5t_{CK},t_{RFC} + 10ns)	-	max(5t_{CK},t_{RFC} + 10ns)	-	max(5t_{CK},t_{RFC} + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK}(min)	-	t_{DLLK}(min)	-	t_{DLLK}(min)	-	t_{DLLK}(min)	-	t_{DLLK}(min)	-	nCK	
Minimum CKE low width for Self refresh entry to exit timing	t_{CKESR}	t_{CKE}(min)+ 1t_{CK}	-	t_{CKE}(min)+ 1t_{CK}	-	t_{CKE}(min)+ 1t_{CK}	-	t_{CKE}(min)+ 1t_{CK}	-	t_{CKE}(min)+ 1t_{CK}	-		
Valid Clock Requirement after Self Refresh Entry (SRE)	t_{CKSRE}	max(5t_{CK},10ns)	-	max(5t_{CK},10ns)	-	max(5t_{CK},10ns)	-	max(5t_{CK},10ns)	-	max(5t_{CK},10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX)	t_{CKSRX}	max(5t_{CK},10ns)	-	max(5t_{CK},10ns)	-	max(5t_{CK},10ns)	-	max(5t_{CK},10ns)	-	max(5t_{CK},10ns)	-		

[Table 53] Timing Parameters by Speed Bin (Cont.)

Speed		gDDR3-1066		gDDR3-1333		gDDR3-1600		gDDR3-1800		gDDR3-2000		Units	Note
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Power Down Timing													
Exit Power Down with DLL on to any valid command;Exit Percharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	max (3nCK, 7.5ns)	-	max (3t_{CK},6ns)	-	max (3t_{CK},6ns)	-	max (3t_{CK},6ns)	-	max (3t_{CK},6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	max (10nCK, 24ns)	-	max (10t_{CK},24ns)	-	max (10t_{CK},24ns)	-	max (10t_{CK},24ns)	-	max (10t_{CK},24ns)	-		2
CKE minimum pulse width	t_{CKE}	max (3nCK, 5.625ns)	-	max (3t_{CK},5.625ns)	-	max (3t_{CK},5ns)	-	max (3t_{CK},5ns)	-	max (3t_{CK},5ns)	-		
Command pass disable delay	t_{CPDED}	1	-	1	-	1	-	2	-	2	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	tCKE(min)	9*tREFI	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}	t_{CKE}(min)	9*t_{REFI}	t_{CK}	15
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	1	-	1	-	1	-	1	-	nCK	20
Timing of PRE command to Power Down entry	t_{PRPDEN}	1	-	1	-	1	-	1	-	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	t_{WRPDEN}	WL + 4 +(tWR/ tCK(avg))	-	WL + 4 +(t_{WR}/ t_{CK})	-	WL + 4 +(t_{WR}/ t_{CK})	-	WL + 4 +(t_{WR}/ t_{CK})	-	WL + 4 +(t_{WR}/ t_{CK})	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	$t_{WRAPDEN}$	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK	10
Timing of WR command to Power Down entry (BL4MRS)	t_{WRPDEN}	WL + 2 +(tWR/ tCK(avg))	-	WL + 2 +(t_{WR}/ $t_{CK(avg)}$)	-	WL + 2 +(t_{WR}/ $t_{CK(avg)}$)	-	WL + 2 +(t_{WR}/ $t_{CK(avg)}$)	-	WL + 2 +(t_{WR}/ $t_{CK(avg)}$)	-	nCK	9
Timing of WRA command to Power Down entry (BL4MRS)	$t_{WRAPDEN}$	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK	10
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	1	-	1	-	2	-	2	-		20,21
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	tMOD(min)	-	$t_{MOD(min)}$	-	$t_{MOD(min)}$	-	$t_{MOD(min)}$	-	$t_{MOD(min)}$	-		
ODT Timing													
ODT high time without write command or with wirte command and BC4	ODTH4	4	-	4	-	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	6	-	6	-	nCK	
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	t_{AONPD}	2	8.5	1	9	1	9	1	9	1	9	ns	
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	t_{AOFPD}	2	8.5	1	9	1	9	1	9	1	9	ns	
ODT turn-on	t_{AON}	-300	300	-250	250	-225	225	-195	195	-170	170	ps	7,f
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	t_{AOF}	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	8,f
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	$t_{CK(avg)}$	f
Write Leveling Timing													
First DQS pulse rising edge after tDQSS margining mode is programmed	t_{WLMRD}	40	-	40	-	40	-	40	-	40	-	t_{CK}	3
DQS/DQS delay after tDQS margining mode is programmed	$t_{WLDQSEN}$	25	-	25	-	25	-	25	-	25	-	t_{CK}	3
Setup time for tDQSS latch	t_{WLS}	245	-	195	-	162	-	128	-	112	-	ps	
Hold time of tDQSS latch	t_{WLH}	245	-	195	-	162	-	128	-	112	-	ps	
Write leveling output delay	t_{WLO}	0	9	0	9	0	7.5	0	7.5	0	7	ns	
Write leveling output error	t_{WLOE}	0	2	0	2	0	2	0	2	0	2	ns	

Jitter Notes

Specific Note a
Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. ex) tMRD =4 [nCK] means; if one Mode Register Set command is registered at Tm, anothe Mode Register Set commdn may be registered at Tm+4, even if (Tm+4-Tm) is 4 x tCK(avg) +tERR(4per) min.

Specific Note b
These parameters are measured from a command/address signal (CKE, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

Specific Note c
These parameters are measured from a data strobe signal (DQS(L/U), $\overline{\text{DQS}}$(L/U)) crossing to its respective clock signal (CK, $\overline{\text{CK}}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing.
That is, these parameters should be met whether clock jitter is present or not.

Specific Note d
These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{\text{DQS}}$(L/U)) crossing.

Specific Note e
For these parameters, the gDDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied.
For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For gDDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

Specific Note f
When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a gDDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for gDDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12

Specific Note g
When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a gDDR3-800 SDRAM has tCK(avg),act =20 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.

2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.

3. The max values are system dependent.

4. WR as programmed in mode register

5. Value must be rounded-up to next higher integer value

6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.

7. For definition of RTT turn-on time tAON see "Device Operation"

8. For definition of RTT turn-off time tAOF see "Device Operation".

9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.

10. WR in clock cycles as programmed in MR0

11. The maximum postamble is bound by tHZDQS(max)

12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD

13. Value is valid for RON34 and RON40

14. Single ended signal parameter. Refer to chapter <8, 9> for definition and measurement method.

15. tREFI depends on TOPER

16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{\text{CK}}$ differential slew rate, Note for DQ and DM signals, V_{REF}(DC) = VrefDQ(DC). FOr input only pins except RESET, VRef(DC)=VRefCA(DC).
See "Address/ Command Setup, Hold and Derating" on page 52.

17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{\text{DQS}}$ differential slew rate. Note for DQ and DM signals, V_{REF}(DC)= VRefDQ(DC). For input only pins except $\overline{\text{RESET}}$, VRef(DC)=VRefCA(DC).
See "Data Setup, Hold and Slew Rate Derating" on page 58.

18. Start of internal write transaction is definited as follows ;
For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL

19. The maximum preamble is bound by tLZDQS(max)

20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.

21. Altough CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation".

22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens x Tdriftrate}) + (\text{VSens x Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) For example, if TSens = 1.5% /°C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.

25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

28. tDQSL describes the instantaneous differential input low pulse width on DQS-$\overline{\text{DQS}}$, as measured from one falling edge to the next consecutive rising edge.

29. tDQSH describes the instantaneous differential input high pulse width on DQS-$\overline{\text{DQS}}$, as measured from one rising edge to the next consecutive falling edge.

30. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

31. tDSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

Address / Command Setup, Hold and Derating:

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value (see Table 53) to the ΔtIS and ΔtIH derating value (see Table 54) respectively.
Example: tIS (total setup time) = tIS(base) + ΔtIS Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IH}(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as
the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IL}(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{REF}(dc) to ac region', use nominal slew rate for derating value (see Figure 23). If the actual signal is later than the nominal slew rate line anywhere between shaded 'V_{REF}(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 25).
Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL}(dc)max and the first crossing of V_{REF}(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(dc)min and the first crossing of V_{REF}(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to V_{REF}(dc) region', use nominal slew rate for derating value (see Figure 24). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{REF}(dc) region', the slew rate of a tangent line to the actual signal from the dc level to V_{REF}(dc) level is used for derating value (see Figure 26).
For a valid transition the input signal has to remain above/below $V_{IH/IL}$(ac) for some time tVAC (see Table 56).
Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL}$(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).
For slew rates in between the values listed in Table 55, the derating values may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization.

[Table 54] ADD/CMD Setup and Hold Base-Values for 1V/ns

[ps]	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	reference
tIS(base)	125	65	45	35	25	$V_{IH/L(ac)}$
tIH(base)	200	140	120	110	100	$V_{IH/L(dc)}$
tIS(base)-AC150	125+150	65+125	45+125	35+125	25+125	$V_{IH/L(ac)}$

Note : AC/DC referenced for 1V/ns DQ-slew rate and 2V/ns DQS slew rate
Note : The tIS(base)-AC150 specifications are further adjusted to add an addi-tional 100ps of derating to accommodate for the lower alternate thresh-old of 150mV and another 25ps to acccount for the earlier reference point [(175mv-150mV)/1 V/ns].

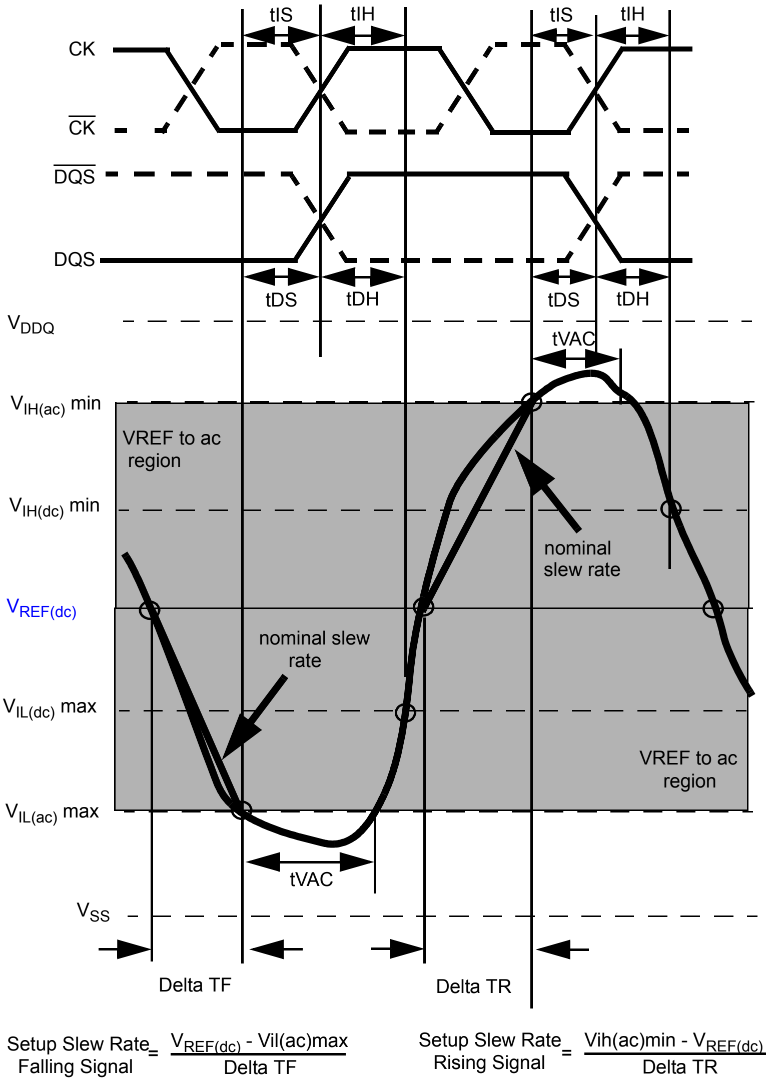
[Table 55] Derating values gDDR3-1333/1600 tIS/tIH-ac/dc based - Alternate AC150 Threshold

ΔtIS, ΔtIH Derating [ps] AC/DC based Alternate AC150 Threshold -> VIH(ac) = VREF(dc) + 150mV, VIL(ac) = V_{REF}(dc) - 150mV																	
		CLK,$\overline{CLK}$ Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

[Table 56] Required time t_{VAC} above V_{IH}(ac) {blow V_{IL}(ac)} for valid transition

Slew Rate[V/ns]	t_{VAC} @175mV [ps]		t_{VAC} @50mV [ps]	
	min	max	min	max
>2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

Note :Clock and Strobe are drawn on a different time scale.



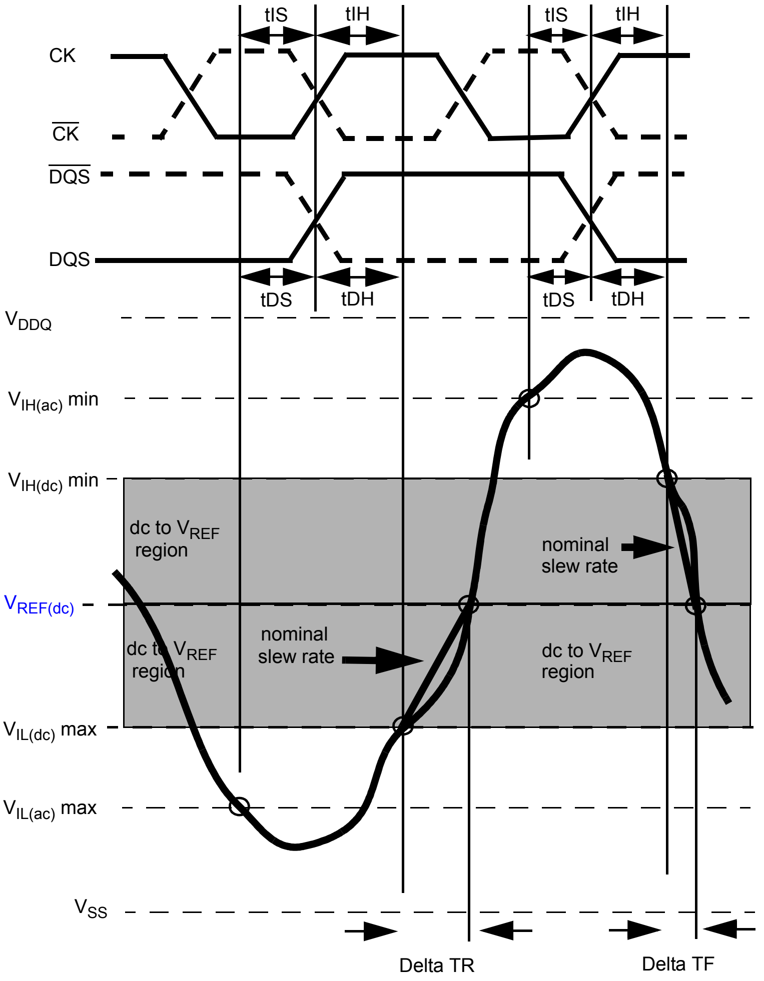
tIS
tIH
tIS
tIH
CK
$\overline{CK}$
$\overline{DQS}$
DQS
tDS
tDH
tDS
tDH
V_{DDQ}
tVAC
$V_{IH(ac)}$ min
VREF to ac region
$V_{IH(dc)}$ min
nominal slew rate
$V_{REF(dc)}$
nominal slew rate
$V_{IL(dc)}$ max
VREF to ac region
$V_{IL(ac)}$ max
tVAC
V_{SS}
Delta TF
Delta TR

$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - Vil(ac)max}{\text{Delta TF}}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{Vih(ac)min - V_{REF(dc)}}{\text{Delta TR}}$$

Figure 21 - Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.


tIS
tIH
tIS
tIH
CK
$\overline{CK}$
$\overline{DQS}$
DQS
tDS
tDH
tDS
tDH
V_{DDQ}
$V_{IH(ac)}$ min
$V_{IH(dc)}$ min
dc to V_{REF} region
nominal slew rate
$V_{REF(dc)}$
dc to V_{REF} region
nominal slew rate
dc to V_{REF} region
$V_{IL(dc)}$ max
$V_{IL(ac)}$ max
V_{SS}
Delta TR
Delta TF

$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - Vil(dc)max}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{Vih(dc)min - V_{REF(dc)}}{\text{Delta TF}}$$

Figure 22 - Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

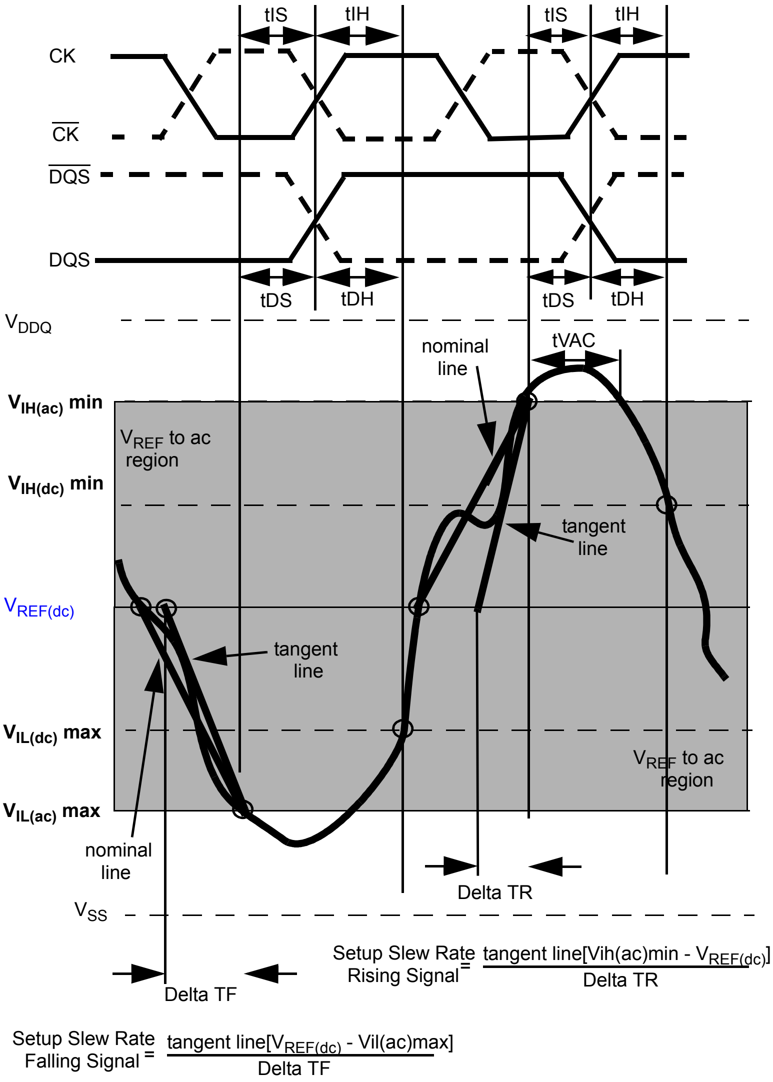
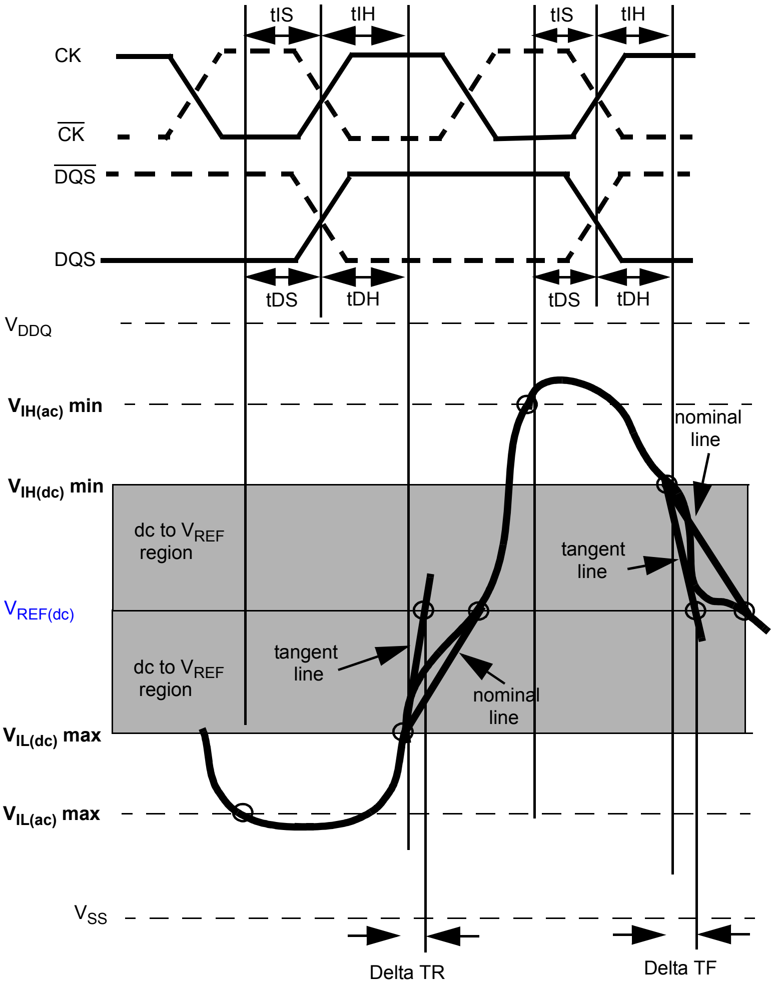

tIS
tIH
tIS
tIH
CK
$\overline{CK}$
$\overline{DQS}$
DQS
tDS
tDH
tDS
tDH
V_{DDQ}
nominal line
tVAC
$V_{IH(ac)}$ min
V_{REF} to ac region
$V_{IH(dc)}$ min
tangent line
$V_{REF(dc)}$
tangent line
$V_{IL(dc)}$ max
V_{REF} to ac region
$V_{IL(ac)}$ max
nominal line
Delta TR
V_{SS}
Setup Slew Rate Rising Signal = tangent line[Vih(ac)min - $V_{REF(dc)}$] / Delta TR
Delta TF
Setup Slew Rate Falling Signal = tangent line[$V_{REF(dc)}$ - Vil(ac)max] / Delta TF

Figure 23. Illustration of tangent line for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock)

Note :Clock and Strobe are drawn on a different time scale.


tIS
tIH
tIS
tIH
CK
$\overline{CK}$
$\overline{DQS}$
DQS
tDS
tDH
tDS
tDH
V_{DDQ}
$V_{IH(ac)}$ min
$V_{IH(dc)}$ min
dc to V_{REF} region
$V_{REF(dc)}$
dc to V_{REF} region
$V_{IL(dc)}$ max
$V_{IL(ac)}$ max
V_{SS}
nominal line
tangent line
tangent line
nominal line
Delta TR
Delta TF

$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - Vil(dc)max]}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [Vih(dc)min - V_{REF(dc)}]}{\text{Delta TF}}$$

Figure 24 - Illustration of tangent line for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock)

Data Setup, Hold and Slew Rate Derating:

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value (see Table 57) to the Δ tDS and ΔtDH (see Table 58) derating value respectively. Example: tDS (total setup time) = tDS(base) + ΔtDS.
Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IH}(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{REF}(dc) and the first crossing of V_{IL}(ac)max (see Figure 27). If the actual signal is always earlier than the nominal slew rate line between shaded 'V_{REF}(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere
between shaded 'V_{REF}(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 29).
Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL}(dc)max and the first crossing of V_{REF}(dc). Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH}(dc)min and the first crossing of V_{REF}(dc) (see Figure 28). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to V_{REF}(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to V_{REF}(dc) region', the slew rate of a tangent line to the actual signal from the dc level to V_{REF}(dc) level is used for derating value (see Figure 30).

For a valid transition the input signal has to remain above/below $V_{IH/IL}$(ac) for some time tVAC (see Table 60).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL}$(ac).
For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.
These values are typically not subject to production test. They are verified by design and characterization

[Table 57] Data Setup and Hold Base-Value

[ps]	gDDR3-1066	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	reference
tDS(base)	25	30	10	0	-10	$V_{IH/L(ac)}$
tDH(base)	100	65	45	35	25	$V_{IH/L(dc)}$

Note : AC/DC referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

[Table 58] Derating values gDDR3-1066/1333/1600/1800/2000 tIS/tIH-ac/dc base

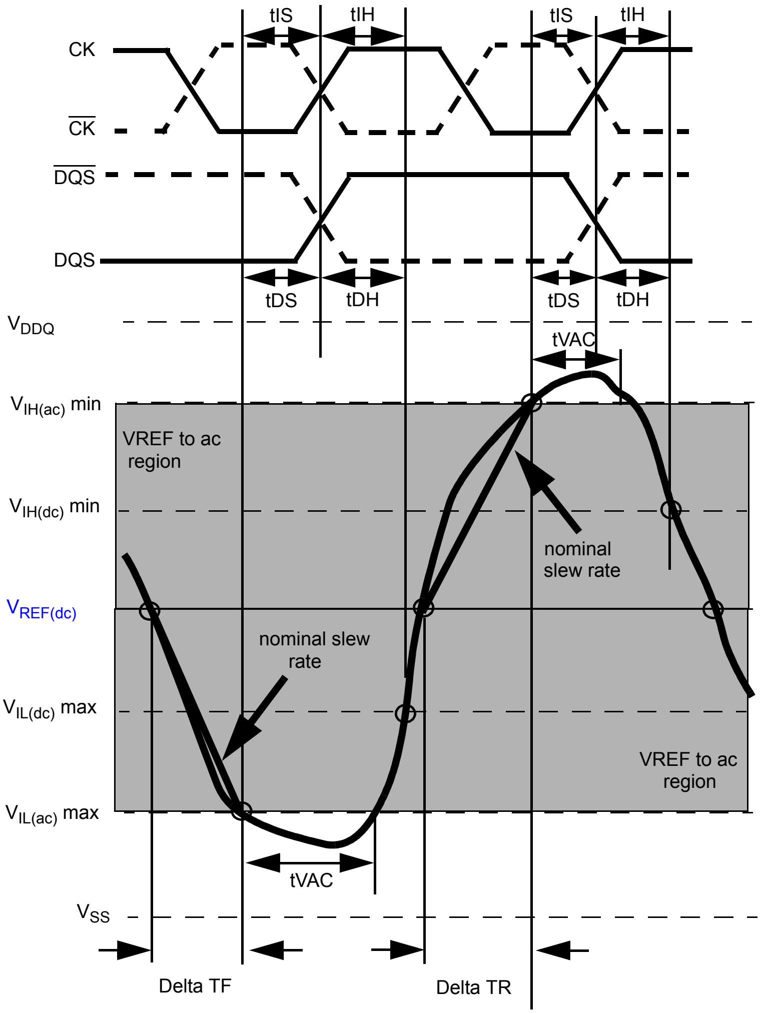
ΔtDS, ΔtDH Derating [ps] AC/DC based[a]																		
			DQS,DQS Differential Slew Rate															
			4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4V/ns		1.2V/ns		1.0V/ns	
			ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
gDDR3 -1066	DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
		1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
		1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
		0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
		0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
		0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
		0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
		0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	6	10
		0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10
gDDR3 -1333 1600	DQ Slew rate V/ns	2.0	75	50	75	50	75	50	-	-	-	-	-	-	-	-	-	-
		1.5	50	34	50	34	50	34	58	42	-	-	-	-	-	-	-	-
		1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
		0.9	-	-	0	-4	0	-4	8	4	16	12	24	20	-	-	-	-
		0.8	-	-	-	-	0	-10	8	-2	16	6	24	14	32	24	-	-
		0.7	-	-	-	-	-	-	8	-8	16	0	24	8	32	18	40	34
		0.6	-	-	-	-	-	-	-	-	15	-10	23	-2	31	8	39	24
		0.5	-	-	-	-	-	-	-	-	-	-	14	-16	22	-6	30	10
		0.4	-	-	-	-	-	-	-	-	-	-	-	-	7	-26	15	-10
gDDR3 -1800 2000	DQ Slew rate V/ns	2.0	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-	-	-	-	-
		1.5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-	-	-
		1.0	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-	-	-
		0.9	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-	-	-
		0.8	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	-	-
		0.7	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		0.6	-	-	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		0.5	-	-	-	-	-	-	-	-	-	-	TBD	TBD	TBD	TBD	TBD	TBD
		0.4	-	-	-	-	-	-	-	-	-	-	-	-	TBD	TBD	TBD	TBD

Note : a. Cell contents shaded in red are defined

[Table 59] Required time t_{VAC} above V_{IH}(ac) {blow V_{IL}(ac)} for valid transition

Slew Rate[V/ns]	t_{VAC}[ps] gDDR3-1066		t_{VAC}[ps] gDDR3-1333/1600		t_{VAC}[ps] gDDR3-1800/2000	
	min	max	min	max	min	max
>2.0	75	-	175	-	TBD	-
2.0	57	-	170	-	TBD	-
1.5	50	-	167	-	TBD	-
1.0	38	-	163	-	TBD	-
0.9	34	-	162	-	TBD	-
0.8	29	-	161	-	TBD	-
0.7	22	-	159	-	TBD	-
0.6	13	-	155	-	TBD	-
0.5	0	-	155	-	TBD	-
<0.5	0	-	150	-	TBD	-

Note :Clock and Strobe are drawn on a different time scale.

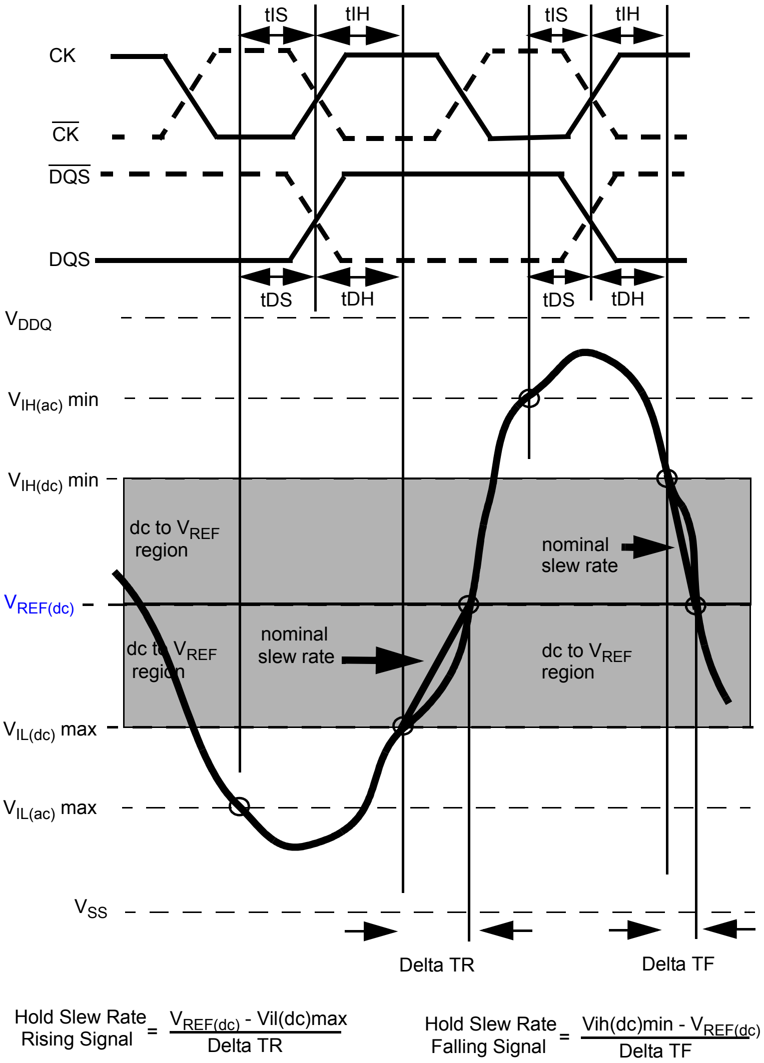

tIS
tIH
tIS
tIH
CK
$\overline{CK}$
$\overline{DQS}$
DQS
tDS
tDH
tDS
tDH
V_{DDQ}
tVAC
$V_{IH(ac)}$ min
VREF to ac region
$V_{IH(dc)}$ min
nominal slew rate
$V_{REF(dc)}$
nominal slew rate
$V_{IL(dc)}$ max
VREF to ac region
$V_{IL(ac)}$ max
tVAC
V_{SS}
Delta TF
Delta TR

$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - \text{Vil(ac)max}}{\text{Delta TF}}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{\text{Vih(ac)min} - V_{REF(dc)}}{\text{Delta TR}}$$

Figure 27 - Illustration of nominal slew rate and tVAC for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.


tIS
tIH
tIS
tIH
CK
CK
DQS
DQS
tDS
tDH
tDS
tDH
VDDQ
VIH(ac) min
VIH(dc) min
dc to VREF region
nominal slew rate
VREF(dc)
dc to VREF region
nominal slew rate
dc to VREF region
VIL(dc) max
VIL(ac) max
VSS
Delta TR
Delta TF

$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - Vil(dc)max}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{Vih(dc)min - V_{REF(dc)}}{\text{Delta TF}}$$

Figure 28 - Illustration of nominal slew rate for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock).

Note :Clock and Strobe are drawn on a different time scale.

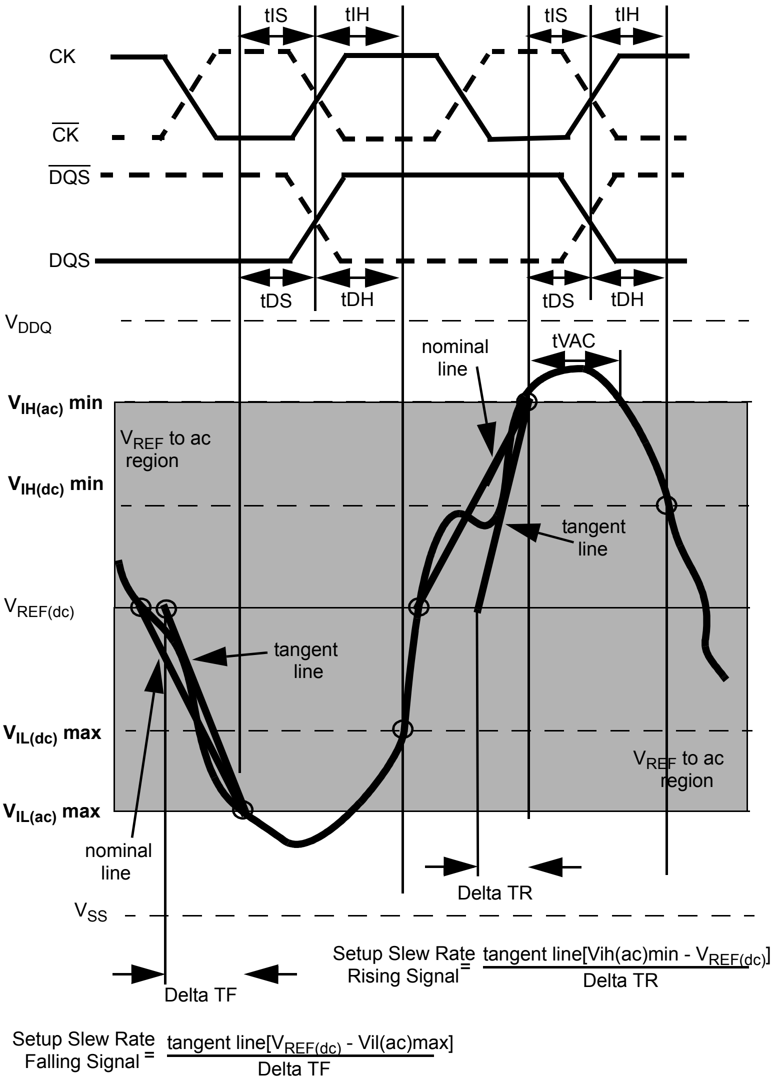
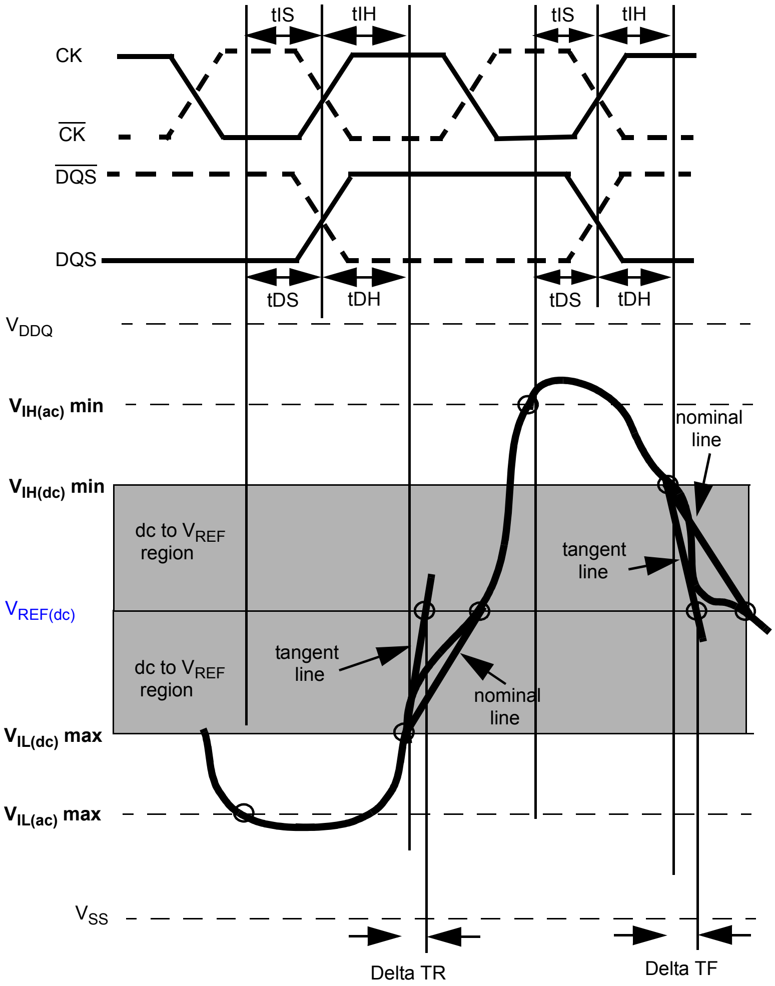

tIS
tIH
tIS
tIH
CK
$\overline{CK}$
$\overline{DQS}$
DQS
tDS
tDH
tDS
tDH
V_{DDQ}
nominal line
tVAC
$V_{IH(ac)}$ min
V_{REF} to ac region
$V_{IH(dc)}$ min
tangent line
$V_{REF(dc)}$
tangent line
$V_{IL(dc)}$ max
V_{REF} to ac region
$V_{IL(ac)}$ max
nominal line
Delta TR
V_{SS}
Setup Slew Rate Rising Signal = tangent line[Vih(ac)min - $V_{REF(dc)}$] / Delta TR
Delta TF
Setup Slew Rate Falling Signal = tangent line[$V_{REF(dc)}$ - Vil(ac)max] / Delta TF

Figure 29 - Illustration of tangent line for setup time tDS (for DQ with respect to strobe) and tIS (for ADD/CMD with respect to clock)

Note :Clock and Strobe are drawn on a different time scale.


tIS
tIH
tIS
tIH
CK
$\overline{\text{CK}}$
$\overline{\text{DQS}}$
DQS
tDS
tDH
tDS
tDH
V_{DDQ}
$V_{IH(ac)}$ min
$V_{IH(dc)}$ min
$V_{REF(dc)}$
$V_{IL(dc)}$ max
$V_{IL(ac)}$ max
V_{SS}
dc to V_{REF} region
dc to V_{REF} region
tangent line
nominal line
tangent line
nominal line
Delta TR
Delta TF

$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - \text{Vil(dc)max}]}{\text{Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [\text{Vih(dc)min} - V_{REF(dc)}]}{\text{Delta TF}}$$

Figure 30 - Illustration of tangent line for hold time tDH (for DQ with respect to strobe) and tIH (for ADD/CMD with respect to clock)

gDDR3 SDRAM Speed Bins include tCK, tRCD, tRP, tRAS and

tRC for each corresponding bin.

14.0 Timing Parameters by Speed Grade

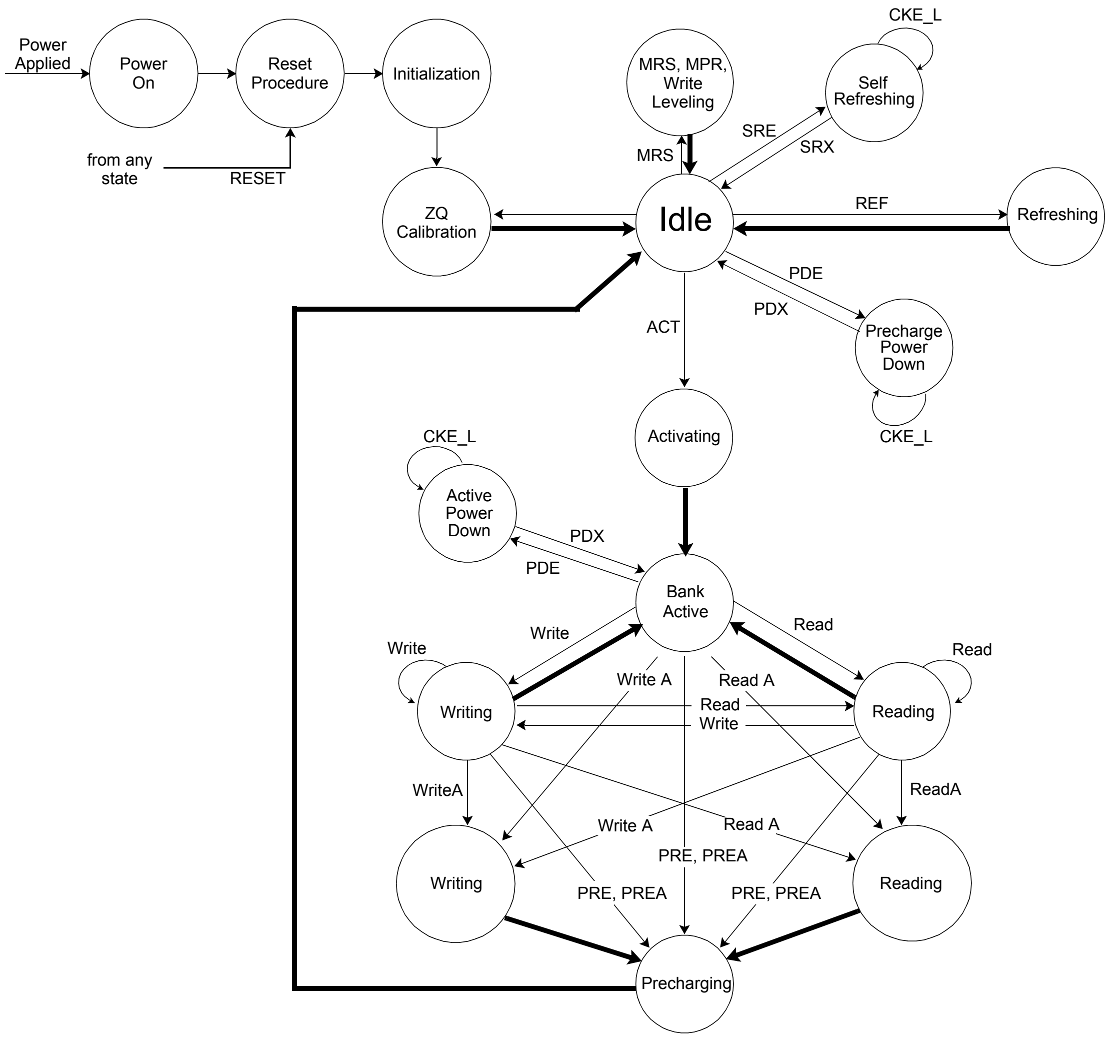

Power Applied
Power On
Reset Procedure
Initialization
from any state
RESET
ZQ Calibration
MRS, MPR, Write Leveling
MRS
CKE_L
Self Refreshing
SRE
SRX
Idle
REF
Refreshing
PDE
PDX
Precharge Power Down
CKE_L
ACT
Activating
CKE_L
Active Power Down
PDX
PDE
Bank Active
Write
Write
Read
Read
Writing
Write A
Read A
Read
Write
Reading
WriteA
ReadA
Write A
Read A
PRE, PREA
Writing
Reading
PRE, PREA
PRE, PREA
Precharging
Automatic Sequence
Command Sequence

Figure 1 - Simplified State Diagram

[Table 1] State Diagram Command Definitions

Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA,RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8	SRX	Self-Refresh exit
REF	Refresh	$\overline{\text{RESET}}$	Start RESET procedure	MPR	Multi Purpose Register

Note : This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

Device Operation & Timing Diagram

The gDDR3 SDRAM is a high-speed CMOS, dynamic random-access memory internally configured as a eight-bank DRAM. The gDDR3 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture, with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the gDDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and two corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the gDDR3 SDRAM are burst oriented, start at a selected location, and continue for a burst length of four or eight in a programmed sequence. Operation begins with the registration of an Active command, which is then followed by a Read or Write command. The address bits registered coincident with the Active command are used to select the bank and row to be accessed (BA0-BA2 select the bank; A0-A15 select the row). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10/AP), and the select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register. Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

Prior to normal operation, the gDDR3 SDRAM must be powered up and initialized in a predefined manner. The following sections provide detailed information covering device reset and initialization, register definition, command descriptions and device operation.

15.0 Functional Description

15.1 Simplified State Diagram

RESET is a CMOS rail to rail signal with DC high and low are 80% and 20% of V_{DD}, i.e. 1.20V for DC high and 0.30V for DC low

- It is a negative active signal (active low)
- It is expected that the RESET signal is referenced to GND
- It is expected that there is no termination required on this signal
- It is expected that the Reset signal will be heavily loaded across multiple chips.
- RESET is destructive to data contents.

15.2 Basic Functionality

The following sequence is required for POWER UP and Initialization.

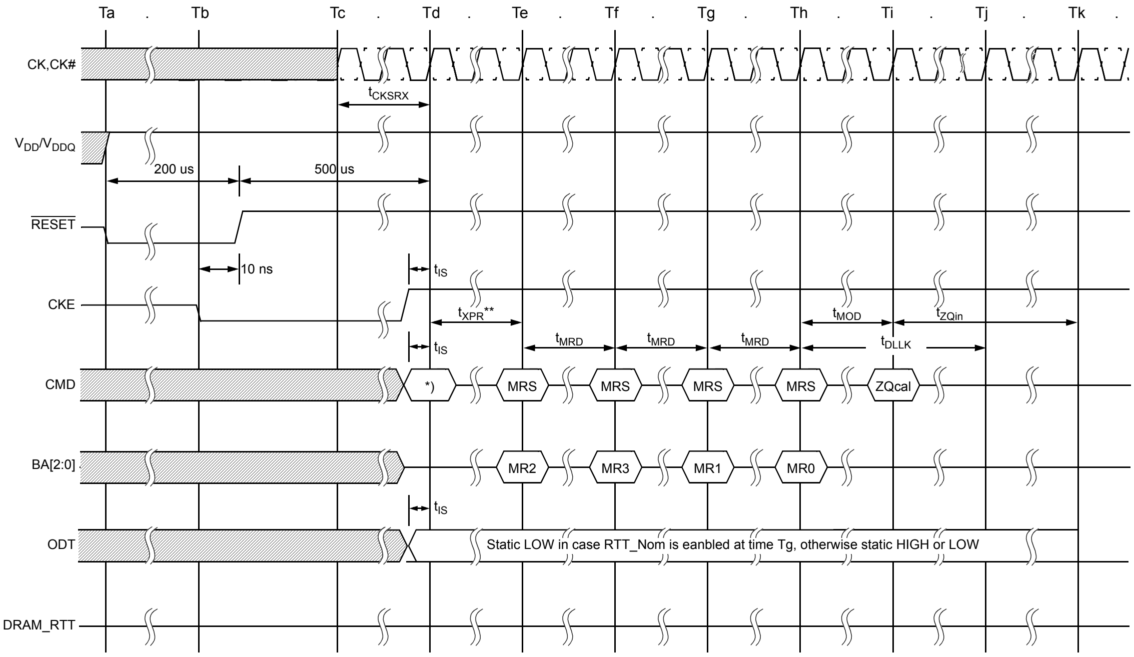
1. Apply power and attempt to maintain $\overline{\text{RESET}}$ below 0.2*V_{DD} (all other inputs may be undefined). $\overline{\text{RESET}}$ needs to be maintained for minimum 200us with stable power. CKE is pulled " Low" anytime before $\overline{\text{RESET}}$ being de-asserted (min. time 10ns). The power voltage ramp time between 300mV to V_{DD}min must be no longer than 200ms; and during the ramp, V_{DD}>V_{DDQ} and V_{DD} -V_{DDQ}<0.3volts.

- V_{DD} and V_{DDQ} are driven from a single power converter output, AND
- The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to 0.95V max once power ramp is finished, AND
- Vref tracks V_{DDQ}/2.

or

- Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
- Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & Vref.
- The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.

2. After $\overline{\text{RESET}}$ is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK, $\overline{\text{CK}}$) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a NOP or Deselect command must be registered (with tIS set up time to clock) before CKE goes active. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit.
4. The gDDR3 SDRAM keeps its on-die termination in high-impedance state as long as $\overline{\text{RESET}}$ is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after $\overline{\text{RESET}}$ deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 and the on-die termination is required to remain in the high impedance state, the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.
5. After CKE is registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=Max(tXS, 5tCK)]
6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable "command, provide "Low" to A0, "Low" to A0, "High" to BA0 and "Low" to BA1-BA2)
9. Issue precharge all command.
10. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).
11. Issue ZQCL command to starting ZQ calibration
12. Wait for both tDLLK and tZQ init completed
13. The gDDR3 SDRAM is now ready for normal operation.


Ta
Tb
Tc
Td
Te
Tf
Tg
Th
Ti
Tj
Tk
CK,CK#
tCKSRX
VDD/VDDQ
200 us
500 us
RESET
10 ns
tIS
CKE
tXPR**
tMRD
tMRD
tMRD
tMOD
tZQinit
tDLLK
tIS
CMD
*)
MRS
MRS
MRS
MRS
ZQcal
BA[2:0]
MR2
MR3
MR1
MR0
tIS
ODT
Static LOW in case RTT_Nom is eanbled at time Tg, otherwise static HIGH or LOW
DRAM_RTT

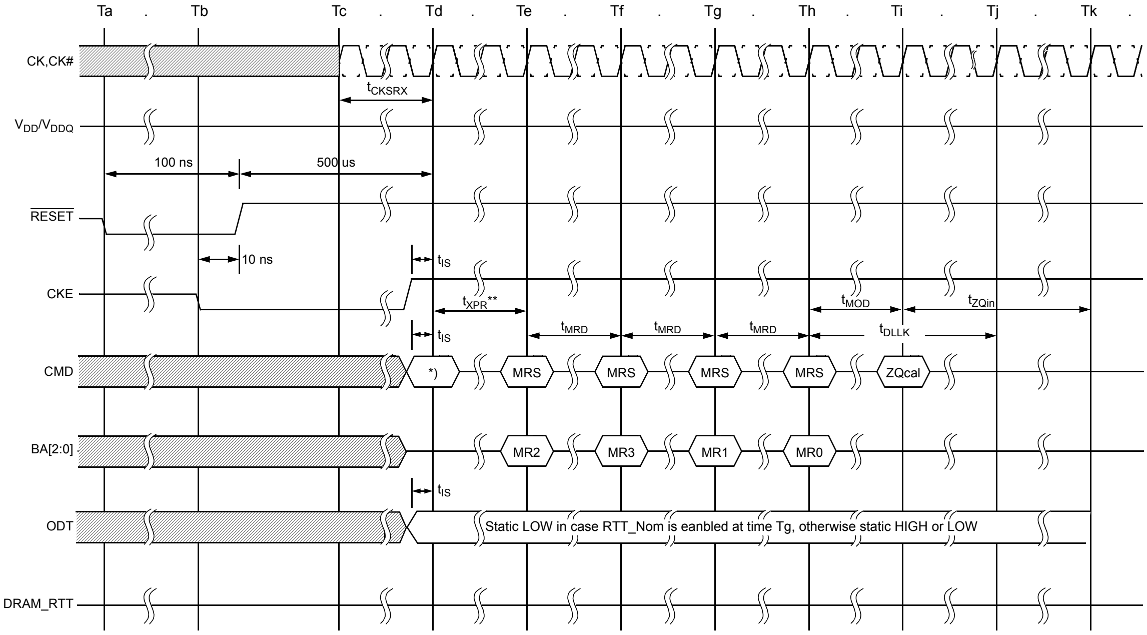
*)From time point ‘Td’ until ‘Tk’, NOP or DES commands must be applied between MRS and ZQcal commands
**)tXPR = max (tXS, 5tCK)

Figure 2 : $\overline{\text{RESET}}$ and Initialization Sequence at Power-on Ramping

15.3 RESET and Initialization Procedure

The following sequence is required for RESET at no power interruption initialization.

1. Asserted RESET below 0.2 * V_{DD} anytime when reset is needed (all other inputs may be undefined). RESET needs to be maintained for minimum 100 ns. CKE is pulled "LOW" before RESET being de-asserted (min. time 10 ns).
2. Follow Power-up Initialization Sequence step 2 to 11.
3. The Reset sequence is now completed, gDDR3 SDRAM is ready for normal operation.


Ta
Tb
Tc
Td
Te
Tf
Tg
Th
Ti
Tj
Tk
CK,CK#
tCKSRX
VDD/VDDQ
100 ns
500 us
RESET
10 ns
tIS
CKE
tXPR**
tMOD
tZQinit
tMRD
tMRD
tMRD
tDLLK
tIS
CMD
*)
MRS
MRS
MRS
MRS
ZQcal
BA[2:0]
MR2
MR3
MR1
MR0
tIS
ODT
Static LOW in case RTT_Nom is eanbled at time Tg, otherwise static HIGH or LOW
DRAM_RTT

*)From time point ‘Td’ until ‘Tk’, NOP or DES commands must be applied between MRS and ZQcal commands
**)tXPR = max (tXS, 5tCK)

Figure 3 - RESET procedure at Power stable condition

15.3.1 RESET Signal Definitions

15.3.2 Power-up Initialization Sequence

For application flexibility, various functions, features and modes are programmable in four Mode Registers, provided by the gDDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers($\overline{MR}$) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 4. The MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features except DLL reset and is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 5. The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE were already high prior to writing into the mode register. The mode registers are divided into various fields depending on the functionality and/or modes.

tMRD: Mode Register Set command cycle time

tMRD is the minimum time required from an MRS command to the next MRS command. As DLL enable and DLL reset are both MRS commands, tMRD is applicable between MRS to MR1 for DLL enable and MRS to MR0 for DLL reset, and not tMOD.

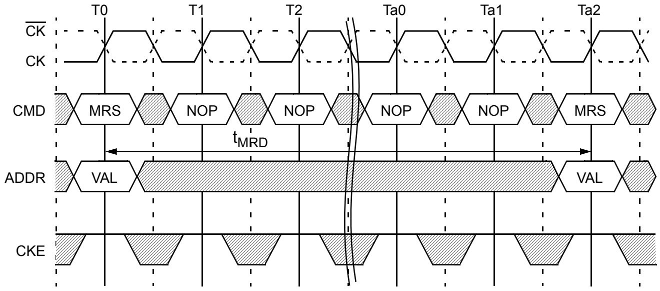


Figure 4 - tMRD Timing

tMOD: MRS command to Non-MRS command delay

tMOD is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES, e.g. MRS to ACT, MRS to ODT, etc. Note that additional restrictions may apply, for example, MRS to MR0 for DLL reset followed by Read.

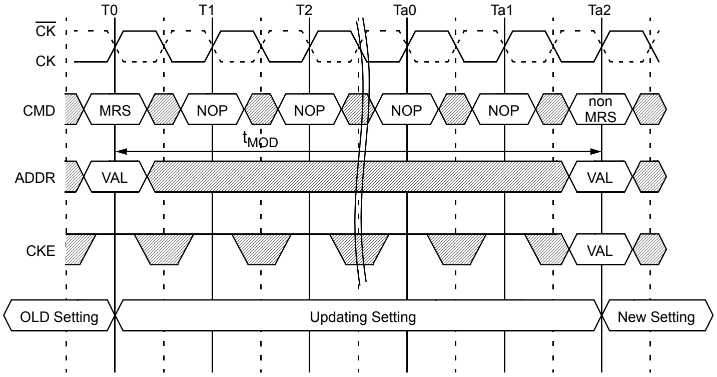


Figure 5 - tMOD Timing

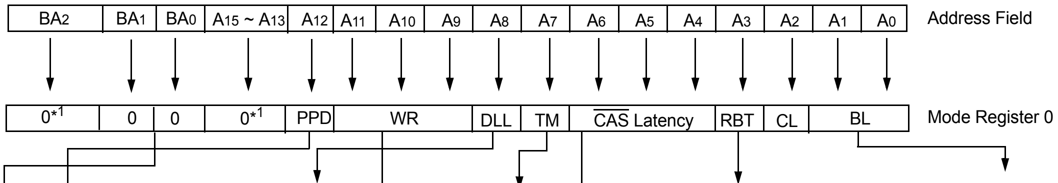
15.3.3 Reset Initialization with Stable Power

15.4 Register Definition

15.4.1 Programming the Mode Registers

15.4.2 Mode Register MR0

Figure 6 - MR0 Programming



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	BL
0	0	8 (Fixed)
0	1	4 or 8(on the fly)
1	0	4 (Fixed)
1	1	Reserved

A12	DLL Control for Pre-charge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	16*2
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	14*2

CAS Latency

A6	A5	A4	A2	Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13

BA1	BA0	MRS mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*1 : BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.

*2 : WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.

The mode register MR0 stores the data for controlling various operating modes of gDDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR and DLL control for precharge power down, which include various vendor specific options to make gDDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 and BA1, while controlling the states of address pins according to the table below.

[Table 2] Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1, 2, 3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1, 2, 3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1, 2, 3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1, 2, 3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1, 2, 3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1, 2, 3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1, 2, 3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1, 2, 3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1, 2, 4, 5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1, 2, 4, 5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2, 4

Notes:

1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Output driver for data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don’t Care.

15.4.2.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 as shown in Figure 6. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 3. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and ’on the fly’ which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/$\overline{BC}$.

15.4.2.2 CAS Latency

The CAS Latency is defined by MR0(bits A9-A11) as shown in Figure 6. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to " Standard Speed Bins" on each component datasheet. For detailed Read operation refer to "READ Operation" on page 34.

15.4.2.3 Test Mode

The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in Figure 6. Programming bit A7 to a ’1’ places the DDR3 SDRAM into a test mode that is only used by the DRAM Manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1.

15.4.2.4 DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of ’0’ after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations).

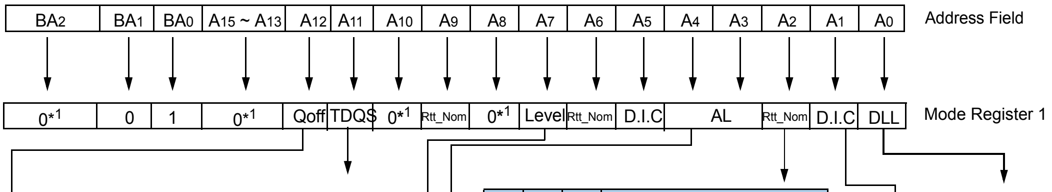
15.4.2.5 Write Recovery

The programmed WR value MR0(bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR(write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal or larger than tWR(min).

15.4.3 Mode Register MR1

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0 and low on BA1, while controlling the states of address pins according to the Figure below.

Figure 7 - MR1 Definition



A11	TDQS enable
0	Disabled
1	Enabled

A7	Write leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A9	A6	A2	Rtt_Nom*3
0	0	0	ODT disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*2
1	0	1	RZQ/8*2
1	1	0	Reserved
1	1	1	Reserved

Note1:RZQ=240ohms

Note2:If RTT_Nom is used during Writes, only the values RZQ/2,RZQ/4 and RZQ/6 are allowed

Note3:In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed

A0	DLL Enable
0	Enable
1	Disable

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled *2

*2: Outputs disabled - DQs, DQSs, $\overline{\text{DQSs}}$.

A5	A1	Output Driver Impedance Control
0	0	Reserved for RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note1:RZQ=240ohms

* 1 : BA2 and A5, A8 ~ A11, A13 ~ A15 are RFU and must be programmed to 0 during MRS

15.4.3.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self- Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. gDDR3 SDRAM does not require DLL for any Write operation. For more detailed information on DLL Disable operation refer to "DLL-off Mode" on page 20.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10, A9}={0,0}, to disable Dynamic ODT externally.

15.4.3.2 Output Driver Impedance Control

The output driver impedance of the gDDR3 SDRAM device is selected by MR1(bits A1 and A5) as shown in Figure 7 .

15.4.3.3 ODT Rtt Values

DRAM RTT_NOM and RTT_WR can be used independent of each other.

15.4.3.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in gDDR3 SDRAM. In this operation, the gDDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table 4 .

[Table 3] Additive Latency (AL) Settings

A4	A3	AL
0	0	(AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note : AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register.

15.4.3.5 Write leveling

For better signal integrity, gDDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the controller should support 'write leveling' in gDDR3 SDRAM to compensate the skew. See 2.8 'Write Leveling' on page 24 for more details.

15.4.3.6 Output Disable

The gDDR3 SDRAM outputs may be enabled/disabled by MR1(bit A12) as shown in Figure 7. When this feature is enabled (A12 = 1), all output pins (DQs, DQS, $\overline{\text{DQS}}$, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring module power for example. For normal operation, A12 should be set to '0'.

15.4.3.7 TDQS, $\overline{\text{TDQS}}$

TDQS (Termination Data Strobe) is a feature of X8 gDDR3 SDRAM that provides additional termination resistance outputs that may be useful in some system configurations.

TDQS is not supported in X4 or X16 configurations. When enabled via the mode register, the same termination resistance function is applied to the TDQS/$\overline{\text{TDQS}}$ pins that is applied to the DQS/$\overline{\text{DQS}}$ pins.

In contrast to the RDQS function of DDR2 SDRAM, TDQS provides the termination resistance function only. The data strobe function of RDQS is not provided by TDQS.

The TDQS and DM functions share the same pin. When the TDQS function is enabled via the mode register, the DM function is not supported. When the TDQS function is disabled, the DM function is provided and the $\overline{\text{TDQS}}$ pin is not used. See Table 5 for details.

The TDQS function is available in X8 gDDR3 SDRAM only and must be disabled via the mode register A11=0 in MR1 for X4 and X16 configurations.

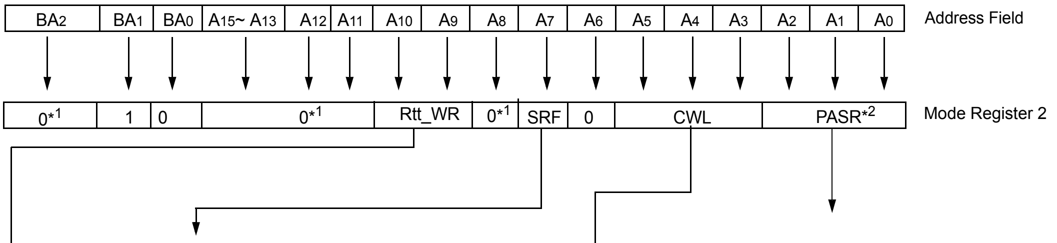
[Table 4] TDQS, $\overline{\text{TDQS}}$ Function Matrix

MR1(A11)	DM / TDQS	NU / TDQS
0 (TDQS Disabled)	DM	Hi-Z
1 (TDQS Enabled)	TDQS	$\overline{\text{TDQS}}$

Note :
1. If TDQS is enabled, the DM function is disabled.
2. When not used, TDQS function can be disabled to save termination power.
3. TDQS function is only available for X8 DRAM and must be disabled for X4 and X16.

15.4.4 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS write latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.



A7	Self-refresh temperature range(SRT)[*1]
0	Normal self-refresh
1	Extend temperature self-refresh (Optional)

Note1:gDDR3 SDRAM must support self refresh operation at all supported temperatures.
Applications requiring self refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately

A2	A1	A0	Partial Array Self Refresh (Optional)
0	0	0	Full Array
0	0	1	HalfArray (BA[2:0]=000,001,010, &011)
0	1	0	Quarter Array (BA[2:0]=000, & 001)
0	1	1	1/8th Array (BA[2:0] = 000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	HalfArray (BA[2:0] = 100, 101, 110, &111)
1	1	0	Quarter Array (BA[2:0]=110, &111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt_WR[*1]
0	0	Dynamic ODT off (Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

Note1: If RTT_Nom is disabled by setting bits 2,6,9 in MR1 to “0”, RTT_WR is also disabled; In Write leveling mode, only RTT_Nom is available

A5	A4	A3	CAS write Latency (CWL)
0	0	0	5 (tCK ≥2.5ns)
0	0	1	6 (2.5ns >tCK≥1.875ns)
0	1	0	7 (1.875ns>tCK≥1.5ns)
0	1	1	8 (1.5ns>tCK≥1.25ns)
1	0	0	9 (1.25ns>tCK≥1.07ns)
1	0	1	10 (1.0ns>tCK≥0.935ns)
1	1	0	Reserved
1	1	1	Reserved

* 1 : BA2, A3 - A4 and A8 ~ A15 are RFU and must be programmed to 0 during MRS

* 2 : Optional in DDR3 SDRAM : If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified address range will be lost if self refresh is entered. Data integrity will be maintained if tREF conditions are met and no Self Refresh command is issued.

Figure 8 - MR2 Definition

15.4.4.1 Partial Array Self-Refresh (PASR)

Optional in gDDR3 SDRAM: Users should refer to the DRAM component data sheet and/or the DIMM SPD to determine if gDDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 8 will be lost if Self-Refresh is entered. Data integrity will be maintained if tREFI conditions are met and no Self-Refresh command is issued.

15.4.4.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 8. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For more information on the supported CWL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on each component datasheet. For detailed Write operation refer to "WRITE Operation"on page 41.

15.4.4.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

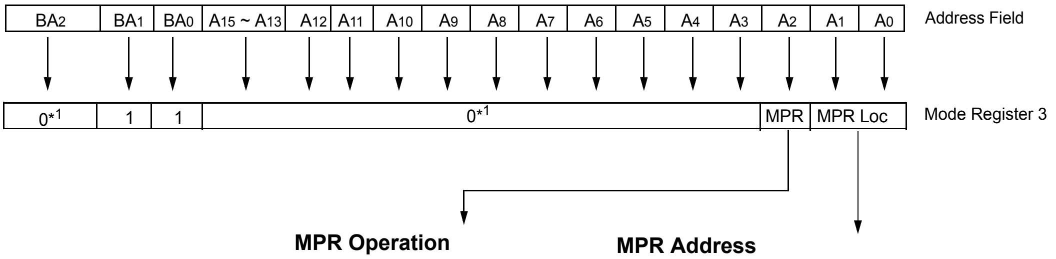
Optional in gDDR3 SDRAM: Users should refer to the DRAM component data sheet and/or the DIMM SPD to determine if gDDR3 SDRAM devices support the following options or requirements referred to in this material. For more details refer to ’Extended Temperature Usage’ on page 27. gDDR3 SDRAM’s must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

15.4.4.4 Dynamic ODT (Rtt_WR)

gDDR3 SDRAM introduces a new feature "Dynamic ODT’. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the gDDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT setings. In Write leveling mode, only RTT_Nom is available. For details on ODT operation, refer to " Dynamic ODT"on page 60.

15.4.5 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and BA0, while controlling the states of address pins according to the table below.



MPR Operation

A2	MPR
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

* 1 : BA2, A3 - A15 are RFU and must be programmed to 0 during MRS.
* 2 : The predefined pattern will be used for read synchronization.
* 3 : When MPR control is set for normal operation, MR3 A[2]=0, MR3 A[1:0] will be ignored

Figure 9 - MR3 Definition

15.4.5.1 Multi-Purpose Register (MPR)

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP/tRPA met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to "Multi Purpose Register" on page 28.

16.0 gDDR3 SDRAM Command Description and Operation

16.1 Command Truth Table

(a) Note 1,2,3,4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write command
[BA=Bank Address, RA=Row Address, CA=Column Address, $\overline{BC}$=Burst Chop, X=Don't care, V=Valid]

[Table 5] Command Truth Table

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 - BA3	A13 - A15	A12 / $\overline{BC}$	A10 / AP	A0 - A9,A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7,8,9,12
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BL4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BL4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BL4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BL4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BL4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BL4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BL4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BL4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselect	DES	H	H	H	X	X	X	X	X	X	X	X	11
ZQ calibration Long	ZQCL	H	H	L	H	H	L	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	L	V	V	V	L	V	
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,a12
				H	V	V	V						
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						

Note :

1. All gDDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device density and configuration dependant
2. $\overline{RESET}$ is an active low asynchronous signal that must be driven high during normal operation
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level"
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the fly BL will be defined by MRS
6. The Power Down Mode does not perform any refresh operations.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self refresh exit is asynchronous.
9. V_{REF}(Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the gDDR3 SDRAM is in an idle or a wait state. The purpose of the No Operation command (NOP) is to prevent the gDDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as a No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition

16.2 Clock Enable (CKE) Truth Table

(a) Note 1~7 apply to the entire Command truth table
(b) see ‘power down chapter’ for detailed definition of power down entry, exit and respective parameters
(c) CKE low is allowed only if tMRD and tMOD are satisfied

[Table 6] CKE Truth Table

Current State [2]	CKE		Command (N) [3]	Action (N) [3]	Notes
	Previous Cycle [1] (N-1)	Current Cycle [1] (N)	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$		
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT or NOP	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT or NOP	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT or NOP	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details will all signals See 2.1 " Command Truth Table"					10

Note:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is the state of the gDDR3 SDRAM immediately prior to clock edge N
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
6. tCKEmin of [TBD] clocks means CKE must be registered on [TBD] consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the [TBD] clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + [TBD] + tIH
7. DESELECT and NOP are defined in the Command truth table
8. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
9. Self Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self Refresh Exit are NOP and DESELECT only.
13. Self Refresh can not be entered while Read or Write operations. See section 2.16 "Power Down Modes" and 2.15 "Self Refresh Operation" for a detailed list of restrictions.
14. The Power Down does not perform any refresh operations.
15. “X” means “don’t care (including floating around V_{REF})” in Self Refresh and Power Down. It also applies to Address pins
16. V_{REF} (Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power Down is entered, otherwise Active Power Down is entered
18. ‘Idle state’ means that all banks are closed(tRP,tDAL,etc. satisfied) and CKE is high and all timings from previous operations are satisfied (tMRD,tMOD,tRFC,tZQinit,tZQoper,tZQCS,etc)as well as all SRF exit and Power Down exit parameters are satisfied (tXS,tXP,tXPDLL,etc)

16.3 No OPeration (NOP) Command

The No OPeration (NOP) command is used to instruct the selected DDR3 SDRAM to perform a NOP ($\overline{\text{CS}}$ LOW and $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ HIGH). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

16.4 Deselect Command

The DESELECT function ($\overline{\text{CS}}$ HIGH) prevents new commands from being executed by the gDDR3 SDRAM. The gDDR3 SDRAM is effectively deselected. Operations already in progress are not affected.

16.5 DLL-off Mode

gDDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0" The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to "Input clock frequency change" on Figure 15,16,17.

The DLL-off Mode operations listed below are an optional feature for gDDR3. The maximum clock frequency for DLLoff Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=6 and CWL=6.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command. Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.

The timing relations on DLL-off mode READ operation have shown at following Timing Diagram (CL=6, BL=8):

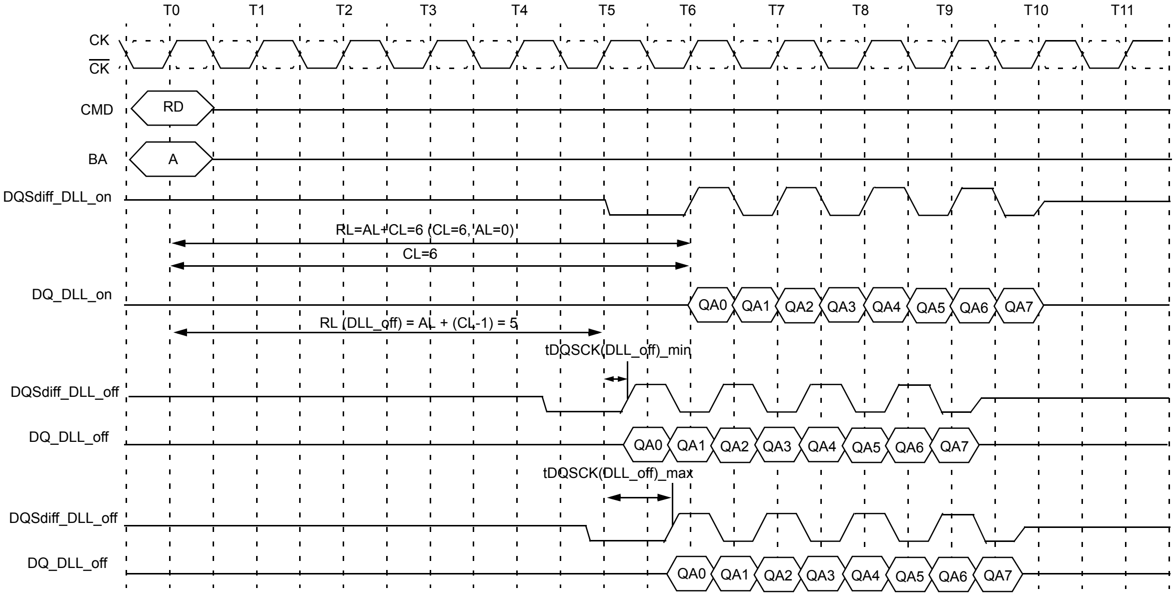

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
CK
CK
CMD
RD
BA
A
DQSdiff_DLL_on
RL=AL+CL=6 (CL=6, AL=0)
CL=6
DQ_DLL_on
QA0
QA1
QA2
QA3
QA4
QA5
QA6
QA7
RL (DLL_off) = AL + (CL-1) = 5
tDQSCK(DLL_off)_min
DQSdiff_DLL_off
DQ_DLL_off
tDQSCK(DLL_off)_max
DQSdiff_DLL_off
DQ_DLL_off

Figure 10 - DLL-off mode READ Timing Operation

16.6 DLL on/off switching procedure

gDDR3 DLL-off mode is entered by setting MR1 bit A0 to "1"; this will disable the DLL for subsequent operations until A0 bit set back to "0".

16.6.1 DLL "on" to DLL "off" Procedure

To switch from DLL "on" to DLL "off" requires the frequency to be changed during Self-Refresh outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT, must be in high impedance state before MRS to MR1 to disable the DLL.)
2. Set MR1 bit A0 to "1" to disable the DLL.
3. Wait tMOD.
4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.
5. Change frequency, in guidance with "Input clock frequency change" on page 23.
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS commad are satisfied. If both ODT features were disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
8. Wait tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS)
9. Wait for tMOD, then DRAM is ready for next command.

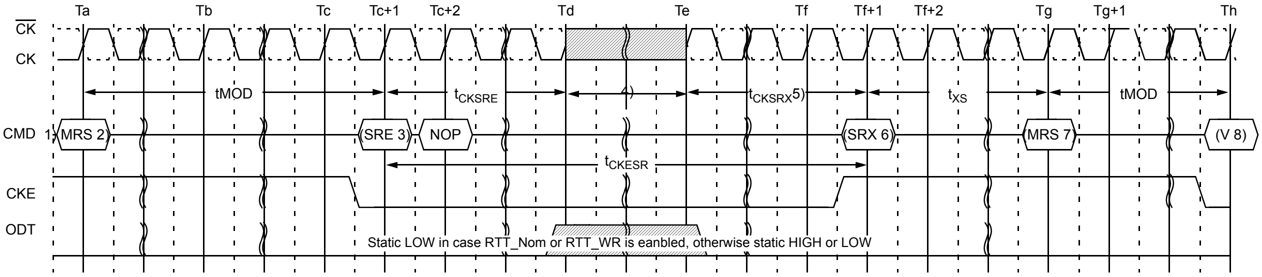


Figure 11 : DLL Switch Sequence from DLL-on to DLL-off

Note :
1) Starting with Idle State, RTT in Hi-Z state
2) Disable DLL by setting MR1 Bit A0 to 1
3) Enter SR
4) Change Frequency
5) Clock must be stable at least t cksrx
6) Exit SR
7) Update Mode registers with DLL off parameters setting
8) Any valid command

16.6.2 DLL "off" to DLL "on" Procedure

To switch from DLL "off" to DLL "on" (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT) must be in high impedance state before Self-Refresh mode is entered.)
2. Enter Self Refresh Mode, wait until tCKSRE satisfied.
3. Change frequency, in guidance with "Input clock frequency change" on page 23.
4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If both ODT features are disabled in the mode registers when Self Refresh mode was entered, ODT signal can be registered LOW or HIGH.
6. Wait tXS, then set MR1 bit A0 to "0" to enable the DLL.
7. Wait tMRD, then set MR0 bit A8 to "1" to start DLL Reset.
8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)
9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCLcommand was issued.

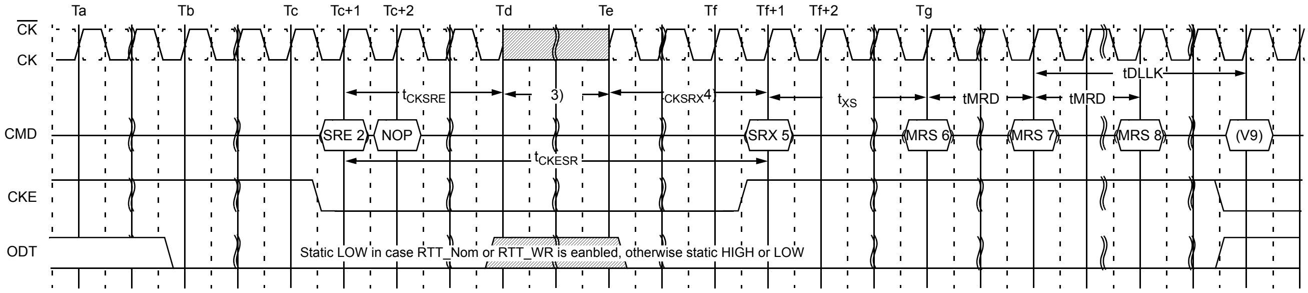


Figure 12 - DLL Switch Sequence from DLL Off to DLLOn

Note :
1) Starting from Idle state
2) Enter SR
3) Frequency Change
4) Clock must be stable for at least tCKSRX
5) Exit SR
6) Set DLL-on by MR1 A0='0'
7) Start DLL Reset
8) Update rest MR register values
9) Ready fo valid command

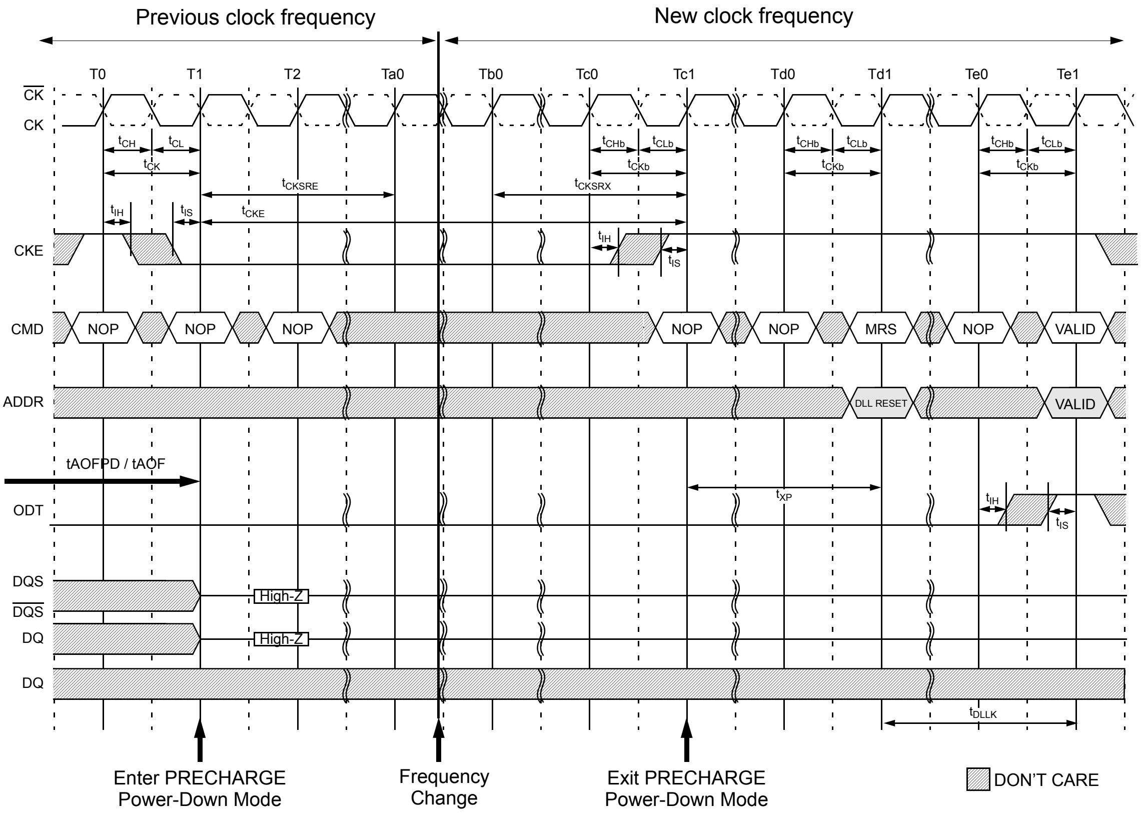
16.7 Input clock frequency change

Once the gDDR3 SDRAM is initialized, the gDDR3 SDRAM requires the clock to be "stable" during almost all states of normal operation. This means once the clock frequency has been set and is to be in the "stable state", the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under two conditions:
(1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.

For the first condition, once the gDDR3 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don't care. Once a don't care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in See 2.15 "Self-Refresh Operation" on page 48. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to "DLL on/off switching procedure" on page 21.

The second condition is when the DDR3 SDRAM is in Precharge Power-down mode (either fast exit mode or slow exit mode). If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change. The gDDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, ODT and CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, the DLL must be RESET via MRS. Depending on the new clock frequency additional MRS commands may need to be issued to appropriately set the WR, CL, and CWL with CKE continuously registered high. During DLL re-lock period, ODT must remain LOW and CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency. This process is depicted in Figure 13 below.



Note :
1. Applicable for both SLOW EXIT and FAST EXIT Precharge Power-down
2. tCKSRE and tCKSRX are Self-Refresh mode specifications but the value they represent are applicable here
{note 2 can be removed when tCKSRE and tCKSRX are redefined in timing table}
3. tAOFPD and tAOP must be satisfied and outputs High-Z prior to T1 : refer to ODT timing section for exact requirements

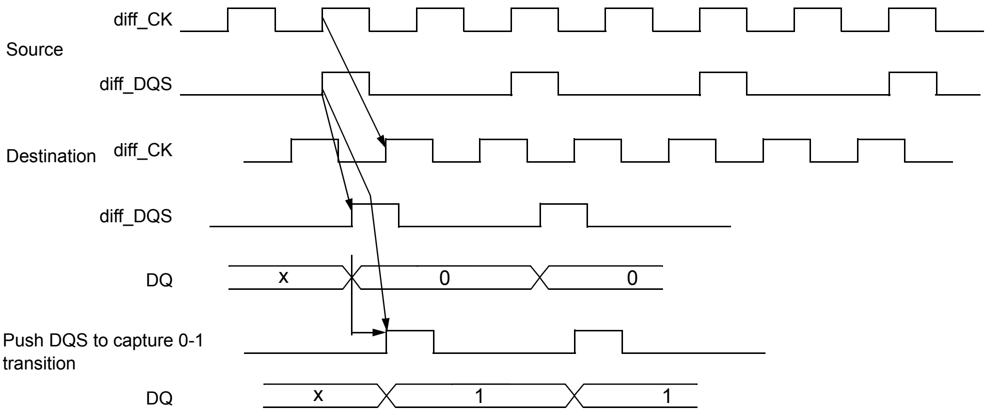
Figure 13 - Change Frequency during Precharge Power-down.

16.8 Write Leveling

For better signal integrity, gDDR3 memory module adopted fly by topology for the commands, addresses, control signals and clocks. The fly by topology has benefits from reducing number of stubs and their length but in other aspect, causes flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the controller should support 'write leveling' in gDDR3 SDRAM to compensate the skew.

Write leveling is a scheme to adjust DQS to CK relationship by the controller, with a simple feedback provided by the DRAM. The memory controller involved in the leveling must have adjustable delay setting on DQS to align the rising edge of DQS with that of the clock at the DRAM pin. DRAM asynchronously feeds back CK, sampled with the rising edge of DQS, through the DQ bus. The controller repeatedly delays DQS until a transition from 0 to 1 is detected. The DQS delay established through this exercise would ensure tDQSS, tDSS and tDSH specification. A conceptual timing of this scheme is shown as below.

Write leveling concept



DQS/$\overline{\text{DQS}}$ driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

One or more data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

16.8.1 DRAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set "High" and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set "Low" (Table 9). Note that in write leveling mode, only DQS/$\overline{\text{DQS}}$ terminations are activated and deactivated via ODT pin not like normal operation (Table 10).

[Table 7] MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

[Table 8] DRAM termination function in the leveling mode

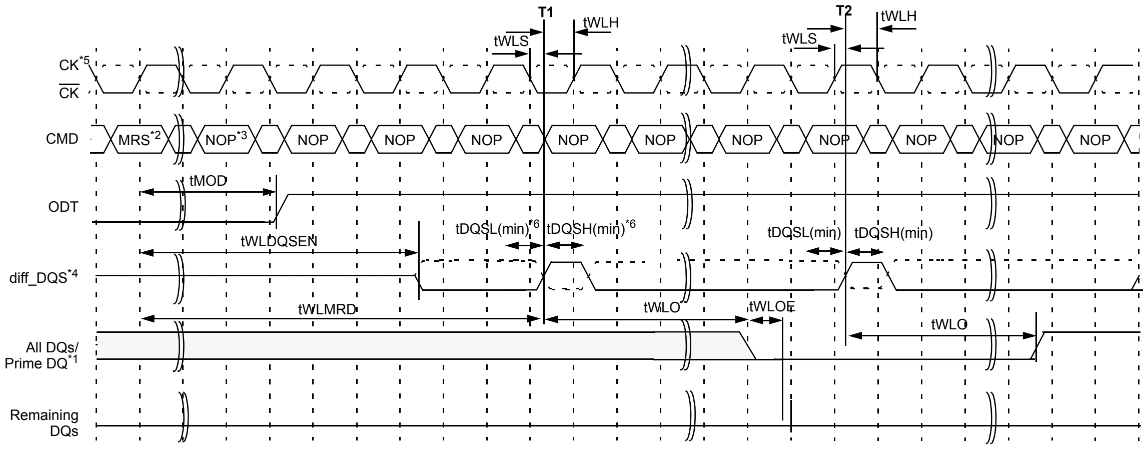
ODT pin @DRAM	DQS/$\overline{\text{DQS}}$ termination	DQs termination
De-asserted	Off	Off
Asserted	On	Off

Note : In Write Leveling Mode with its output buffer disabled (MR1[bit7] = 1 with MR1[bit12] = 1) all RTT_Nom settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit7] = 1 with MR1[bit12] = 0) only RTT_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.

16.8.2 Procedure Description

Memory controller initiates Leveling mode of all DRAMs by setting bit 7 of MR1 to 1. With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed. Since the controller levels one rank at a time, the output of other rank must be disabled by setting MR1 bit A12 to 1. Controller may assert ODT after tMOD, time at which DRAM is ready to accept the ODT signal.
Controller may drive DQS low and $\overline{\text{DQS}}$ high after a delay of tWLDQSEN, at which time DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, controller provides a single DQS, $\overline{\text{DQS}}$ edge which is used by the DRAM to sample CK driven from controller. tWLMRD(max) timing is controller dependent. DRAM samples CK status with rising edge of DQS and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits; there are no read strobes (DQS/$\overline{\text{DQS}}$) needed for these DQs. Controller samples incoming DQ and decides to increment or decrement DQS delay setting and launches the next DQS/$\overline{\text{DQS}}$ pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS delay setting and write leveling is achieved for the device.
Figure 14 describes the timing diagram and parameters for the overall Write Leveling procedure.

Figure 14 - Timing details of Write leveling sequence [DQS is capturing CK low at T1 and CK high at T2]



Note *:
1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS : Load MR1 to enter write leveling mode
3. NOP : NOP or deselect
4. diff_DQS is the differential data strobe (DQS-$\overline{\text{DQS}}$). Timing reference points are the zero crossings. DQS is shown with solid line, $\overline{\text{DQS}}$ is shown with dotted line
5. CK/$\overline{\text{CK}}$: CK is shown with solid dark line, where as $\overline{\text{CK}}$ is drawn with dotted line.
6. DQS needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

16.8.3 Write Leveling Mode Exit

The following sequence describes how Write Leveling Mode should be exited:

1. After the last rising strobe (see ~T111) edge, stop driving the strobe signals (see ~T128). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MR command (T145).
2. Drive ODT pin low (tIS must be satisfied) and keep it low. (see T128).
3. After the RTT is switched off, disable Write Level Mode via MR command (see T132).
4. After tMOD is satisfied (T145), a any valid command may be registered. (MR commands may already be issued after tMRD (T136).

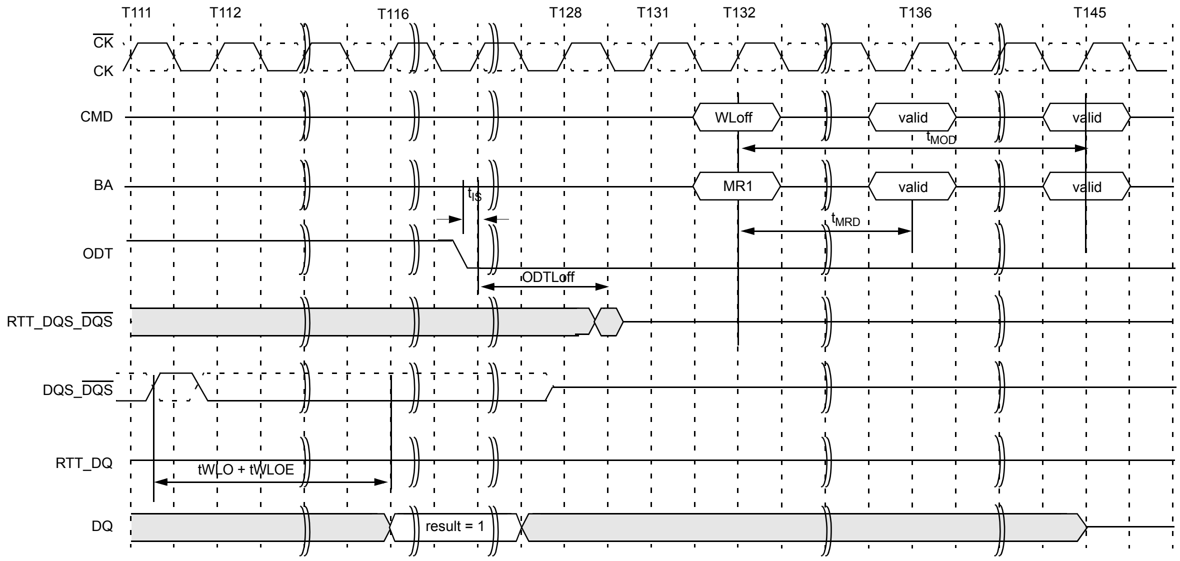

T111
T112
T116
T128
T131
T132
T136
T145
CK̄
CK
CMD
WLoff
valid
valid
t_{MOD}
BA
MR1
valid
valid
t_{IS}
t_{MRD}
ODT
ODTLoff
RTT_DQS_DQS̄
DQS_DQS̄
RTT_DQ
tWLO + tWLOE
DQ
result = 1

Figure 15 - Timing details of Write leveling exit

16.9 Extended Temperature Usage

Users should refer to the SAMSUNG data sheet and/or the DIMM SPD to determine if gDDR3 SDRAM devices support the following options or requirements referred to in this material:

a. Auto Self-refresh supported
b. Extended Temperature Range supported
c. Double refresh required for operation in the Extended Temperature Range (applies only for devices supporting the Extended Temperature Range)

[Table 9] Mode Register Description

Field	Bits	Description
SRT	MR2(A7)	**Self-Refresh Temperature (SRT) Range** If ASR = 0, the SRT bit must be programmed to indicate TOPER during subsequent Self-Refresh operation If ASR = 1, SRT bit must be set to 0b 0 = Normal operating temperature range 1 = Extended (optional) operating temperature range

16.9.1 Self-Refresh Temperature Range - SRT

SRT applies to devices supporting Extended Temperature Range only. If ASR = ’0’, the Self-Refresh Temperature (SRT) Range bit must be programmed to guarantee proper self-refresh operation. If SRT = ’0’, then the DRAM will set an appropriate refresh rate for Self-Refresh operation in the Normal Temperature Range. If SRT = ’1’ then the DRAM will set an appropriate, potentially different, refresh rate to allow Self-Refresh operation in either the Normal or Extended Temperature Ranges. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.

For parts that do not support the Extended Temperature Range, MR2 bit A7 must be set to ’0’ and the DRAM should not be operated outside the Normal Temperature Range.
Please refer to the component data sheet and/or the DIMM SPD for Extended Temperature Range availability.

[Table 10] Self-Refresh mode summary

MR2 A[6]	MR2 A[7]	Self-Refresh operation	Allowed Operating Temperature Range for Self-Refresh Mode
0	0	Self-refresh rate appropriate for the Normal Temperature Range	Normal (0 - 85 °C)
0	1	Self-refresh rate appropriate for either the Normal or Extended Temperature Ranges. The DRAM must support Extended Temperature Range. The value of the SRT bit can effect self-refresh power consumption, please refer to the IDD table for details.	Normal and Extended (0 - 95 °C)
1	0	ASR enabled (not supported). Self-Refresh power consumption is temperature dependent	Normal (0 - 85 °C)
1	0	ASR enabled (not supported). Self-Refresh power consumption is temperature dependent	Normal and Extended (0 - 95 °C)
1	1	Illegal	

16.10 Multi Purpose Register

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence.
The basic concept of the MPR is shown in Figure 16.

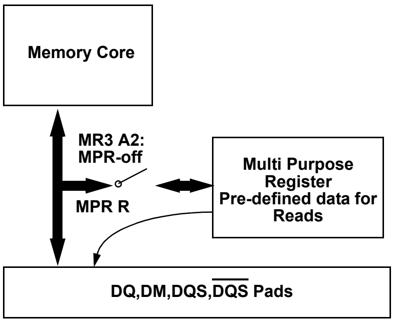

Memory Core
MR3 A2:
MPR-off
MPR R
Multi Purpose Register Pre-defined data for Reads
DQ,DM,DQS,$\overline{DQS}$ Pads

Figure 16 - MPR Block Diagram

To enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2 = 1, as shown in Table 13. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP/tRPA met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation when a RD or RDA command is issued is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 14. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3 bit A2 = 0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

[Table 11] MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0	don't care	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1	See Table 14	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0].

16.10.1 MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x4:
  DQ[0] drives information from MPR.
  DQ[3:1] either drive the same information as DQ[0], or they drive '0'.
- Register Read on x8:
  DQ[0] drives information from MPR.
  DQ[7:1] either drive the same information as DQ[0], or they drive '0'.
- Register Read on x16:
  DQL[0] and DQU[0] drive information from MPR.
  DQL[7:1] and DQU[7:1] either drive the same information as DQL[0], or they drive '0'.
- Addressing during for Multi Purpose Register reads for all MPR agents:
  BA[2:0]: don't care
  A[1:0]: A[1:0] must be equal to '00'. Data read burst order in nibble is fixed
  A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7], *) For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3 *) A[2]=1b, Burst order : 4,5,6,7 *)
  A[9:3]: don't care
  A10/AP: don't care
  A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
  A11, A13,... (if available): don't care
- Regular interface functionality during register reads:
  Support two Burst Ordering which are switched with A2 and A[1:0]=00.
  Support of read burst chop (MRS and on-the-fly via A12/BC)
  All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
  Regular read latencies and AC timings apply.
  DLL must be locked prior to MPR Reads.

Note: *) Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

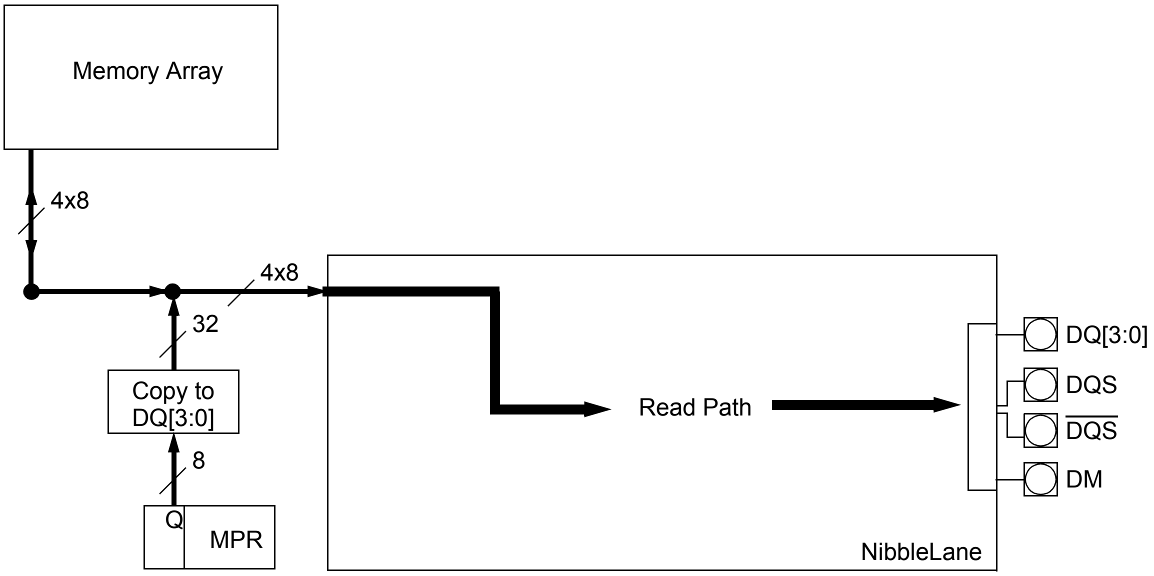

Memory Array
4x8
4x8
32
Copy to DQ[3:0]
8
Q
MPR
Read Path
NibbleLane
DQ[3:0]
DQS
$\overline{\text{DQS}}$
DM

Figure 17 - MPR Functional Block Diagram (x4 config)

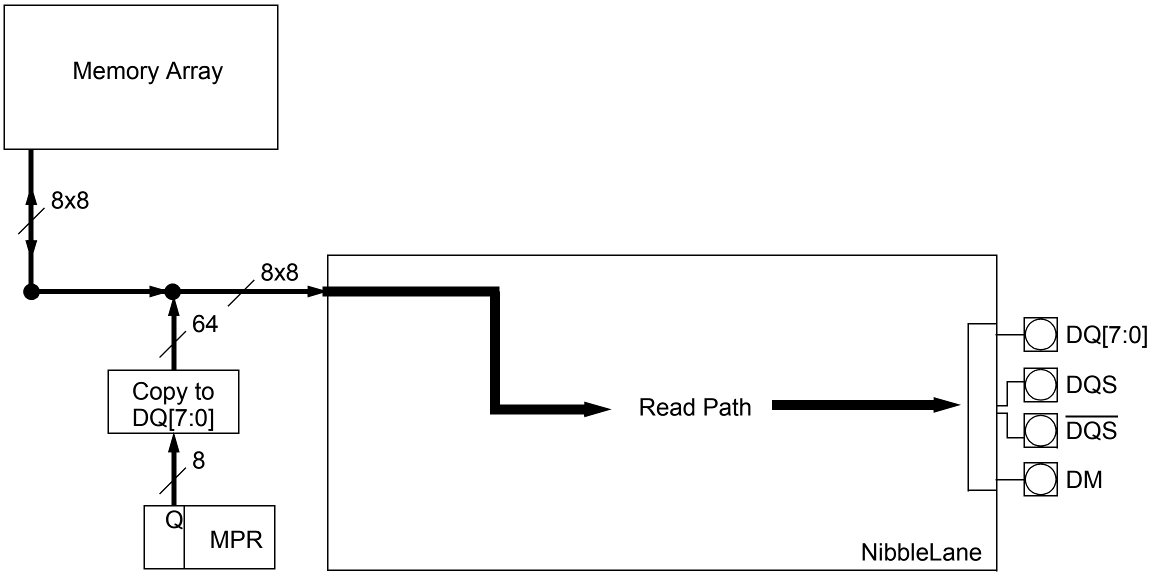

Memory Array
8x8
8x8
64
Copy to DQ[7:0]
8
Q
MPR
Read Path
NibbleLane
DQ[7:0]
DQS
$\overline{\text{DQS}}$
DM

Figure 18 - MPR Functional Block Diagram (x8 config)

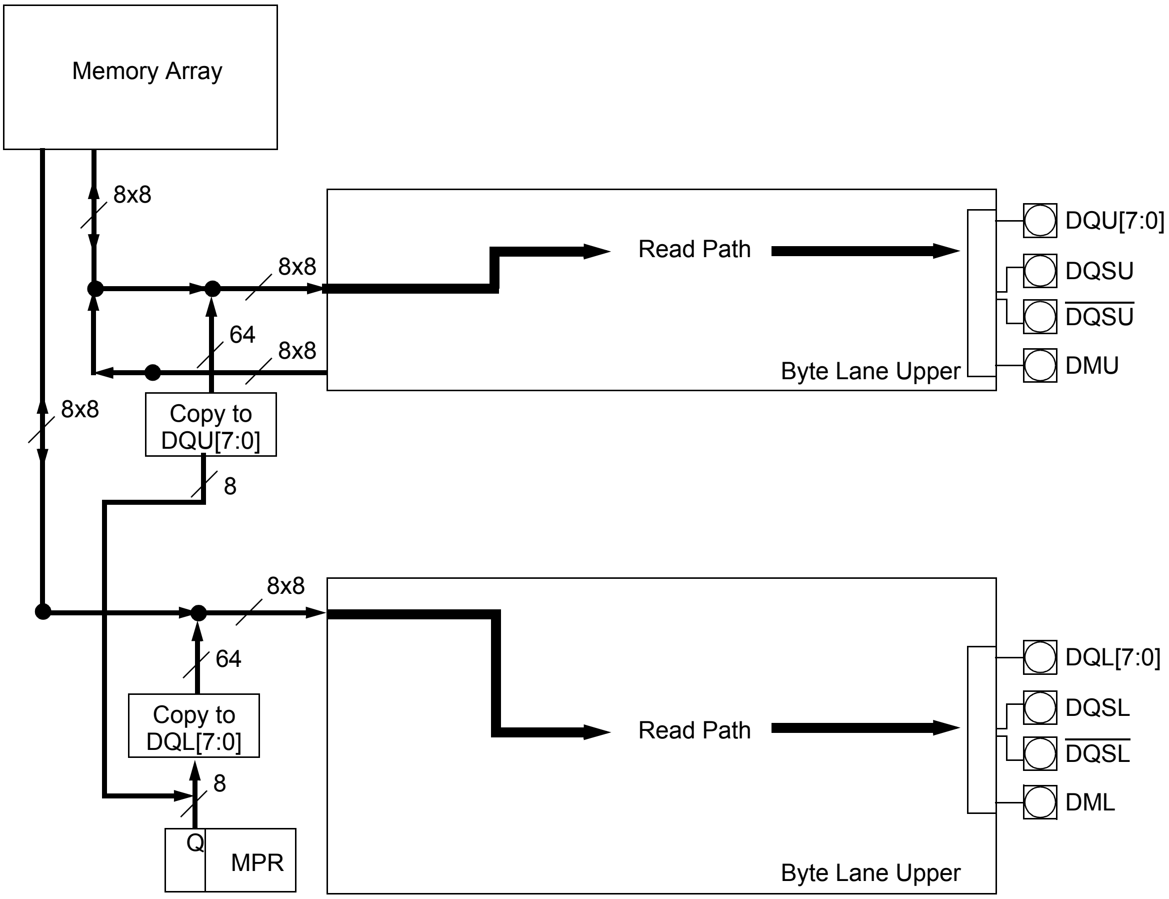

Memory Array
8x8
8x8
64
8x8
8x8
Copy to DQU[7:0]
8
Read Path
Byte Lane Upper
DQU[7:0]
DQSU
$\overline{\text{DQSU}}$
DMU
8x8
64
Copy to DQL[7:0]
8
Q
MPR
Read Path
Byte Lane Upper
DQL[7:0]
DQSL
$\overline{\text{DQSL}}$
DML

Figure 19 - MPR Functional Block Diagram (x16 config)

16.10.2 MPR Register Address Definition

Table 14 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

[Table 12] MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read Predefined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	BL8 000b Burst order 0,1,2,3,4,5,6,7
			BC4	000b	BC4 000b Burst order 0,1,2,3
			BC4	100b	BC4 100b Burst order 4,5,6,7

Note : Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.

16.10.3 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to "Electrical Characteristics & AC Timing for gDDR3-1333 to gDDR3-2000" on each component datasheet.

16.10.4 Protocol Example

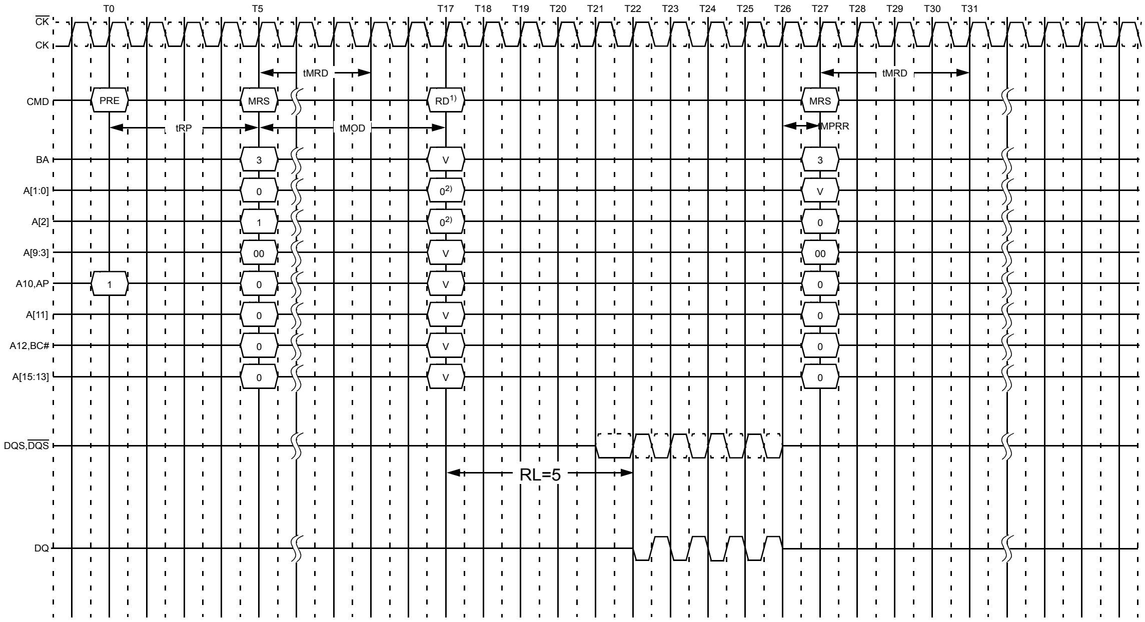
Protocol Example (This is one example) : Read out predetermined read-calibration pattern.

Description: Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until tRP is satisfied.
- MRS MR3, Opcode "A2 = 1" and "A[1:0] = 00"
  Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the period MR3 A2 =1, no data write operation is allowed.
- Read:
  A[1:0] = ’00’ (Data burst order is fixed starting at nibble, always ’00’ here)
  A[2] = ’0’ (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)
  A12/BC = 1 (use regular burst length of 8)
  All other address pins (including BA[2:0] and A10/AP): don’t care
- After RL = AL + CL, DRAM bursts out the predefined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst, wait until tMPRR is satisfied.
- MRS MR3, Opcode "A2 = 0" and "A[1:0] = valid data but value are don’t care"
  All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
- Wait until tMRD and tMOD are satisfied.
- Continue with "regular" DRAM commands, like activate a memory bank for regular read or write access,...

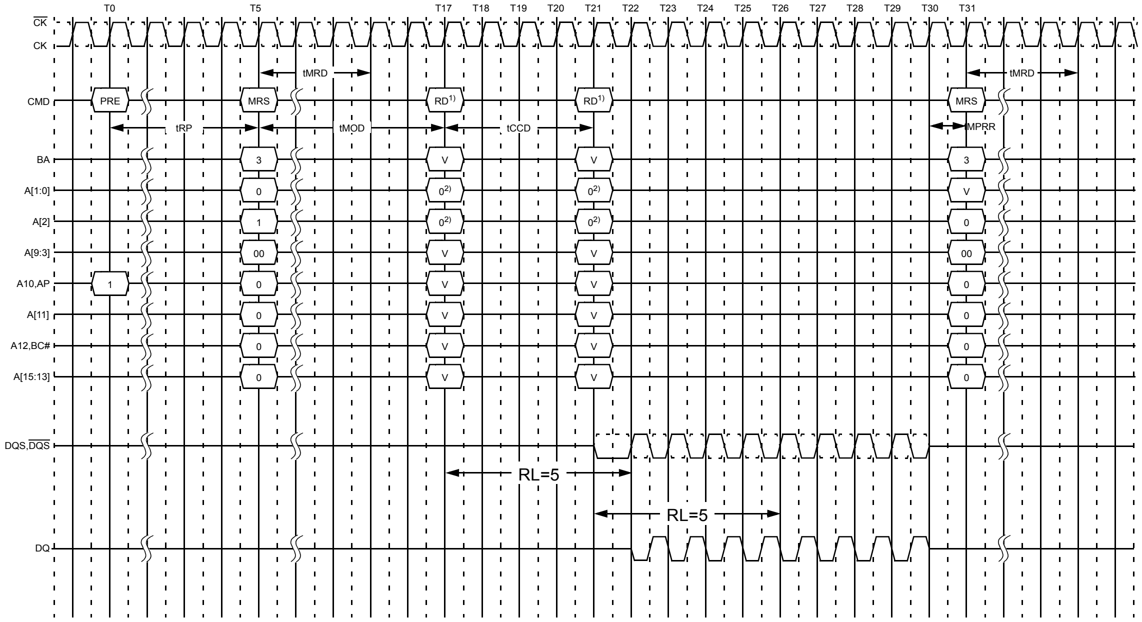
Readout of predefined pattern for system read calibration with BL8
(RL=5tCK, Fixed Burst order and Single Readout)


T0
T5
T17
T18
T19
T20
T21
T22
T23
T24
T25
T26
T27
T28
T29
T30
T31
CK
CK
CMD
PRE
MRS
RD 1)
MRS
tMRD
tMRD
tRP
tMOD
tMPRR
BA
A[1:0]
A[2]
A[9:3]
A10,AP
A[11]
A12,BC#
A[15:13]
DQS,DQS
RL=5
DQ

Notes :
1) RD with BL8 either by MRS or On the fly
2) Memory Controller must drive Low on A[2:0]

Figure 20 - MPR Readout of predefined pattern, BL8 fixed burst order, single readout

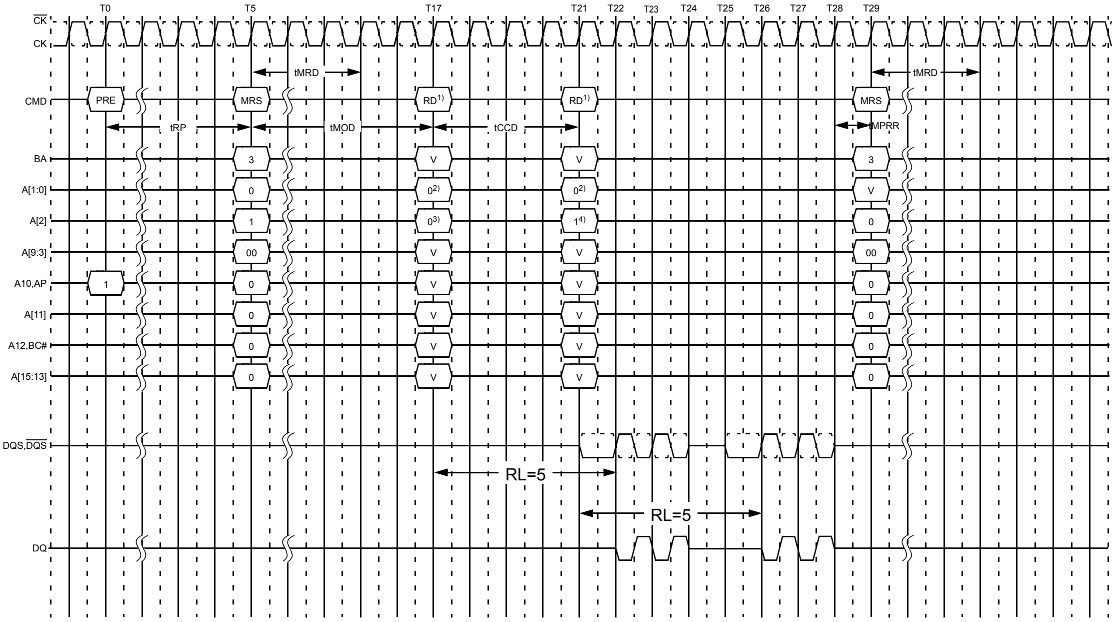
Readout of predefined pattern for system read calibration with BL8
(RL=5tCK, Fixed Burst order and Back-to-Back Readout)


T0
T5
T17
T18
T19
T20
T21
T22
T23
T24
T25
T26
T27
T28
T29
T30
T31
CK
CK
CMD
PRE
MRS
RD 1)
RD 1)
MRS
tMRD
tMRD
tRP
tMOD
tCCD
tMPRR
BA
A[1:0]
A[2]
A[9:3]
A10,AP
A[11]
A12,BC#
A[15:13]
DQS,DQS
RL=5
RL=5
DQ

Notes :
1) RD with BL8 either by MRS or On the fly
2) Memory Controller must drive Low on A[2:0]

Figure 21 - MPR Readout of predefined pattern, BL8 fixed burst order, back-to-back readout

Readout of predefined pattern for system read calibration with BC4
(RL=5tCK, First Lower Nibble than Upper Nibble)

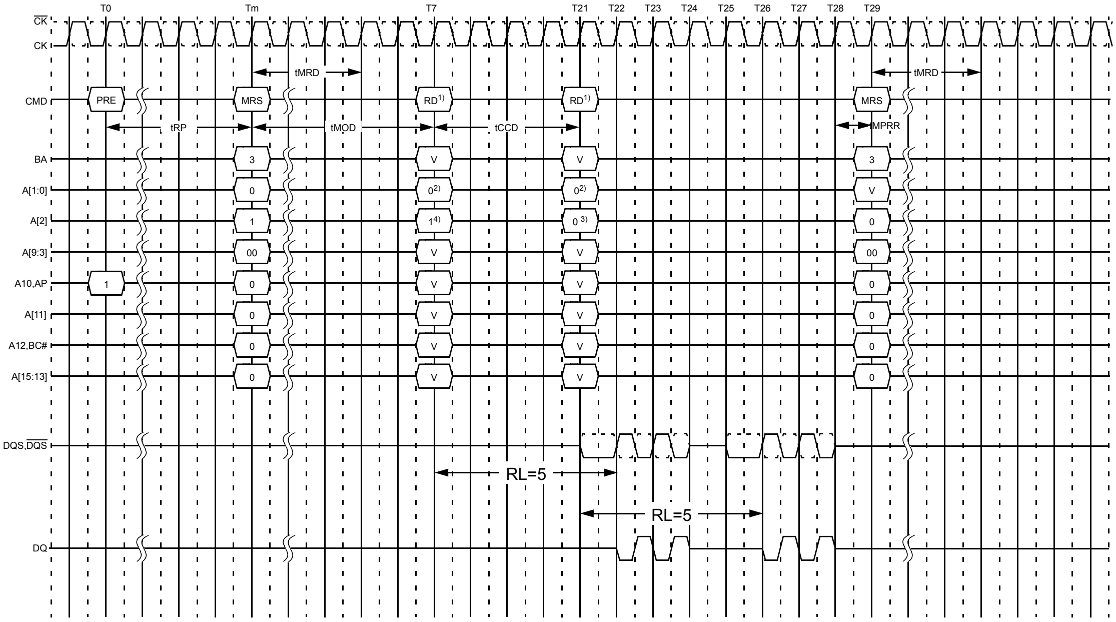

CK
CK
T0
T5
T17
T21
T22
T23
T24
T25
T26
T27
T28
T29
tMRD
CMD
PRE
MRS
RD1)
RD1)
MRS
tRP
tMOD
tCCD
tMPRR
BA
A[1:0]
A[2]
A[9:3]
A10,AP
A[11]
A12,BC#
A[15:13]
1
3
0
1
00
0
0
0
0
V
02)
03)
14)
DQS,DQS
RL=5
RL=5
DQ

Notes :
1) RD with BL4 either by MRS or On the fly
2) Memory Controller must drive Low on A[2:0]
3) A[2]=0 selects lower 4 nibble bits 0...3
4) A[2]=1 selects upper 4 nibble bits 4...7

Figure 22 - MPR Readout predefined pattern, BC4, lower nibble then upper nibble

Figure 23 - MPR Readout of predefined pattern, BC4, upper nibble then lower nibble

Readout of predefined pattern for system read calibration with BC4
(RL=5tCK, First Upper Nibble than Lower Nibble)


CK
CK
T0
Tm
T7
T21
T22
T23
T24
T25
T26
T27
T28
T29
tMRD
CMD
PRE
MRS
RD1)
RD1)
MRS
tRP
tMOD
tCCD
tMPRR
BA
A[1:0]
A[2]
A[9:3]
A10,AP
A[11]
A12,BC#
A[15:13]
1
3
0
1
00
0
0
0
0
V
02)
14)
0 3)
DQS,DQS
RL=5
RL=5
DQ

Notes :
1) RD with BL4 either by MRS or On the fly
2) Memory Controller must drive Low on A[2:0]
3) A[2]=0 selects lower 4 nibble bits 0...3
4) A[2]=1 selects upper 4 nibble bits 4...7

16.11 ACTIVE Command

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0-BA2 inputs selects the bank, and the address provided on inputs A0-A15 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

16.12 PRECHARGE Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

16.13 READ Operation

16.13.1 READ Burst Operation

During a READ or WRITE command, gDDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).
A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)
A12 = 1, BL8
A12 is used only for burst length control, not as a column address.

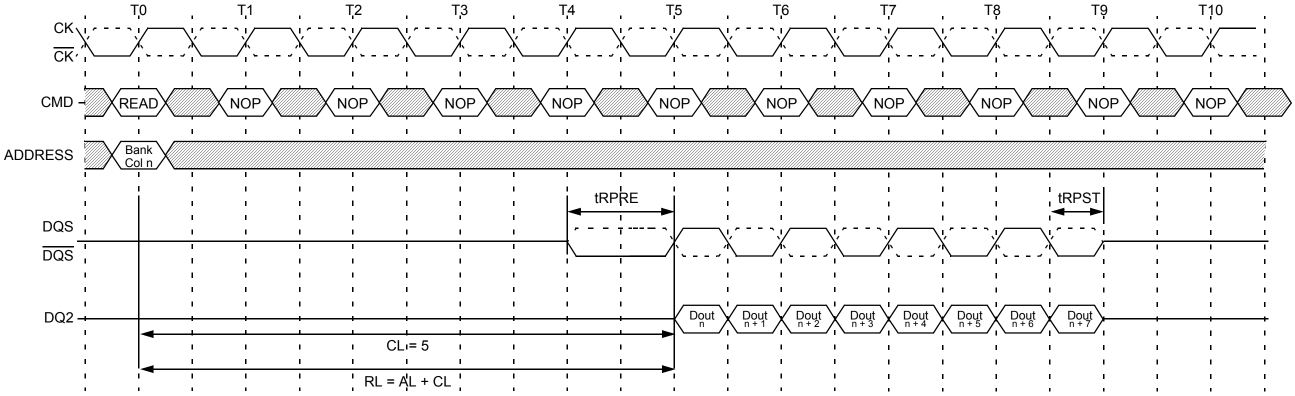

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CK
CK
CMD
READ
NOP
ADDRESS
Bank Col n
tRPRE
tRPST
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout n + 4
Dout n + 5
Dout n + 6
Dout n + 7
CL = 5
RL = AL + CL

Figure 24 - READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8)

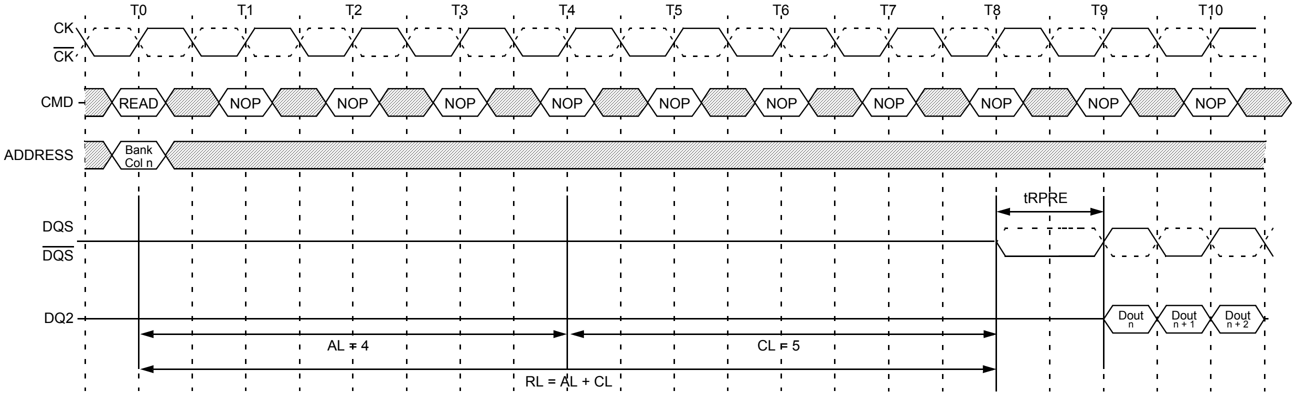

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CK
CK
CMD
READ
NOP
ADDRESS
Bank Col n
tRPRE
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
AL = 4
CL = 5
RL = AL + CL

Figure 25 - READ Burst Operation RL = 9 (AL = 4, CL = 5, BL8)

16.13.2 READ Timing Definitions

(Applied when the DLL is enabled and locked)

16.13.2.1 gDDR3 Clock to Data Strobe relationship

Rising data strobe edge parameters:
- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK, $\overline{CK}$.
- tDQSCK is the actual position of a rising strobe edge relative to CK, $\overline{CK}$.
- tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:
- tQSL describes the data strobe low pulse width.

tLZ(DQS), tHZ(DQS) for preamble/postamble (see 2.13.2.3 and Figure 36)

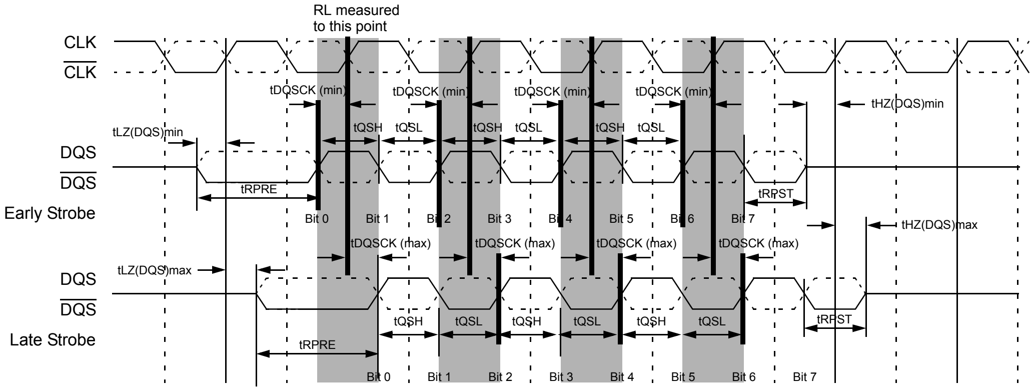

RL measured
to this point
CLK
$\overline{CLK}$
tDQSCK (min)
tQSH
tQSL
tLZ(DQS)min
tHZ(DQS)min
DQS
$\overline{DQS}$
Early Strobe
tRPRE
tRPST
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
tDQSCK (max)
tHZ(DQS)max
tLZ(DQS)max
Late Strobe

Figure 26 - Clock to Data Strobe Relationship

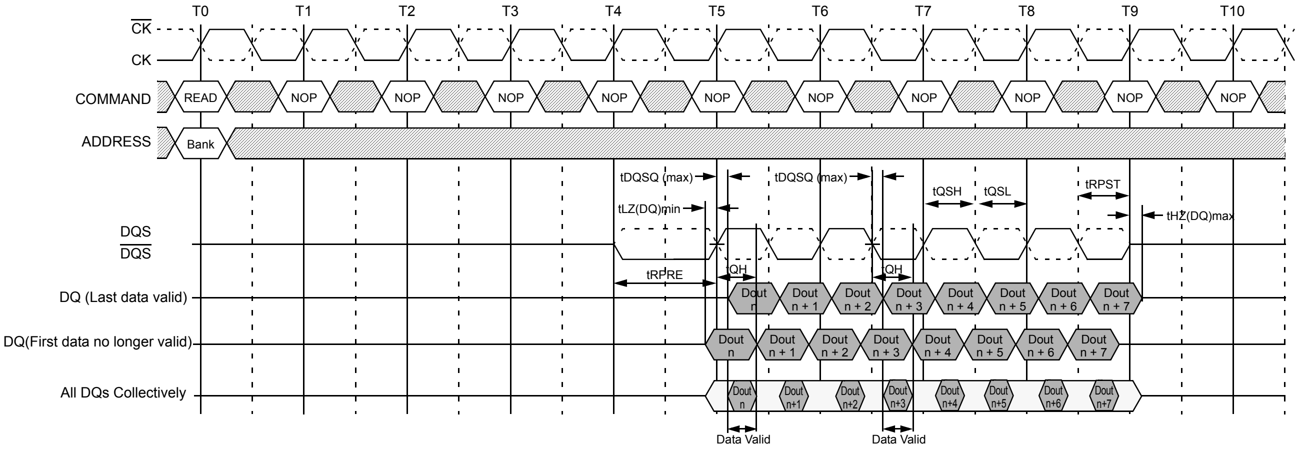
Note:
Within a burst, rising strobe edge is not necessarily fixed to be always at tDQSCK(min) or tDQSCK(max). Instead, rising strobe edge can vary between tDQSCK(min) and tDQSCK(max).
The DQS high pulse width is defined by tQSH and the DQS low pulse width is defined by tQSL Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case); However, they will tend to track each other.
The minimum pulse width of read preamble is defined by tRPRE(min). The minimum pulse width of read postamble is defined by tRPST(min).

16.13.2.2 gDDR3 Data Strobe to Data relationship

Rising data strobe edge parameters:
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

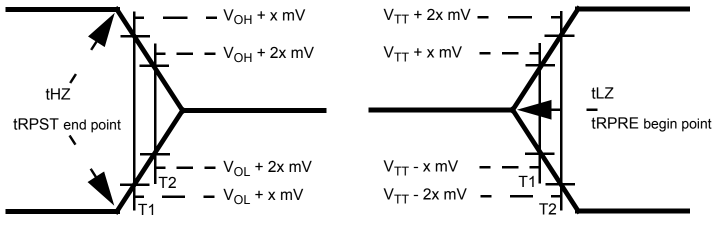
Falling data strobe edge parameters:
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
$\overline{CK}$
CK
COMMAND
READ
NOP
ADDRESS
Bank
tDQSQ (max)
tLZ(DQ)min
tQSH
tQSL
tRPST
tHZ(DQ)max
DQS
$\overline{DQS}$
tRPRE
tQH
DQ (Last data valid)
DQ(First data no longer valid)
All DQs Collectively
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout n + 4
Dout n + 5
Dout n + 6
Dout n + 7
Data Valid

16.13.2.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

tHZ and tLZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). Figure 28 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as singled ended.


V_{OH} + x mV
V_{OH} + 2x mV
tHZ
tRPST end point
V_{OL} + 2x mV
V_{OL} + x mV
T2
T1
V_{TT} + 2x mV
V_{TT} + x mV
tLZ
tRPRE begin point
V_{TT} - x mV
V_{TT} - 2x mV
T1
T2

tHZ,tRPST end point = 2*T1-T2 tLZ,tRPRE begin point = 2*T1-T2

Figure 28 - tLZ and tHZ method for calculating transitions and endpoints

16.13.2.4 tRPRE Calculation

Method for calculating differential pulse widths for tRPRE.
Figure is TBD

16.13.2.5 tRPST Calculation

Method for calculating differential pulse widths for tRPST.

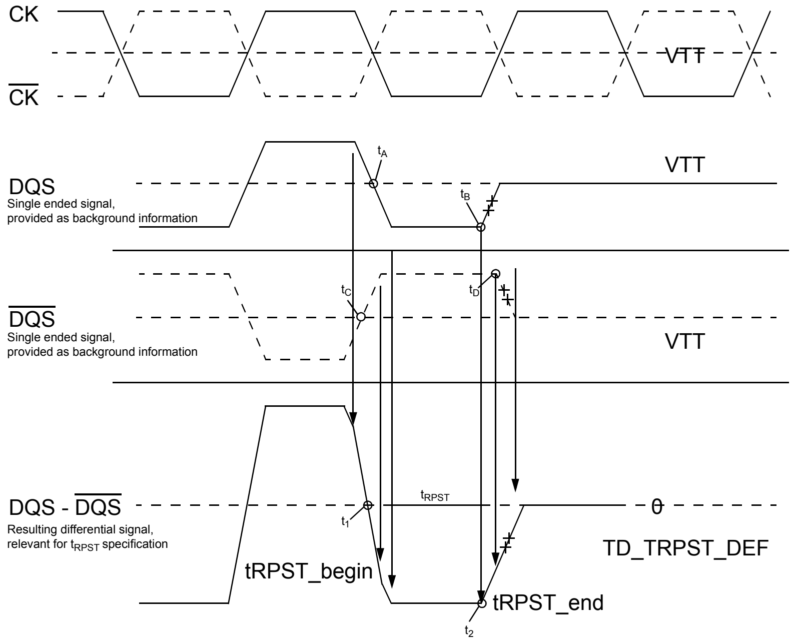
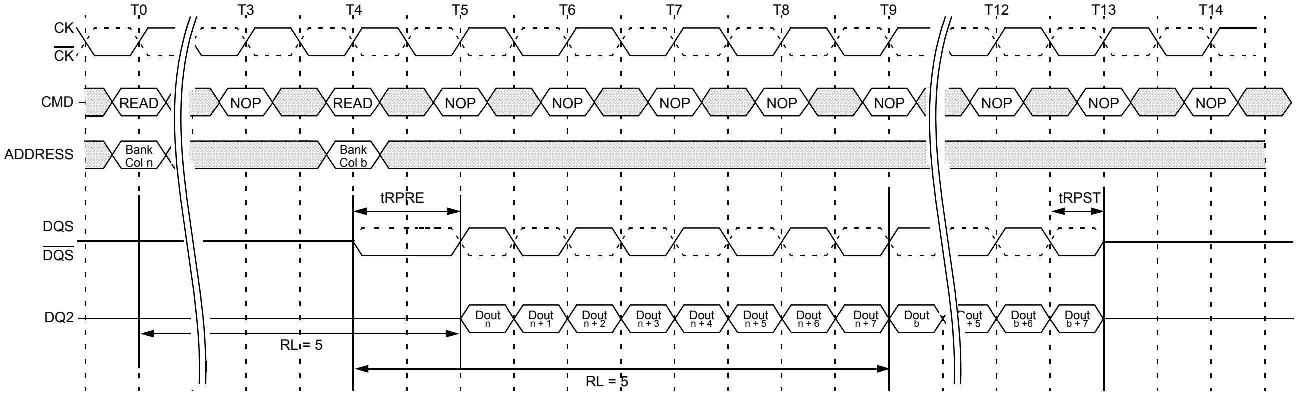

CK
CK
VTT
DQS
Single ended signal, provided as background information
t_A
t_B
VTT
DQS
Single ended signal, provided as background information
t_C
t_D
VTT
DQS - DQS
Resulting differential signal, relevant for t_{RPST} specification
t_1
t_{RPST}
0
TD_TRPST_DEF
tRPST_begin
tRPST_end
t_2

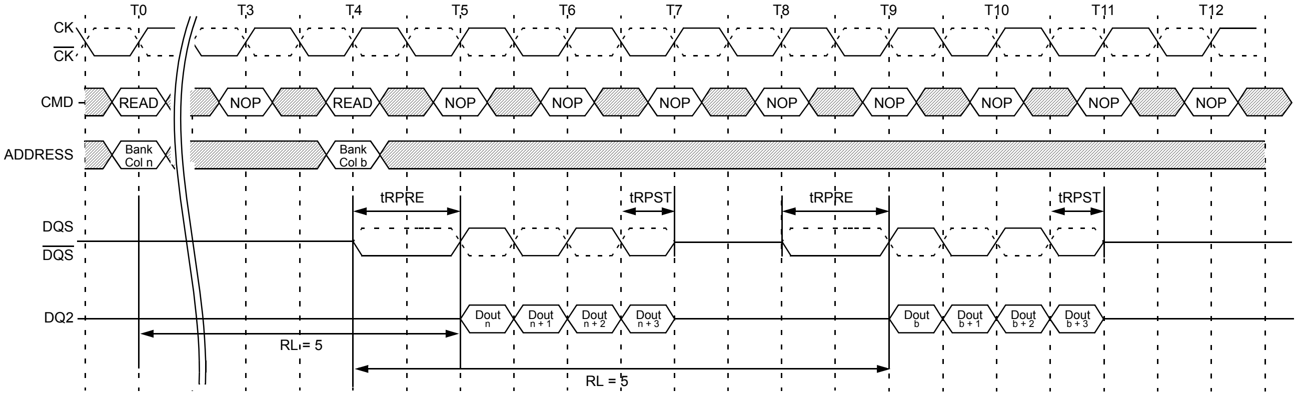
Figure 30 - Method for calculating tRPST transitions and endpoints

Figure 31 - READ (BL8) to READ (BL8)


T0
T3
T4
T5
T6
T7
T8
T9
T12
T13
T14
CK
CK
CMD
READ
NOP
READ
NOP
ADDRESS
Bank Col n
Bank Col b
tRPRE
tRPST
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout n + 4
Dout n + 5
Dout n + 6
Dout n + 7
Dout b
Dout b + 5
Dout b +6
Dout b + 7
RL = 5
RL = 5

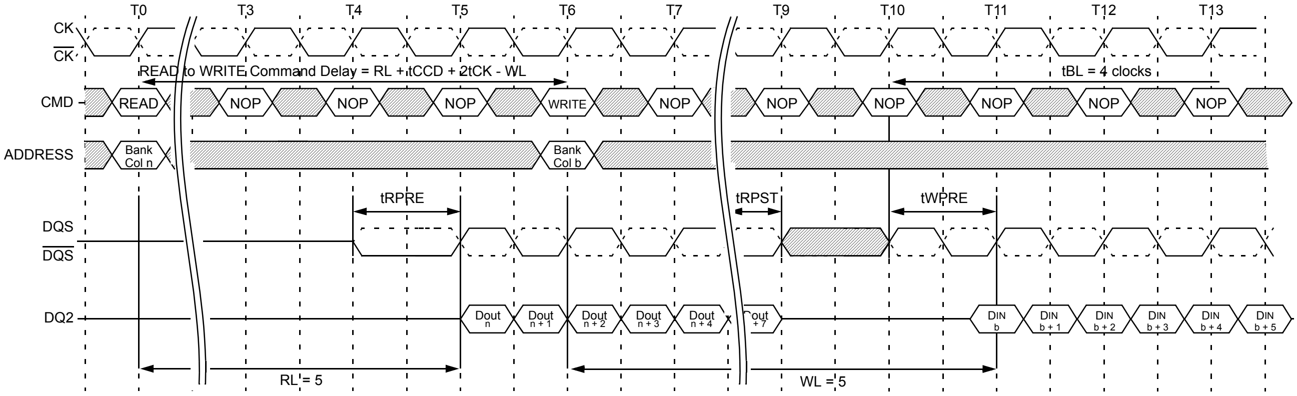
Notes :
1. BL8, RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01]and A12 = 1 during READ commands at T0 and T4.

Figure 32 - READ (BC4) to READ (BC4)


T0
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK
CK
CMD
READ
NOP
READ
NOP
ADDRESS
Bank Col n
Bank Col b
tRPRE
tRPST
tRPRE
tRPST
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout b
Dout b + 1
Dout b + 2
Dout b + 3
RL = 5
RL = 5

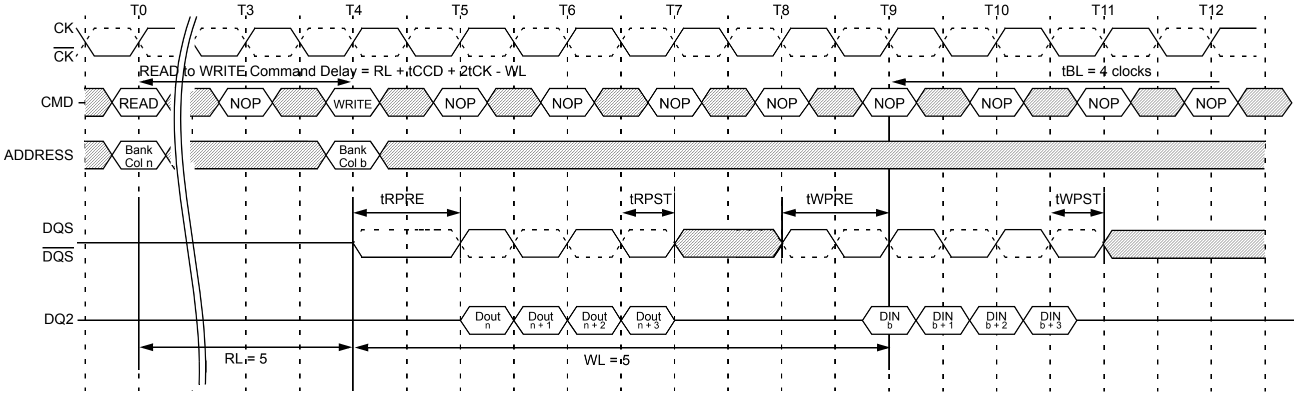
Notes :
1. BL4, RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01]and A12 = 0 during READ commands at T0 and T4.

Figure 33 - READ (BL8) to WRITE (BL8)


T0
T3
T4
T5
T6
T7
T9
T10
T11
T12
T13
CK
CK
READ to WRITE Command Delay = RL + tCCD + 2tCK - WL
tBL = 4 clocks
CMD
READ
NOP
WRITE
ADDRESS
Bank Col n
Bank Col b
tRPRE
tRPST
tWPRE
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout n + 4
Dout n + 7
DIN b
DIN b + 1
DIN b + 2
DIN b + 3
DIN b + 4
DIN b + 5
RL = 5
WL = 5

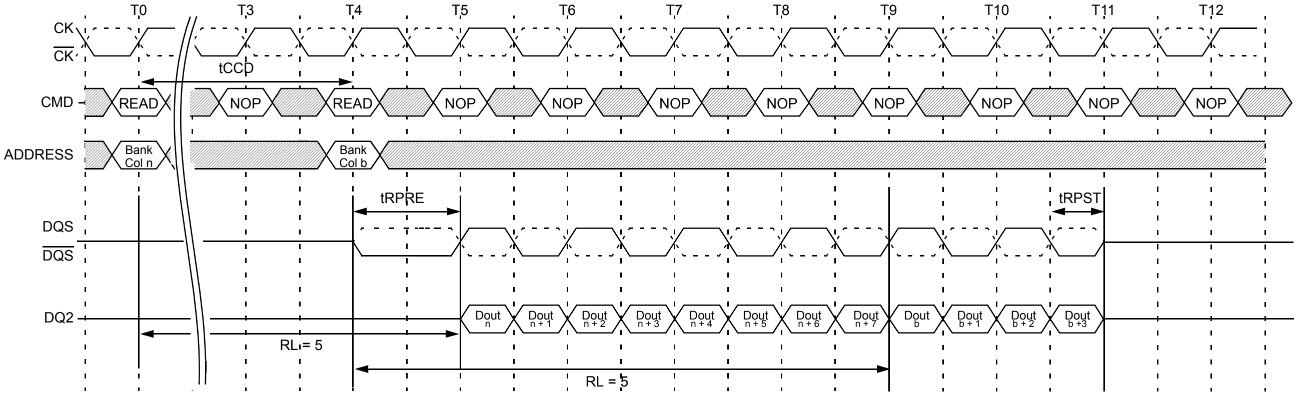
Notes :
1. BL8, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01]and A12 = 1 during READ commands at T0 and WRITE command at T6.

Figure 34 - READ (BC4) to WRITE (BC4) OTF


T0
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK
CK
READ to WRITE Command Delay = RL + tCCD + 2tCK - WL
tBL = 4 clocks
CMD
READ
NOP
WRITE
ADDRESS
Bank Col n
Bank Col b
tRPRE
tRPST
tWPRE
tWPST
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
DIN b
DIN b + 1
DIN b + 2
DIN b + 3
RL = 5
WL = 5

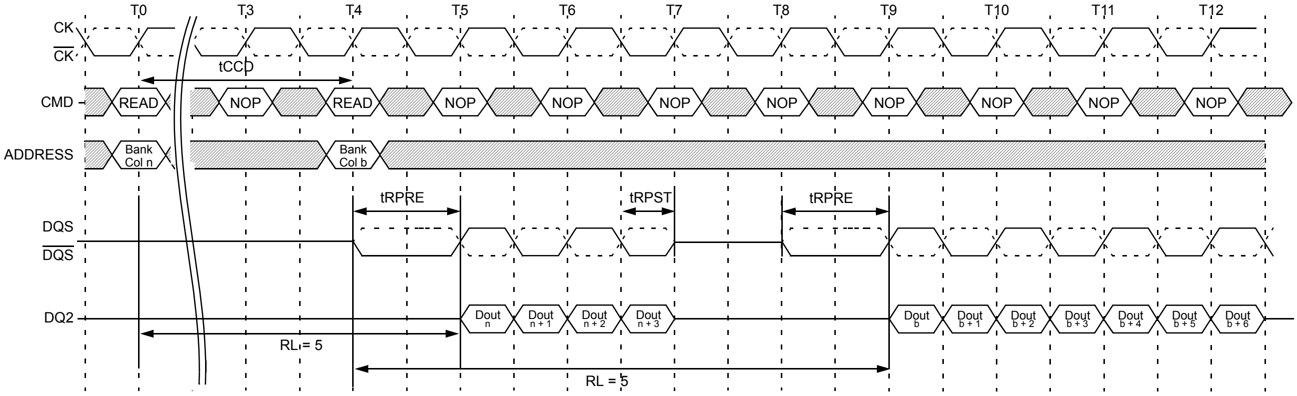
Notes :
1. BL4, RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL4 setting activated by either MR0[A1:0=00] or MR0[A1:0 = 01]and A12 = 1 during READ commands at T0 and WRITE command at T4.

Figure 35 - READ (BL8) to READ (BC4) OTF


T0
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK
CK
tCCD
CMD
READ
NOP
READ
NOP
ADDRESS
Bank Col n
Bank Col b
tRPRE
tRPST
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout n + 4
Dout n + 5
Dout n + 6
Dout n + 7
Dout b
Dout b + 1
Dout b + 2
Dout b +3
RL = 5
RL = 5

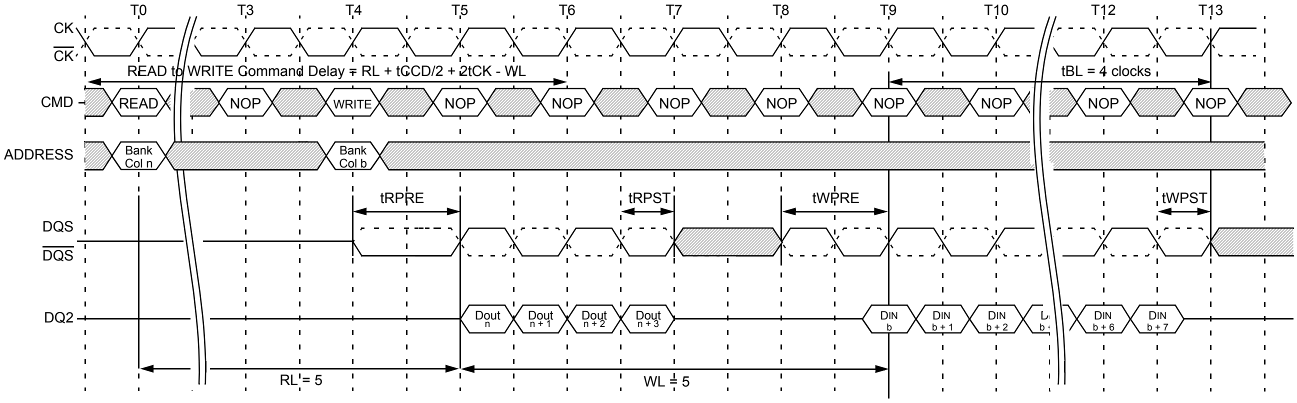
Notes :
1. RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
   BC4 setting activated by either MR0[A1:0=01] and A12 = 0 during READ commands at T4.

Figure 36 - READ (BC4) to READ (BL8) OTF


T0
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK
CK
tCCD
CMD
READ
NOP
READ
NOP
ADDRESS
Bank Col n
Bank Col b
tRPRE
tRPST
tRPRE
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout b
Dout b + 1
Dout b + 2
Dout b + 3
Dout b + 4
Dout b + 5
Dout b + 6
RL = 5
RL = 5

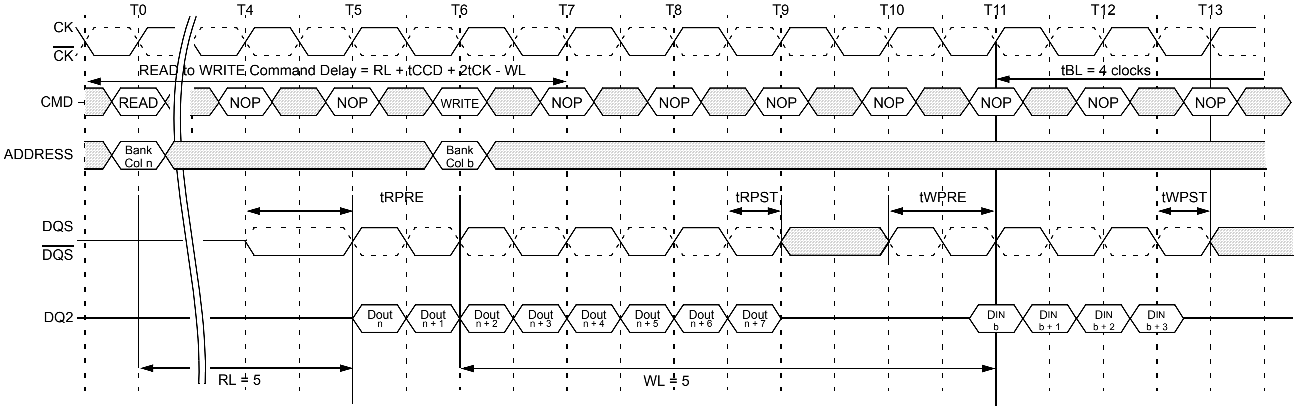
Notes :
1. RL = 5 (CL = 5, AL = 0)
2. Dout n (or b) = data-out from column n (or column b).
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
   BL8 setting activated by either MR0[A1:0=01] and A12 = 0 during READ commands at T4.

Figure 37 - READ (BC4) to WRITE (BL8) OTF


T0
T3
T4
T5
T6
T7
T8
T9
T10
T12
T13
CK
CK
READ to WRITE Command Delay = RL + tCCD/2 + 2tCK - WL
tBL = 4 clocks
CMD
READ
NOP
WRITE
NOP
ADDRESS
Bank Col n
Bank Col b
tRPRE
tRPST
tWPRE
tWPST
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
DIN b
DIN b + 1
DIN b + 2
DIN b + 6
DIN b + 7
RL = 5
WL = 5

Notes :
1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL -1, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:0=00] and A12 = 0 during READ commands at T0.
BL8 setting activated by either MR0[A1:0=01] and A12 = 1 during WRITE commands at T4.

Figure 38 - READ (BL8) to WRITE (BC4)


T0
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
CK
CK
READ to WRITE Command Delay = RL + tCCD + 2tCK - WL
tBL = 4 clocks
CMD
READ
NOP
WRITE
ADDRESS
Bank Col n
Bank Col b
tRPRE
tRPST
tWPRE
tWPST
DQS
DQS
DQ2
Dout n
Dout n + 1
Dout n + 2
Dout n + 3
Dout n + 4
Dout n + 5
Dout n + 6
Dout n + 7
DIN b
DIN b + 1
DIN b + 2
DIN b + 3
RL = 5
WL = 5

Notes :
1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL = 0)
2. Dout n = data-out from column, DIN b = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] and A12 = 1 during READ commands at T0.
BC4 setting activated by either MR0[A1:0=01] and A12 = 0 during WRITE commands at T6.

16.14 WRITE Operation

16.14.1 gDDR3 Burst Operation

During a READ or WRITE command, gDDR3 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).
A12 = 0, BC4 (BC4 = burst chop, tCCD = 4)
A12 = 1, BL8
A12 is used only for burst length control, not as a column address.

16.14.2 WRITE Timing Violations

16.14.2.1 Motivation

Generally, if timing parameters are violated, a complete reset/initialization procedure has to be initiated to make sure the DRAM works properly. However, it is desireable for certain minor violations that the DRAM is guaranteed not to "hang up" and errors be limited to that particular operation. (for reference: add more motivation here later, or refer to the "Read Synchronization" section if availible) For the following, it will be assumed that there are no timing violations w.r.t. to the Write command itself (including ODT, etc.) and that it does satisfy all timing requirements not mentioned below.

16.14.2.2 Data Setup and Hold Violations

Should the data to strobe timing requirements (tDS, tDH) be violated, for any of the strobe edges associated with a write burst, then wrong data might be written to the memory location addressed with this WRITE command. In the example (Figure 39), the relevant strobe edges for write burst A are associated with the clock edges: T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5.Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.

16.14.2.3 Strobe to Strobe and Strobe to Clock Violations

Should the strobe timing requirements (tDQSH, tDQSL, tWPRE, tWPST) or the strobe to clock timing requirements (tDSS, tDSH, tDQSS) be violated, for any of the strobe edges associated with a Write burst, then wrong data might be written to the memory location addressed with the offending WRITE command. Subsequent reads from that location might result in unpredictable read data, however the DRAM will work properly otherwise.
In the example (Figure 39) the relevant strobe edges for Write burst A are associated with the clock edges: T4, T4.5, T5, T5.5, T6, T6.5, T7, T7.5, T8, T8.5 and T9. Any timing requirements starting or ending on one of these strobe edges need to be fullfilled for a valid burst.
For Write burst B the relevant edges are T8, T8.5, T9, T9.5, T10, T10.5, T11, T11.5, T12, T12.5 and T13. Some edges are associated with both bursts.

16.14.2.4 Write Timing Parameters

This drawing is for example only to enumerate the strobe edges that "belong" to a Write burst. No actual timing violations are shown here. For a valid burst all timing parameters for each edge of a burst need to be satisfied (not only for one edge - as shown).

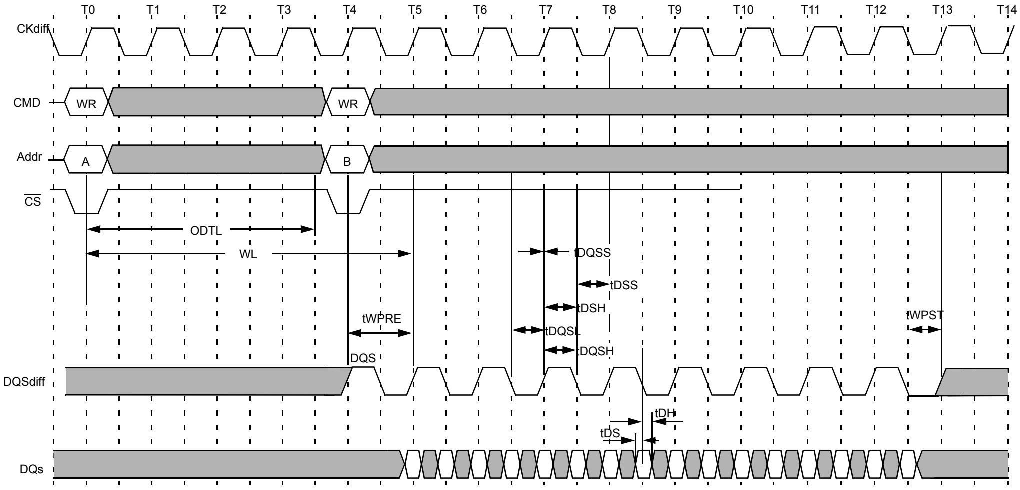
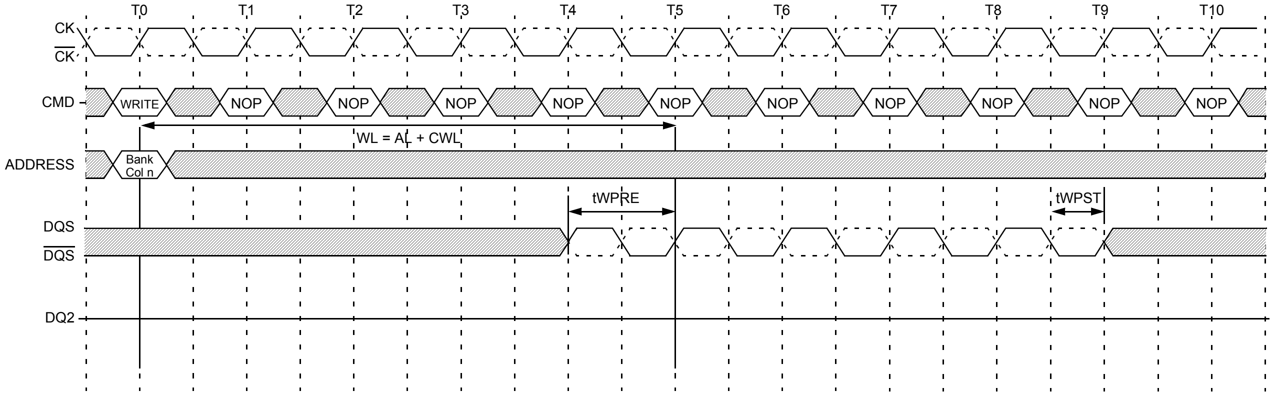


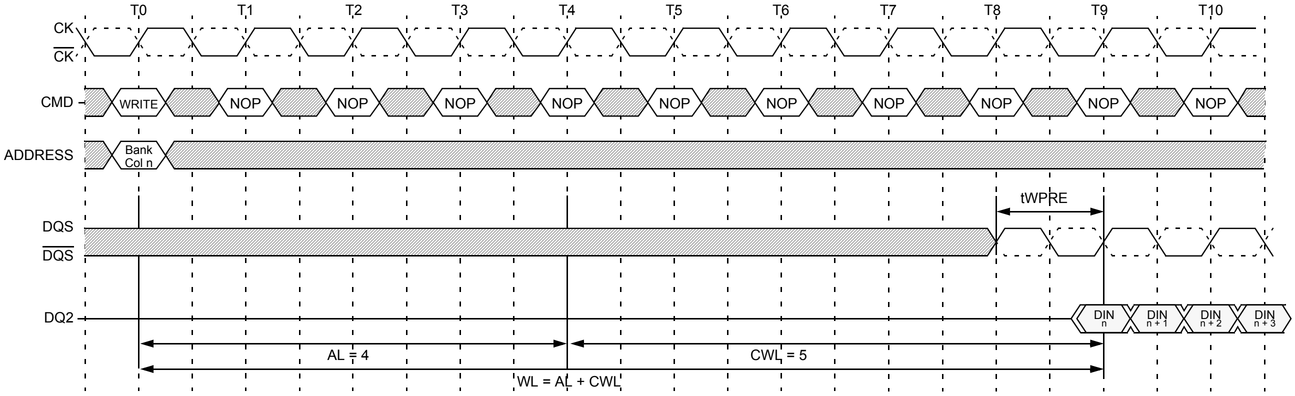
Figure 39 - Write Timing Parameters

Figure 40 - WRITE Burst Operation WL = 5 (AL = 0, CWL = 5, BL8)


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CK
CK
CMD
WRITE
NOP
WL = AL + CWL
ADDRESS
Bank
Col n
tWPRE
tWPST
DQS
DQS
DQ2

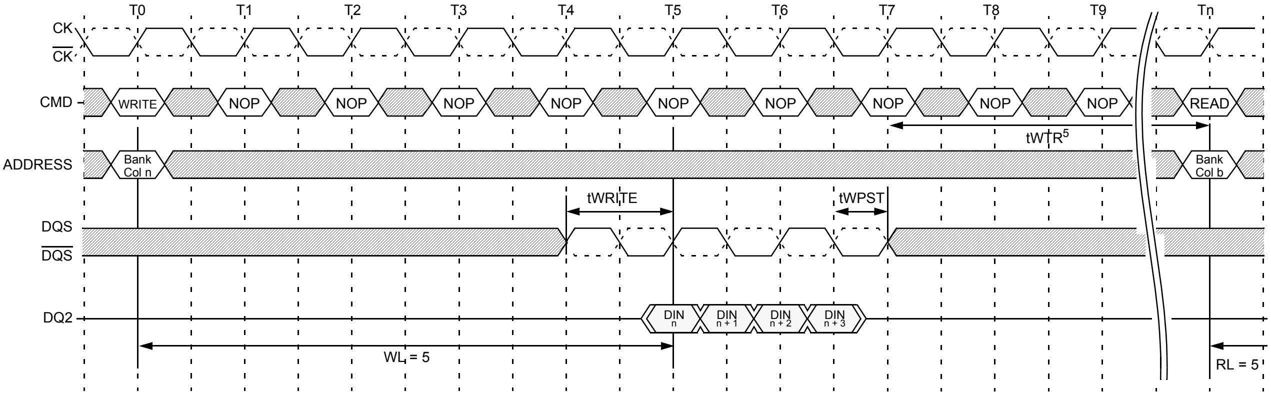
Notes :
1. BL8, WL = 5, AL = 0, CWL = 5
2. DIN n = data-in from column n.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0.

Figure 41 - WRITE Burst Operation WL = 9 (AL = CL-1, CWL = 5, BL8)


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CK
CK
CMD
WRITE
NOP
ADDRESS
Bank
Col n
tWPRE
DQS
DQS
DQ2
DIN n
DIN n + 1
DIN n + 2
DIN n + 3
AL = 4
CWL = 5
WL = AL + CWL

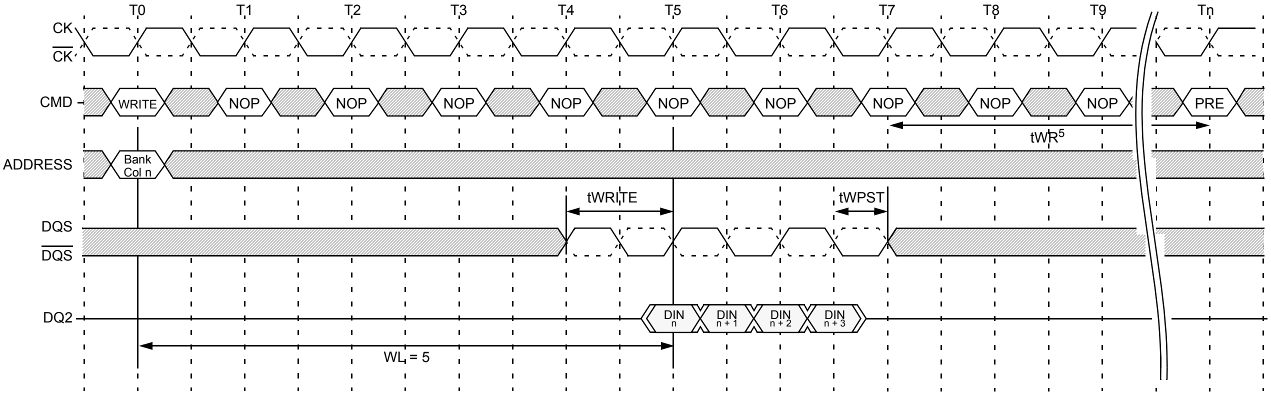
Notes :
1. BL8, WL = 9, AL = (CL - 1), CL = 5, CWL = 5
2. DIN n = data-in from column n.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0.

Figure 42 - WRITE (BC4) to READ (BC4) Operation


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
Tn
CK
CK
CMD
WRITE
NOP
READ
tWTR5
ADDRESS
Bank Col n
Bank Col b
tWRITE
tWPST
DQS
DQS
DQ2
DIN n
DIN n+1
DIN n+2
DIN n+3
WL = 5
RL = 5

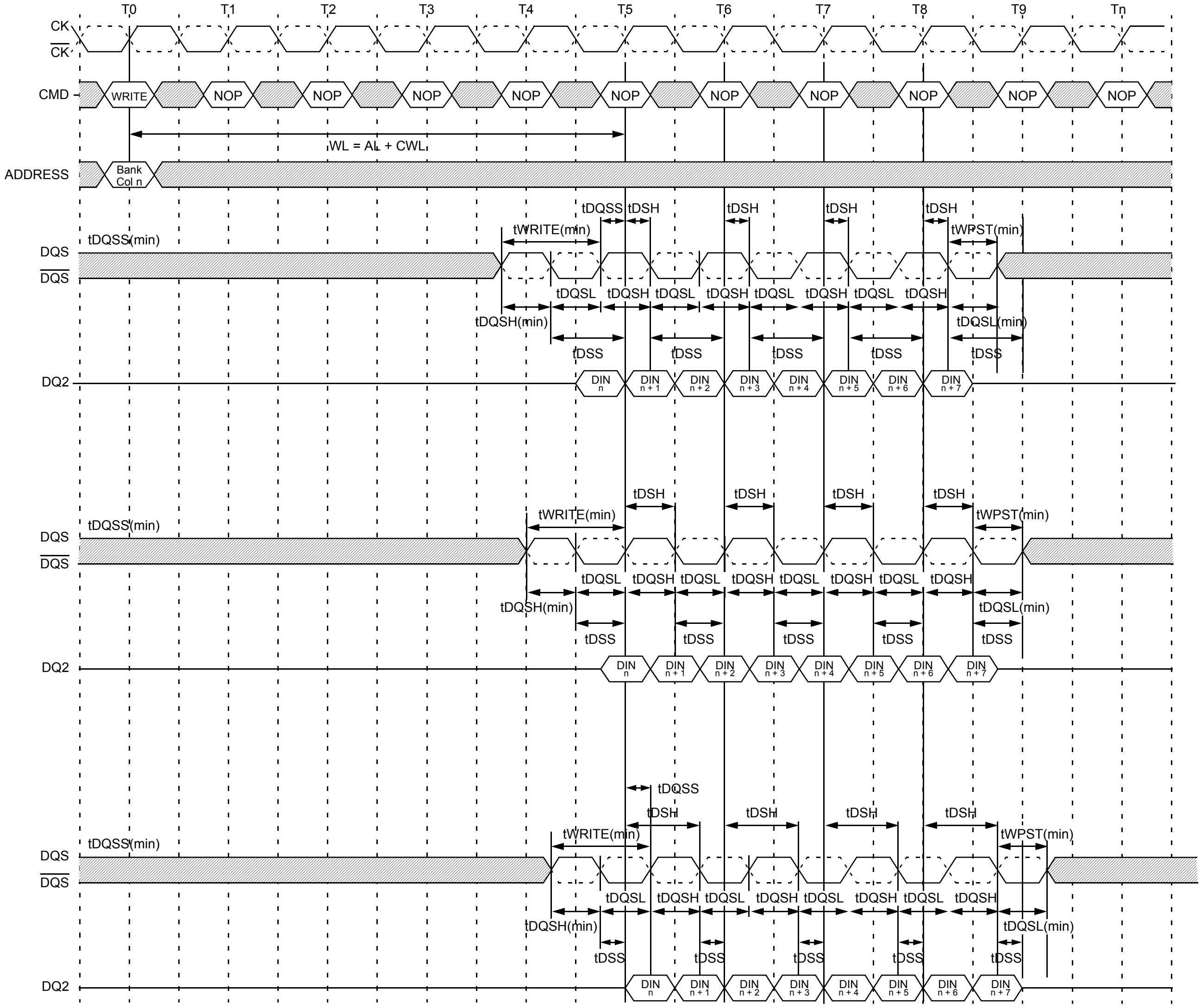
Notes :
1. BC4, WL = 5, RL = 0
2. DIN n = data-in from column n ; Dout b = data-out from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0=10] during WRITE commands at T0 and READ command at Tn.
5. tWTR controls the write to read delay to the same device and starts with the first rising clcok edge after the last write data shown at T7.

Figure 43 - WRITE (BC4) to PRECHARGE Operation


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
Tn
CK
CK
CMD
WRITE
NOP
PRE
tWR5
ADDRESS
Bank Col n
tWRITE
tWPST
DQS
DQS
DQ2
DIN n
DIN n+1
DIN n+2
DIN n+3
WL = 5

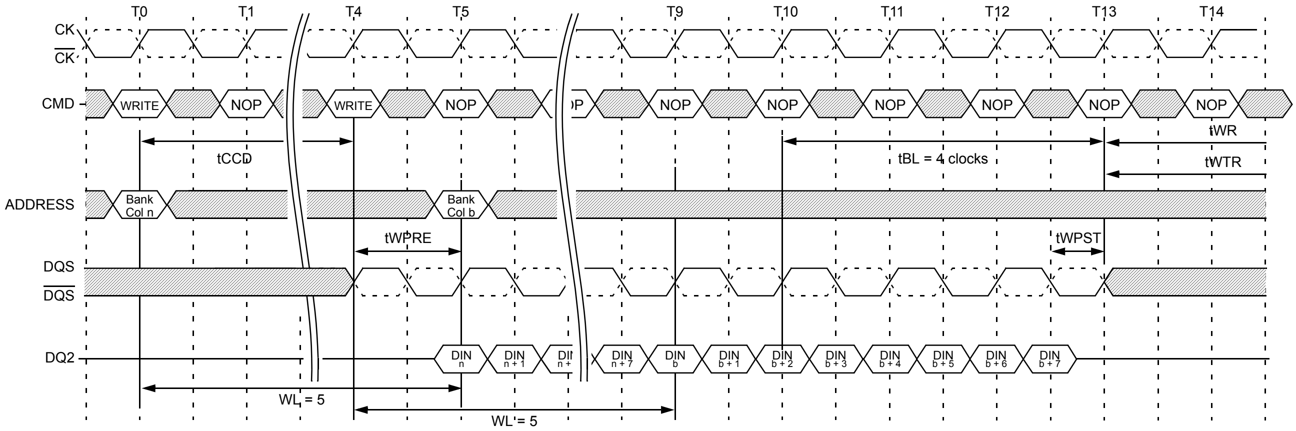
Notes :
1. BC4, WL = 5, RL = 5.
2. DIN n = data-in from column n; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 10] during WRITE command at T0.
5. The write recovery time (tWR) referenced from the first rising clock edge after the last write data shown at T7.
tWR specifies the last burst write cycle until the precharge command can be issued to the same bank .

Figure 44 - DDR3 Write Timing Definition


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
Tn
CK
CK
CMD
WRITE
NOP
WL = AL + CWL
ADDRESS
Bank Col n
DQS
DQS
DQ2
tDQSS(min)
tDQSS
tDSH
tWRITE(min)
tWPST(min)
tDQSL
tDQSH
tDQSH(min)
tDQSL(min)
tDSS
DIN n
DIN n + 1
DIN n + 2
DIN n + 3
DIN n + 4
DIN n + 5
DIN n + 6
DIN n + 7

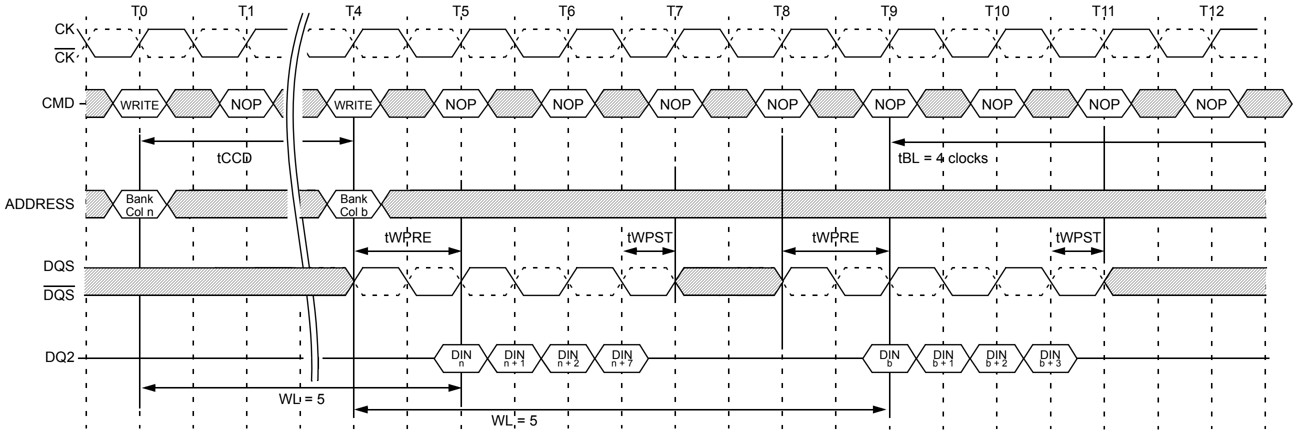
Notes :
1. BL8, WL = 5 (AL = 0, CWL = 5)
2. DIN n = data-in from column n
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0=10] or MR0[A1:0 = 01] and A12 = 1 during WRITE commands at T0.
5. tDQSS must be met at each rising clock edge.

Figure 45 - WRITE (BL8) to WRITE (BL8)


T0
T1
T4
T5
T9
T10
T11
T12
T13
T14
CK
CK
CMD
WRITE
NOP
tCCD
tBL = 4 clocks
tWR
tWTR
ADDRESS
Bank Col n
Bank Col b
tWPRE
tWPST
DQS
DQS
DQ2
DIN n
DIN n+1
DIN n+7
DIN b
DIN b+1
DIN b+2
DIN b+3
DIN b+4
DIN b+5
DIN b+6
DIN b+7
WL = 5
WL = 5

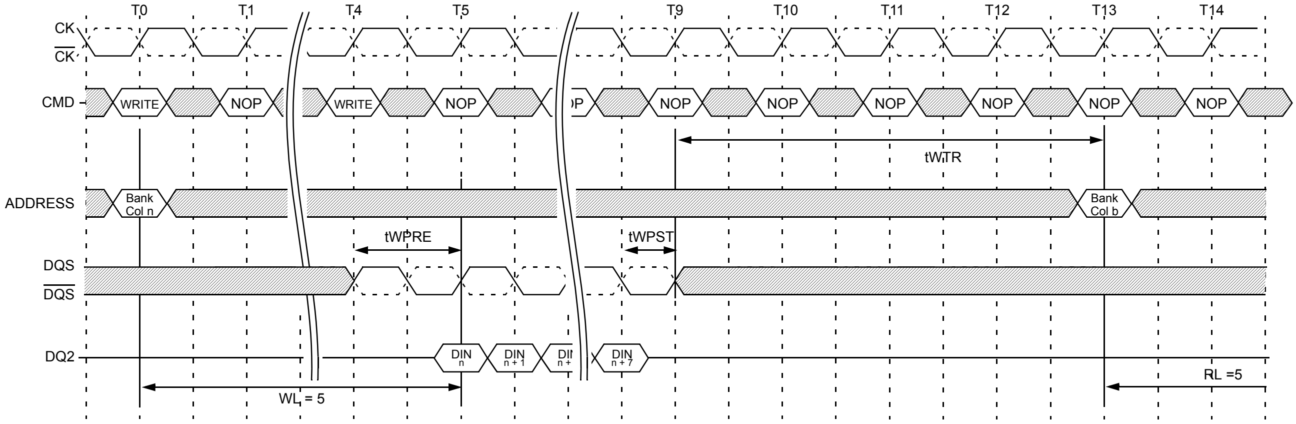
Notes :
1. BL8, WL = 5(CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n (or column b.)
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0 and T4

Figure 46 - WRITE (BC4) to WRITE (BC4) OTF


T0
T1
T4
T5
T6
T7
T8
T9
T10
T11
T12
CK
CK
CMD
WRITE
NOP
tCCD
tBL = 4 clocks
ADDRESS
Bank Col n
Bank Col b
tWPRE
tWPST
DQS
DQS
DQ2
DIN n
DIN n+1
DIN n+2
DIN n+3
DIN b
DIN b+1
DIN b+2
DIN b+3
WL = 5
WL = 5

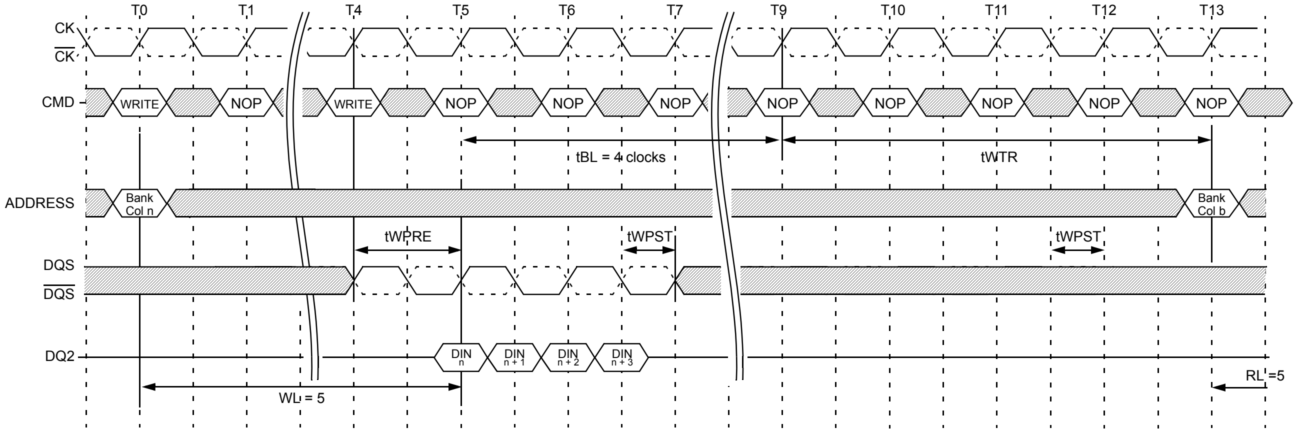
Notes :
1. BC4, WL = 5(CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n (or column b.)
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0=01] and A12 = 0 during WRITE commands at T0 and T4

Figure 47 - WRITE (BL8) to READ (BC4/BL8) OTF


T0
T1
T4
T5
T9
T10
T11
T12
T13
T14
CK
CK
CMD
WRITE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
NOP
tWTR
ADDRESS
Bank Col n
Bank Col b
tWPRE
tWPST
DQS
DQS
DQ2
DIN n
DIN n + 1
DIN n + 7
RL =5
WL = 5

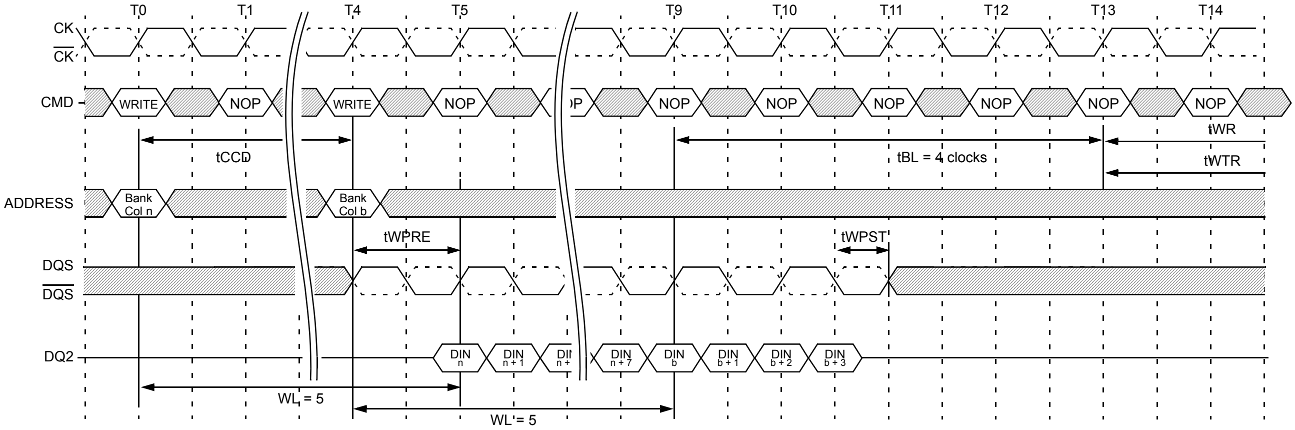
Notes :
1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL = 5, AL =0)
2. DIN n = data-in from column n Dout = data-in from column b.
3. NOP commands are shown for ease of illustration ; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0=00] or MR0[A1:0=01] and A12 = 1 during WRITE commands at T0.
READ command at T11 can be either BC4 or BL8 depending on MR0[A1 : 0] and A12 status at T13.

Figure 48 - WRITE (BC4) to READ (BC4/BL8) OTF


T0
T1
T4
T5
T6
T7
T9
T10
T11
T12
T13
CK
CK
CMD
WRITE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
tBL = 4 clocks
tWTR
ADDRESS
Bank Col n
Bank Col b
tWPRE
tWPST
tWPST
DQS
DQS
DQ2
DIN n
DIN n + 1
DIN n + 2
DIN n + 3
RL =5
WL = 5

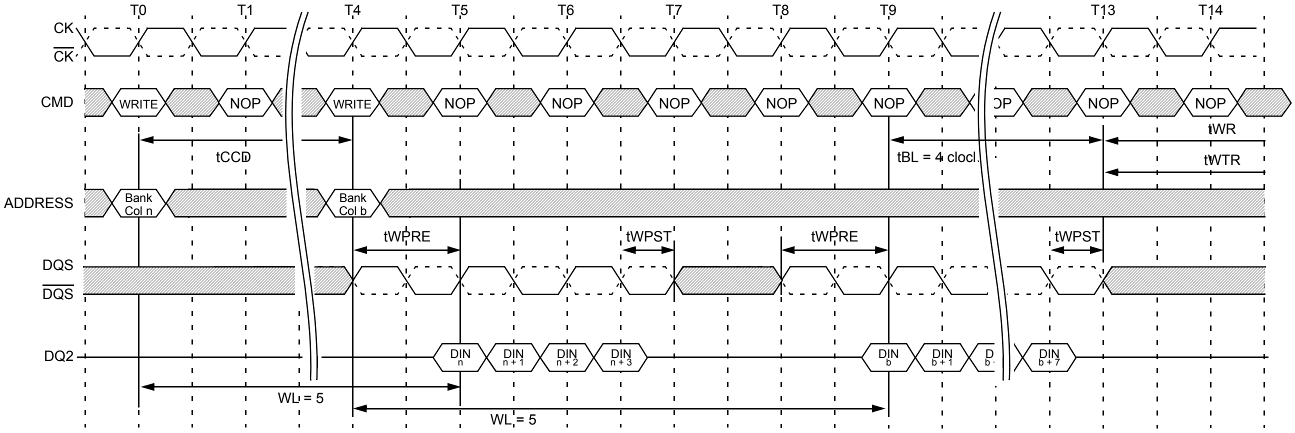
Notes :
1. RL = 5 (CL = 5, AL = 0), WL = 5 (CWL =5, AL = 0)
2. DIN n = data-in from column n; DOUT b = data-out from column b.
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
READ command at T11 can be either BC4 or BL8 depending on A12 status at T13.

Figure 49 - WRITE (BL8) to WRITE (BC4) OTF


T0
T1
T4
T5
T9
T10
T11
T12
T13
T14
CK
CK
CMD
WRITE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
NOP
tCCD
tBL = 4 clocks
tWR
tWTR
ADDRESS
Bank Col n
Bank Col b
tWPRE
tWPST
DQS
DQS
DQ2
DIN n
DIN n + 1
DIN n + 7
DIN b
DIN b + 1
DIN b + 2
DIN b + 3
WL = 5
WL = 5

Notes :
1. WL = 5 (CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0.
BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T4.

Figure 50 - WRITE (BC4) to WRITE (BL8) OTF


T0
T1
T4
T5
T6
T7
T8
T9
T13
T14
CK
CK
CMD
WRITE
NOP
WRITE
NOP
NOP
NOP
NOP
NOP
NOP
NOP
tCCD
tBL = 4 clocks
tWR
tWTR
ADDRESS
Bank Col n
Bank Col b
tWPRE
tWPST
tWPRE
tWPST
DQS
DQS
DQ2
DIN n
DIN n + 1
DIN n + 2
DIN n + 3
DIN b
DIN b + 1
DIN b + 7
WL = 5
WL = 5

Notes :
1. WL = 5 (CWL = 5, AL = 0)
2. DIN n (or b) = data-in from column n (or column b).
3. NOP commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during WRITE command at T0.
BL8 setting activated by MR0[A1:0 = 01] and A12 = 1 during WRITE command at T4.

16.15 Refresh Command

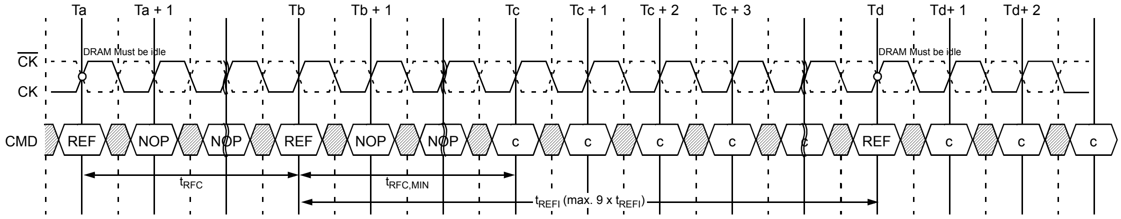
The Refresh command (REF) is used during normal operation of the gDDR3 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required.

The gDDR3 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When $\overline{CS}$, $\overline{RAS}$ and $\overline{CAS}$ are held Low and $\overline{WE}$ High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don’t Care" during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started.

When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except NOP or DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min). Note that the tRFC timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR3 SDRAM regularly every tREFI interval. To allow for improved efficeincy in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of 8 Refresh commands can be postponed during operation of the gDDR3 SDRAM, meaning that at no point in time more than a total of 8 Refresh commands are allowed to be postponed. In case that 8 Refresh commands are postponeds is limited to 9 x tREFI (see Figure 51). A maximum of 8 additional Refresh commands can be issud in advance ("pulled in"), with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8 Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 x tREFI(see Figure 52). Before entering Self-Refresh Mode, all postponed Refresh commands must be excuted.

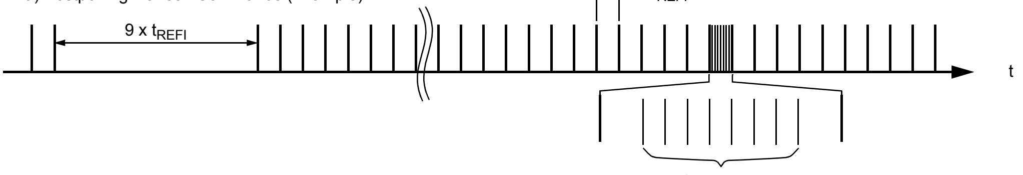


c : NOP,DES or other valid Command
NOP : NOP or DES Command

Figure 51 - Refresh Command Example

Note :
1. Only NOP/DES commands allowed after Refresh command registered until tRFC.Min expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 x tREFI

a) Postponing Refresh Commands (Example)



b) Pulling-in Refresh Commands (Example)

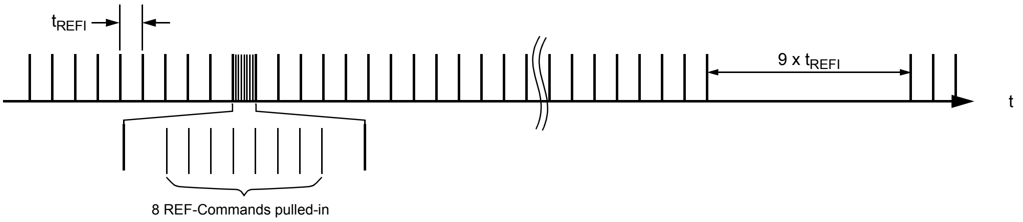


Figure 52 - Examples for Postponing (a) and Pulling-in (b) Refresh-Commands

16.16 Self-Refresh Operation

The Self-Refresh command can be used to retain data in the DDR3 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the gDDR3 SDRAM retains data without external clocking. The gDDR3 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and CKE held low with $\overline{WE}$ high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the gDDR3 SDRAM must be idle with all bank precharge state with tRP satisfied. Also, on-die termination must be turned off before issuing Self-Refresh-Entry command, by either registering ODT pin low "ODTL + 0.5tCK" prior to the Self-Refresh Entry command or using MRS to MR1 command. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. During normal operation (DLL on), MR1(A0 = 0), the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the gDDR3 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and $\overline{RESET}$, are "don't care". For proper Self-Refresh operation, all power supply and reference pins (V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ}, VRefCA and VRefDQ) must be at valid levels. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the gDDR3 SDRAM must remain in Self-Refresh mode is tCKE. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and either NOP or Deselect on command bus) is registered, a delay of at least tXS must be satisfied before a valid command not requiring a locked DLL can be issued to the device to allow for any internal refresh in progress. Before a command which requires a locked DLL can be applied, a delay of at least tXSDLL and applicable ZQCAL function requirements (TBD) must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the gDDR3 SDRAM can be put back into Self-Refresh mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). NOP or deselct commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. ODT must be turned off during tXSDLL.

The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the gDDR3 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

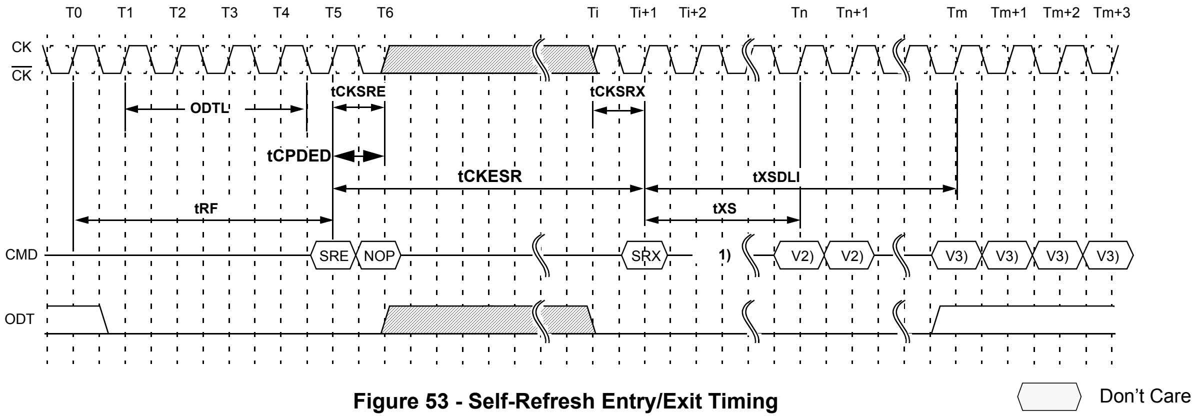


Figure 53 - Self-Refresh Entry/Exit Timing

Note :
1. Only NOP or DES commands
2. Valid commands not requiring a locked DLL
3. Valid commands requiring a locked DLL

16.17 Power-Down Modes

16.17.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with NOP or Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figures 52 through Figures 65 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK, $\overline{CK}$, ODT, CKE and $\overline{RESET}$. To protect DRAM internal delay on CKE line to block the input signals, multiple NOP or Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

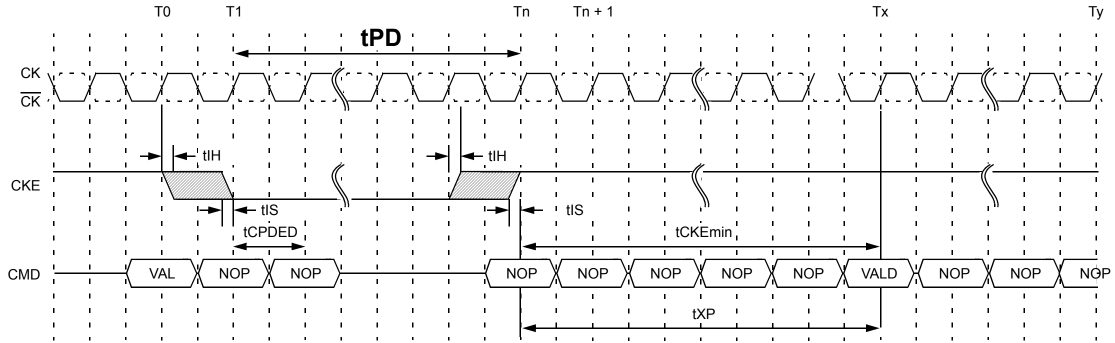
Table 15 - Power-Down Entry Definitions

Status of DRAM	MRS bit A12	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	Don't Care	On	Fastd	**tXP** to any valid comman
Pre Charged (All banks Precharged)	0	Off	Slow	**tXP** to any valid command. Since it is in precharge state, commands here will be ACT, AR, MRS/EMRS, PR or PRA **tXPDLL** to commands who need DLL to operate, such as RD, RDA or ODT control line.
Pre Charged (All Banks Precharged)	1	On	Fast	**tXP** to any valid command

Also, the DLL is disabled upon entering precharge power-down (Slow Exit Mode), but the DLL is kept enabled during precharge power-down (Fast Exit Mode) or active power-down. In power-down mode, CKE low, $\overline{RESET}$ high and a stable clock signal must be maintained at the inputs of the DDR3 SDRAM, and ODT should be in a valid state but all other input signals are "Don't Care" (If $\overline{RESET}$ goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

The power-down state is synchronously exited when CKE is registered high (along with a NOP or Deselect command).
CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP and/or tXPDLL after CKE goes high. Power-down exit latency is defined at AC spec table of component data sheet.

Active Power Down Entry and Exit timing diagram example is shown below. Note, all existing Power Down "entry to exit" timing diagrams using tCKE will be updated to tPD and use the values listed in the above table (including Precharge Power Down drawings). Note, this does not affect the "exit to entry/ re-entry" condition which still uses tCKE (shown between states Tn and Tx).



Note :
1. VAL command at T0 is ACT, NOP, DES or Precharge with still one bank remaining open after completion of precharge command.

Figure 54 − Active Power-Down Entry and Exit Timing Diagram

16.17.2 Timing Diagrams for CKE with PD Entry, PD Exit with Read, READ with Auto Precharge, Write and Write with Auto Precharge, Activate, Precharge, Refresh, MRS:

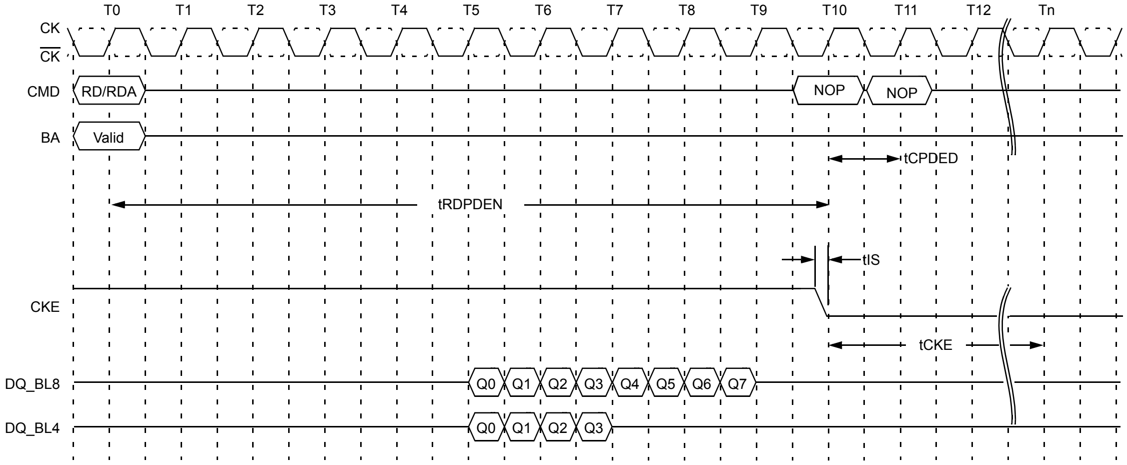

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
Tn
CK
CK
CMD
RD/RDA
NOP
NOP
BA
Valid
tCPDED
tRDPDEN
tIS
CKE
tCKE
DQ_BL8
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
DQ_BL4
Q0
Q1
Q2
Q3

Figure 55 − Power-Down Entry after Read and Read with Auto Precharge

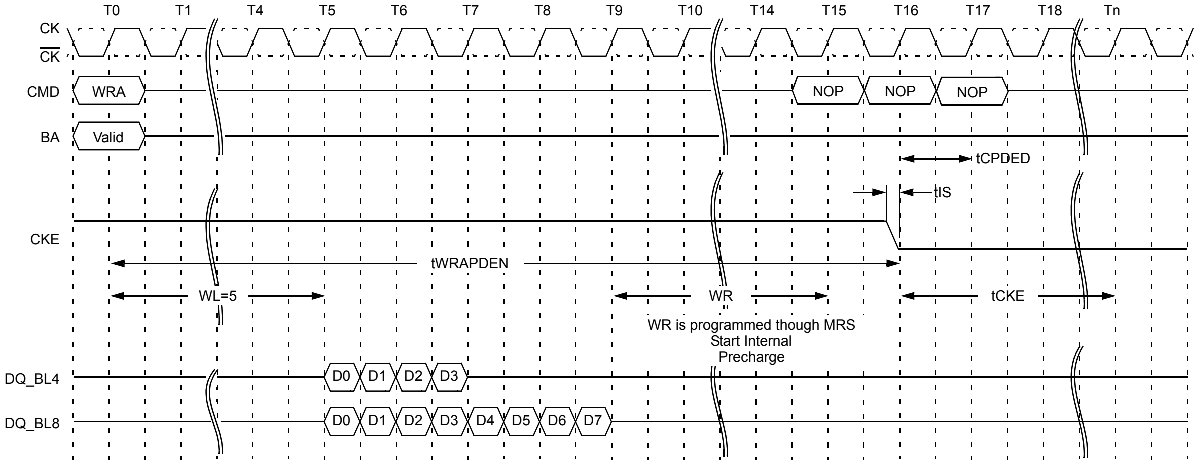

T0
T1
T4
T5
T6
T7
T8
T9
T10
T14
T15
T16
T17
T18
Tn
CK
CK
CMD
WRA
NOP
NOP
NOP
BA
Valid
tCPDED
tIS
CKE
tWRAPDEN
WL=5
WR
tCKE
WR is programmed though MRS
Start Internal
Precharge
DQ_BL4
D0
D1
D2
D3
DQ_BL8
D0
D1
D2
D3
D4
D5
D6
D7

Figure 56 − Power-Down Entry After Write with Auto Precharge

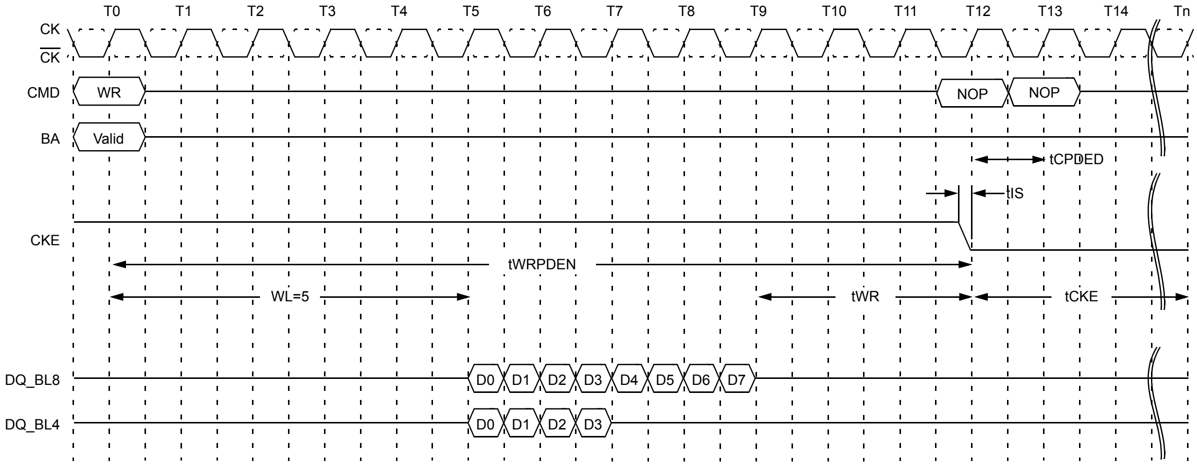
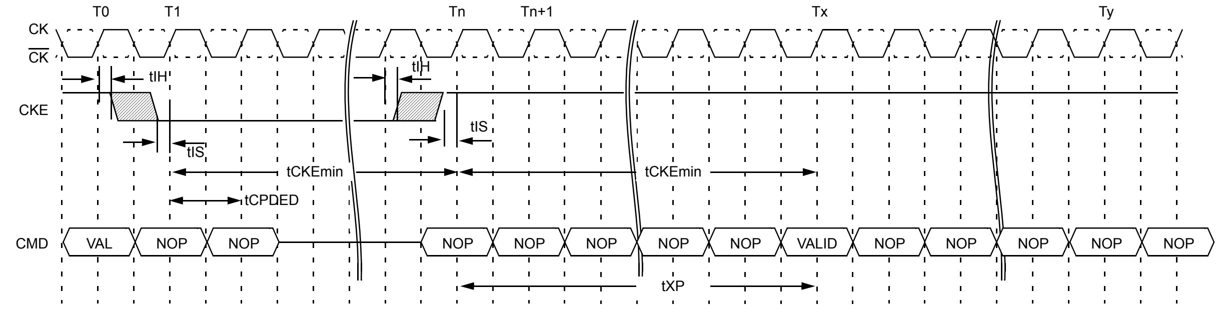

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
Tn
CK
CK
CMD
WR
NOP
NOP
BA
Valid
tCPDED
tIS
CKE
tWRPDEN
WL=5
tWR
tCKE
DQ_BL8
D0
D1
D2
D3
D4
D5
D6
D7
DQ_BL4
D0
D1
D2
D3

Figure 57 – Power-Down Entry after Write


T0
T1
Tn
Tn+1
Tx
Ty
CK
CK
tIH
tIH
CKE
tIS
tIS
tCKEmin
tCKEmin
tCPDED
CMD
VAL
NOP
NOP
NOP
NOP
NOP
NOP
NOP
VALID
NOP
NOP
NOP
NOP
NOP
tXP

Note : VAL command at T0 is ACT, NOP, DES or Precharge with still one bank remaining open

Figure 58 – Active Power-Down Entry and Exit Timing Diagram

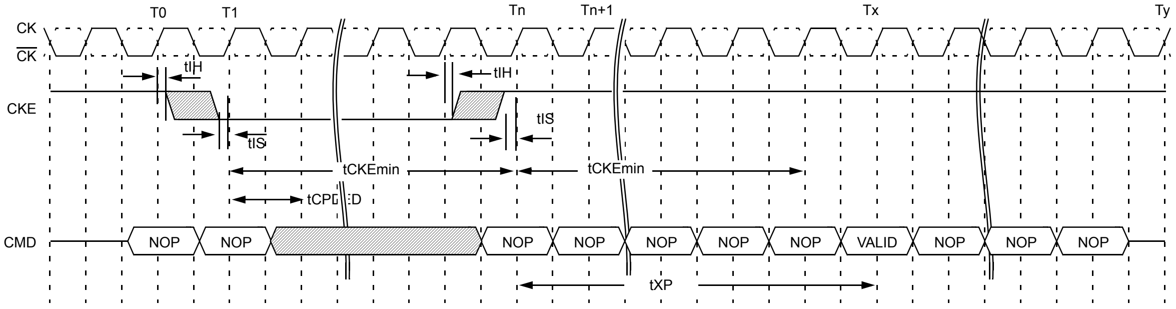

T0
T1
Tn
Tn+1
Tx
Ty
CK
CK
CKE
tIH
tIH
tIS
tIS
tCKEmin
tCKEmin
tCPDED
CMD
NOP
NOP
NOP
NOP
NOP
NOP
NOP
VALID
NOP
NOP
NOP
tXP

Figure 59 – Precharge Power-Down (Fast Exit Mode) Entry and Exit

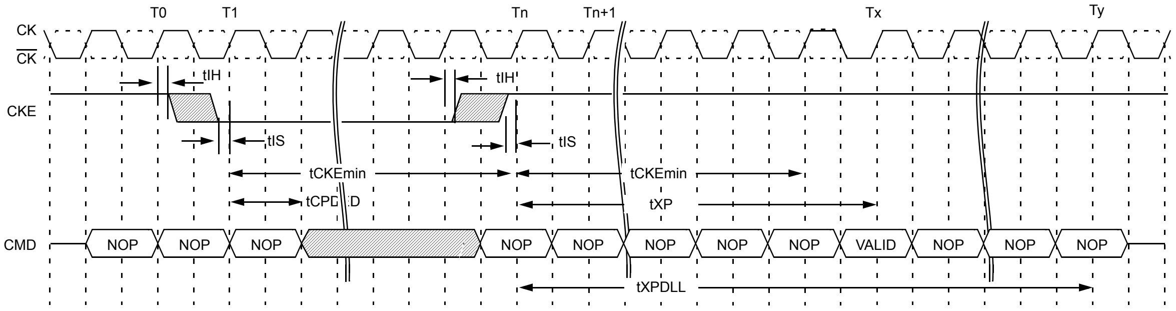

T0
T1
Tn
Tn+1
Tx
Ty
CK
CK
CKE
tIH
tIH
tIS
tIS
tCKEmin
tCKEmin
tCPDED
tXP
CMD
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
VALID
NOP
NOP
NOP
tXPDLL

Figure 60 – Precharge Power-Down (Slow Exit Mode) Entry and Exit

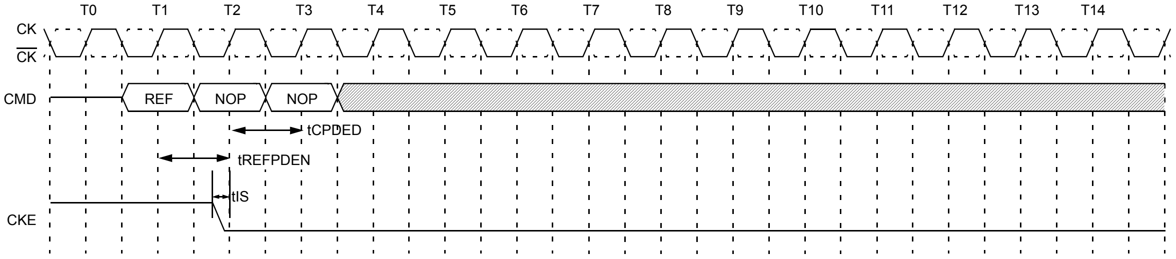

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
CK
CK
CMD
REF
NOP
NOP
tCPDED
tREFPDEN
tIS
CKE

Figure 61 – Refresh Command to Power-Down Entry

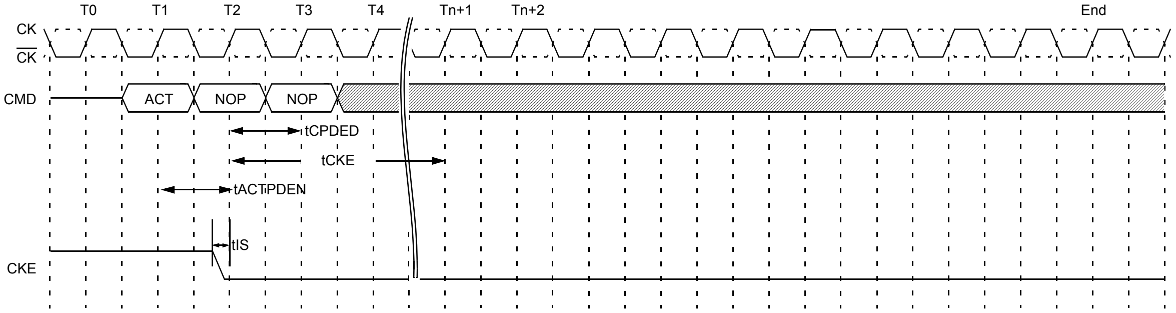

T0
T1
T2
T3
T4
Tn+1
Tn+2
End
CK
CK
CMD
ACT
NOP
NOP
tCPDED
tCKE
tACTPDEN
tIS
CKE

Figure 62 – Active Command to Power-Down Entry

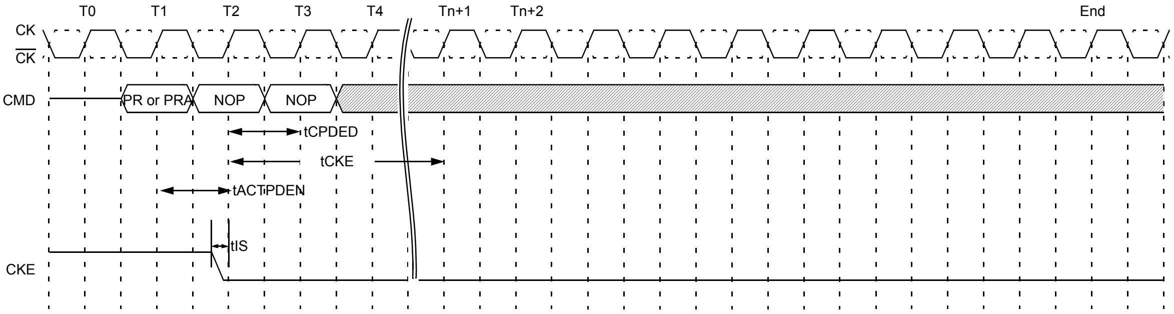

T0
T1
T2
T3
T4
Tn+1
Tn+2
End
CK
CK
CMD
PR or PRA
NOP
NOP
tCPDED
tCKE
tACTPDEN
tIS
CKE

Figure 63 – Precharge/Precharge all Command to Power-Down Entry

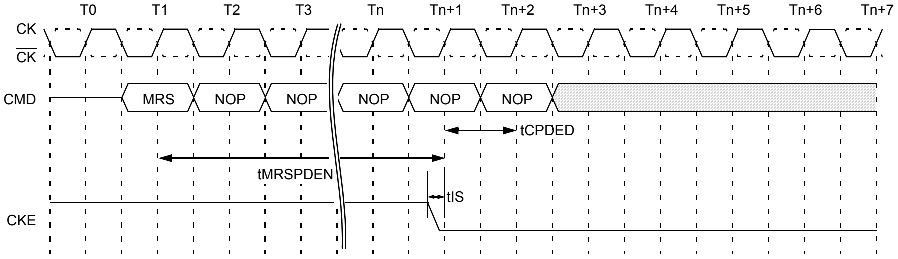
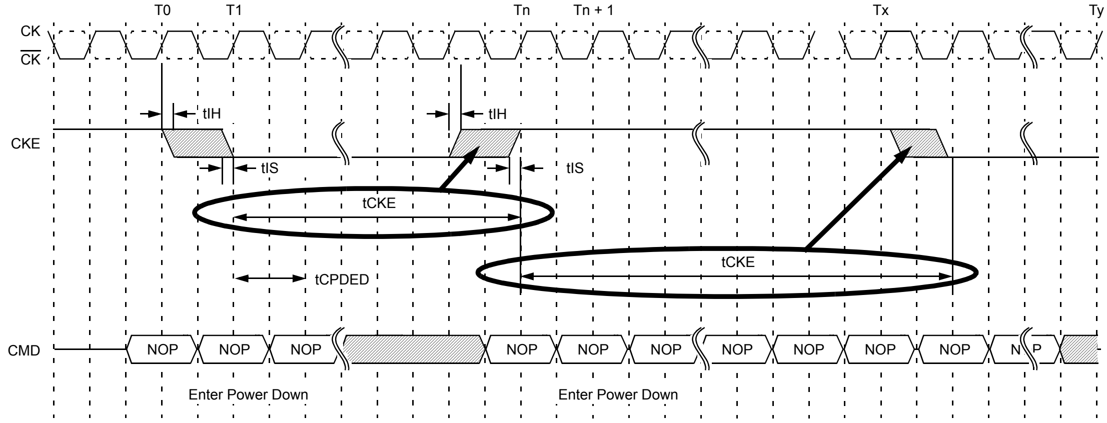

T0
T1
T2
T3
Tn
Tn+1
Tn+2
Tn+3
Tn+4
Tn+5
Tn+6
Tn+7
CK
CK
CMD
MRS
NOP
NOP
NOP
NOP
NOP
tCPDED
tMRSPDEN
tIS
CKE

Figure 64 - MRS Command to Power-Down Entry

Table 16 – Timing Values tXXXPDEN Parameters

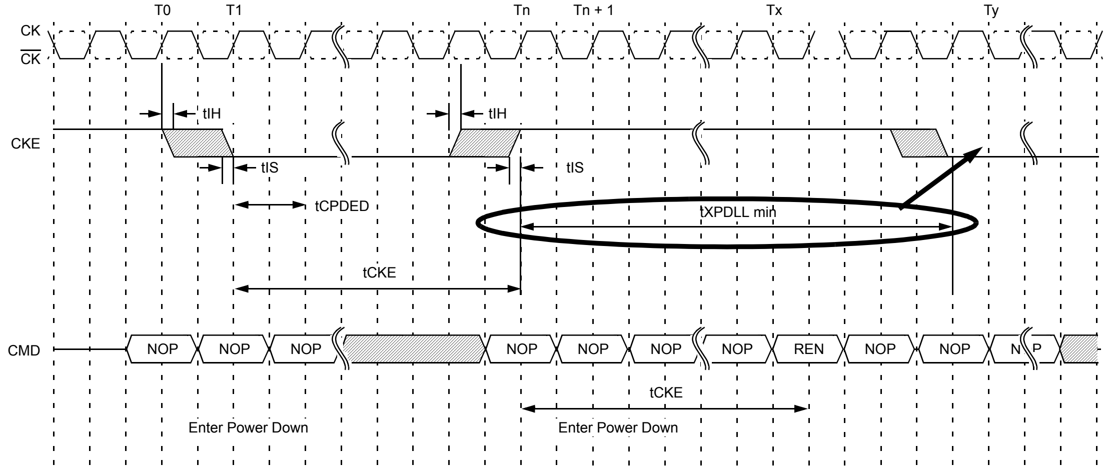
Status of DRAM	Last Command before CKE_low	Parameter	Parameter Value	Unit	Notes
Idle or Active	Activate	tACTPDEN	1	tCK	
Idle or Active	Precharge	tPRPDEN	1	tCK	
Active	RD/RDA	tRDPDEN	RL + 4 + 1	tCK	
Active	WR for BL8OTF, BL8MRS, BC4OTF, BC4MRS	tWRPDEN	WL + 4 + (tWR / tCK)	tCK	1
Active	WRA for BL8OTF, BL8MRS, BC4OTF, BC4MRS	tWRAPDEN	WL + 4 + WR + 1	tCK	2
Idle	Refresh	tREFPDEN	1	tCK	
Idle	Mode Register Set	tMRSPDEN	tMOD		

Note :
1. tWR is defined in ns, for calculation of tWRPDEN, it is necessary to round up tWR / tCK to next integer.
2. WR in clock cycles as programmed in mode register.


T0
T1
Tn
Tn + 1
Tx
Ty
CK
CK
CKE
tIH
tIH
tIS
tIS
tCKE
tCKE
tCPDED
CMD
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
NOP
N P
Enter Power Down
Enter Power Down

Case 1 :
When CKE registered low for PD Entry, tCKE must be satisfied before CKE can be registered high as PD Exit
Case 1a :
After PD Exit, tCKE must be satisfied before CKE can be registered low again.

Figure 65 − Power-Down Entry/Exit Clarifications - Case 1

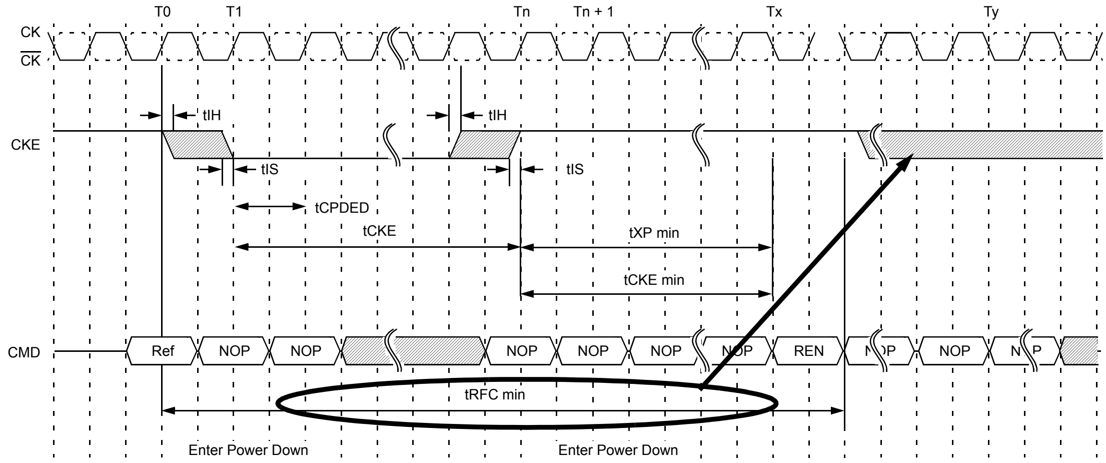

T0
T1
Tn
Tn + 1
Tx
Ty
CK
CK
CKE
tIH
tIH
tIS
tIS
tCPDED
tXPDLL min
tCKE
CMD
NOP
NOP
NOP
NOP
NOP
NOP
NOP
REN
NOP
NOP
N P
tCKE
Enter Power Down
Enter Power Down

Case 2 :
For certain CKE intensive operations, for example, repeated "PD Exit - Refresh - PD Entry" sequence, the number of clock cycles between PD Exit and PD Entry may be insuffcient to keep the DLL updated. Therefore the following conditions must be met in addition to tCKE in order to maintain proper DRAM operation when Refresh command is issued in bet ween PD Exit and PD Entry.

Power down mode can be used in conjunction with Refresh command if the following conditions are met:

1. tXP must be satisfied before issuing the command
2. tXPDLL must be satisfied (referenced to registration of PD exit) before next power down can be entered.

Figure 66 − Power-Down Entry/Exit Clarifications - Case 2


T0
T1
Tn
Tn + 1
Tx
Ty
CK
CK
CKE
tIH
tIH
tIS
tIS
tCPDED
tCKE
tXP min
tCKE min
CMD
Ref
NOP
NOP
NOP
NOP
NOP
NOP
REN
NOP
NOP
NOP
tRFC min
Enter Power Down
Enter Power Down

Case 3 :
If an early PD Entry is issued after Refresh command, once PD Exit is issued, NOP or DES with CKE High must be issued until tRFC from the Refresh command is satisfied. This means CKE can not be registered low twice within tRFC window.

Figure 67 − Power-Down Entry/Exit Clarifications - Case 3

17.0 On-Die Termination (ODT)

ODT (On-Die Termination) is a feature of the DDR3 SDRAM that allows the DRAM to turn on/off termination resistance for each DQ, DQS, $\overline{\text{DQS}}$ and DM for x4 and x8 configuration (and TDQS, $\overline{\text{TDQS}}$ for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin. For x16 configuration, ODT is applied to each DQU, DQL, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$, DMU and DML signal via the ODT control pin. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document :

- The ODT control modes are described in 3.1.
- The ODT synchronous mode is described in 3.2
- The dynamic ODT feature is described in 3.3
- The ODT asynchronous mode is described in 3.4
- The transitions between ODT synchronous and asynchronous are described in 3.4.1 through 3.4.4

The ODT feature is turned off and not supported in Self-Refresh mode.
A simple functional representation of the DRAM ODT feature is shown in Figures 66.

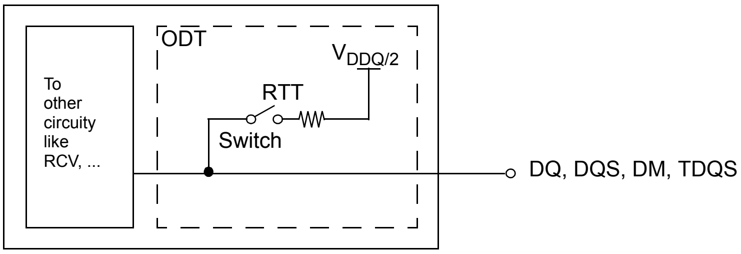


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Figure 68 - Functional Representation of ODT

determined by the settings of Mode Register bits (see Figure on page 12). The ODT pin will be ignored if the Mode Register MR1 is programmed to disable ODT and in self-refresh mode.

17.1 ODT Mode Register and ODT Truth Table

The ODT Mode is enabled if either of MR1 bits A2 or A6 or A9 are non zero. In this case, the value of RTT is determined by the settings of those bits (see Figure on page 12).

Application: Controller sends WR command together with ODT asserted.
- One possible application: The rank that is being written to provides termination.
- DRAM turns ON termination if it sees ODT asserted (except ODT is disabled by MR).
- DRAM does not use any write or read command decode information.
- The Termination Truth Table is shown in Table 17.

Table 17 - Termination Truth Table

ODT pin	DRAM Termination State
0	OFF
1	ON, (OFF, if disabled by MR1 bits A2, A6 and A9 in general)

17.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:
- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode (regardless of MR0 bit A12)
- Precharge power down mode if DLL is enabled during precharge power down by MR0 bit A12.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode.

In synchronous ODT mode, RTT will be turned on ODTLon clock cycles after ODT is sampled high by a rising clock edge and turned off ODTLoff clock cycles after ODT is registered low by a rising clock edge. The ODT latency is tied to the write latency (WL) by: ODTLon = WL - 2; ODTLoff = WL - 2 .

17.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) programmed into the Mode Register (MR1) also applies to the ODT signal. The DRAM internal ODT signal is delayed for a number of clock cycles defined by the Additive Latency (AL) relative to the external ODT signal. ODTLon = CWL + AL - 2; ODTLoff = CWL + AL - 2. For details, refer to DDR3 SDRAM latency definitions.

Table 18 - ODT Latency

Symbol	Parameter	gDDR3-1333	gDDR3-1600	gDDR3-1800	gDDR3-2000	Unit	Symbol
ODTLon	ODT turn on Latency	WL - 2.0 = CWL + AL - 2.0				tCK	ODTLon
ODTLoff	ODT turn on Latency	WL - 2.0 = CWL + AL - 2.0					ODTLoff

17.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply (see also Figures 67):

ODTLon, ODTLoff, tAON,min,max, tAOF,min,max.

Minimum RTT turn-on time (tAONmin) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (tAONmax) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.

Minimum RTT turn-off time (tAOFmin) is the point in time when the device starts to turn off the ODT resistance.
Maximum RTT turn off time (tAOFmax) is the point in time when the on-die termination has reached high impedance.
Both are measured from ODTLoff.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 68). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

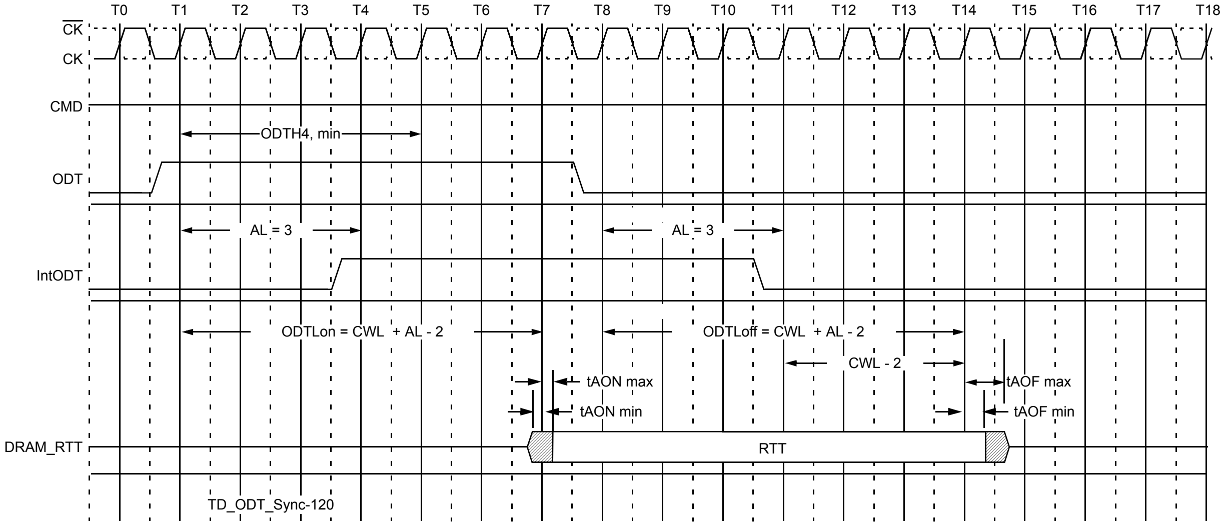

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
CK
CK
CMD
ODTH4, min
ODT
AL = 3
AL = 3
IntODT
ODTLon = CWL + AL - 2
ODTLoff = CWL + AL - 2
CWL - 2
tAON max
tAON min
tAOF max
tAOF min
DRAM_RTT
RTT
TD_ODT_Sync-120

Figure 69 - Synchronous ODT Timing Example for AL = 3; CWL = 5;
ODTLon = AL + CWL - 2 = 6.0; ODTLoff = AL + CWL - 2 = 6

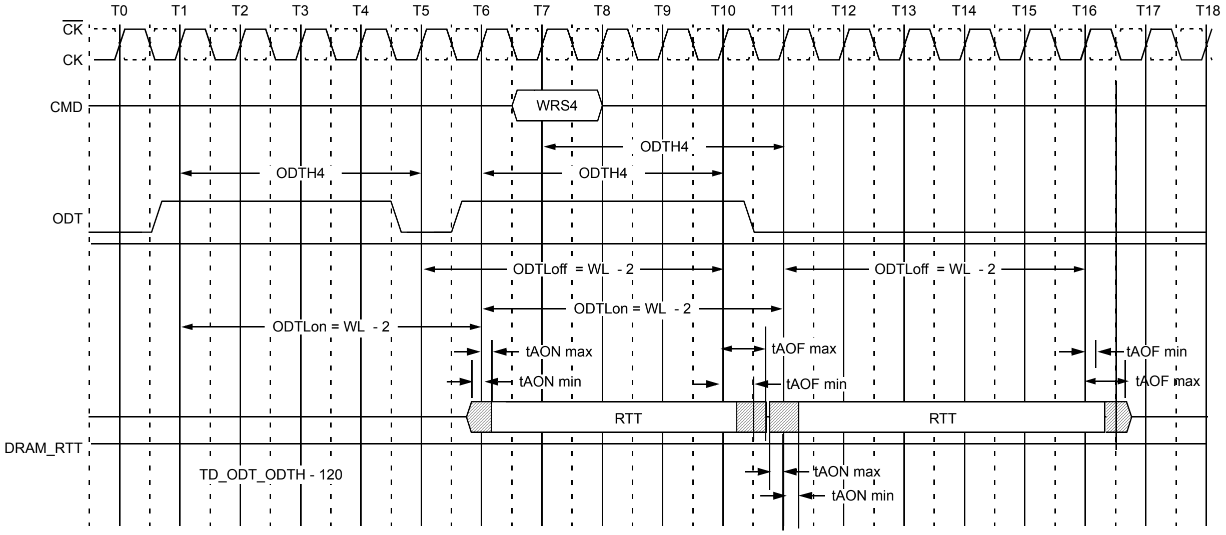

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
CK
CK
CMD
WRS4
ODTH4
ODTH4
ODTH4
ODT
ODTLoff = WL - 2
ODTLoff = WL - 2
ODTLon = WL - 2
ODTLon = WL - 2
tAON max
tAON min
tAOF max
tAOF min
tAOF min
tAOF max
RTT
RTT
DRAM_RTT
TD_ODT_ODTH - 120
tAON max
tAON min

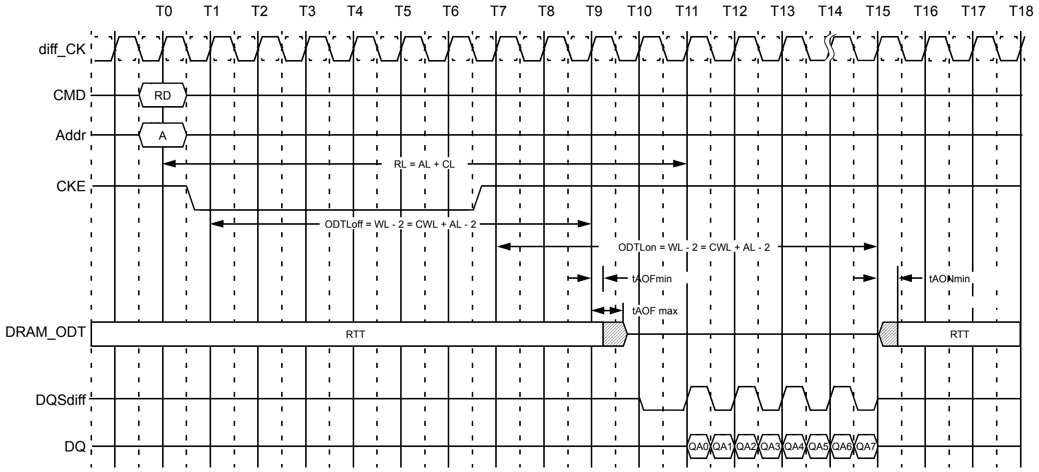
Figure 70 - Synchronous ODT example with BL = 4, WL = 7.

ODT must be held high for at least ODTH4 after assertion (T1); ODT must be kept high ODTH4 (BL = 4) or ODTH8 (BL = 8) after Write command (T7). ODTH is measured from ODT first registered high to ODT first registered low, or from registration of Write command with ODT high to ODT registered low. Note that although ODTH4 is satisfied from ODT registered high at T6 ODT must not go low before T11 as ODTH4 must also be satisfied from the registration of the Write command at T7.

17.2.3 ODT during Reads:

As the DDR3 SDRAM can not terminate and drive at the same time, RTT must be disabled at least half a clock cycle before the read preamble by driving the ODT pin low appropriately. RTT may nominally not be enabled until one clock cycle after the end of the post-amble as shown in the example in Figure 69. As shown in Figure 69 below at cycle T15, DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e tHZ is early) than tAONmin timing may apply. If DRAM stops driving late (i.e tHZ is late) than DRAM complies with tAONmax timing. Note that ODT may be disabled earlier before the Read and enabled later after the Read than shown in this example in Figure 69.

Figure 71 - ODT must be disabled externally during Reads by driving ODT low. (example: CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTLon = CWL + AL - 2 = 8 ; ODTLoff = CWL + AL - 2 = 8)


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
diff_CK
CMD
RD
Addr
A
RL = AL + CL
CKE
ODTLoff = WL - 2 = CWL + AL - 2
ODTLon = WL - 2 = CWL + AL - 2
tAOFmin
tAONmin
tAOF max
DRAM_ODT
RTT
RTT
DQSdiff
DQ
QA0
QA1
QA2
QA3
QA4
QA5
QA6
QA7

17.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

17.3.1 Functional Description:

The Dynamic ODT Mode is enabled if bit (A9) or (A10) of MR2 is set to ’1’. The function is described as follows:

- Two RTT values are available:RTT_Nom and RTT_WR.
  - The value for RTT_Nom is preselected via bits A[9,6,2] in MR1
  - The value for RTT_WR is preselected via bits A[10,9] in MR2
- During operation without commands, the termination is controlled as follows;
  - Nominal termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and latencies ODTLon and ODTLoff.
- When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8)is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
  - A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
  - A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF)or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_Nom is selected.
  - Termination on/off timing is controlled via ODT pin and ODTLon, ODTLoff.

The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10,A9}={0,0}, to disable Dynamic ODT externally.

When ODT is asserted, it must remain high until ODTH4 is satisfied. If a Write command is registered by the SDRAM with ODT high, then ODT must remain high until ODTH4 (BL = 4) or ODTH8 (BL = 8) after the Write command (see Figure 68). ODTH4 and ODTH8 are measured from ODT registered high to ODT registered low or from the registration of a Write command until ODT is registered low.

Table 19 - Latencies and timing parameters relevant for Dynamic ODT

Name and Description	Abbr.	Defined from	Define to	Definition for all DDR3 speed bins	Unit
ODT turn-on Latency	ODTLon	registering external ODT signal high	turning termination on	ODTLon = WL - 2	tCK
ODT turn-off Latency	ODTLoff	registering external ODT signal low	turning termination off	ODTLoff = WL - 2	tCK
ODT Latency for changing from RTT_Nom to RTT_WR	ODTLcnw	registering external write command	change RTT strength from RTT_Nom to RTT_WR	ODTLcnw = WL - 2	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL = 4)	ODTLcwn4	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn4 = 4 + ODTLoff	tCK
ODT Latency for change from RTT_WR to RTT_Nom (BL = 8)	ODTLcwn8	registering external write command	change RTT strength from RTT_WR to RTT_Nom	ODTLcwn8 = 6 + ODTLoff	tCK
minimum ODT hold time after ODT assertion	ODTH4	registering ODT high	ODT registered low	ODTH4 = 4	tCK
minimum ODT hold time after Write (BL = 4)	ODTH4	registering Write with ODT high	ODT registered low	ODTH4 = 4	tCK
minimum ODT hold time after Write (BL = 8)	ODTH8	registering Write with ODT high	ODT registered low	ODTH8 = 6	tCK
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	Min=0.3, Max=0.7	tCK

Table 20 - **Mode Register for RTT selection**

MR1			RTT_Nom(RZQ)	RTT_NOM(ohms)	MR2		RTT_WR(RZQ)	RTT_WR(ohms)
A9	A6	A2			A10	A9		
0	0	0	off	off	0	0	Dynamic ODT OFF : Write does not affect RTT value	
0	0	1	RZQ/4	60	0	1	RZQ/4	60
0	1	0	RZQ/2	120	1	0	RZQ/2	120
0	1	1	RZQ/6	40	1	1	reserved	reserved
1	0	0	RZQ/12	20	-	-	-	-
1	0	1	RZQ/8	30	-	-	-	-
1	1	0	reserved	reserved	-	-	-	-
1	1	1	reserved	reserved	-	-	-	-

Note :

1. RZQ = 240Ω ± 1%
2. If RTT_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

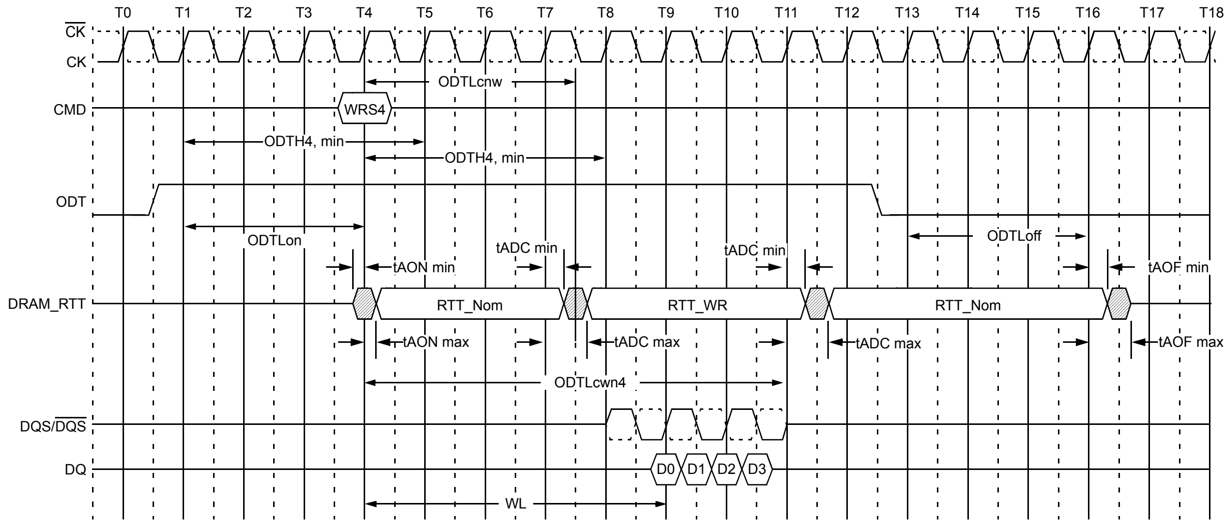

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
CK
CK
CMD
WRS4
ODTLcnw
ODTH4, min
ODTH4, min
ODT
ODTLon
ODTLoff
tAON min
tADC min
tADC min
tAOF min
DRAM_RTT
RTT_Nom
RTT_WR
RTT_Nom
tAON max
tADC max
tADC max
tAOF max
ODTLcwn4
DQS/DQS
DQ
D0
D1
D2
D3
WL

Figure 72 - Dynamic ODT : Behavior with ODT being asserted before and after the write, example for BC4(via MRS or OTF), AL= 0, CWL=5

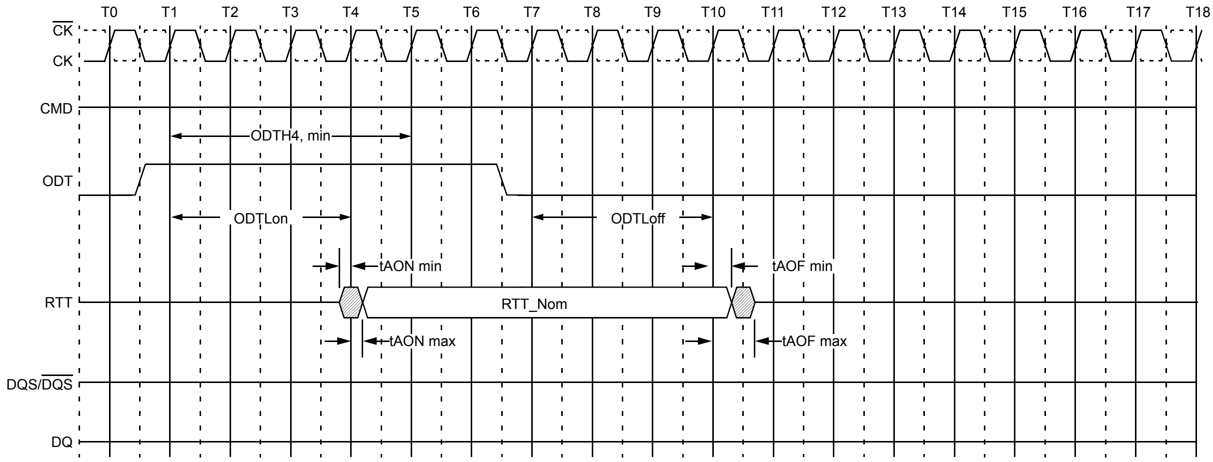

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
CK
CK
CMD
ODTH4, min
ODT
ODTLon
ODTLoff
tAON min
tAOF min
RTT
RTT_Nom
tAON max
tAOF max
DQS/DQS
DQ

Figure 73 - Dynamic ODT : Behavior without write command, AL = 0, CWL = 5

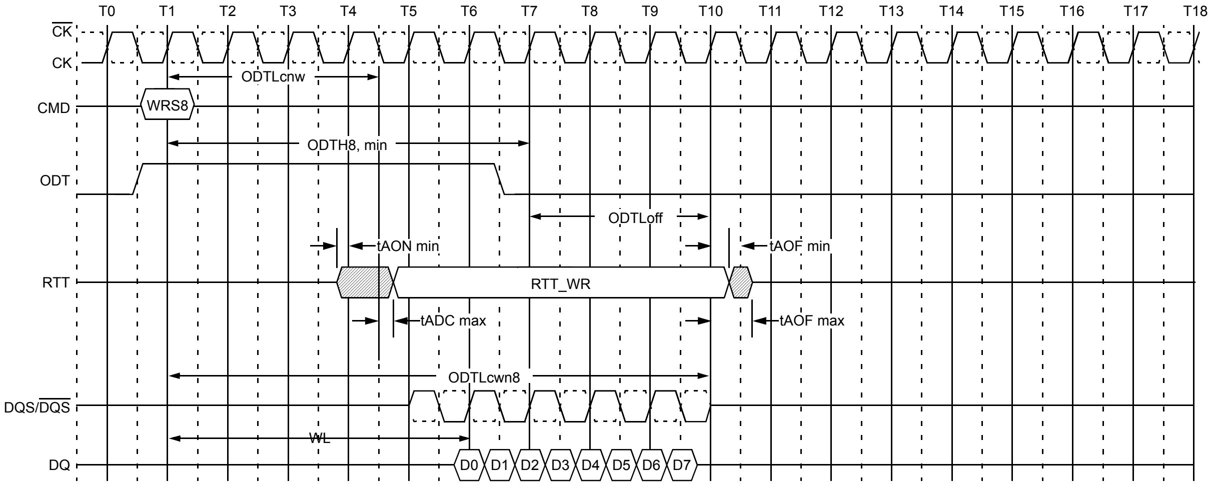

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
CK
CK
CMD
WRS8
ODTLcnw
ODTH8, min
ODT
ODTLoff
tAON min
tAOF min
RTT
RTT_WR
tADC max
tAOF max
ODTLcwn8
DQS/DQS
WL
DQ
D0
D1
D2
D3
D4
D5
D6
D7

Figure 74 - Dynamic ODT : Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BL8 (via MRS or OTF), AL = 0, CWL = 5.

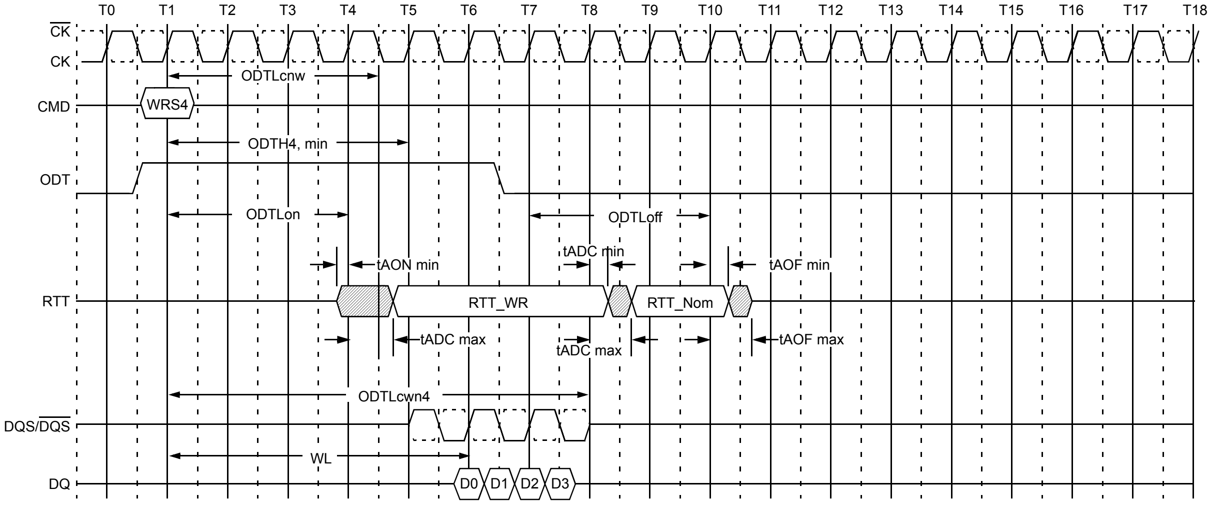

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
CK
CK
CMD
WRS4
ODTLcnw
ODTH4, min
ODT
ODTLon
ODTLoff
tADC min
tAON min
tAOF min
RTT
RTT_WR
RTT_Nom
tADC max
tADC max
tAOF max
ODTLcwn4
DQS/DQS
WL
DQ
D0
D1
D2
D3

Figure 75 - Dynamic ODT : Behavior with ODT pin being asserted together with write command for a duration of 6 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.

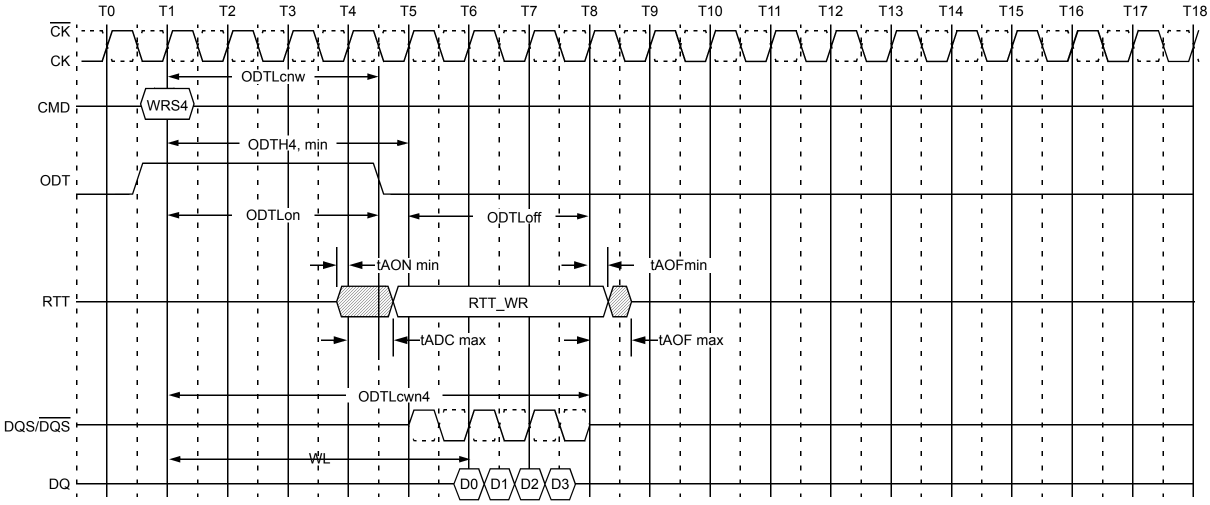

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
T16
T17
T18
CK
CK
CMD
WRS4
ODTLcnw
ODTH4, min
ODT
ODTLon
ODTLoff
tAON min
tAOFmin
RTT
RTT_WR
tADC max
tAOF max
ODTLcwn4
DQS/DQS
WL
DQ
D0
D1
D2
D3

Figure 76 - Dynamic ODT : Behavior with ODT pin being asserted together with write command for a duration of 4 clock cycles, example for BC4 (via MRS or OTF), AL = 0, CWL = 5.

17.4 Asynchronous ODT mode

Asynchronous ODT mode is selected when DRAM runs in DLLon mode, but DLL is temporarily disabled (i.e. frozen) in precharge power-down(by MR0 bit A12). Based on the power down mode definitions, this is currently Precharge power down mode if DLL is disabled during precharge power down by MR0 bit A12.

In asynchronous ODT timing mode, internal ODT command is NOT delayed by Additive Latency (AL) relative to the external ODT command.

In asynchronous ODT mode, the following timing parameters apply

$t_{AONPD,min, max}$, $t_{AOFPD,min,max}$.

Minimum RTT turn-on time (t_{AONPD}min)is the point in time when the device termination circuit leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time(t_{AONPD}max)is the point in time when the ODT resistance is fully on.

t_{AONPD}min and t_{AONPD}max are measured from ODT being sampled high.

Minimum RTT turn-off time (t_{AOFPD}min) is the point in time when the devices termination circuit starts to turn off the ODT resistance. Maximum ODT turn off time (t_{AOFPD}max) is the point in time when the on-die termination has reached high impedance. t_{AOFPD}min and t_{AOFPD}max are measured from ODT being sampled low.

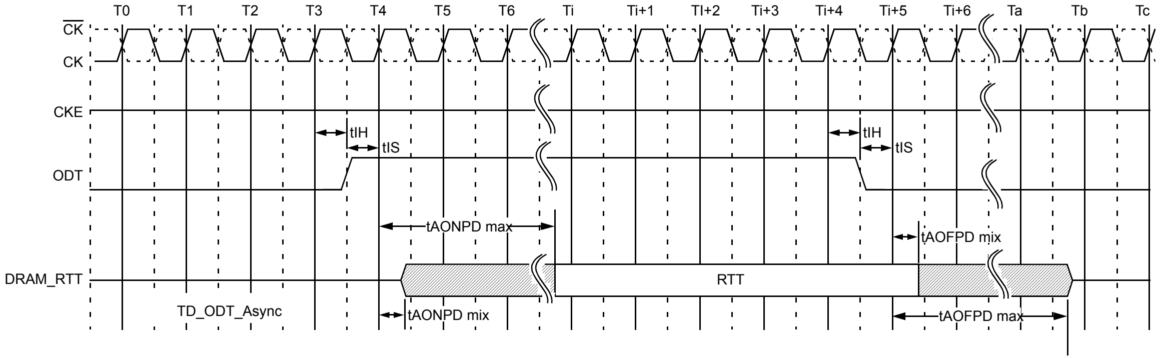


Figure 77 - Asynchronous ODT Timings on DDR3 SDRAM with fast ODT transition: AL is ignored

In Precharge Power Down, ODT receiver remains active, however no Read or Write command can be issued, as the respective ADD/CMD receivers may be disabled.

Table 22 - Asynchronous ODT Timing Parameters for all Speed Bins

Symbol	Description	min	max	Unit
t_{AONPD}	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	1	9	ns
t_{AOFPD}	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	1	9	ns

17.4.1 Synchronous to Asynchronous ODT Mode Transition

Table 23 - ODT timing parameters for Power Down (with DLL frozen)entry and exit transition period

Description	min	max
ODT to RTT turn-on delay	min{ODTLon *t_{CK} + t_{AON}min; t_{AONPD}min}	max{ODTLon *t_{CK} + t_{AON}max; t_{AONPD}max}
	min{ (WL - 2.0) *t_{CK} + t_{AON}min; t_{AONPD}min}	max{ (WL - 2.0) *t_{CK} + t_{AON}max; t_{AONPD}max}
ODT to RTT turn-off delay	min{ODTLoff *t_{CK} + t_{AOF}min; t_{AOFPD}min}	max{ODTLoff *t_{CK} + t_{AOF}max; t_{AOFPD}max}
	min{ (WL - 2.0) *t_{CK} + t_{AOF}min; t_{AOFPD}min}	max{ (WL - 2.0) *t_{CK} + t_{AOF}max; t_{AOFPD}max}
tANPD	WL - 1	

17.4.2 Synchronous to Asynchronous ODT Mode Transition during Powerdown Entry

if DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0" there is a transition period around power down entry, where the DDR3 SDRAM may show either synchronous or asynchronous ODT behavior.

This transition period ends when CKE is first registered low and starts t_{ANPD} before that. If there is a Refresh command in progress while CKE goes low, then the transition period ends tRFC after the Refresh command. t_{ANPD} is equal to (WL-1) and is counted (backwards)from the clock cycle where CKE is first registered low.

ODT assertion during the transition period may result in an RTT change as early as the smaller of t_{AONPD} min and (ODTLon * t_{CK} + t_{AON}min) and as late as the larger of t_{AONPD} max and (ODTLoff * t_{CK} + t_{AON}max). ODT de-assertion during the transition period may late as the larger of t_{AOFPD} max and (ODTLoff * t_{CK} + t_{AOF}max). Note that, if AL has a large Value, the range where RTT is uncertain becomes quite large. it shows the three different cases: ODT_A, synchronous behavior before t_{ANPD}; ODT_B has a state change during the transition period; ODT_C shows a state change after the transition period.

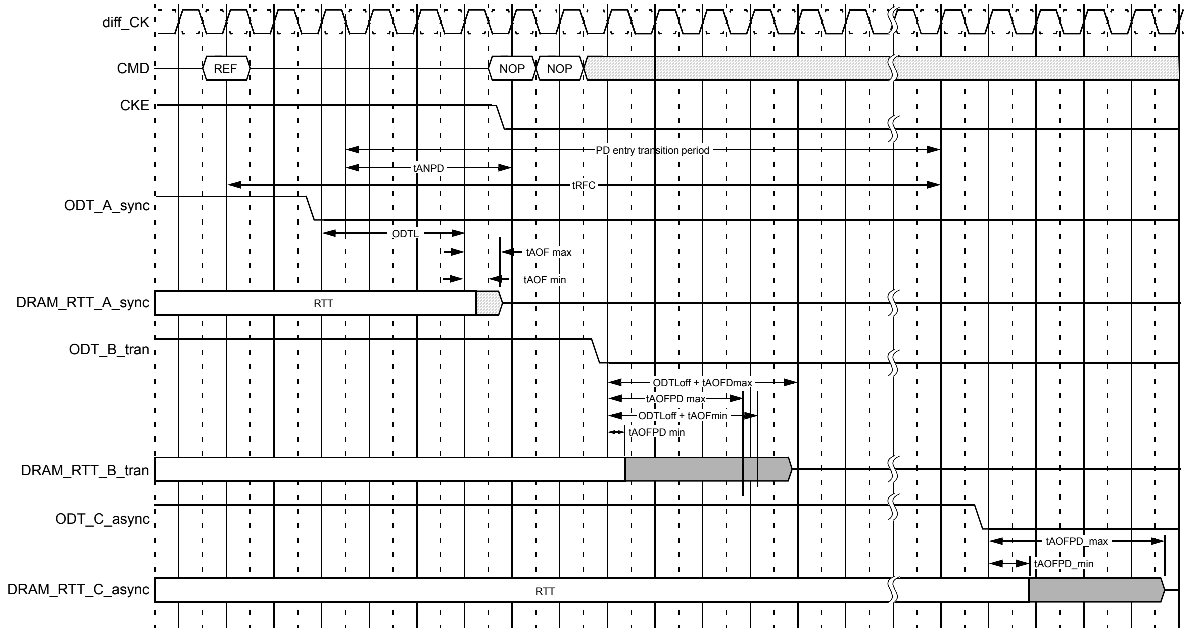

diff_CK
CMD
REF
NOP
NOP
CKE
PD entry transition period
tANPD
tRFC
ODT_A_sync
ODTL
tAOF max
tAOF min
DRAM_RTT_A_sync
RTT
ODT_B_tran
ODTLoff + tAOFDmax
tAOFPD max
ODTLoff + tAOFmin
tAOFPD min
DRAM_RTT_B_tran
ODT_C_async
tAOFPD_max
tAOFPD_min
DRAM_RTT_C_async
RTT

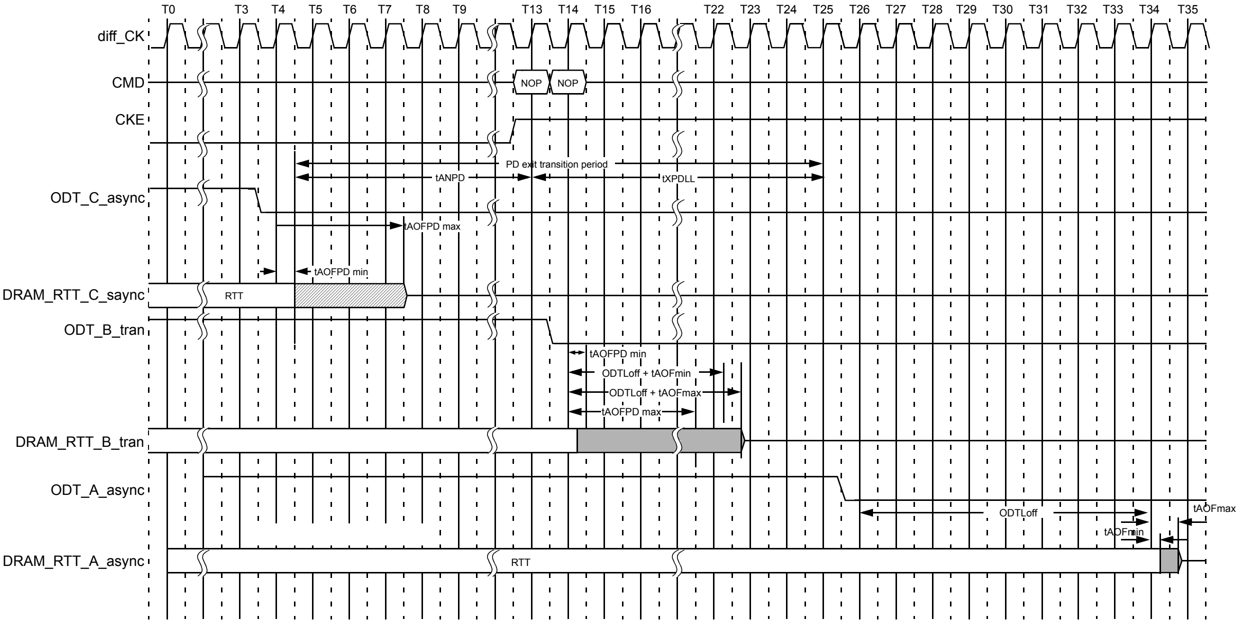
Figure 78 - Synchronous to asynchronous transition during Precharge Power Down (with DLL frozen) entry (AL = 0; CWL = 5; tANPD = WL - 1 = 4)

17.4.3 Asynchronous to Synchronous ODT Mode Transition during Power-Down Exit

If DLL is selected to be frozen in Precharge Power Down Mode by the setting of bit A12 in MR0 to "0", there is also a transition period around power down exit, where either synchronous or asynchronous response to a change in ODT must be expected from the DDR3 SDRAM.
This transition period starts tANPD before CKE is first registered high, and ends tXPDLL after CKE is first registered high. tANPD is equal to max{ODTLoff, ODTLon} and is counted from the clock cycle where CKE is first registered high.

ODT assertion during the transition period may result in an RTT change as early as the smaller of t_{AONPD} min and (ODTLon * t_{CK} + t_{AON}min) and as late as the larger of t_{AONPD} max and (ODTLon * t_{CK} + t_{AON}max). ODT de-assertion during the transition period may result in an RTT change as early as the smaller of t_{AOFPD} min and (ODTLoff * t_{CK} + t_{AOF}min) and as late as the larger of t_{AOFPD} max and (ODTLoff * t_{CK} + t_{AOF}max).

Note that, if AL has a large Value, the range where RTT is uncertain becomes quite large.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T24
T25
T26
T27
T28
T29
T30
T31
T32
T33
T34
T35
diff_CK
CMD
NOP
NOP
CKE
PD exit transition period
tANPD
tXPDLL
ODT_C_async
tAOFPD max
tAOFPD min
DRAM_RTT_C_saync
RTT
ODT_B_tran
tAOFPD min
ODTLoff + tAOFmin
ODTLoff + tAOFmax
tAOFPD max
DRAM_RTT_B_tran
ODT_A_async
ODTLoff
tAOFmax
tAOFmin
DRAM_RTT_A_async
RTT

Figure 79 - Asynchronous to synchronous transition during Precharge Power Down (with DLL frozen) exit (CL = 6; AL = CL - 1; CWL = 5; tANPD = WL - 1 = 9)

17.4.4 Asynchronous to Synchronous ODT Mode during short CKE high and short CKE low periods

If the total time in Precharge Power Down state or Idle state is very short, the transition periods for PD entry and PD exit may overlap. In this case the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD entry transition period to the end of the PD exit transition period (even if the entry period ends later than the exit period).

If the total time in Idle state is very short, the transition periods for PD exit and PD exit and PD entry may overlap. In this case the response of the DDR3 SDRAMs RTT to a change in ODT state at the input may be synchronous OR asynchronous from the start of the PD exit transition period to the end of the PD entry transition period. Note that, it is assumed that there was no Refresh command in progress when Idle state was entered.

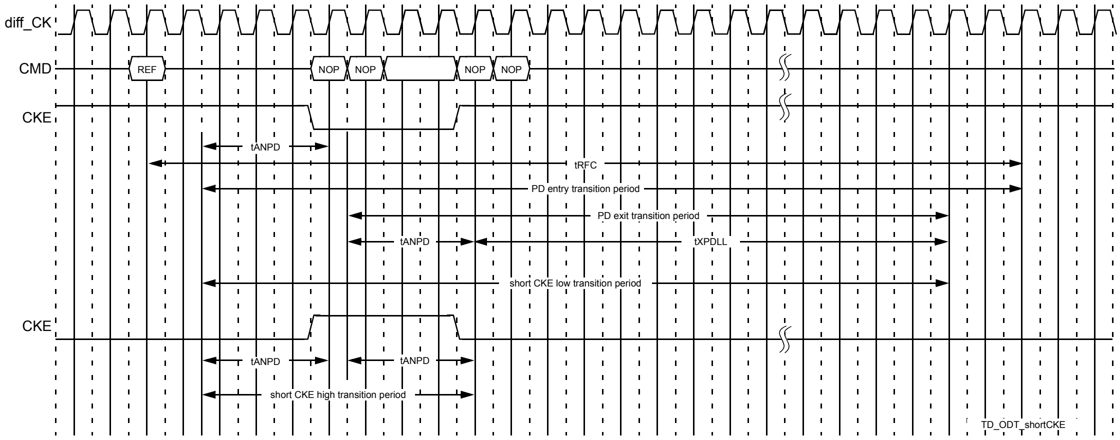
diff_CK
CMD
REF
NOP
NOP
NOP
NOP
CKE
tANPD
tRFC
PD entry transition period
PD exit transition period
tANPD
tXPDLL
short CKE low transition period
CKE
tANPD
tANPD
short CKE high transition period
TD_ODT_shortCKE

Figure 80 - Transition period for short CKE cycles with entry and exit period overlapping (AL = 0, WL = 5, tANPD = WL - 1 = 4)

17.5 ZQ Calibration Commands

17.5.1 ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values over PVT. DDR3 SDRAM needs longer time to calibrate Ron & ODT at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and once calibration is achieved the calirated values are transferred from calibration engine to DRAM IO which gets reflected as updated Ron and ODT values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET is allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for VT variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS.

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper or tZQCS. The quiet time on the DRAM channel helps in accurate calibration of Ron and ODT. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR3 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is tXS.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper or tZQinit or tZQCS between the devices.

Table 24 - ZQ Calibration Command Truth Table

Function	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA2-BA0	A15-A13	$\overline{\text{A12}}$	$\overline{\text{A10}}$	A11 A9-A10
	Prev Cycle	Next Cycle									
ZQ Calibration Long	H	H	L	H	H	L	X	X	X	1	X
ZQ Calibration Short (ZQCS)	H	H	L	H	H	L	X	X	X	0	X

17.5.2 ZQ Calibration Timing

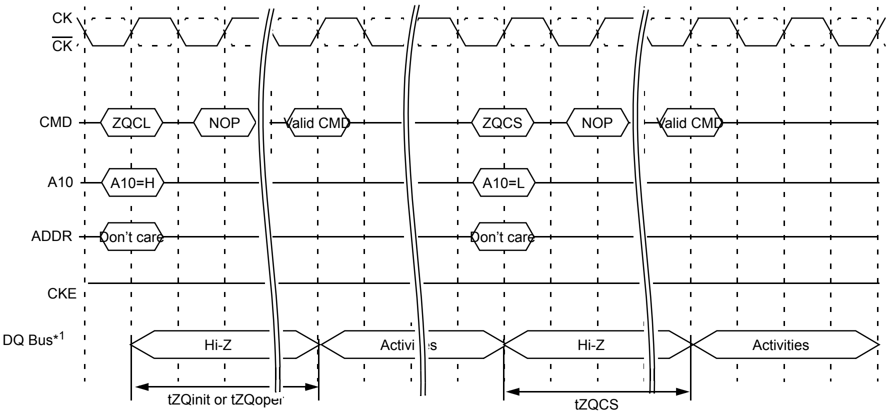

Figure 81 - ZQ Calibration Timing

Note :ODT must be disabled during calibration procedure
*1: All devices connected to DQ bus should be high impedance during calibration

17.5.3 ZQ External Resistor Value and Tolerance and Capacitive loading on ZQ

In order to use the ZQ Calibration function, a 240 ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. The single resistor can be used for each SDRAM or one resistor can be shared between two SDRAMs if the ZQ calibration timings for each SDRAM do not overlap. The total capacitive loading on the ZQ pin must be limited.