# 4Mb Sync. Burst SRAM Specification

## 100 TQFP with Pb & Pb-Free

## (RoHS compliant)

## Document Title

**128Kx36 & 256Kx18-Bit Synchronous Burst SRAM**

## Revision History

| Rev. No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | 1. Initial draft | May. 15. 2001 | Preliminary |
| 0.1 | 1. Changed DC parameters<br>Icc ; from 300mA to 250mA at -65,<br>from 280mA to 230mA at -75,<br>from 260mA to 210mA at -80,<br>from 240mA to 190mA at -90,<br><br>Icc ; from 140mA to 130mA at -65,<br>from 130mA to 120mA at -75,<br>from 120mA to 110mA at -80,<br>from 110mA to 100mA at -90,<br><br>$I_{SB1}$ ; from 100mA to 80mA | June. 12. 2001 | Preliminary |
| 0.2 | 1. Add x32 org. and industrial temperature | Aug. 11. 2001 | Preliminary |
| 1.0 | 1. Final spec release<br>2. Changed Pin Capacitance<br>- Cin ; from 5pF to 4pF<br>- Cout ; from 7pF to 6pF | Nov. 15. 2001 | Final |
| 2.0 | 1. Remove x32 organization<br>2. Remove -80 speed bin | Nov. 17. 2003 | Final |
| 3.0 | 1. Add lead-free package | Jul. 3, 2006 | Final |

## 4Mb SB SRAM Ordering Information

| Org. | VDD (V) | Speed (ns) | Access Time (ns) | Part Number | RoHS Avail. |
|---|---|---|---|---|---|
| 256Kx18 | 3.3 | 7.5 | 6.5 | K7B401825B-P(Q)[1]C(I)[2]65 | √ |
| | | 8.5 | 7.5 | K7B401825B-Q[3]C(I)[2]75 | • |
| 128Kx32 | | 7.5 | 6.5 | K7B403225B-P(Q)[1]C(I)[2]65 | √ |
| | | 8.5 | 7.5 | K7B403225B-Q[3]C(I)75 | • |
| 128Kx36 | | 7.5 | 6.5 | K7B403625B-P(Q)[1]C(I)[2]65 | √ |
| | | 8.5 | 7.5 | K7B403625B-Q[3]C(I)[2]75 | • |

Note 1. P(Q) [Package type]: P-Pb Free, Q-Pb
2. C(I) [Operating Temperature]: C-Commercial, I-Industrial
3. Support only Pb package parts at this frequency. To use Pb-Free package, use faster frequency parts.

# 128Kx36 & 256Kx18-Bit Synchronous Burst SRAM

## FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- $V_{DD}$= 3.3V+0.3V/-0.165V Power Supply.
- $V_{DDQ}$ Supply Voltage 3.3V+0.3V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-TQFP-1420A (Lead and Lead-Free package)
- Operating in commeical and industrial temperature range.

## FAST ACCESS TIMES

| PARAMETER | Symbol | -65 | -75 | Unit |
|---|---|---|---|---|
| Cycle Time | $t_{CYC}$ | 7.5 | 8.5 | ns |
| Clock Access Time | $t_{CD}$ | 6.5 | 7.5 | ns |
| Output Enable Access Time | $t_{OE}$ | 3.5 | 3.5 | ns |

## GENERAL DESCRIPTION

The K7B403625B and K7B401825B are 4,718,592 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium/Power PC based system. And with $\overline{CS_1}$ high, $\overline{ADSP}$ is blocked to control signals.

It can be organized as 128K(256K) words of 36(18) bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

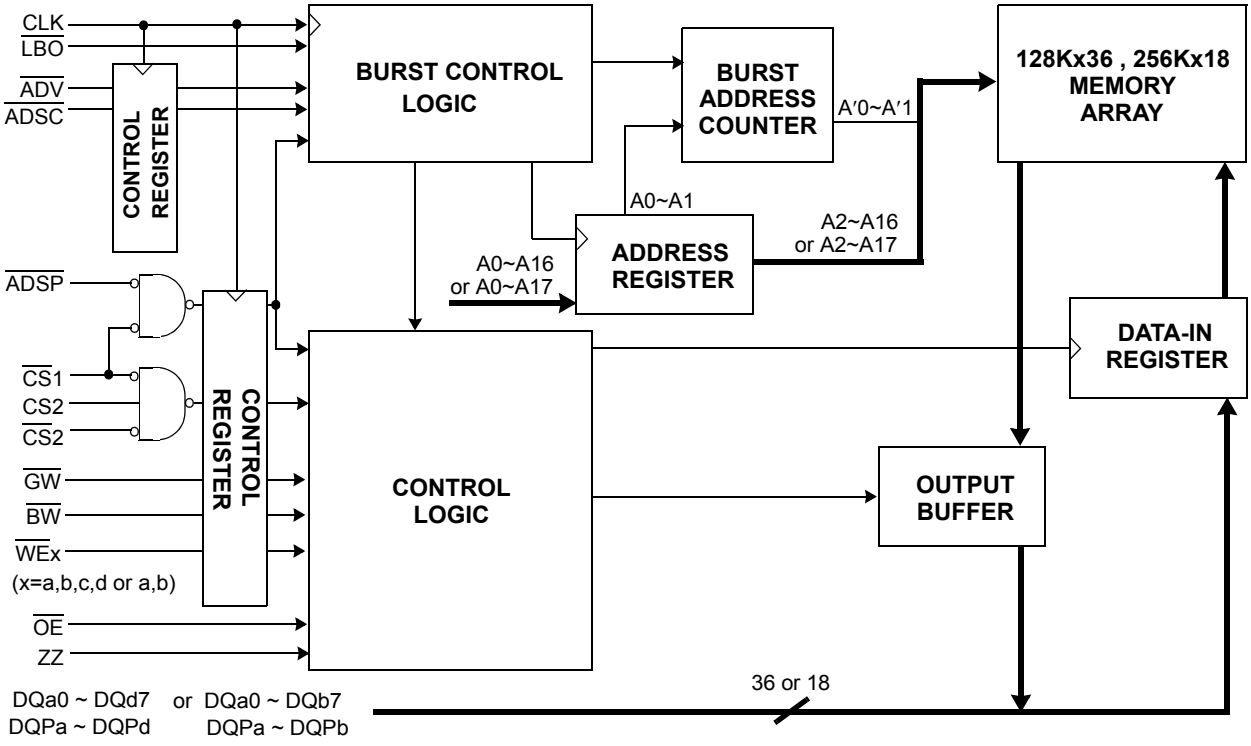
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B403625B and K7B401825B are implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

## LOGIC BLOCK DIAGRAM



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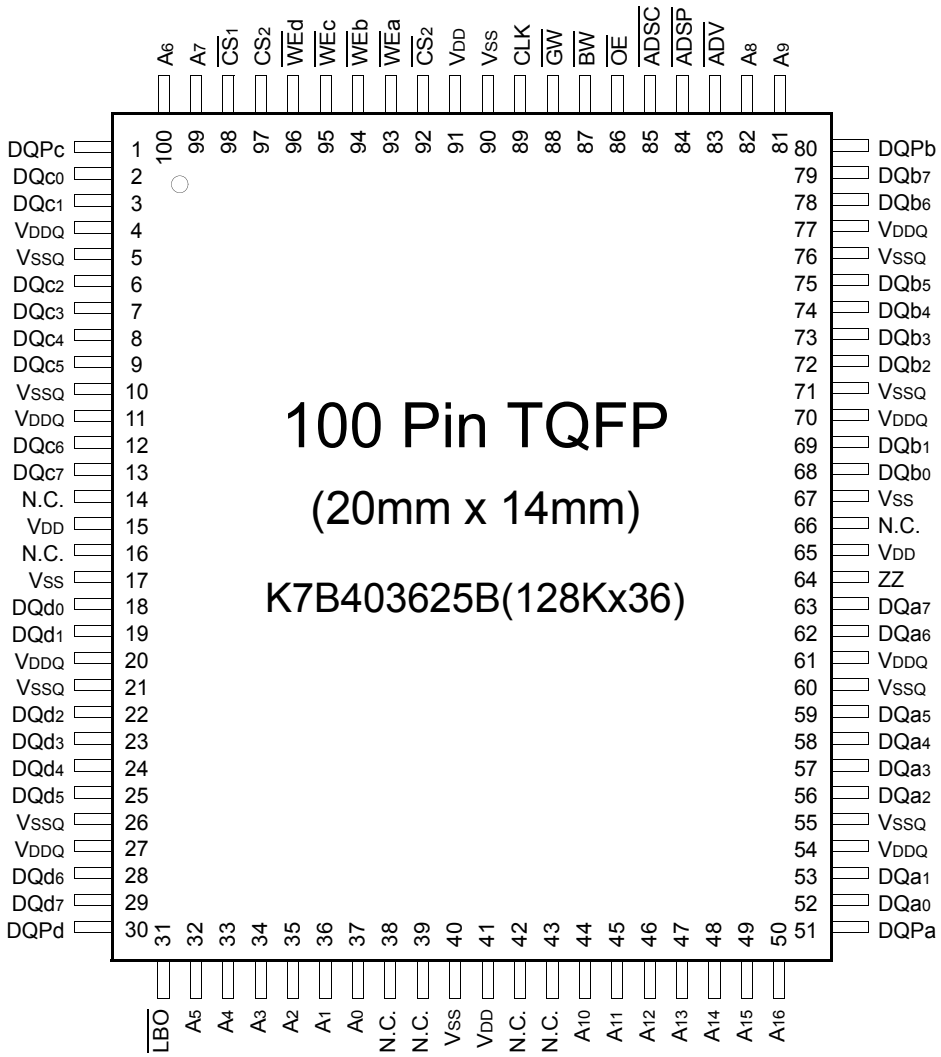
## PIN CONFIGURATION(TOP VIEW)



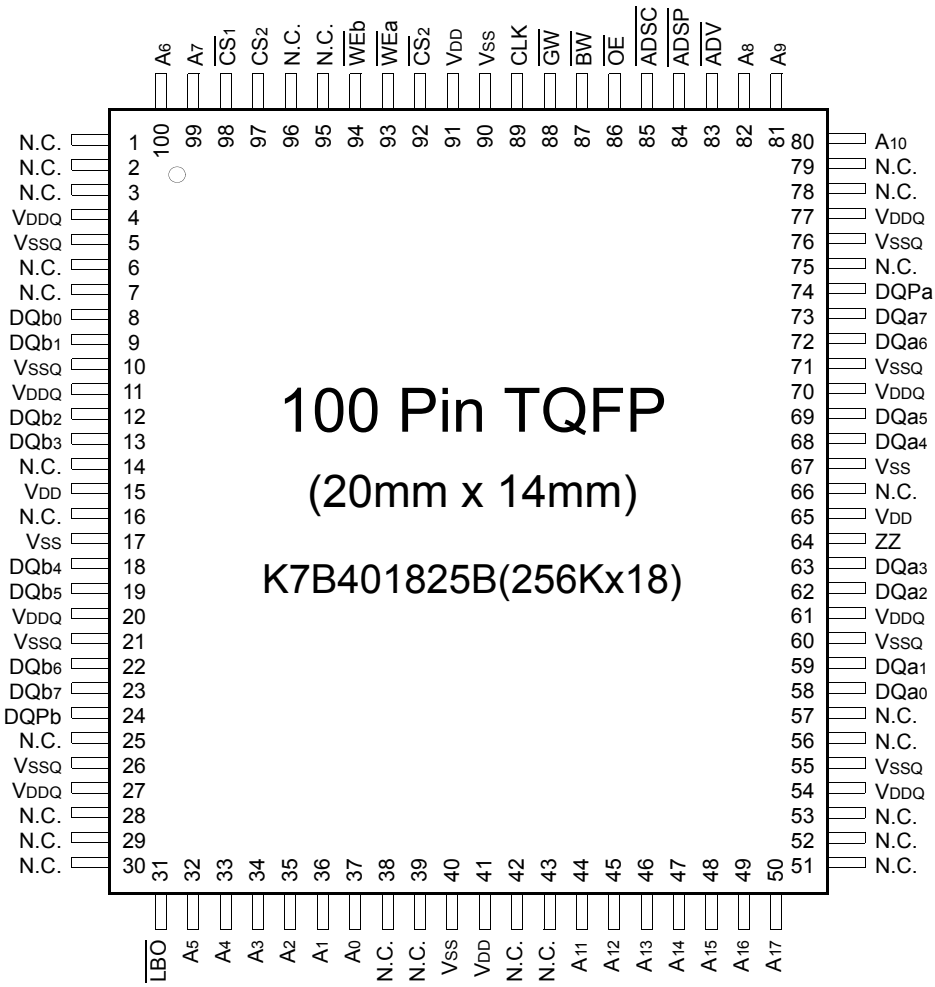

## PIN NAME

| SYMBOL | PIN NAME | TQFP PIN NO. | SYMBOL | PIN NAME | TQFP PIN NO. |
|---|---|---|---|---|---|
| $A_0$ - $A_{16}$ | Address Inputs | 32,33,34,35,36,37 44,45,46,47,48,49 50,81,82,99,100 | $V_{DD}$ | Power Supply(+3.3V) | 15,41,65,91 |
| | | | $V_{SS}$ | Ground | 17,40,67,90 |
| $\overline{ADV}$ | Burst Address Advance | 83 | N.C. | No Connect | 14,16,38,39,42,43,66 |
| $\overline{ADSP}$ | Address Status Processor | 84 | | | |
| $\overline{ADSC}$ | Address Status Controller | 85 | $DQa_0$~$a_7$ | Data Inputs/Outputs | 52,53,56,57,58,59,62,63 |
| CLK | Clock | 89 | $DQb_0$~$b_7$ | | 68,69,72,73,74,75,78,79 |
| $\overline{CS_1}$ | Chip Select | 98 | $DQc_0$~$c_7$ | | 2,3,6,7,8,9,12,13 |
| $\overline{CS_2}$ | Chip Select | 97 | $DQd_0$~$d_7$ | | 18,19,22,23,24,25,28,29 |
| $\overline{CS_2}$ | Chip Select | 92 | DQPa~Pd | | 51,80,1,30 |
| $\overline{WEx}$ (x=a,b,c,d) | Byte Write Inputs | 93,94,95,96 | $V_{DDQ}$ | Output Power Supply (2.5V or 3.3V) | 4,11,20,27,54,61,70,77 |
| $\overline{OE}$ | Output Enable | 86 | | | |
| $\overline{GW}$ | Global Write Enable | 88 | $V_{SSQ}$ | Output Ground | 5,10,21,26,55,60,71,76 |
| $\overline{BW}$ | Byte Write Enable | 87 | | | |
| $\overline{ZZ}$ | Power Down Input | 64 | | | |
| LBO | Burst Mode Control | 31 | | | |



SAMSUNG ELECTRONICS

## PIN CONFIGURATION(TOP VIEW)




## PIN NAME

| SYMBOL | PIN NAME | TQFP PIN NO. | SYMBOL | PIN NAME | TQFP PIN NO. |
|---|---|---|---|---|---|
| A0 - A17 | Address Inputs | 32,33,34,35,36,37, 44,45,46,47,48,49, 50,80,81,82,99,100 | VDD | Power Supply(+3.3V) | 15,41,65,91 |
| | | | VSS | Ground | 17,40,67,90 |
| | | | N.C. | No Connect | 1,2,3,6,7,14,16,25,28,29, 30,38,39,42,43,51,52,53, 56,57,66,75,78,79,95,96 |
| $\overline{ADV}$ | Burst Address Advance | 83 | | | |
| $\overline{ADSP}$ | Address Status Processor | 84 | | | |
| $\overline{ADSC}$ | Address Status Controller | 85 | | | |
| $\overline{CLK}$ | Clock | 89 | DQa0~a7 | Data Inputs/Outputs | 58,59,62,63,68,69,72,73 |
| $\overline{CS_1}$ | Chip Select | 98 | DQb0~b7 | | 8,9,12,13,18,19,22,23 |
| $\overline{CS_2}$ | Chip Select | 97 | DQPa, Pb | | 74,24 |
| $\overline{CS_2}$ | Chip Select | 92 | VDDQ | Output Power Supply (2.5V or 3.3V) | 4,11,20,27,54,61,70,77 |
| $\overline{WEx}$ (x=a,b) | Byte Write Inputs | 93,94 | | | |
| | | | VSSQ | Output Ground | 5,10,21,26,55,60,71,76 |
| $\overline{OE}$ | Output Enable | 86 | | | |
| $\overline{GW}$ | Global Write Enable | 88 | | | |
| $\overline{BW}$ | Byte Write Enable | 87 | | | |
| $\overline{ZZ}$ | Power Down Input | 64 | | | |
| LBO | Burst Mode Control | 31 | | | |



SAMSUNG ELECTRONICS

## FUNCTION DESCRIPTION

The K7B403625B and K7B401825B are synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, $\overline{LBO}$ and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WE}$a, $\overline{WE}$b, $\overline{WE}$c, and $\overline{WE}$d are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WE}$x.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In K7B403625B, a 128Kx36 organization, $\overline{WE}$a controls DQa0 ~ DQa7 and DQPa, $\overline{WE}$b controls DQb0 ~ DQb7 and DQPb, $\overline{WE}$c controls DQc0 ~ DQc7 and DQPc and $\overline{WE}$d controls DQd0 ~ DQd7 and DQPd.

$\overline{CS_1}$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the $\overline{LBO}$ pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

## BURST SEQUENCE TABLE

**(Interleaved Burst)**

| $\overline{LBO}$ PIN | HIGH | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|---|
| | | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ |
| First Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |

**Note :** 1. $\overline{LBO}$ pin must be tied to high or low, and floating state must not be allowed.

**(Linear Burst)**

| $\overline{LBO}$ PIN | LOW | Case 1 | | Case 2 | | Case 3 | | Case 4 | |
|---|---|---|---|---|---|---|---|---|---|
| | | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ | $A_0$ |
| First Address | | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| ↓ | | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| Fourth Address | | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |

**Note :** 1. $\overline{LBO}$ pin must be tied to high or low, and floating state must not be allowed.

## ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

| OPERATION | ZZ | $\overline{OE}$ | I/O STATUS |
|---|---|---|---|
| Sleep Mode | H | X | High-Z |
| Read | L | L | DQ |
| | L | H | High-Z |
| Write | L | X | Din, High-Z |
| Deselected | L | X | High-Z |

**Notes**

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffersmust be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

## TRUTH TABLES

### SYNCHRONOUS TRUTH TABLE

| $\overline{CS_1}$ | $CS_2$ | $\overline{CS_2}$ | $\overline{ADSP}$ | $\overline{ADSC}$ | $\overline{ADV}$ | $\overline{WRITE}$ | CLK | ADDRESS ACCESSED | OPERATION |
|---|---|---|---|---|---|---|---|---|---|
| H | X | X | X | L | X | X | ↑ | N/A | Not Selected |
| L | L | X | L | X | X | X | ↑ | N/A | Not Selected |
| L | X | H | L | X | X | X | ↑ | N/A | Not Selected |
| L | L | X | X | L | X | X | ↑ | N/A | Not Selected |
| L | X | H | X | L | X | X | ↑ | N/A | Not Selected |
| L | H | L | L | X | X | X | ↑ | External Address | Begin Burst Read Cycle |
| L | H | L | H | L | X | L | ↑ | External Address | Begin Burst Write Cycle |
| L | H | L | H | L | X | H | ↑ | External Address | Begin Burst Read Cycle |
| X | X | X | H | H | L | H | ↑ | Next Address | Continue Burst Read Cycle |
| H | X | X | X | H | L | H | ↑ | Next Address | Continue Burst Read Cycle |
| X | X | X | H | H | L | L | ↑ | Next Address | Continue Burst Write Cycle |
| H | X | X | X | H | L | L | ↑ | Next Address | Continue Burst Write Cycle |
| X | X | X | H | H | H | H | ↑ | Current Address | Suspend Burst Read Cycle |
| H | X | X | X | H | H | H | ↑ | Current Address | Suspend Burst Read Cycle |
| X | X | X | H | H | H | L | ↑ | Current Address | Suspend Burst Write Cycle |
| H | X | X | X | H | H | L | ↑ | Current Address | Suspend Burst Write Cycle |

**Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
   $\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

### WRITE TRUTH TABLE( x36)

| $\overline{GW}$ | $\overline{BW}$ | $\overline{WEa}$ | $\overline{WEb}$ | $\overline{WEc}$ | $\overline{WEd}$ | OPERATION |
|---|---|---|---|---|---|---|
| H | H | X | X | X | X | READ |
| H | L | H | H | H | H | READ |
| H | L | L | H | H | H | WRITE BYTE a |
| H | L | H | L | H | H | WRITE BYTE b |
| H | L | H | H | L | L | WRITE BYTE c and d |
| H | L | L | L | L | L | WRITE ALL BYTEs |
| L | X | X | X | X | X | WRITE ALL BYTEs |

**Notes :** 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

### WRITE TRUTH TABLE(x18)

| $\overline{GW}$ | $\overline{BW}$ | $\overline{WEa}$ | $\overline{WEb}$ | OPERATION |
|---|---|---|---|---|
| H | H | X | X | READ |
| H | L | H | H | READ |
| H | L | L | H | WRITE BYTE a |
| H | L | H | L | WRITE BYTE b |
| H | L | L | L | WRITE ALL BYTEs |
| L | X | X | X | WRITE ALL BYTEs |

**Notes :** 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

## ABSOLUTE MAXIMUM RATINGS*

| PARAMETER | | SYMBOL | RATING | UNIT |
|---|---|---|---|---|
| Voltage on $V_{DD}$ Supply Relative to $V_{SS}$<br>Voltage on $V_{DDQ}$ Supply Relative to $V_{SS}$ | | $V_{DD}$ | -0.3 to 4.6 | V |
| | | $V_{DDQ}$ | $V_{DD}$ | V |
| Voltage on Input Pin Relative to $V_{SS}$ | | $V_{IN}$ | -0.3 to $V_{DD}$+0.3 | V |
| Voltage on I/O Pin Relative to $V_{SS}$ | | $V_{IO}$ | -0.3 to $V_{DDQ}$+0.3 | V |
| Power Dissipation | | $P_D$ | 1.4 | W |
| Storage Temperature | | $T_{STG}$ | -65 to 150 | °C |
| Operating Temperature | Commercial | $T_{OPR}$ | 0 to 70 | °C |
| | Industrial | $T_{OPR}$ | -40 to 85 | °C |
| Storage Temperature Range Under Bias | | $T_{BIAS}$ | -10 to 85 | °C |

***Note :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING CONDITIONS at 3.3V I/O (0°C≤ $T_A$≤70°C)

| PARAMETER | SYMBOL | MIN | Typ. | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 3.135 | 3.3 | 3.6 | V |
| | $V_{DDQ}$ | 3.135 | 3.3 | 3.6 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |

* The above parameters are also guaranteed at industrial temperature range.

## OPERATING CONDITIONS at 2.5V I/O(0°C ≤ $T_A$ ≤ 70°C)

| PARAMETER | SYMBOL | MIN | Typ. | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 3.135 | 3.3 | 3.6 | V |
| | $V_{DDQ}$ | 2.375 | 2.5 | 2.9 | V |
| Ground | $V_{SS}$ | 0 | 0 | 0 | V |

* The above parameters are also guaranteed at industrial temperature range.

## CAPACITANCE*($T_A$=25°C, f=1MHz)

| PARAMETER | SYMBOL | TEST CONDITION | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 4 | pF |
| Output Capacitance | $C_{OUT}$ | $V_{OUT}$=0V | - | 6 | pF |

***Note :** Sampled not 100% tested.

## DC ELECTRICAL CHARACTERISTICS($T_A$=0 to 70°C, $V_{DD}$=3.3V+0.3V/-0.165V)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | MAX | UNI |
|---|---|---|---|---|---|---|
| Input Leakage Current(except ZZ) | $I_{IL}$ | $V_{DD}$=Max , $V_{IN}$=$V_{SS}$ to $V_{DD}$ | | -2 | +2 | μA |
| Output Leakage Current | $I_{OL}$ | Output Disabled, $V_{OUT}$=$V_{SS}$ to $V_{DDQ}$ | | -2 | +2 | μA |
| Operating Current | $I_{CC}$ | Device Selected, $I_{OUT}$=0mA, ZZ≤$V_{IL}$, All Inputs=$V_{IL}$ or $V_{IH}$ | -65 | - | 250 | mA |
| | | | -75 | - | 230 | |
| Standby Current | $I_{SB}$ | Device deselected, $I_{OUT}$=0mA, ZZ≤$V_{IL}$, f=Max, All Inputs≤0.2V or ≥ $V_{DD}$-0.2V | -65 | - | 130 | mA |
| | | | -75 | - | 120 | |
| | $I_{SB1}$ | Device deselected, $I_{OUT}$=0mA, ZZ≤0.2V, f=0, All Inputs=fixed ($V_{DD}$-0.2V or 0.2V) | | - | 80 | mA |
| | $I_{SB2}$ | Device deselected, $I_{OUT}$=0mA, ZZ≥$V_{DD}$-0.2V, f=Max, All Inputs≤$V_{IL}$ or ≥$V_{IH}$ | | - | 50 | mA |
| Output Low Voltage(3.3V I/O) | $V_{OL}$ | $I_{OL}$ = 8.0mA | | - | 0.4 | V |
| Output High Voltage(3.3V I/O) | $V_{OH}$ | $I_{OH}$ = -4.0mA | | 2.4 | - | V |
| Output Low Voltage(2.5V I/O) | $V_{OL}$ | $I_{OL}$ = 1.0mA | | - | 0.4 | V |
| Output High Voltage(2.5V I/O) | $V_{OH}$ | $I_{OH}$ = -1.0mA | | 2.0 | - | V |
| Input Low Voltage(3.3V I/O) | $V_{IL}$ | | | -0.5* | 0.8 | V |
| Input High Voltage(3.3V I/O) | $V_{IH}$ | | | 2.0 | $V_{DD}$+03** | V |
| Input Low Voltage(2.5V I/O) | $V_{IL}$ | | | -0.3* | 0.7 | V |
| Input High Voltage(2.5V I/O) | $V_{IH}$ | | | 1.7 | $V_{DD}$+0.3** | V |

The above parameters are also guaranteed at industrial temperature range.

* $V_{IL}$(Min)=-2.0(Pulse Width ≤ $t_{CYC}$/2)

** $V_{IH}$(Max)=4.6(Pulse Width ≤ $t_{CYC}$/2)

** In Case of I/O Pins, the Max. $V_{IH}$=$V_{DDQ}$+0.3V

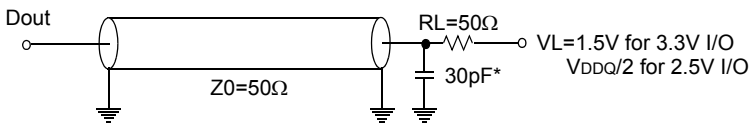
## TEST CONDITIONS

($V_{DD}$=3.3V+0.3V/-0.165V,$V_{DDQ}$=3.3V+0.3/-0.165V or $V_{DD}$=3.3V+0.3V/-0.165V,$V_{DDQ}$=2.5V+0.4V/-0.125V, $T_A$=0 to 70°C)

| PARAMETER | VALUE |
|---|---|
| Input Pulse Level(for 3.3V I/O) | 0 to 3V |
| Input Pulse Level(for 2.5V I/O) | 0 to 2.5V |
| Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O) | 1ns |
| Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O) | 1ns |
| Input and Output Timing Reference Levels for 3.3V I/O | 1.5V |
| Input and Output Timing Reference Levels for 2.5V I/O | $V_{DDQ}$/2 |
| Output Load | See Fig. 1 |

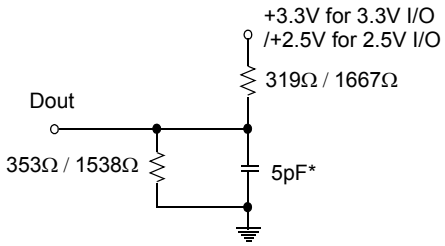
* The above parameters are also guaranteed at industrial temperature range.

Output Load(A)




* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for $t_{LZC}$, $t_{LZOE}$, $t_{HZOE}$ & $t_{HZC}$)




* Including Scope and Jig Capacitance

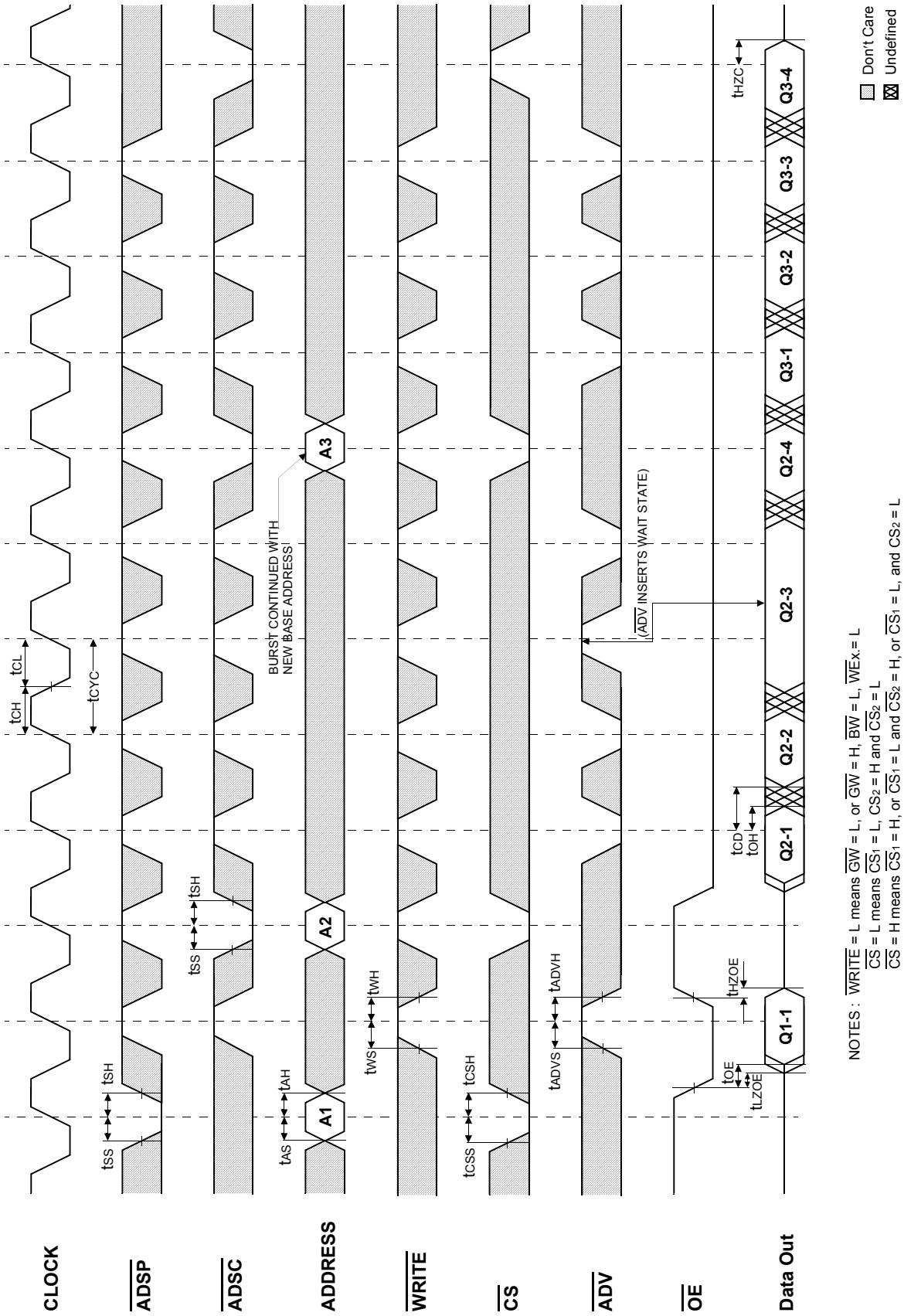
**Fig. 1**

## AC TIMING CHARACTERISTICS($T_A$=0 to 70°C, $V_{DD}$=3.3V+0.3V/-0.165V)

| PARAMETER | Symbol | -65 | | -75 | | UNIT |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| Cycle Time | $t_{CYC}$ | 7.5 | - | 8.5 | - | ns |
| Clock Access Time | $t_{CD}$ | - | 6.5 | - | 7.5 | ns |
| Output Enable to Data Valid | $t_{OE}$ | - | 3.5 | - | 3.5 | ns |
| Clock High to Output Low-Z | $t_{LZC}$ | 0 | - | 0 | - | ns |
| Output Hold from Clock High | $t_{OH}$ | 2.5 | - | 2.5 | - | ns |
| Output Enable Low to Output Low-Z | $t_{LZOE}$ | 0 | - | 0 | - | ns |
| Output Enable High to Output High-Z | $t_{HZOE}$ | - | 3.5 | - | 3.5 | ns |
| Clock High to Output High-Z | $t_{HZC}$ | 2 | 3.5 | 2 | 3.5 | ns |
| Clock High Pulse Width | $t_{CH}$ | 2.5 | - | 3 | - | ns |
| Clock Low Pulse Width | $t_{CL}$ | 2.5 | - | 3 | - | ns |
| Address Setup to Clock High | $t_{AS}$ | 1.5 | - | 2.0 | - | ns |
| Address Status Setup to Clock High | $t_{SS}$ | 1.5 | - | 2.0 | - | ns |
| Data Setup to Clock High | $t_{DS}$ | 1.5 | - | 2.0 | - | ns |
| Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x) | $t_{WS}$ | 1.5 | - | 2.0 | - | ns |
| Address Advance Setup to Clock High | $t_{ADVS}$ | 1.5 | - | 2.0 | - | ns |
| Chip Select Setup to Clock High | $t_{CSS}$ | 1.5 | - | 2.0 | - | ns |
| Address Hold from Clock High | $t_{AH}$ | 0.5 | - | 0.5 | - | ns |
| Address Status Hold from Clock High | $t_{SH}$ | 0.5 | - | 0.5 | - | ns |
| Data Hold from Clock High | $t_{DH}$ | 0.5 | - | 0.5 | - | ns |
| Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x) | $t_{WH}$ | 0.5 | - | 0.5 | - | ns |
| Address Advance Hold from Clock High | $t_{ADVH}$ | 0.5 | - | 0.5 | - | ns |
| Chip Select Hold from Clock High | $t_{CSH}$ | 0.5 | - | 0.5 | - | ns |
| ZZ High to Power Down | $t_{PDS}$ | 2 | - | 2 | - | cycle |
| ZZ Low to Power Up | $t_{PUS}$ | 2 | - | 2 | - | cycle |

**Notes :** 1 The above parameters are also guaranteed at industrial temperature range.
2. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
3. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.
4. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.
5. At any given voltage and temperature, $t_{HZC}$ is less than $t_{LZC}$.

## TIMING WAVEFORM OF READ CYCLE




NOTES : WRITE = L means GW = L, or GW = H, BW = L, WEx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L



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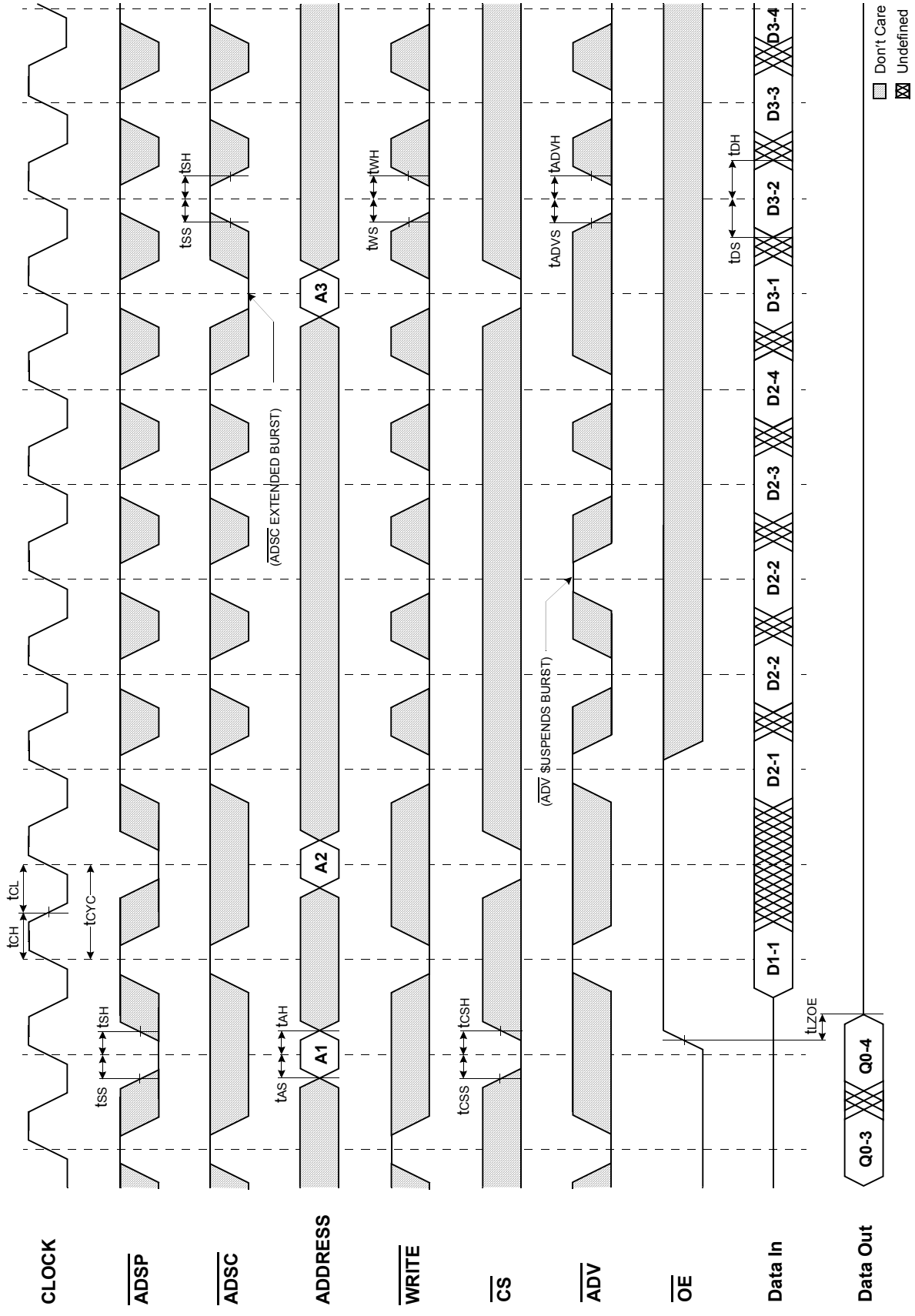
## TIMING WAVEFORM OF WRTE CYCLE



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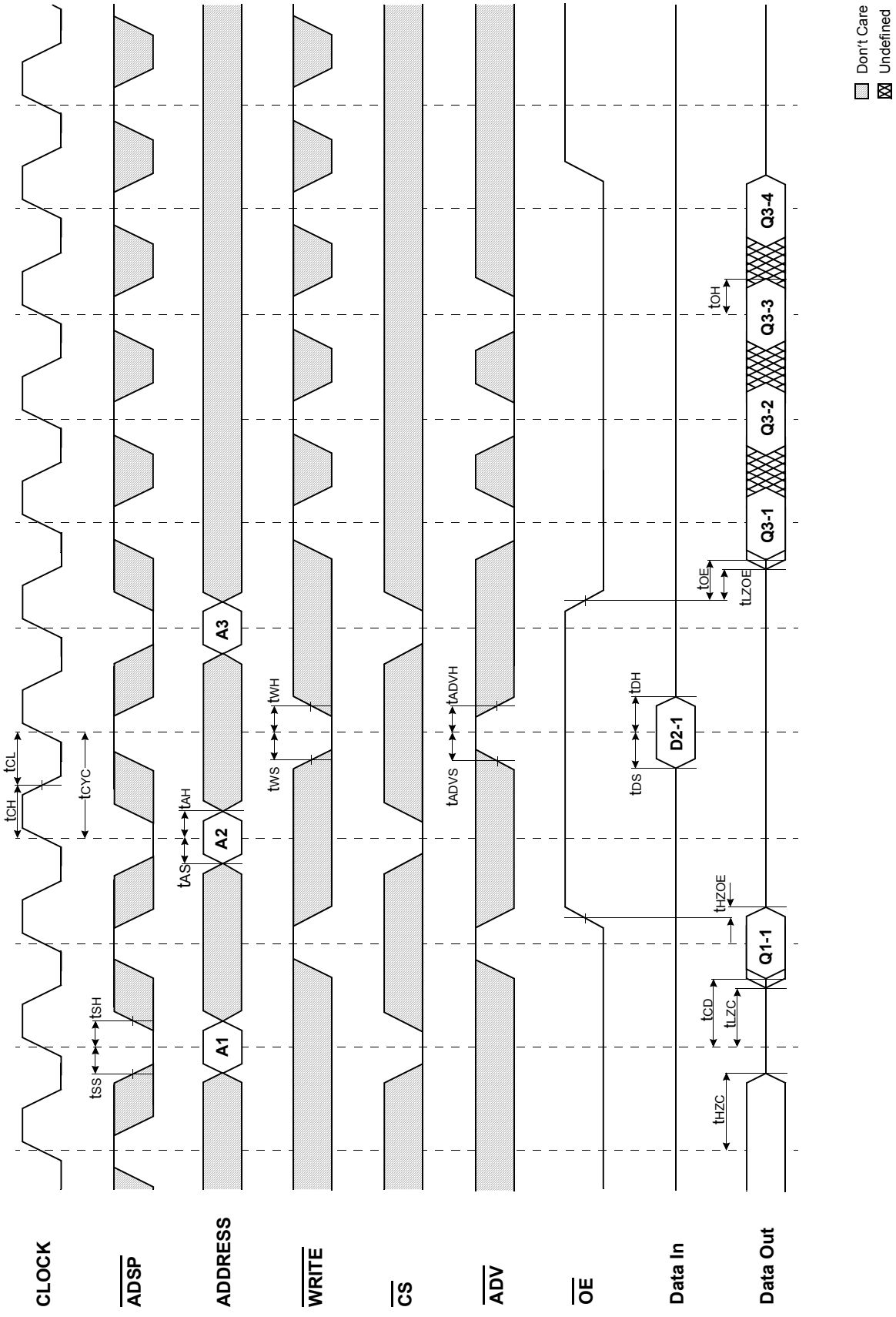
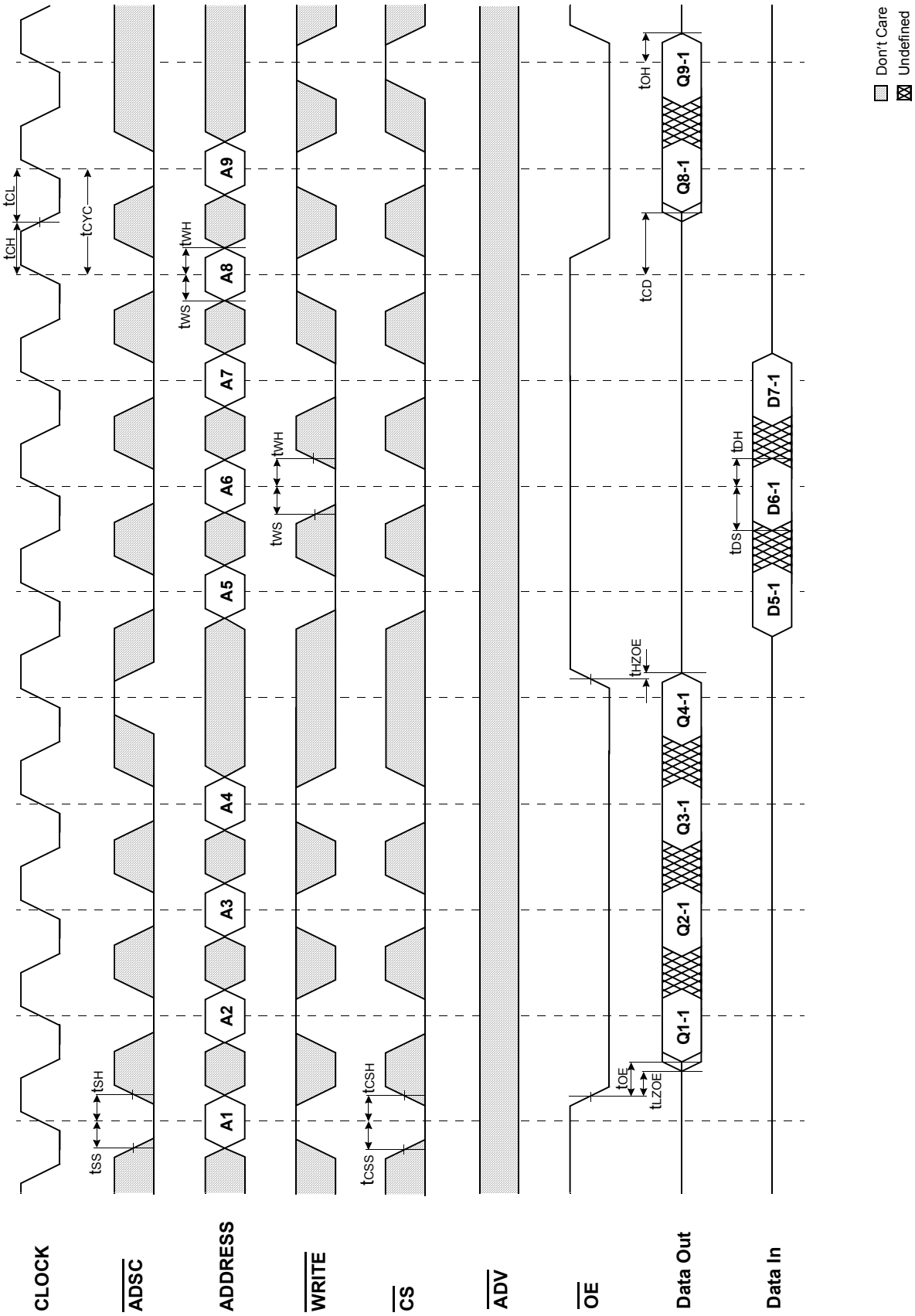
## TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED, ADSC=HIGH)



## TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



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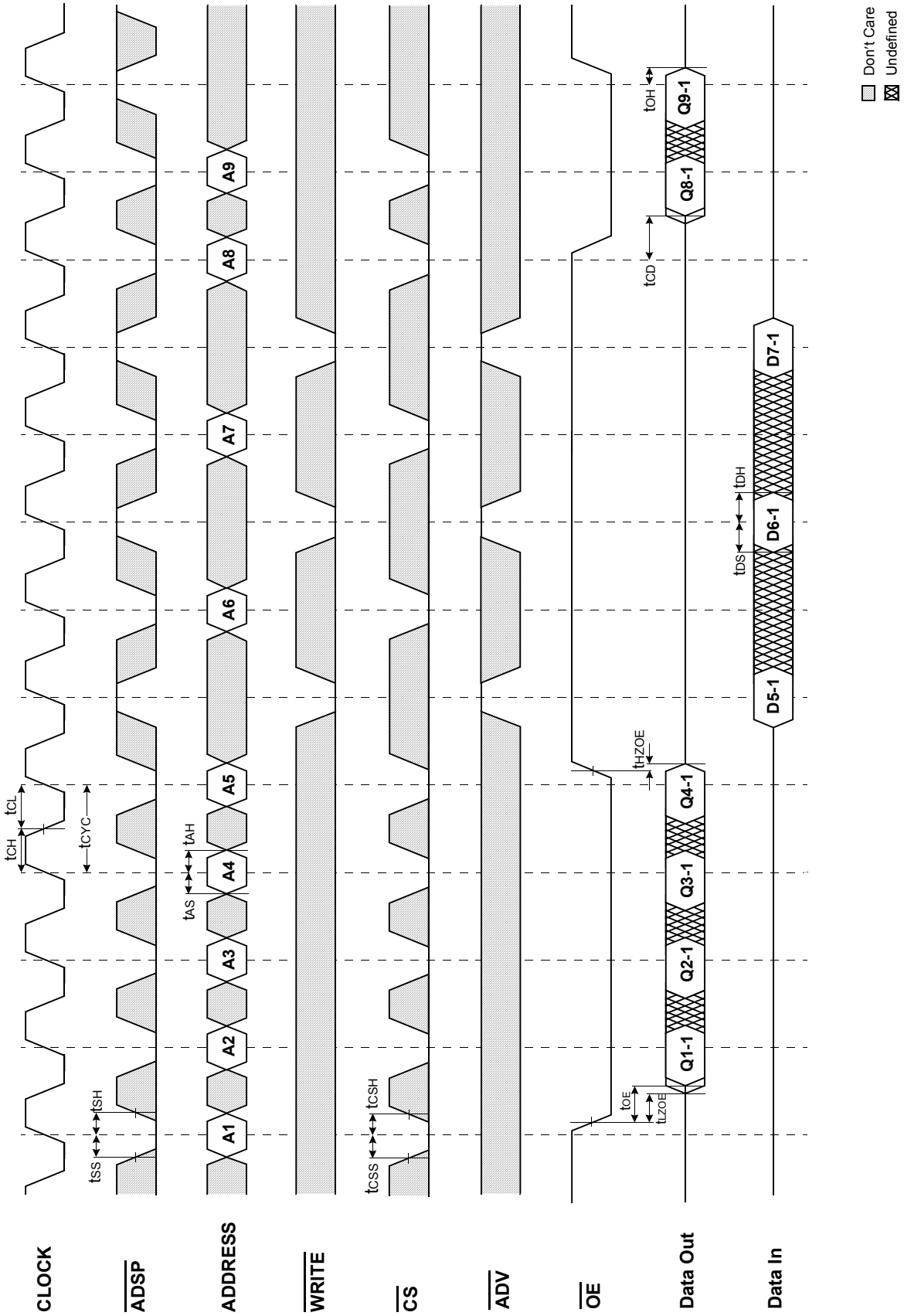
## TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



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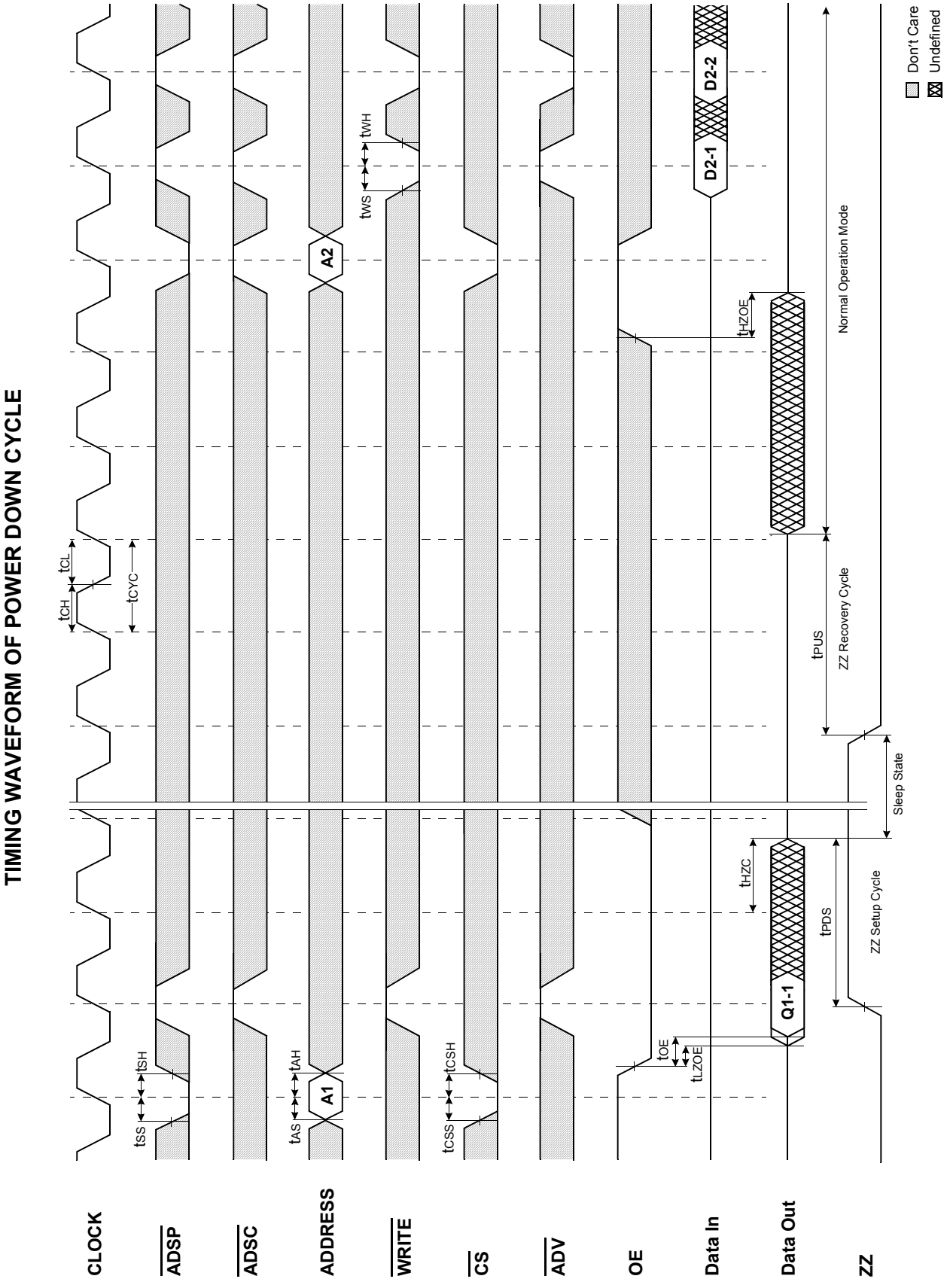
## TIMING WAVEFORM OF POWER DOWN CYCLE



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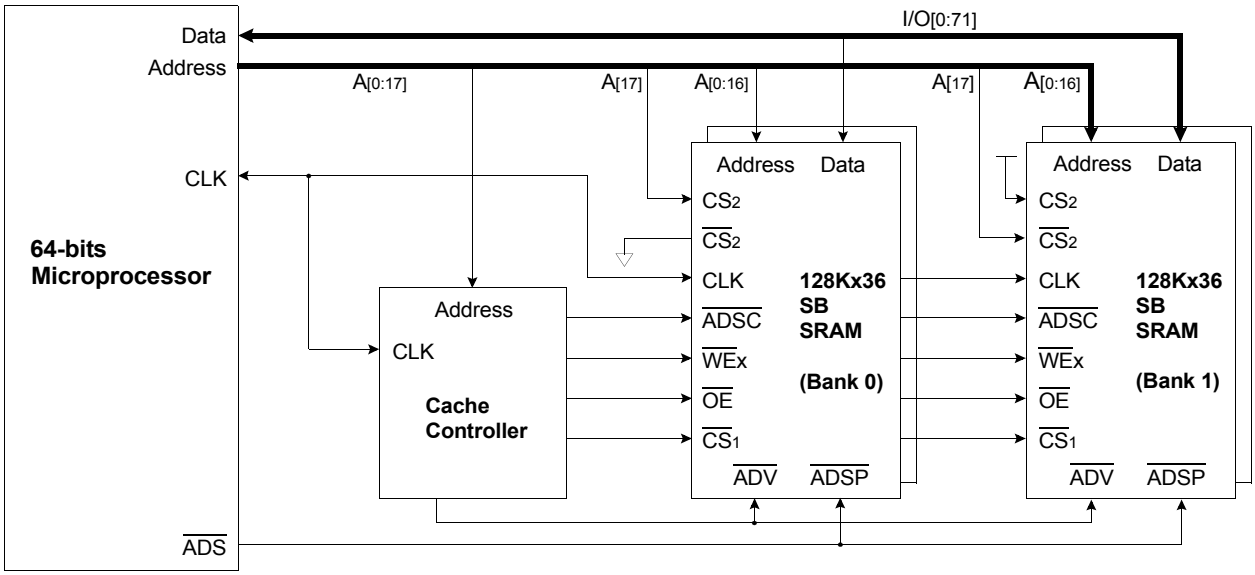
## APPLICATION INFORMATION

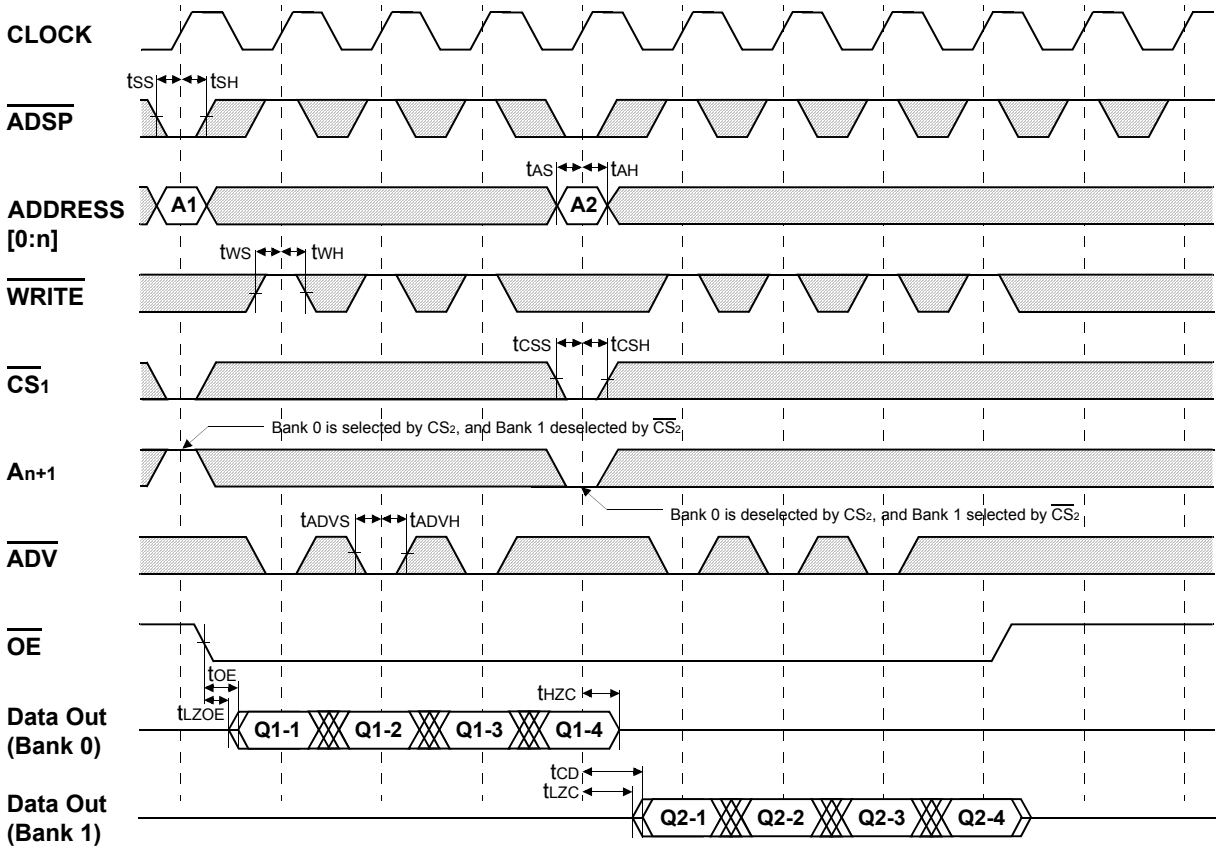
### DEPTH EXPANSION

The Samsung 128Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.




### INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

**($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HiGH)**




***Notes :** n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

Don't Care Undefined



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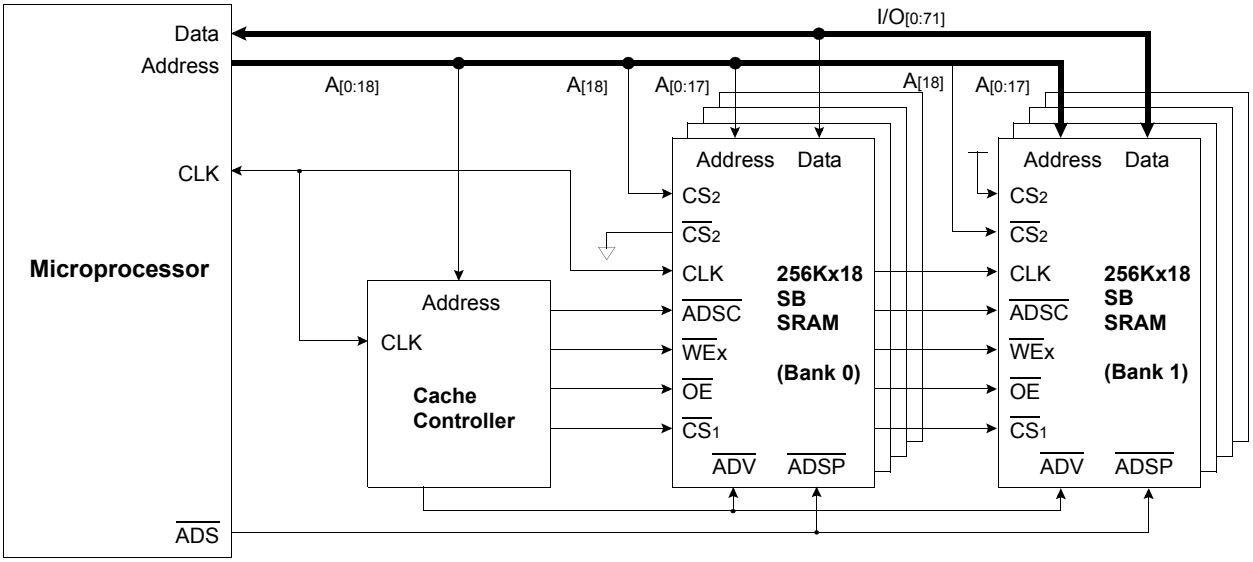
## APPLICATION INFORMATION

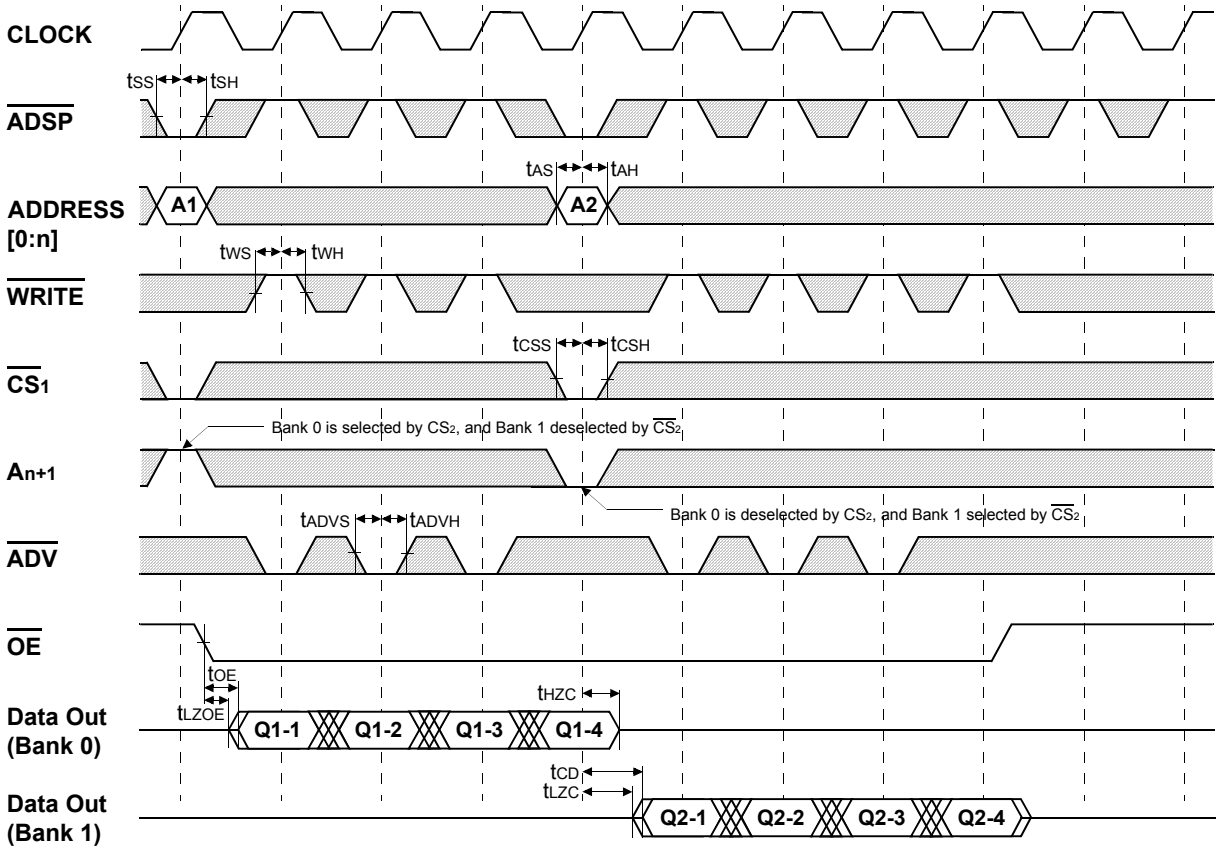
### DEPTH EXPANSION

The Samsung 256Kx18 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 256K depth to 512K depth without extra logic.




## INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

**($\overline{ADSP}$ CONTROLLED , $\overline{ADSC}$=HIGH)**




***Notes :** n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

Don't Care Undefined



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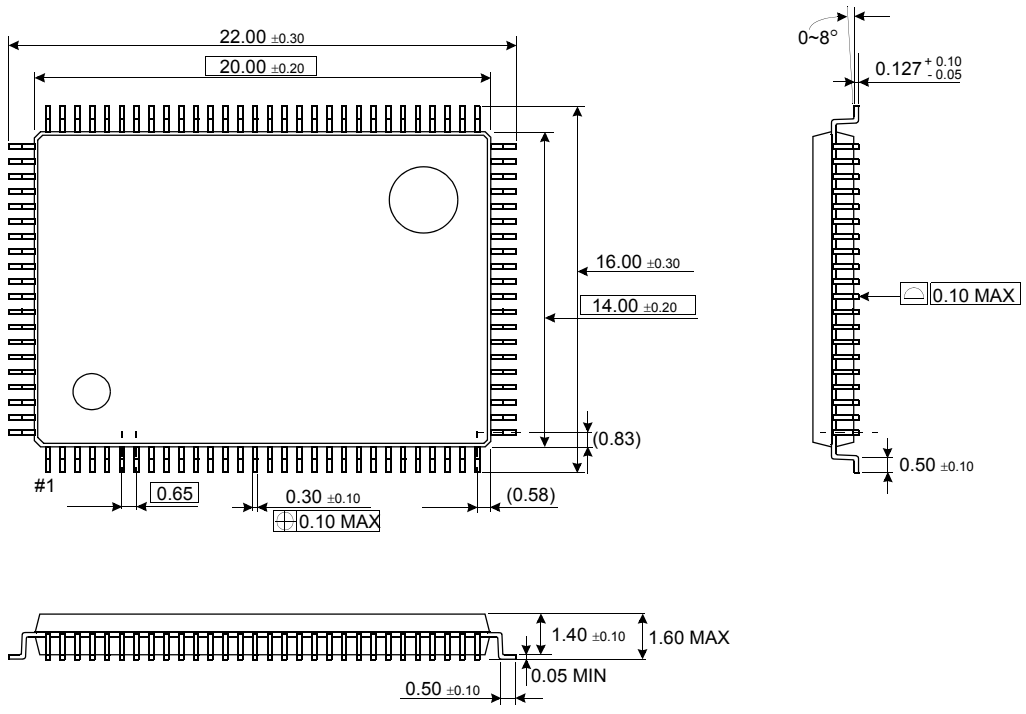
## PACKAGE DIMENSIONS

**100-TQFP-1420A (Lead & Lead-Free)**

Units:millimeters/inches



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