

K7P403622B
K7P401822B

128Kx36 & 256Kx18 SRAM

Document Title

128Kx36 & 256Kx18 Synchronous Pipelined SRAM

Revision History

| <u>Rev. No.</u> | <u>History</u> | <u>Draft Date</u> | <u>Remark</u> |
|------------------------|---|--------------------------|----------------------|
| Rev. 0.0 | - Initial Document. | May. 2002 | Preliminary |
| Rev. 0.1 | - Update Pin Discription. (M2=VDDQ -> M2=VDD) - Add AC characteristics. (250Mhz, 166Mhz) | Oct. 2002 | Preliminary |
| Rev. 0.2 | - Update DC CHARACTERISTICS x36 : IDD25 : TBD -> 370, IDD20 -> 340, IDD16 -> 320. x18 : IDD25 : TBD -> 360, IDD20 -> 330, IDD16 -> 310. | Jan. 2003 | Preliminary |
| Rev. 1.0 | - Final Version | Jun. 2003 | Final |
| Rev. 1.1 | - Add single ended or differential LVTTTL clock Inputs on clock comment. | Jul. 2003 | Final |
| Rev. 1.2 | - Change AC Characteristics tKHQV : 25 - 2.5ns, 20 - 2.7ns | Jul. 2003 | Final |

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

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128Kx36 & 256Kx18 SRAM

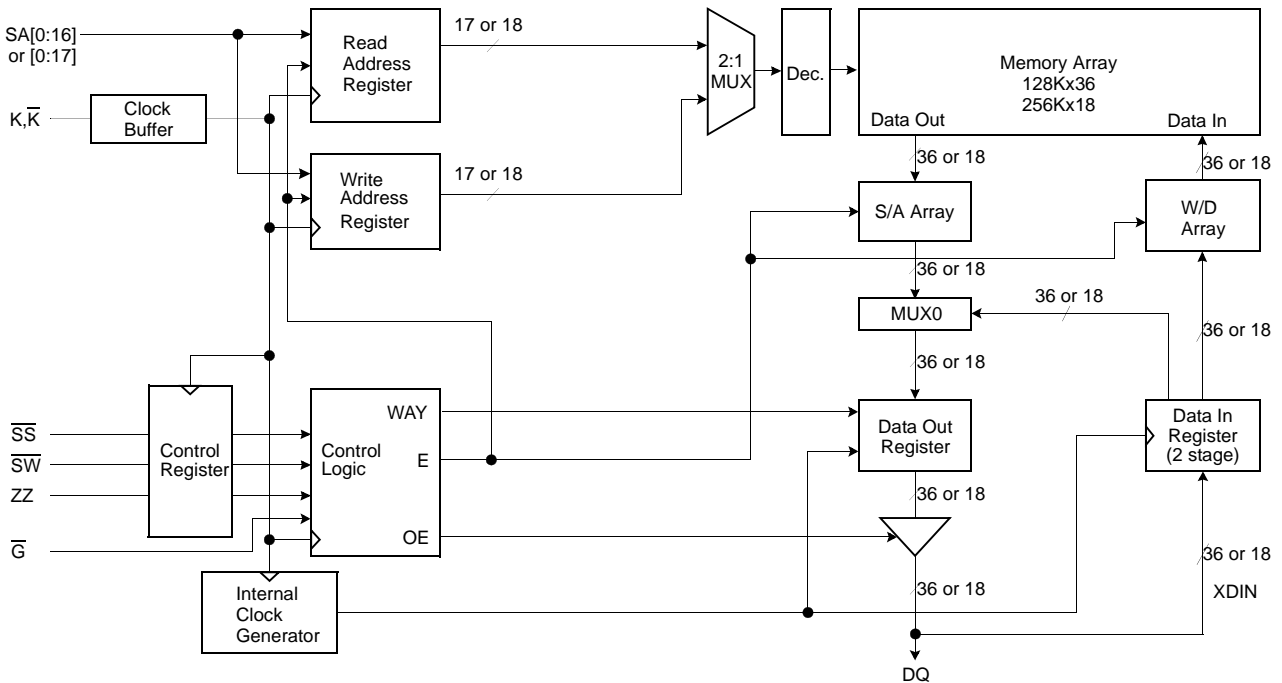
128Kx36 & 256Kx18 Synchronous Pipelined SRAM

FEATURES

- 128Kx36 or 256Kx18 Organizations.
- 3.3V V_{DD}, 2.5/3.3V V_{DDQ}.
- LVTTTL Input and Output Levels.
- Differential, PECL clock / Single ended or differential LVTTTL clock Inputs
- Synchronous Read and Write Operation.
- Registered Input and Registered Output.
- Internal Pipeline Latches to Support Late Write.
- Byte Write Capability(four byte write selects, one for each 9bits)
- Synchronous or Asynchronous Output Enable.
- Power Down Mode via ZZ Signal.
- JTAG Boundary Scan (subset of IEEE std. 1149.1).
- 119(7x17)Pin Ball Grid Array Package(14mmx22mm).

| Organization | Part Number | Maximum Frequency | Access Time |
|--------------|-----------------|-------------------|-------------|
| 128Kx36 | K7P403622B-HC25 | 250MHz | 2.5 |
| 128Kx36 | K7P403622B-HC20 | 200MHz | 2.7 |
| 128Kx36 | K7P403622B-HC16 | 166MHz | 3.0 |
| 256Kx18 | K7P401822B-HC25 | 250MHz | 2.5 |
| 256Kx18 | K7P401822B-HC20 | 200MHz | 2.7 |
| 256Kx18 | K7P401822B-HC16 | 166MHz | 3.0 |

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

| Pin Name | Pin Description | Pin Name | Pin Description |
|--------------|--|------------------|----------------------------|
| K, \bar{K} | Differential Clocks | ZZ | Asynchronous Power Down |
| SAn | Synchronous Address Input | \bar{G} | Asynchronous Output Enable |
| DQn | Bi-directional Data Bus | TCK | JTAG Test Clock |
| \bar{SS} | Synchronous Select | TMS | JTAG Test Mode Select |
| \bar{SW} | Synchronous Global Write Enable | TDI | JTAG Test Data Input |
| \bar{SW}_a | Synchronous Byte a Write Enable | TDO | JTAG Test Data Output |
| \bar{SW}_b | Synchronous Byte b Write Enable | V _{DD} | Power Supply |
| \bar{SW}_c | Synchronous Byte c Write Enable | V _{DDQ} | Output Power Supply |
| \bar{SW}_d | Synchronous Byte d Write Enable | V _{SS} | GND |
| M1, M2 | Read Protocol Mode Pins (M1=V _{SS} , M2=V _{DD}) | NC | No Connection |

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PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7P403622B(128Kx36)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| A | V _{DDQ} | SA ₁₃ | SA ₁₀ | NC | SA ₇ | SA ₄ | V _{DDQ} |
| B | NC | NC | SA ₉ | NC | SA ₈ | NC | NC |
| C | NC | SA ₁₂ | SA ₁₁ | V _{DD} | SA ₆ | SA ₅ | NC |
| D | DQ _{c8} | DQ _{c9} | V _{SS} | NC | V _{SS} | DQ _{b9} | DQ _{b8} |
| E | DQ _{c6} | DQ _{c7} | V _{SS} | \overline{SS} | V _{SS} | DQ _{b7} | DQ _{b6} |
| F | V _{DDQ} | DQ _{c5} | V _{SS} | \overline{G} | V _{SS} | DQ _{b5} | V _{DDQ} |
| G | DQ _{c3} | DQ _{c4} | \overline{SWc} | NC | \overline{SWb} | DQ _{b4} | DQ _{b3} |
| H | DQ _{c1} | DQ _{c2} | V _{SS} | NC | V _{SS} | DQ _{b2} | DQ _{b1} |
| J | V _{DDQ} | V _{DD} | NC | V _{DD} | NC | V _{DD} | V _{DDQ} |
| K | DQ _{d1} | DQ _{d2} | V _{SS} | K | V _{SS} | DQ _{a2} | DQ _{a1} |
| L | DQ _{d3} | DQ _{d4} | \overline{SWd} | \overline{K} | \overline{SWa} | DQ _{a4} | DQ _{a3} |
| M | V _{DDQ} | DQ _{d5} | V _{SS} | \overline{SW} | V _{SS} | DQ _{a5} | V _{DDQ} |
| N | DQ _{d6} | DQ _{d7} | V _{SS} | SA ₁₆ | V _{SS} | DQ _{a7} | DQ _{a6} |
| P | DQ _{d8} | DQ _{d9} | V _{SS} | SA ₀ | V _{SS} | DQ _{a9} | DQ _{a8} |
| R | NC | SA ₁₅ | M ₁ | V _{DD} | M ₂ | SA ₂ | NC |
| T | NC | NC | SA ₁₄ | SA ₁ | SA ₃ | NC | ZZ |
| U | V _{DDQ} | TMS | TDI | TCK | TDO | NC | V _{DDQ} |

K7P401822B(256Kx18)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| A | V _{DDQ} | SA ₁₃ | SA ₁₀ | NC | SA ₇ | SA ₄ | V _{DDQ} |
| B | NC | NC | SA ₉ | NC | SA ₈ | NC | NC |
| C | NC | SA ₁₂ | SA ₁₁ | V _{DD} | SA ₆ | SA ₅ | NC |
| D | DQ _{b1} | NC | V _{SS} | NC | V _{SS} | DQ _{a9} | NC |
| E | NC | DQ _{b2} | V _{SS} | \overline{SS} | V _{SS} | NC | DQ _{a8} |
| F | V _{DDQ} | NC | V _{SS} | \overline{G} | V _{SS} | DQ _{a7} | V _{DDQ} |
| G | NC | DQ _{b3} | \overline{SWb} | NC | NC | NC | DQ _{a6} |
| H | DQ _{b4} | NC | V _{SS} | NC | V _{SS} | DQ _{a5} | NC |
| J | V _{DDQ} | V _{DD} | NC | V _{DD} | NC | V _{DD} | V _{DDQ} |
| K | NC | DQ _{b5} | V _{SS} | K | V _{SS} | NC | DQ _{a4} |
| L | DQ _{b6} | NC | NC | \overline{K} | \overline{SWa} | DQ _{a3} | NC |
| M | V _{DDQ} | DQ _{b7} | V _{SS} | \overline{SW} | V _{SS} | NC | V _{DDQ} |
| N | DQ _{b8} | NC | V _{SS} | SA ₁₆ | V _{SS} | DQ _{a2} | NC |
| P | NC | DQ _{b9} | V _{SS} | SA ₁ | V _{SS} | NC | DQ _{a1} |
| R | NC | SA ₁₅ | M ₁ | V _{DD} | M ₂ | SA ₂ | NC |
| T | NC | SA ₁₇ | SA ₁₄ | NC | SA ₃ | SA ₀ | ZZ |
| U | V _{DDQ} | TMS | TDI | TCK | TDO | NC | V _{DDQ} |

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128Kx36 & 256Kx18 SRAM

FUNCTION DESCRIPTION

The K7P403622B and K7P401822B are 4,718,592 bit Synchronous Pipeline Mode SRAM devices. They are organized as 131,072 words by 36 bits for K7P403622B and 262,144 words by 18 bits for K7P401822B, fabricated using Samsung's advanced CMOS technology.

Single differential PECL level K clocks or Single ended or differential LVTTTL clocks are used to initiate read/write operation and all internal operations are self-timed. At the rising edge of K clock, Addresses, Write Enables, Synchronous Select and Data Ins are registered internally. Data outs are updated from output registers at the next rising edge of K clock. An internal write data buffer allows write data to follow one cycle after addresses and controls. The package is 119(7x17) Ball Grid Array with balls on a 1.27mm pitch.

Read Operation

During read operations, addresses and controls are registered during the first rising edge of K clock and then the internal array is read between first and second edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During consecutive read operations where the address is the same, the data output must be held constant without any glitches. This characteristic is because the SRAM will be read by devices that will operate slower than the SRAM frequency and will require multiple SRAM cycles to perform a single read operation.

Write Operation(Late Write)

During write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write operation are data inputs fully written into SRAM array. Byte write operation is supported using $\overline{SW}[a:d]$ and the timing of $\overline{SW}[a:d]$ is the same as the \overline{SW} signal.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array. Bypass read operation occurs on a byte to byte basis. If only one byte is written during a write operation but a read operation is required on the same address, a partial bypass read operation occurs since the new byte data is from the data in registers while the remaining bytes are from SRAM array.

Sleep Mode

Sleep mode is a low power mode initiated by bringing the asynchronous ZZ pin high. During sleep mode, all other inputs are ignored and outputs are brought to a High-Impedance state. Sleep mode current and output High-Z are guaranteed after the specified sleep mode enable time. During sleep mode the memory array data content is preserved. Sleep mode must not be initiated until after all pending operations have completed, since any pending operation will not be guaranteed once sleep mode is initiated. Normal operations can be resumed by bringing the ZZ pin low, but only after the specified sleep mode recovery time.

Mode Control

There are two mode control select pins (M1 and M2) used to set the proper read protocol. This SRAM supports single clock pipelined operating mode. For proper specified device operation, M1 must be connected to Vss and M2 must be connected to VDD. These mode pins must be set at power-up and must not change during device operation.

Power-Up/Power-Down Supply Voltage Sequence

The following power-up supply voltage sequence is recommended: Vss, VDD, VDDQ, and VIN. VDD and VDDQ can be applied simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: VIN, VREF, VDDQ, VDD, Vss. VDD and VDDQ can be removed simultaneously, as long as VDDQ does not exceed VDD by more than 0.5V during power-down.

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TRUTH TABLE

| K | ZZ | \bar{G} | \bar{SS} | \bar{SW} | \bar{SWa} | \bar{SWb} | \bar{SWc} | \bar{SWd} | DQa | DQb | DQc | DQd | Operation |
|---|----|-----------|------------|------------|-------------|-------------|-------------|-------------|------|------|------|------|-------------------------------|
| X | H | X | X | X | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Power Down Mode. No Operation |
| X | L | H | X | X | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Output Disabled. |
| ↑ | L | L | H | X | X | X | X | X | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Output Disabled. No Operation |
| ↑ | L | L | L | H | X | X | X | X | DOUT | DOUT | DOUT | DOUT | Read Cycle |
| ↑ | L | X | L | L | H | H | H | H | Hi-Z | Hi-Z | Hi-Z | Hi-Z | No Bytes Written |
| ↑ | L | X | L | L | L | H | H | H | DIN | Hi-Z | Hi-Z | Hi-Z | Write first byte |
| ↑ | L | X | L | L | H | L | H | H | Hi-Z | DIN | Hi-Z | Hi-Z | Write second byte |
| ↑ | L | X | L | L | H | H | L | H | Hi-Z | Hi-Z | DIN | Hi-Z | Write third byte |
| ↑ | L | X | L | L | H | H | H | L | Hi-Z | Hi-Z | Hi-Z | DIN | Write fourth byte |
| ↑ | L | X | L | L | L | L | L | L | DIN | DIN | DIN | DIN | Write all bytes |

NOTE : K & \bar{K} are complementary

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit | Note |
|--|--------|-----------------|------|------|
| Core Supply Voltage Relative to Vss | VDD | -0.3 to 4.6 | V | |
| Output Supply Voltage Relative to Vss | VDDQ | VDD | V | |
| Voltage on any I/O pin Relative to Vss | VTERM | -0.3 to VDD+0.3 | V | |
| Output Short-Circuit Current | IOUT | 25 | mA | |
| Operating Temperature | TOPR | 0 to 70 | °C | |
| Storage Temperature | TSTG | -65 to 150 | °C | |

NOTE : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|----------------------|-------|-----|---------|------|------|
| Core Power Supply Voltage | VDD | 3.15 | 3.3 | 3.45 | V | |
| Output Power Supply Voltage (for 2.5V I/O) | VDDQ | 2.375 | 2.5 | 2.9 | V | |
| Output Power Supply Voltage (for 3.3V I/O) | VDDQ | 3.135 | 3.3 | 3.6 | V | |
| Input High Level (for 2.5V I/O) | V _{IH} | 1.7 | - | VDD+0.3 | V | |
| Input Low Level (for 2.5V I/O) | V _{IL} | -0.3 | - | 0.7 | V | |
| Input High Level (for 3.3V I/O) | V _{IH} | 2.0 | - | VDD+0.3 | V | |
| Input Low Level (for 3.3V I/O) | V _{IL} | -0.3 | - | 0.8 | V | |
| PECL Clock Input High Level | V _{IH-PECL} | 2.135 | - | 2.420 | V | 1 |
| PECL Clock Input Low Level | V _{IL-PECL} | 1.490 | - | 1.825 | V | 1 |
| Clock Input Signal Voltage | V _{IN} | -0.3 | - | 3.45 | V | 2 |
| Clock Input Differential Voltage | V _{DIF-CLK} | 0.2 | - | VDD+0.6 | V | 2 |
| Clock Input Common Mode Voltage | V _{CM-CLK} | 1.1 | - | 2.1 | V | 2 |
| Operating Junction Temperature | T _J | 10 | - | 110 | °C | |

NOTE

1. For operation with differential PECL clock inputs.
2. For operation with single ended or differential LVCMOS / LVTTTL clock input.

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PIN CAPACITANCE

| Parameter | Symbol | Test Condition | TYP | Max | Unit |
|-------------------------|------------------|----------------------|-----|-----|------|
| Input Capacitance | C _{IN} | V _{IN} =0V | - | 5 | pF |
| Data Output Capacitance | C _{OUT} | V _{OUT} =0V | - | 7 | pF |

NOTE : Periodically sampled and not 100% tested. (TA=25°C, f=1MHz)

DC CHARACTERISTICS

| Parameter | Symbol | Min | Max | Unit | Note |
|--|---|-----------------|-------------------|------|------|
| Average Power Supply Operating Current-x36 (V _{IN} =V _{IH} or V _{IL} , ZZ & SS=V _{IL}) | I _{DD25} I _{DD20} I _{DD16} | - | 370 340 320 | mA | 1, 2 |
| Average Power Supply Operating Current-x18 (V _{IN} =V _{IH} or V _{IL} , ZZ & SS=V _{IL}) | I _{DD25} I _{DD20} I _{DD16} | - | 360 330 310 | mA | 1, 2 |
| Power Supply Standby Current (V _{IN} =V _{IH} or V _{IL} , ZZ=V _{IH}) | I _{SB} | - | 120 | mA | 1 |
| Input Leakage Current (V _{IN} =V _{SS} or V _{DD}) | I _{LI} | -1 | 1 | μA | |
| Output Leakage Current (V _{OUT} =V _{SS} or V _{DDQ} , ZZ=V _{IH} , \bar{G} =V _{IH}) | I _{LO} | -1 | 1 | μA | |
| Output High Voltage(I _{OH} =-4mA) for V _{DDQ} =3.3V | V _{OH1} | 2.4 | V _{DDQ} | V | |
| Output High Voltage(I _{OH} =-4mA) for V _{DDQ} =2.5V | V _{OH2} | 2.0 | | | |
| Output Low Voltage(I _{OL} =4mA) | V _{OL} | V _{SS} | 0.4 | V | |

NOTE :1. Minimum cycle. I_{OUT}=0mA.
2. 50% read cycles.

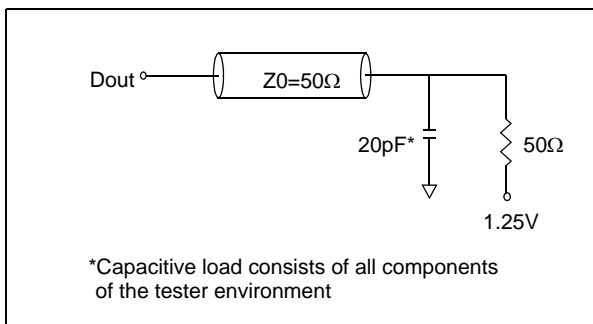
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128Kx36 & 256Kx18 SRAM

AC TEST CONDITIONS

| Parameter | Symbol | Value | Unit |
|--------------------------------------|----------------------------------|-------------|------|
| Core Power Supply Voltage | V _{DD} | 3.15~3.45 | V |
| Output Power Supply Voltage | V _{DDQ} | 2.4~2.6 | V |
| Input High/Low Level | V _{IH} /V _{IL} | 1.7/0.7 | V |
| Clock Input High/Low Level(PECL) | V _{IH} /V _{IL} | 2.4/1.5 | V |
| Input Rise/Fall Time | T _R /T _F | 1.0/1.0 | ns |
| Clock Input Rise/Fall Time(PECL) | T _R /T _F | 1.0/1.0 | ns |
| Input and Out Timing Reference Level | | 1.25 | V |
| Clock Input Timing Reference Level | | Cross Point | V |

AC TEST OUTPUT LOAD



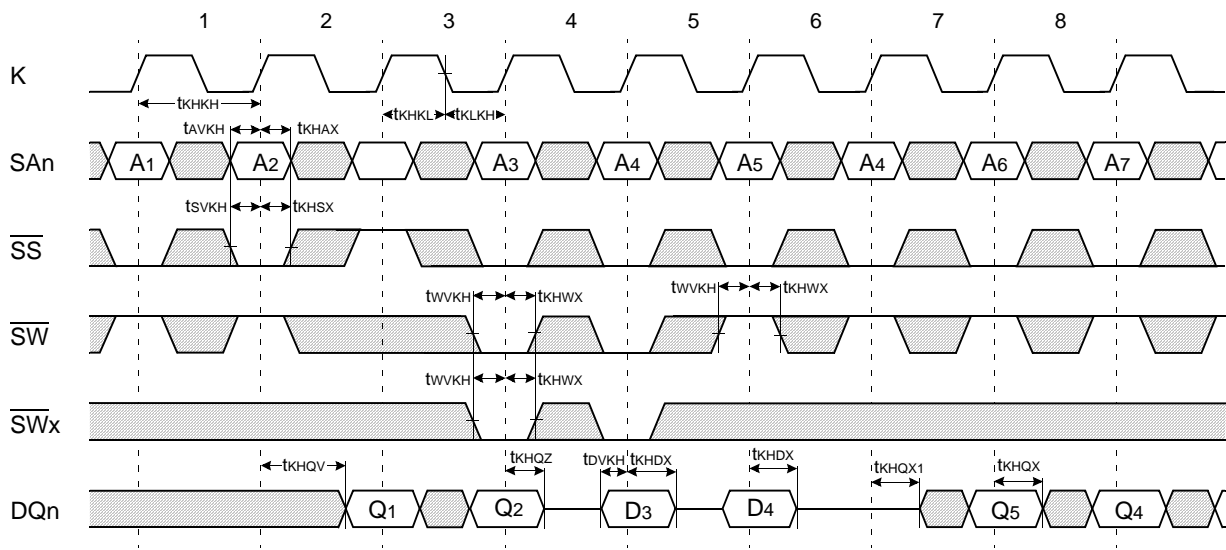
AC CHARACTERISTICS

| Parameter | Symbol | -25 | | -20 | | -16 | | Unit | Note |
|---|--------------------|-----|-----|-----|-----|-----|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| Clock Cycle Time | t _{KHKH} | 4.0 | - | 5.0 | - | 6.0 | - | ns | |
| Clock High Pulse Width | t _{KHKL} | 1.4 | - | 1.5 | - | 1.5 | - | ns | |
| Clock Low Pulse Width | t _{KLKH} | 1.4 | - | 1.5 | - | 1.5 | - | ns | |
| Clock High to Output Valid | t _{KHQV} | - | 2.5 | - | 2.7 | - | 3.0 | ns | |
| Clock High to Output Hold | t _{KHQX} | 0.5 | - | 0.5 | - | 0.5 | - | ns | |
| Address Setup Time | t _{AVKH} | 0.4 | - | 0.5 | - | 0.5 | - | ns | |
| Address Hold Time | t _{KHAX} | 0.7 | - | 1.0 | - | 1.0 | - | ns | |
| Write Data Setup Time | t _{DVKH} | 0.4 | - | 0.5 | - | 0.5 | - | ns | |
| Write Data Hold Time | t _{KHDX} | 0.7 | - | 1.0 | - | 1.0 | - | ns | |
| \overline{SW} , $\overline{SW}[a:d]$ Setup Time | t _{WVKH} | 0.4 | - | 0.5 | - | 0.5 | - | ns | |
| \overline{SW} , $\overline{SW}[a:d]$ Hold Time | t _{KHWX} | 0.7 | - | 1.0 | - | 1.0 | - | ns | |
| \overline{SS} Setup Time | t _{SVKH} | 0.4 | - | 0.5 | - | 0.5 | - | ns | |
| \overline{SS} Hold Time | t _{KHSX} | 0.7 | - | 1.0 | - | 1.0 | - | ns | |
| Clock High to Output Hi-Z | t _{KHQZ} | - | 2.3 | - | 2.5 | - | 3.0 | ns | |
| Clock High to Output Low-Z | t _{KHQX1} | 0.5 | - | 0.5 | - | 0.5 | - | ns | |
| \overline{G} High to Output High-Z | t _{GHQZ} | - | 2.3 | - | 2.5 | - | 3.0 | ns | |
| \overline{G} Low to Output Low-Z | t _{GLQX} | 0.5 | - | 0.5 | - | 0.5 | - | ns | |
| \overline{G} Low to Output Valid | t _{GLQV} | - | 2.3 | - | 2.5 | - | 3.0 | ns | |
| ZZ High to Power Down(Sleep Time) | t _{ZZE} | - | 15 | - | 15 | - | 15 | ns | |
| ZZ Low to Recovery(Wake-up Time) | t _{ZZR} | - | 20 | - | 20 | - | 20 | ns | |

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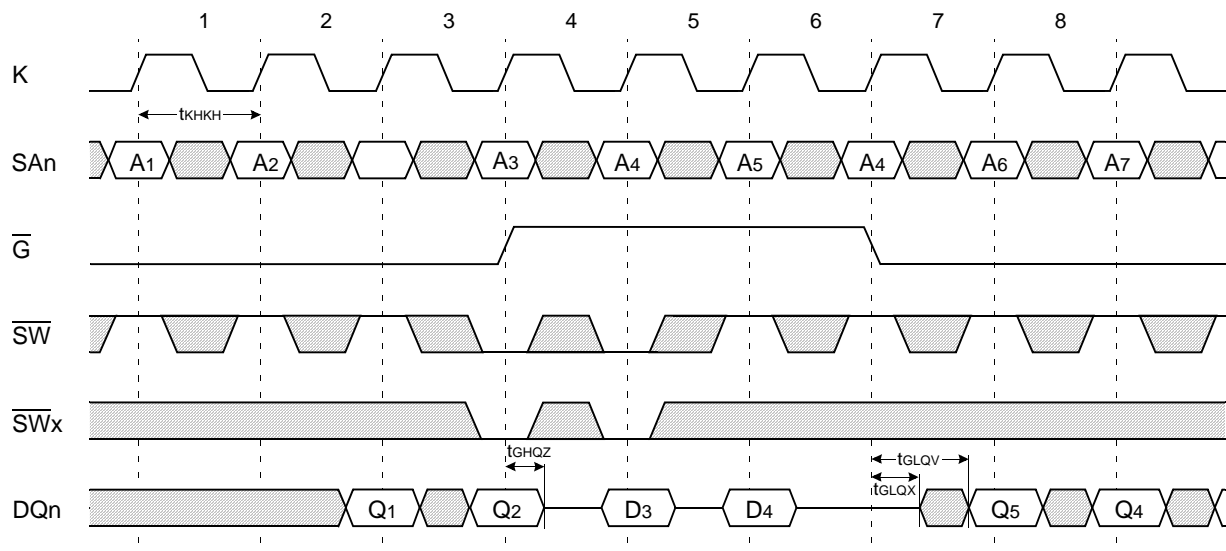
TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES (\overline{SS} Controlled, \overline{G} =Low)



NOTE

1. D₃ is the input data written in memory location A₃.
2. Q₄ is the output data read from the write data buffer(not from the cell array), as a result of address A₄ being a match from the last write cycle address.

TIMING WAVEFORMS OF NORMAL ACTIVE CYCLES (\overline{G} Controlled, \overline{SS} =Low)



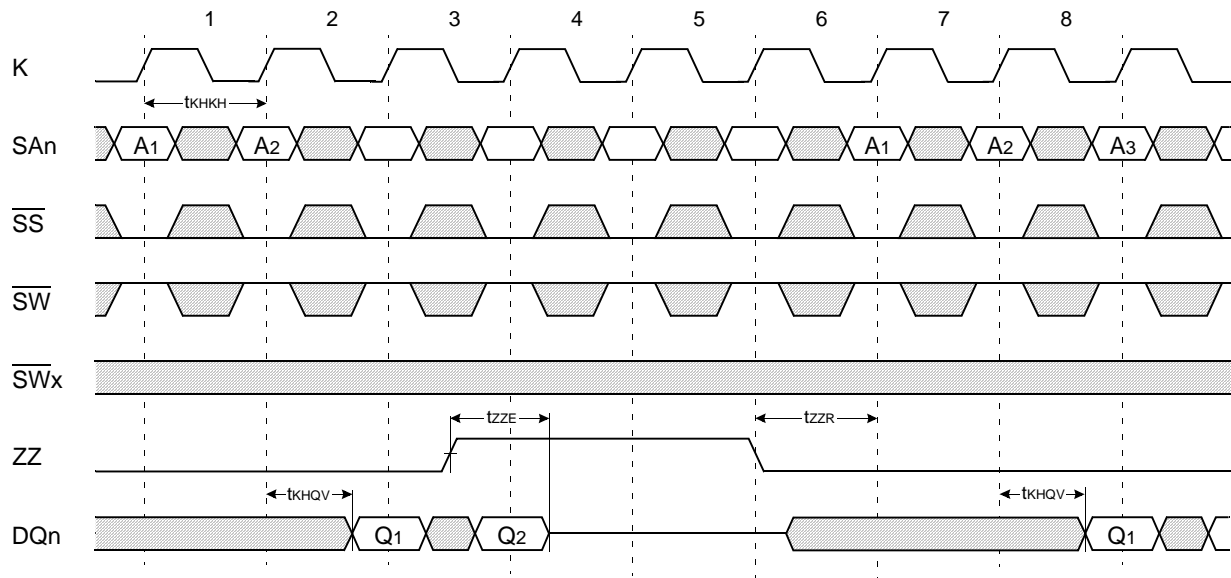
NOTE

1. D₃ is the input data written in memory location A₃.
2. Q₄ is the output data read from the write data buffer(not from the cell array), as a result of address A₄ being a match from the last write cycle address.

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TIMING WAVEFORMS OF STANDBY CYCLES



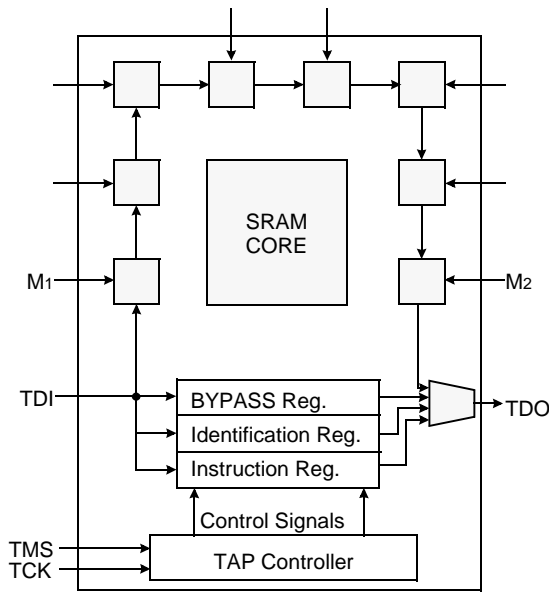
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IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to Vss to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and therefore can be left unconnected. But they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



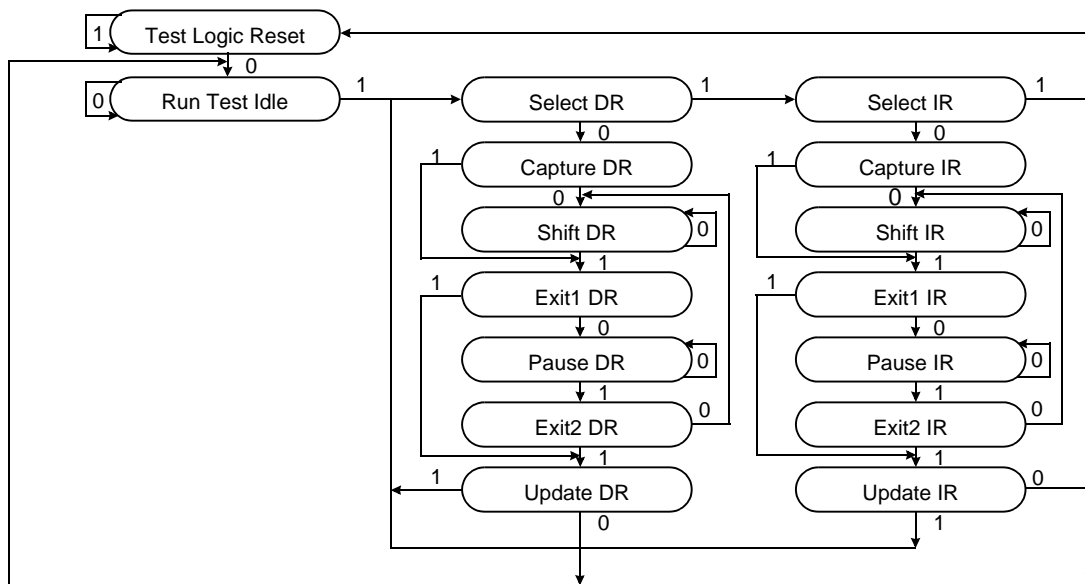
JTAG Instruction Coding

| IR2 | IR1 | IR0 | Instruction | TDO Output | Notes |
|-----|-----|-----|-------------|-------------------------|-------|
| 0 | 0 | 0 | SAMPLE-Z | Boundary Scan Register | 1 |
| 0 | 0 | 1 | IDCODE | Identification Register | 2 |
| 0 | 1 | 0 | SAMPLE-Z | Boundary Scan Register | 1 |
| 0 | 1 | 1 | BYPASS | Bypass Register | 3 |
| 1 | 0 | 0 | SAMPLE | Boundary Scan Register | 4 |
| 1 | 0 | 1 | BYPASS | Bypass Register | 3 |
| 1 | 1 | 0 | BYPASS | Bypass Register | 3 |
| 1 | 1 | 1 | BYPASS | Bypass Register | 3 |

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not places DQs in Hi-Z.

TAP Controller State Diagram



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SCAN REGISTER DEFINITION

| Part | Instruction Register | Bypass Register | ID Register | Boundary Scan |
|---------|----------------------|-----------------|-------------|---------------|
| 128Kx36 | 3 bits | 1 bits | 32 bits | 70 bits |
| 256Kx18 | 3 bits | 1 bits | 32 bits | 51 bits |

ID REGISTER DEFINITION

| Part | Revision Number (31:28) | Part Configuration (27:18) | Vendor Definition (17:12) | Samsung JEDEC Code (11: 1) | Start Bit(0) |
|---------|-------------------------|----------------------------|---------------------------|----------------------------|--------------|
| 128Kx36 | 0000 | 00101 00100 | XXXXXX | 00001001110 | 1 |
| 256Kx18 | 0000 | 00110 00011 | XXXXXX | 00001001110 | 1 |

BOUNDARY SCAN EXIT ORDER(x36)

| | | | | | | |
|----|----|------------------|--|------------------|----|----|
| 36 | 3B | SA ₉ | | SA ₈ | 5B | 35 |
| 37 | 2B | NC | | NC | 6B | 34 |
| 38 | 3A | SA ₁₀ | | SA ₇ | 5A | 33 |
| 39 | 3C | SA ₁₁ | | SA ₆ | 5C | 32 |
| 40 | 2C | SA ₁₂ | | SA ₅ | 6C | 31 |
| 41 | 2A | SA ₁₃ | | SA ₄ | 6A | 30 |
| 42 | 2D | DQ _{c9} | | DQ _{b9} | 6D | 29 |
| 43 | 1D | DQ _{c8} | | DQ _{b8} | 7D | 28 |
| 44 | 2E | DQ _{c7} | | DQ _{b7} | 6E | 27 |
| 45 | 1E | DQ _{c6} | | DQ _{b6} | 7E | 26 |
| 46 | 2F | DQ _{c5} | | DQ _{b5} | 6F | 25 |
| 47 | 2G | DQ _{c4} | | DQ _{b4} | 6G | 24 |
| 48 | 1G | DQ _{c3} | | DQ _{b3} | 7G | 23 |
| 49 | 2H | DQ _{c2} | | DQ _{b2} | 6H | 22 |
| 50 | 1H | DQ _{c1} | | DQ _{b1} | 7H | 21 |
| 51 | 3G | \overline{SWc} | | \overline{SWb} | 5G | 20 |
| 52 | 4D | NC | | \overline{G} | 4F | 19 |
| 53 | 4E | \overline{SS} | | K | 4K | 18 |
| 54 | 4G | NC | | \overline{K} | 4L | 17 |
| 55 | 4H | NC | | \overline{SWa} | 5L | 16 |
| 56 | 4M | \overline{SW} | | DQ _{a1} | 7K | 15 |
| 57 | 3L | \overline{SWd} | | DQ _{a2} | 6K | 14 |
| 58 | 1K | DQ _{d1} | | DQ _{a3} | 7L | 13 |
| 59 | 2K | DQ _{d2} | | DQ _{a4} | 6L | 12 |
| 60 | 1L | DQ _{d3} | | DQ _{a5} | 6M | 11 |
| 61 | 2L | DQ _{d4} | | DQ _{a6} | 7N | 10 |
| 62 | 2M | DQ _{d5} | | DQ _{a7} | 6N | 9 |
| 63 | 1N | DQ _{d6} | | DQ _{a8} | 7P | 8 |
| 64 | 2N | DQ _{d7} | | DQ _{a9} | 6P | 7 |
| 65 | 1P | DQ _{d8} | | ZZ | 7T | 6 |
| 66 | 2P | DQ _{d9} | | SA ₃ | 5T | 5 |
| 67 | 3T | SA ₁₄ | | SA ₂ | 6R | 4 |
| 68 | 2R | SA ₁₅ | | SA ₁ | 4T | 3 |
| 69 | 4N | SA ₁₆ | | SA ₀ | 4P | 2 |
| 70 | 3R | M ₁ | | M ₂ | 5R | 1 |

BOUNDARY SCAN EXIT ORDER(x18)

| | | | | | | |
|----|----|-------------------|--|------------------|----|----|
| 26 | 3B | SA ₉ | | SA ₈ | 5B | 25 |
| 27 | 2B | NC | | NC | 6B | 24 |
| 28 | 3A | SA ₁₀ | | SA ₇ | 5A | 23 |
| 29 | 3C | SA ₁₁ | | SA ₆ | 5C | 22 |
| 30 | 2C | SA ₁₂ | | SA ₅ | 6C | 21 |
| 31 | 2A | SA ₁₃ | | SA ₄ | 6A | 20 |
| | | | | DQ _{a9} | 6D | 19 |
| 32 | 1D | DQ _{b1} | | | | |
| 33 | 2E | DQ _{b2} | | | | |
| | | | | DQ _{a8} | 7E | 18 |
| | | | | DQ _{a7} | 6F | 17 |
| 34 | 2G | DQ _{b3} | | | | |
| | | | | DQ _{a6} | 7G | 16 |
| | | | | DQ _{a5} | 6H | 15 |
| 35 | 1H | $\overline{DQb4}$ | | | | |
| 36 | 3G | \overline{SWb} | | | | |
| 37 | 4D | NC | | \overline{G} | 4F | 14 |
| 38 | 4E | \overline{SS} | | K | 4K | 13 |
| 39 | 4G | NC | | \overline{K} | 4L | 12 |
| 40 | 4H | NC | | \overline{SWa} | 5L | 11 |
| 41 | 4M | \overline{SW} | | DQ _{a4} | 7K | 10 |
| | | | | | | |
| | | | | | | |
| 42 | 2K | DQ _{b5} | | DQ _{a3} | 6L | 9 |
| 43 | 1L | DQ _{b6} | | | | |
| | | | | | | |
| 44 | 2M | DQ _{b7} | | DQ _{a2} | 6N | 8 |
| 45 | 1N | DQ _{b8} | | DQ _{a1} | 7P | 7 |
| | | | | | | |
| | | | | ZZ | 7T | 6 |
| 46 | 2P | DQ _{b9} | | SA ₃ | 5T | 5 |
| 47 | 3T | SA ₁₄ | | SA ₂ | 6R | 4 |
| 48 | 2R | SA ₁₅ | | | | |
| 49 | 4N | SA ₁₆ | | SA ₁ | 4P | 3 |
| 50 | 2T | SA ₁₇ | | SA ₀ | 6T | 2 |
| 51 | 3R | M ₁ | | M ₂ | 5R | 1 |

NOTE : 1. Pins 6B and 2B are no connection pin to internal chip. These pins are place holders for 8Mb and 16Mb parts and the scanned data are fixed to "0" for this 4M parts.

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K7P401822B

128Kx36 & 256Kx18 SRAM

JTAG DC OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|--|-----------------|-----------------|-----|----------------------|------|------|
| Power Supply Voltage | V _{DD} | 3.15 | 3.3 | 3.45 | V | |
| Input High Level | V _{IH} | 1.7 | - | V _{DD} +0.3 | V | |
| Input Low Level | V _{IL} | -0.3 | - | 0.8 | V | |
| Output High Voltage(I _{OH} =-2mA) | V _{OH} | 2.1 | - | V _{DD} | V | |
| Output Low Voltage(I _{OL} =2mA) | V _{OL} | V _{SS} | - | 0.2 | V | |

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

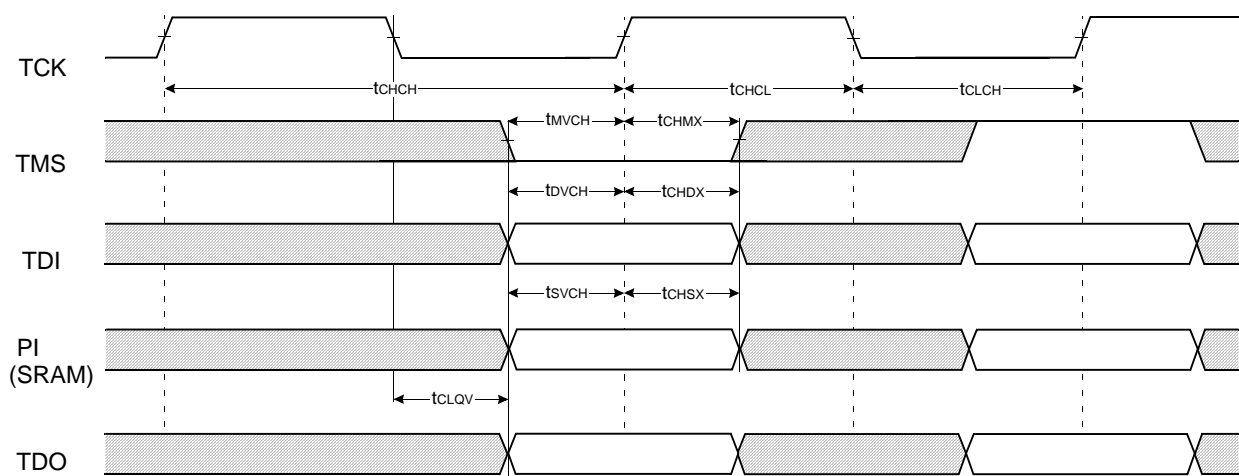
| Parameter | Symbol | Min | Unit | Note |
|---|----------------------------------|---------|------|------|
| Input High/Low Level | V _{IH} /V _{IL} | 2.5/0.0 | V | |
| Input Rise/Fall Time | T _R /T _F | 1.0/1.0 | ns | |
| Input and Output Timing Reference Level | | 1.25 | V | 1 |

NOTE : 1. See SRAM AC test output load on page 7.

JTAG AC Characteristics

| Parameter | Symbol | Min | Max | Unit | Note |
|---------------------------|-------------------|-----|-----|------|------|
| TCK Cycle Time | t _{CHCH} | 50 | - | ns | |
| TCK High Pulse Width | t _{CHCL} | 20 | - | ns | |
| TCK Low Pulse Width | t _{CLCH} | 20 | - | ns | |
| TMS Input Setup Time | t _{MVCH} | 5 | - | ns | |
| TMS Input Hold Time | t _{CHMX} | 5 | - | ns | |
| TDI Input Setup Time | t _{DVCH} | 5 | - | ns | |
| TDI Input Hold Time | t _{CHDX} | 5 | - | ns | |
| SRAM Input Setup Time | t _{SVCH} | 5 | - | ns | |
| SRAM Input Hold Time | t _{CHSX} | 5 | - | ns | |
| Clock Low to Output Valid | t _{CLQV} | 0 | 10 | ns | |

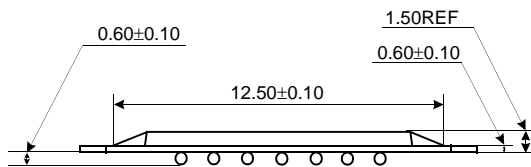
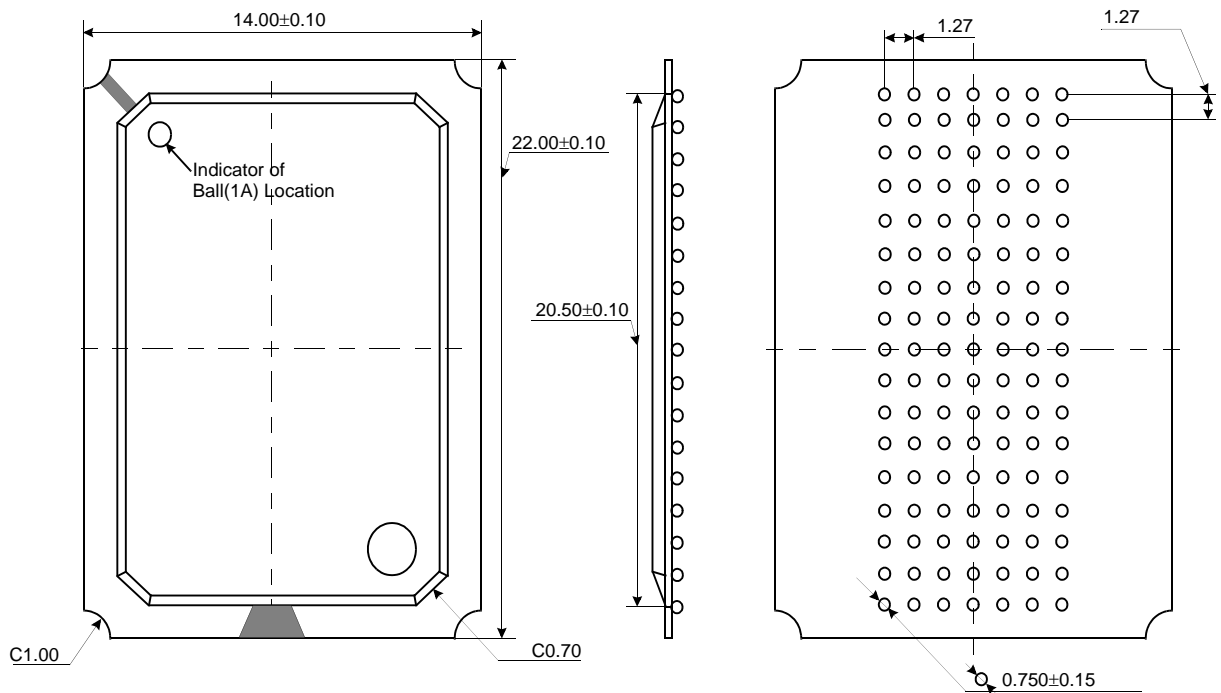
JTAG TIMING DIAGRAM



**K7P403622B
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128Kx36 & 256Kx18 SRAM

119 BGA PACKAGE DIMENSIONS



NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

119 BGA PACKAGE THERMAL CHARACTERISTICS

| Parameter | Symbol | Thermal Resistance | Unit | Note |
|-------------------------|----------|--------------------|------|------|
| Junction to Ambient | Theta_JA | TBD | °C/W | |
| Junction to Case | Theta_JC | TBD | °C/W | |
| Junction to Solder Ball | Theta_JB | TBD | °C/W | |

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D \times \text{Theta_JA}$.