Unbuffered 4Mx64 DIMM

(4Mx16 base)

Revision 0.0

Jan. 1999

Revision History

Version 0.0 (Jan. 1999)

• The 4th generation of 64M DRAM components are applied to this module.

M366F040(8)4CT1-C EDO Mode without buffer

4M x 64 DRAM DIMM Using 4Mx16, 4K & 8K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung M366F040(8)4CT1-C is a 4Mx64bits Dynamic RAM high density memory module. The Samsung M366F040(8)4CT1-C consists of four CMOS 4Mx16bits DRAMs in TSOP 400mil packages and one 2K EEPROM for SPD in 8-pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The M366F040(8)4CT1-C is a Dual In-line Memory Module and is intended for mounting into 168 pin edge connector sockets.

PERFORMANCE RANGE

Speed	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
-C50	50ns	13ns	84ns	20ns
-C60	60ns	15ns	104ns	25ns

FEATURES

- Part Identification

Part number	PKG	Ref.	CBR Ref.	ROR Ref.
M366F0404CT1-C	TSOP	4K	4K/64ms	
M366F0484CT1-C	TSOP	8K	4K/64ms	8K/64ms

- New JEDEC standard proposal without buffer
- Serial Presence Detect with EEPROM
- Extended Data Out Mode Operation
- $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- Single +3.3V±0.3V power supply
- PCB : Height(1000mil), single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	Vss	29	$\overline{CAS1}$	57	DQ18	85	Vss	113	$\overline{CAS5}$	141	DQ50
2	DQ0	30	$\overline{RAS0}$	58	DQ19	86	DQ32	114	*$\overline{RAS1}$	142	DQ51
3	DQ1	31	$\overline{OE0}$	59	Vcc	87	DQ33	115	DU	143	Vcc
4	DQ2	32	Vss	60	DQ20	88	DQ34	116	Vss	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	Vcc	34	A2	62	DU	90	Vcc	118	A3	146	DU
7	DQ4	35	A4	63	NC	91	DQ36	119	A5	147	NC
8	DQ5	36	A6	64	Vss	92	DQ37	120	A7	148	Vss
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	A11	150	DQ54
11	DQ8	39	A12	67	DQ23	95	DQ40	123	*A13	151	DQ55
12	Vss	40	Vcc	68	Vss	96	Vss	124	Vcc	152	Vss
13	DQ9	41	Vcc	69	DQ24	97	DQ41	125	DU	153	DQ56
14	DQ10	42	DU	70	DQ25	98	DQ42	126	DU	154	DQ57
15	DQ11	43	Vss	71	DQ26	99	DQ43	127	Vss	155	DQ58
16	DQ12	44	$\overline{OE2}$	72	DQ27	100	DQ44	128	DU	156	DQ59
17	DQ13	45	$\overline{RAS2}$	73	Vcc	101	DQ45	129	*$\overline{RAS3}$	157	Vcc
18	Vcc	46	$\overline{CAS2}$	74	DQ28	102	Vcc	130	$\overline{CAS6}$	158	DQ60
19	DQ14	47	$\overline{CAS3}$	75	DQ29	103	DQ46	131	$\overline{CAS7}$	159	DQ61
20	DQ15	48	W2	76	DQ30	104	DQ47	132	DU	160	DQ62
21	*CB0	49	Vcc	77	DQ31	105	*CB4	133	Vcc	161	DQ63
22	*CB1	50	NC	78	Vss	106	*CB5	134	NC	162	Vss
23	Vss	51	NC	79	NC	107	Vss	135	NC	163	NC
24	NC	52	*CB2	80	NC	108	NC	136	*CB6	164	NC
25	NC	53	*CB3	81	NC	109	NC	137	*CB7	165	SA0
26	Vcc	54	Vss	82	SDA	110	Vcc	138	Vss	166	SA1
27	$\overline{W0}$	55	DQ16	83	SCL	111	DU	139	DQ48	167	SA2
28	$\overline{CAS0}$	56	DQ17	84	Vcc	112	$\overline{CAS4}$	140	DQ49	168	Vcc

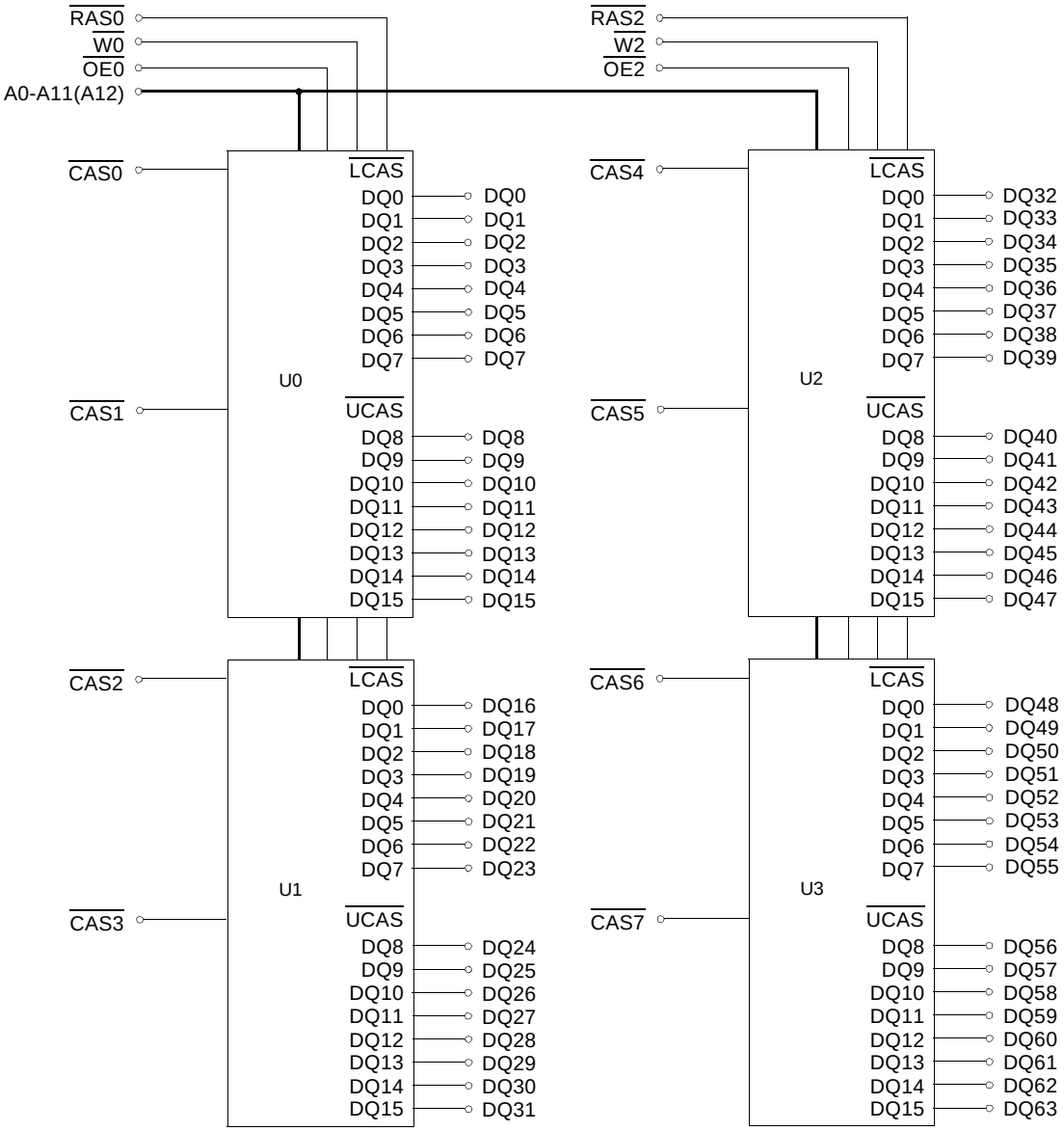
Note : A12 is used for only M366F0484CT1-C (8K ref.)

PIN NAMES

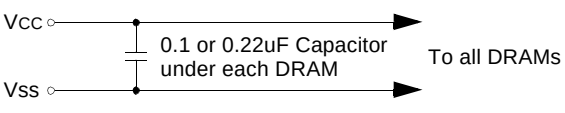
Pin Name	Function
A0 - A11	Address Input (4K ref.)
A0 - A12	Address Input (8K ref.)
DQ0 - DQ63	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
$\overline{OE0}$, $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
Vcc	Power(+3.3V)
Vss	Ground
NC	No Connection
DU	Don't use
SDA	Serial Address /Data I/O
SCL	Serial Clock
SA0 -SA2	Address in EEPROM
*CB0 - CB7	Check Bit

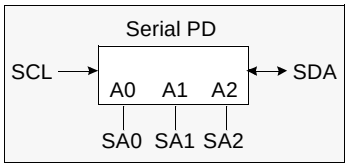
* These pins are not used in this module.

FUNCTIONAL BLOCK DIAGRAM



Note : A12 is used for only M366F0484CT1 (8K ref.)





ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V_{SS}	V_{IN}, V_{OUT}	-0.5 to +4.6	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Storage Temperature	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	4	W
Short Circuit Output Current	I_{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.0*2	-	V_{CC}+0.3*1	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

*1 : V_{CC}+1.3V at pulse width≤15ns which is measured at V_{CC}.

*2 : -1.3V at pulse width≤15ns which is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	M366F0484CT1		M366F0404CT1		Unit
		Min	Max	Min	Max	
I_{CC1}	-50	-	320	-	480	mA
	-60	-	280	-	440	mA
I_{CC2}	Don't care	-	4	-	4	mA
I_{CC3}	-50	-	320	-	480	mA
	-60	-	280	-	440	mA
I_{CC4}	-50	-	360	-	360	mA
	-60	-	320	-	320	mA
I_{CC5}	Don't care	-	2	-	2	mA
I_{CC6}	-50	-	480	-	480	mA
	-60	-	440	-	440	mA
$I_{I(L)}$	Don't care	-10	10	-10	10	uA
$I_{O(L)}$		-5	5	-5	5	uA
V_{OH}	Don't care	2.4	-	2.4	-	V
V_{OL}		-	0.4	-	0.4	V

I_{CC1} : Operating Current * ($\overline{RAS}$, $\overline{CAS}$, Address cycling @t_{RC}=min)

I_{CC2} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{IH})

I_{CC3} : $\overline{RAS}$ Only Refresh Current * ($\overline{CAS}$=V_{IH}, $\overline{RAS}$ cycling @t_{RC}=min)

I_{CC4} : Extended Data Out Mode Current * ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling : t_{HPC}=min)

I_{CC5} : Standby Current ($\overline{RAS}$=$\overline{CAS}$=$\overline{W}$=V_{CC}-0.2V)

I_{CC6} : $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Current * ($\overline{RAS}$ and $\overline{CAS}$ cycling @t_{RC}=min)

$I_{(IL)}$: Input Leakage Current (Any input 0≤V_{IN}≤V_{CC}+0.3V, all other pins not under test=0 V)

$I_{(OL)}$: Output Leakage Current(Data Out is disabled, 0V≤V_{OUT}≤V_{CC})

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* NOTE : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}$=V_{IL}. In I_{CC4}, address can be changed maximum once within one EDO mode cycle time, t_{HPC}.

CAPACITANCE (T_A = 25°C, V_{CC}=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A12]	C_{IN1}	-	30	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	C_{IN2}	-	24	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	C_{IN3}	-	24	pF
Input capacitance[$\overline{CAS0}$ - $\overline{CAS7}$]	C_{IN4}	-	17	pF
Input/Output capacitance[DQ0-DQ63]	CDQ	-	17	pF

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84		104		ns	
Read-modify-write cycle time	t_{RWC}	128		153		ns	
Access time from $\overline{RAS}$	t_{RAC}		50		60	ns	3,4,9
Access time from $\overline{CAS}$	t_{CAC}		13		15	ns	3,4,5
Access time from column address	t_{AA}		25		30	ns	3,9
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	3
$\overline{OE}$ to output in Low-Z	t_{OLZ}	3		3		ns	3
Output buffer turn-off delay from $\overline{CAS}$	t_{CEZ}	3	13	3	13	ns	6,12
Transition time(rise and fall)	t_T	1	50	1	50	ns	2
$\overline{RAS}$ precharge time	t_{RP}	30		40		ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10K	60	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	8		10		ns	
$\overline{CAS}$ hold time	t_{CSH}	38		40		ns	
$\overline{CAS}$ pulse width	t_{CAS}	8	10K	10	10K	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	17	37	20	45	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	12	25	15	30	ns	9
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row address set-up time	t_{ASR}	0		0		ns	
Row address hold time	t_{RAH}	7		10		ns	
Column address set-up time	t_{ASC}	0		0		ns	13
Column address hold time	t_{CAH}	7		10		ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	25		30		ns	
Read command set-up time	t_{RCS}	0		0		ns	
Read command hold referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	8
Read command hold referenced to $\overline{RAS}$	t_{RRH}	0		0		ns	8
Write command hold time	t_{WCH}	7		10		ns	
Write command pulse width	t_{WP}	7		10		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	8		10		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	7		10		ns	16
Data set-up time	t_{DS}	0		0		ns	
Data hold time	t_{DH}	7		10		ns	
Refresh period (4K & 8K Ref.)	t_{REF}		64		64	ms	
Write command set-up time	t_{WCS}	0		0		ns	7
$\overline{CAS}$ to $\overline{W}$ dealy time	t_{CWD}	33		38		ns	7, 15
$\overline{RAS}$ to $\overline{W}$ dealy time	t_{RWD}	70		84		ns	7

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

Test condition : V_{ih}/V_{il}=2.2/0.7V, V_{oh}/V_{ol}=2.0/0.8V, output loading C_L=100pF

Parameter	Symbol	-50		-60		Unit	Note
		Min	Max	Min	Max		
Column address to $\overline{W}$ delay time	t_{AWD}	45		53		ns	7
$\overline{CAS}$ precharge to $\overline{W}$ delay time	t_{CPWD}	47		58		ns	
$\overline{CAS}$ setup time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CSR}	5		5		ns	17
$\overline{CAS}$ hold time ($\overline{CAS}$-before-$\overline{RAS}$ refresh)	t_{CHR}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	5		5		ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		28		35	ns	3
Hyper page mode cycle time	t_{HPC}	20		25		ns	10
Hyper page mode read-modify write cycle time	t_{HPRWC}	67		73		ns	10
$\overline{CAS}$ precharge time (Hyper page cycle)	t_{CP}	7		10		ns	14
$\overline{RAS}$ pulse width (Hyper page cycle)	t_{RASP}	50	200K	60	200K	ns	
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	30		35		ns	
$\overline{OE}$ access time	t_{OEA}		13		15	ns	
$\overline{OE}$ to data delay	t_{OED}	10		13		ns	
Output buffer turn off delay time from $\overline{OE}$	t_{OEZ}	3	13	3	13	ns	6
$\overline{OE}$ command hold time	t_{OEH}	5		5		ns	
Output data hold time	t_{DOH}	5		5		ns	
Output buffer turn off delay from $\overline{RAS}$	t_{REZ}	3	13	3	13	ns	6,12
Output buffer turn off delay from $\overline{W}$	t_{WEZ}	3	13	3	13	ns	6
$\overline{W}$ to data delay	t_{WED}	15		15		ns	
$\overline{OE}$ to $\overline{CAS}$ hold time	t_{OCH}	5		5		ns	
$\overline{CAS}$ hold time to $\overline{OE}$	t_{CHO}	5		5		ns	
$\overline{OE}$ precharge time	t_{OEP}	5		5		ns	
$\overline{W}$ pulse width (Hyper page cycle)	t_{WPE}	5		5		ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles before proper device operation is achieved.

2. Input voltage levels are V_{ih}/V_{il}. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH}(min) and V_{IL}(max) and are assumed to be 5ns for all inputs.

3. Measured with a load equivalent to 1 TTL loads and 100pF.

4. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

5. Assumes that $t_{RCD} \geq t_{RCD}$(max).

6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

7. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are non-restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$(min), $t_{RWD} \geq t_{RWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), then the cycle is a read-write cycle and the data output will contain the data read from the selected address. If neither of the above contitions are satisfied, The condition of the data out is indeterminated.

8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

9. Operation within the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.

10. $t_{ASC} \geq 6$ns, Assume $t_T = 2.0$ns

11. For all of the refresh mode except distributed $\overline{CAS}$-before $\overline{RAS}$ refresh, 4096 cycle of burst refresh must be executed within 16ms before and after self-refresh in order to meet refresh specification.

12. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condtion of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condtion of the output is achieved by $\overline{RAS}$ high going.

13. t_{ASC}, t_{CAH} are referenced to the earlier $\overline{CAS}$ falling edge.

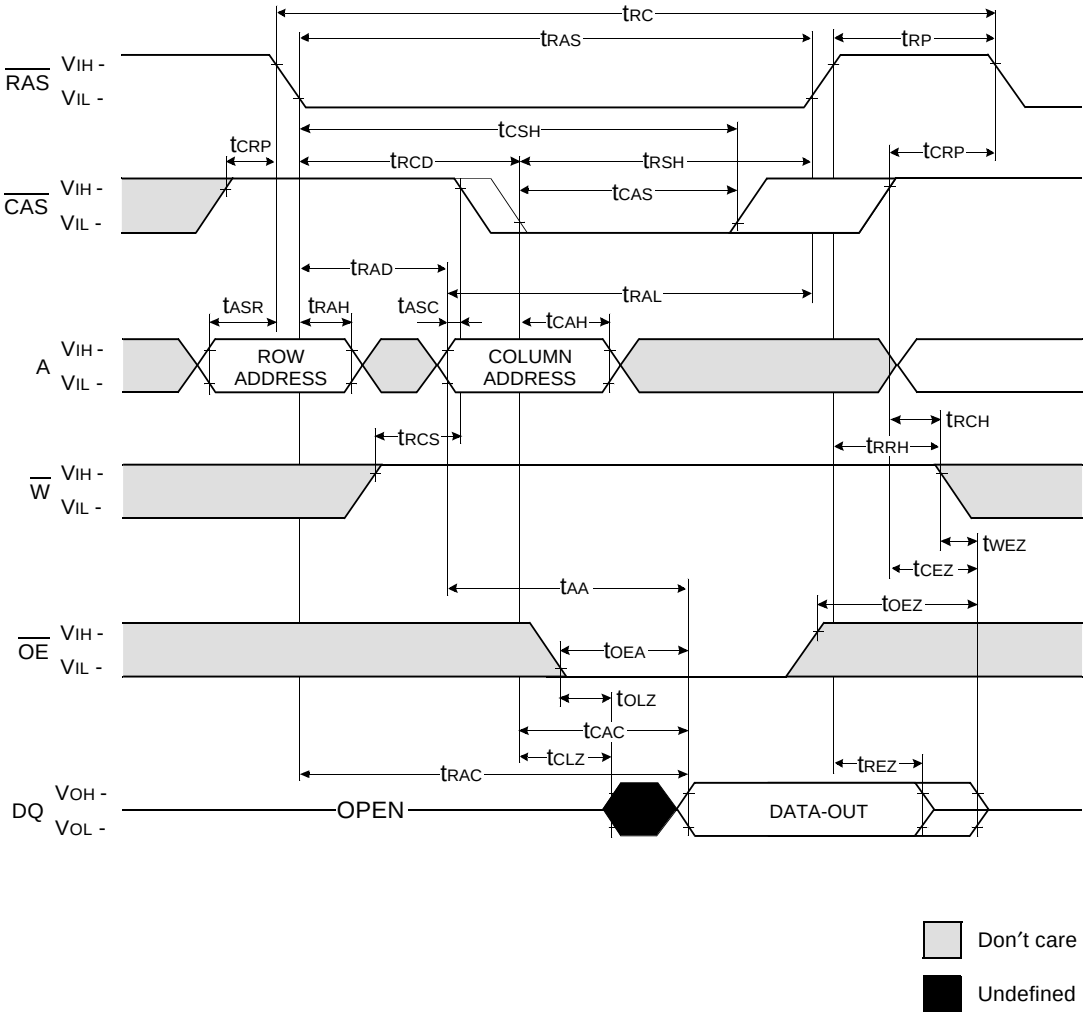
14. t_{CP} is specified from the last $\overline{CAS}$ rising edge in the previous cycle to the first $\overline{CAS}$ falling edge in the next cycle.

15. t_{CWD} is referenced to the later $\overline{CAS}$ falling edge at word read-modify-write cycle.

16. t_{CWL} is specified from $\overline{W}$ falling edge to the earlier $\overline{CAS}$ rising edge.

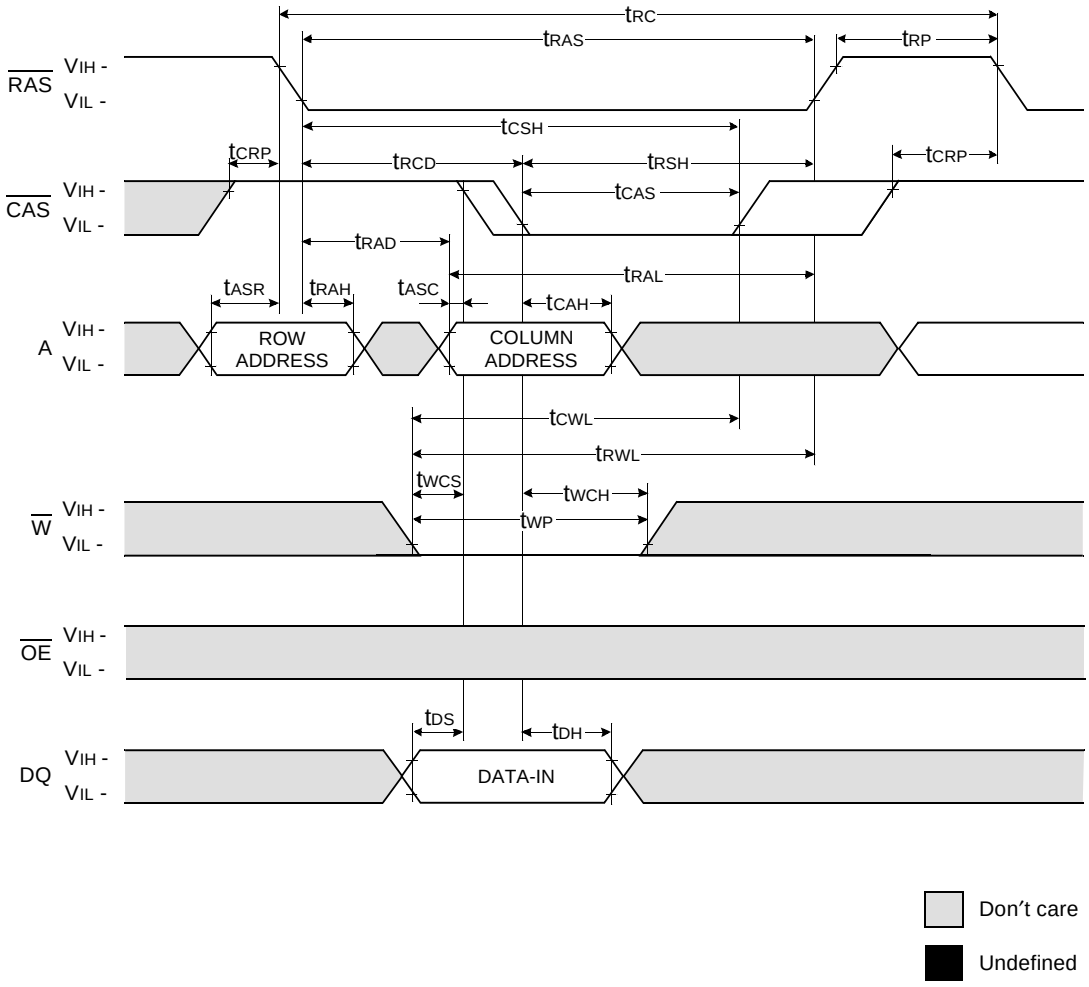
17. t_{CSR} is referenced to earlier $\overline{CAS}$ falling low before $\overline{RAS}$ transition low.

READ CYCLE



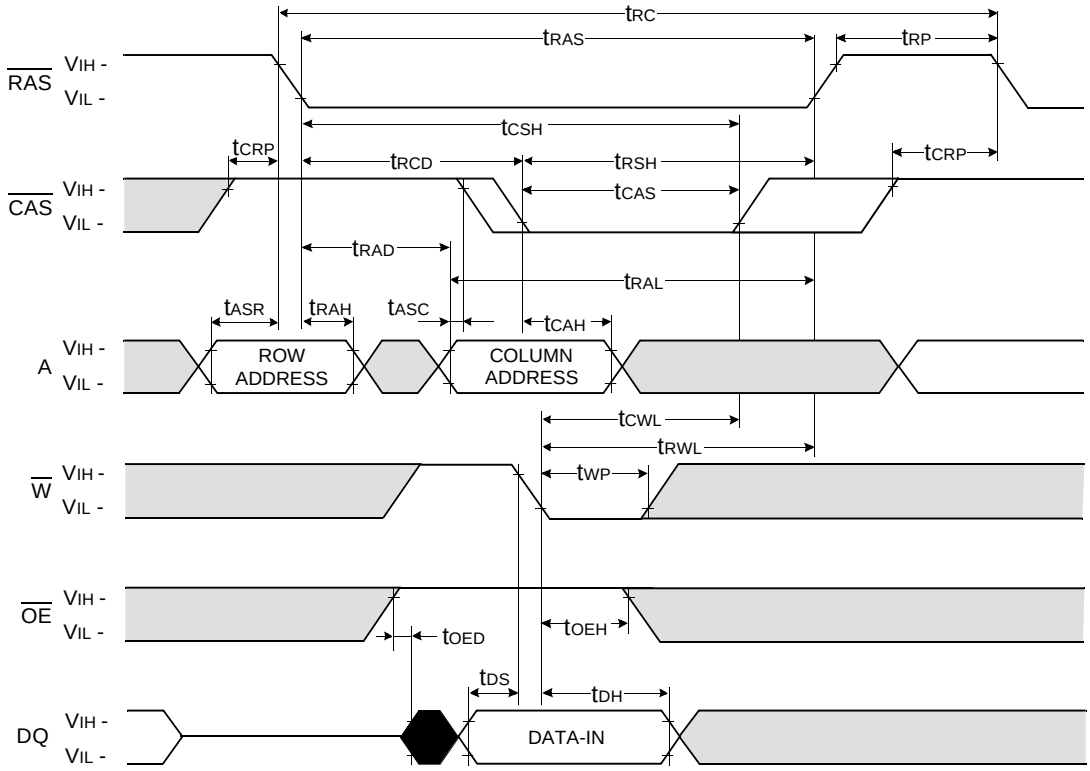
WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN

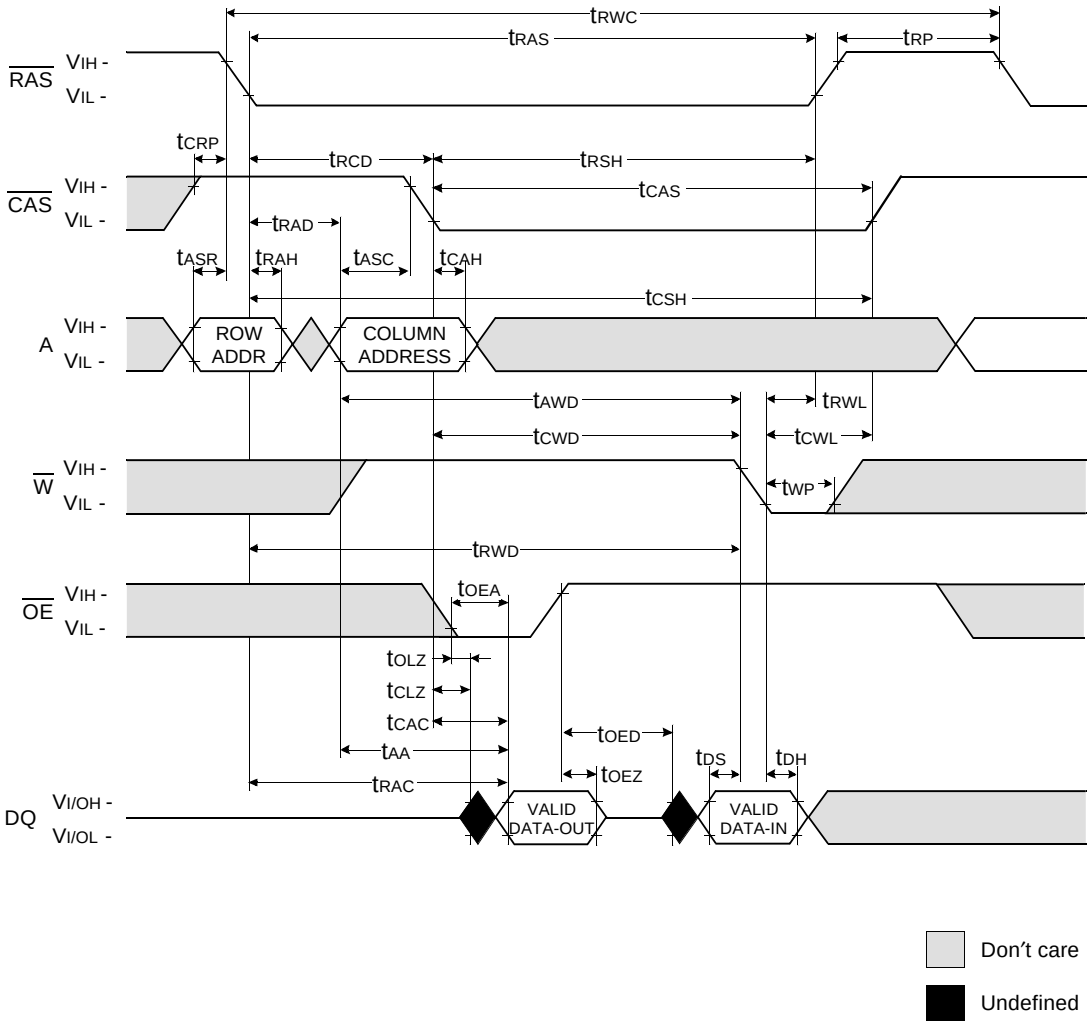


WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

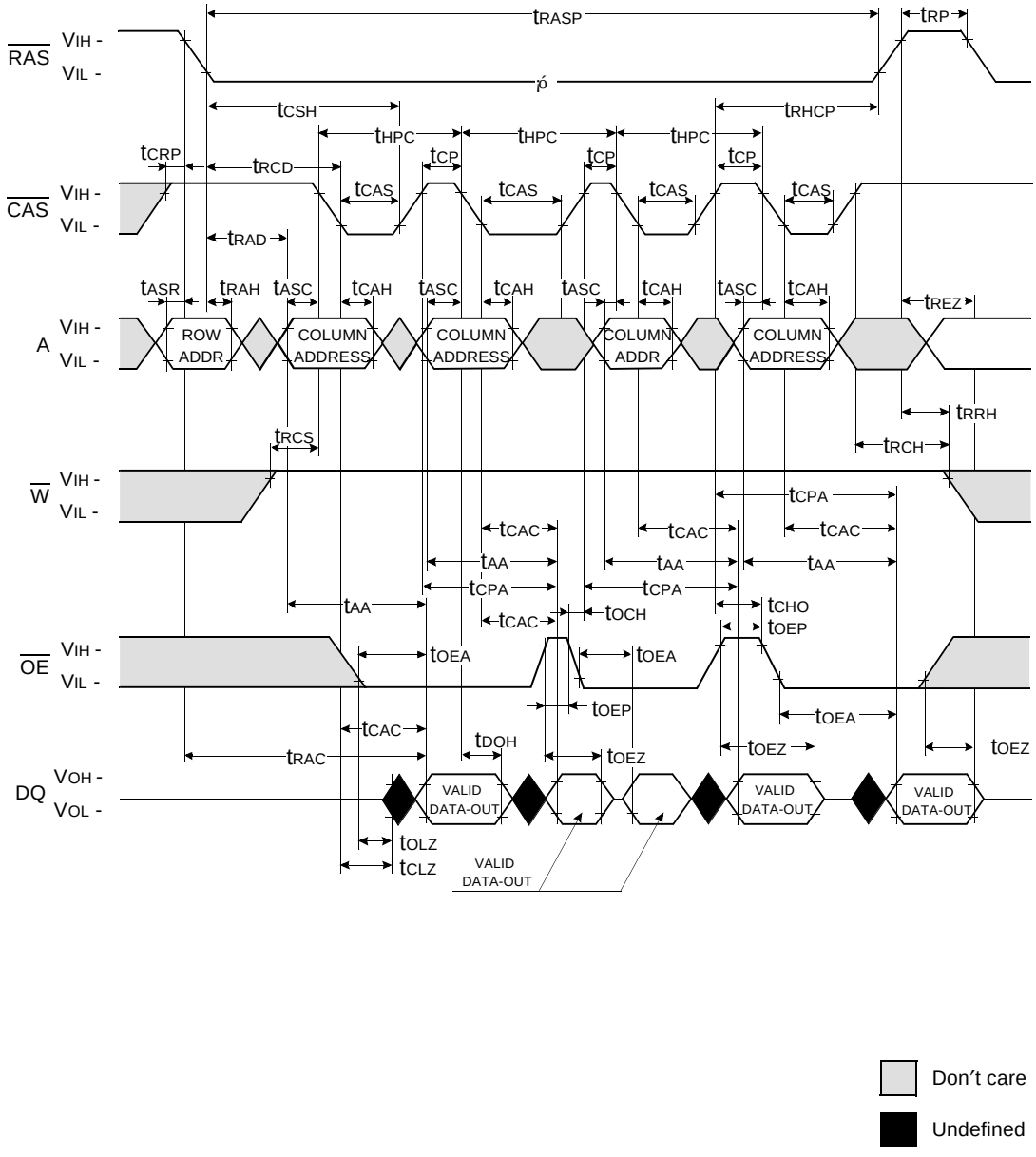
NOTE : DOUT = OPEN



READ - MODIFY - WRITE CYCLE

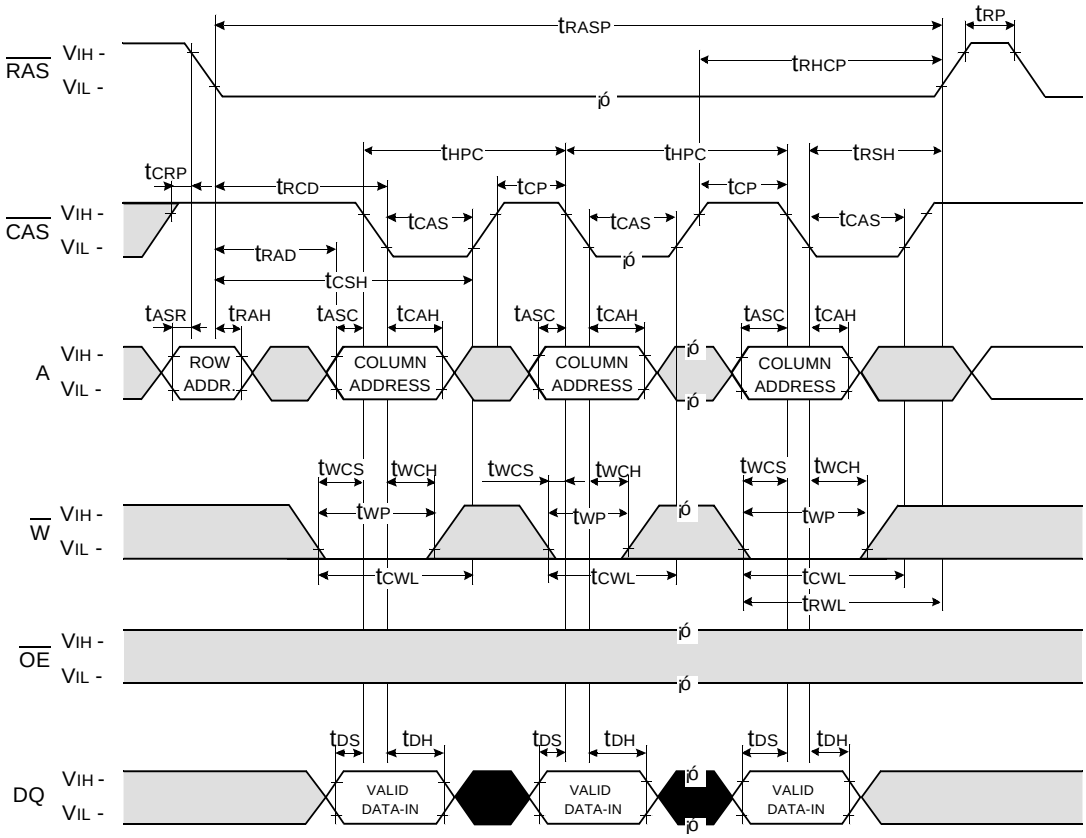


HYPER PAGE READ CYCLE



HYPER PAGE WRITE CYCLE (EARLY WRITE)

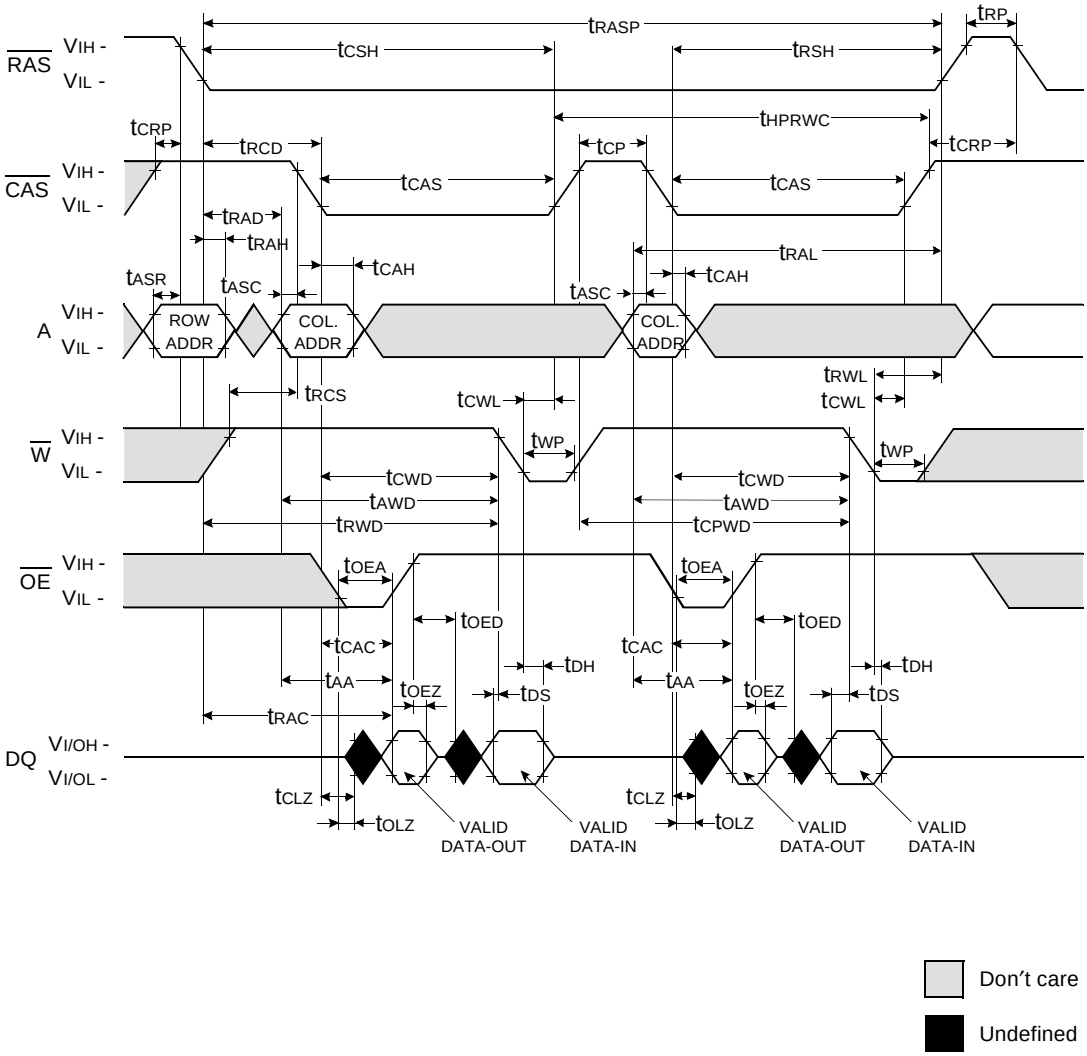
NOTE : DOUT = OPEN



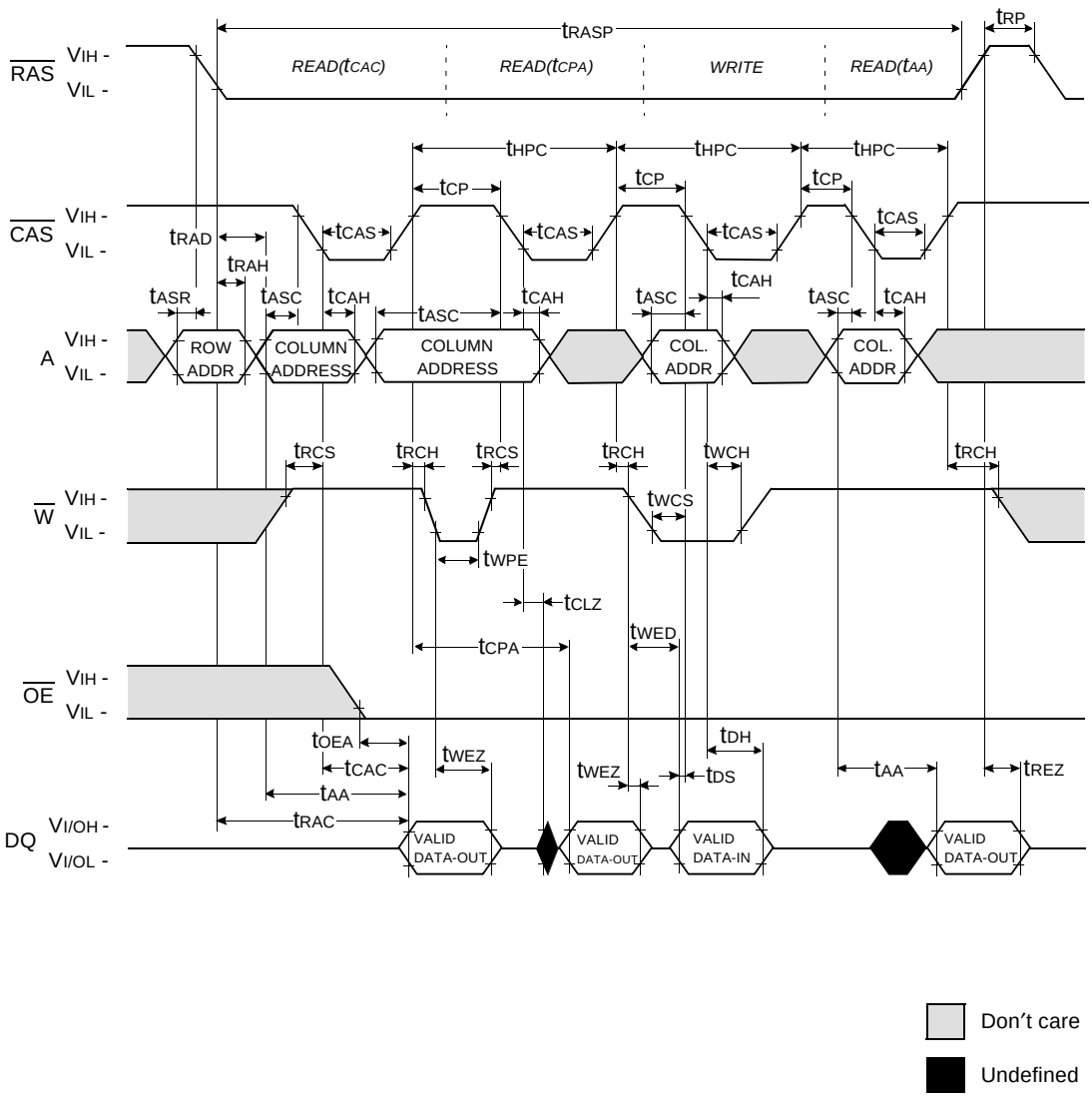
Don't care

Undefined

HYPER PAGE READ-MODIFY-WRITE CYCLE



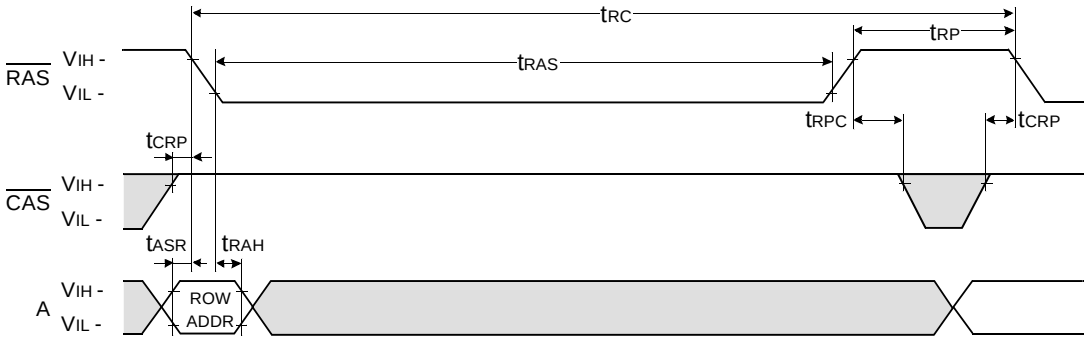
HYPER PAGE READ AND WRITE MIXED CYCLE



$\overline{RAS}$ - ONLY REFRESH CYCLE*

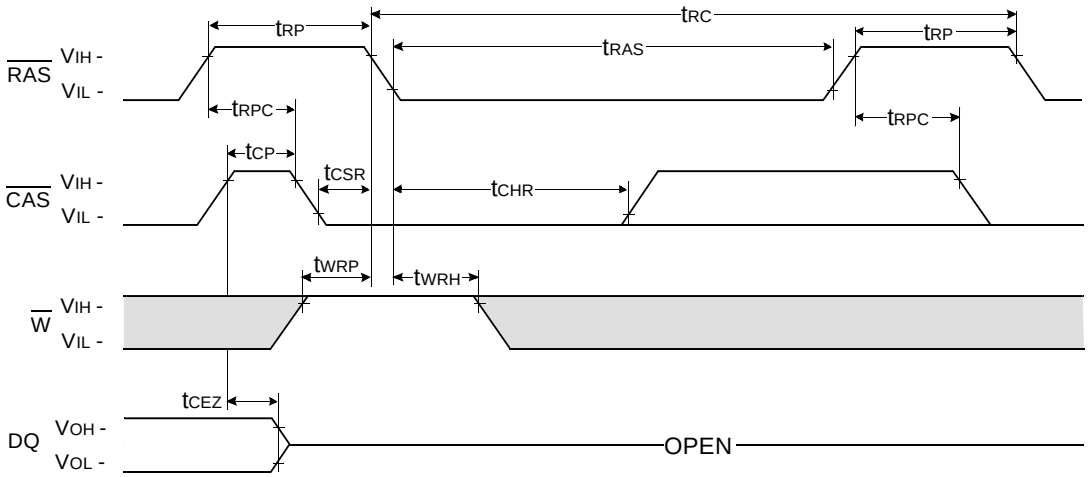
NOTE : $\overline{W}$, $\overline{OE}$, D_{IN} = Don't care

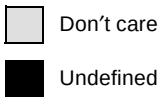
D_{OUT} = OPEN



$\overline{CAS}$ - BEFORE - $\overline{RAS}$ REFRESH CYCLE

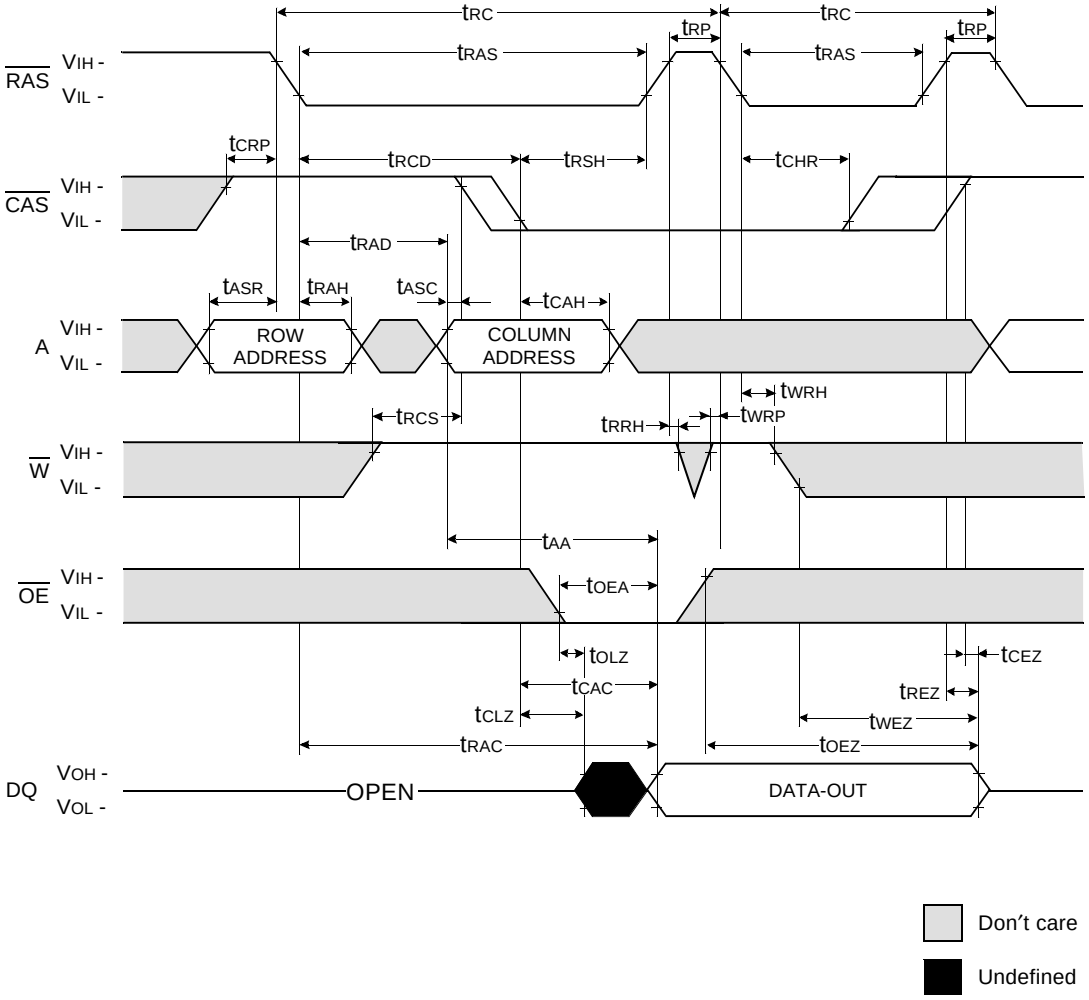
NOTE : $\overline{OE}$, A = Don't care





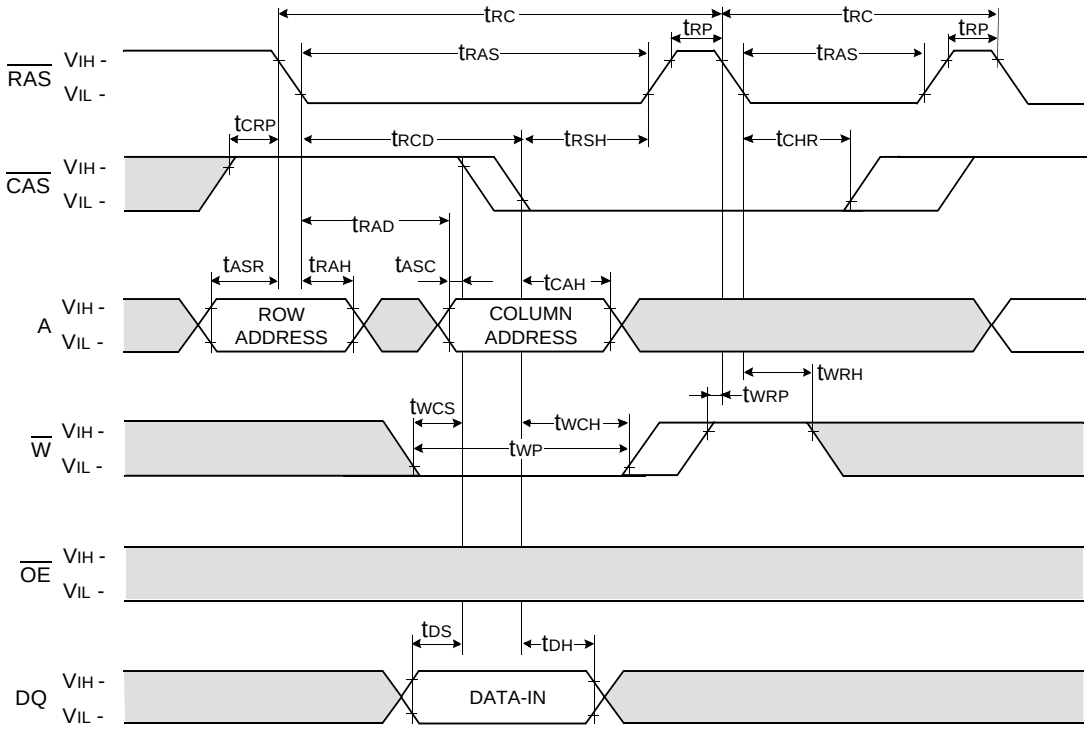
* In $\overline{RAS}$-only refresh cycle of 64Mb A-dile & B-die, when $\overline{CAS}$ signal transits from Low to High, the valid data may be cut off.

HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

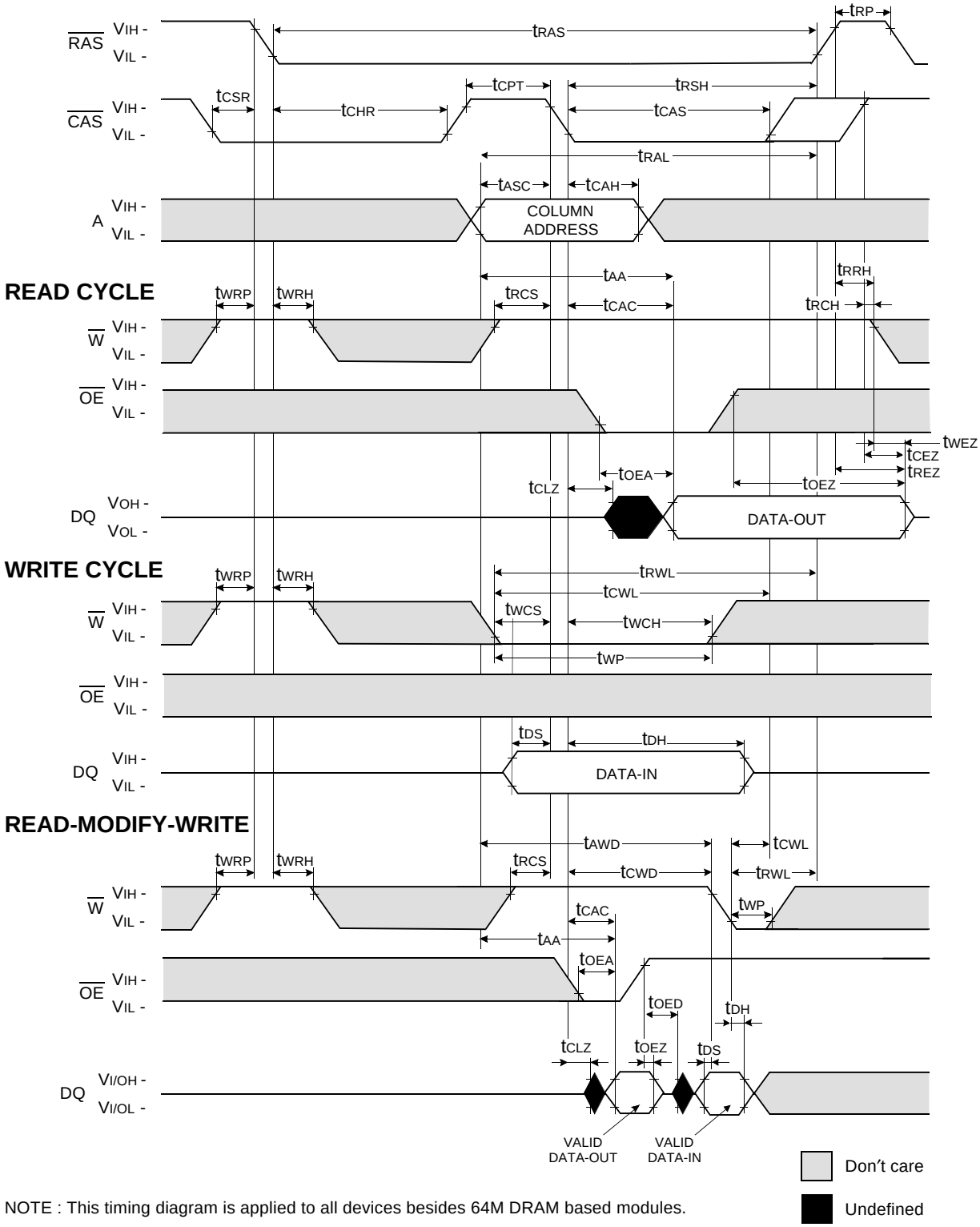
NOTE : DOUT = OPEN



Don't care

Undefined

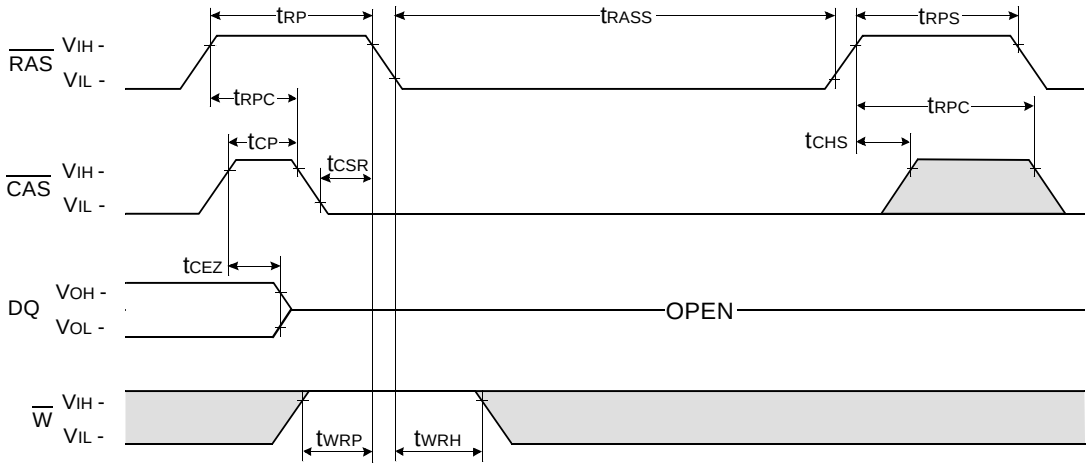
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

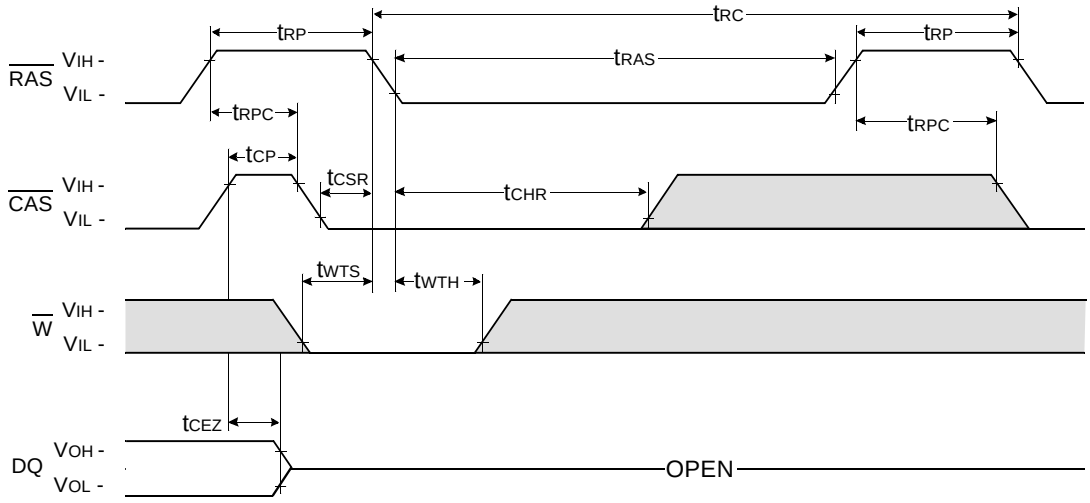
$\overline{CAS}$ - BEFORE - $\overline{RAS}$ SELF REFRESH CYCLE

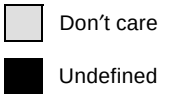
NOTE : $\overline{OE}$, A = Don't care



TEST MODE IN CYCLE

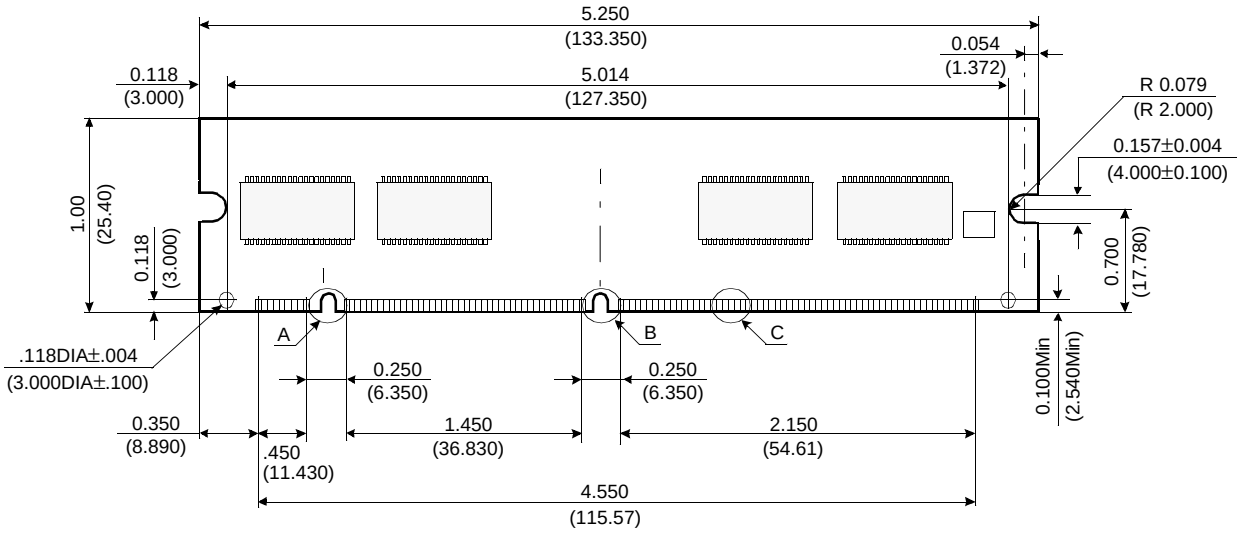
NOTE : $\overline{OE}$, A = Don't care



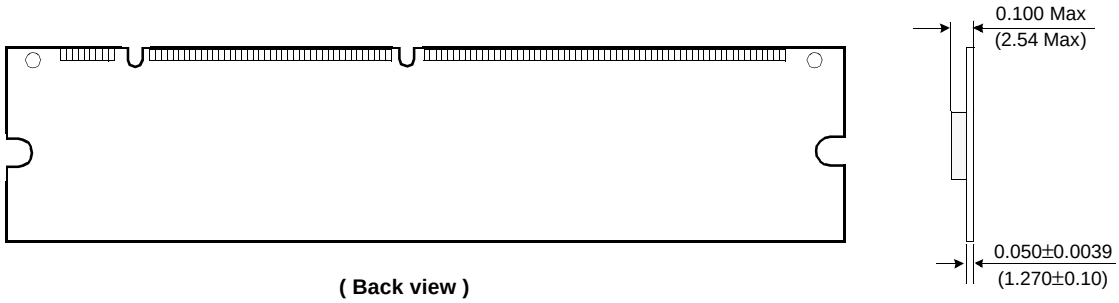


PACKAGE DIMENSIONS

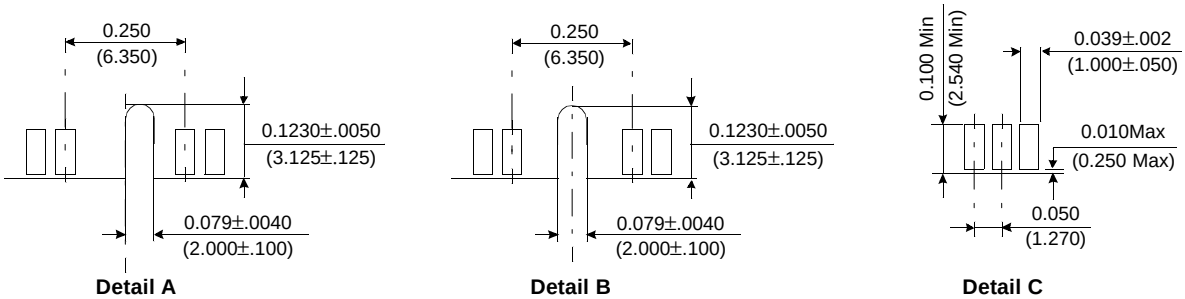
Units : Inches (millimeters)



(Front view)



(Back view)



Detail A **Detail B** **Detail C**

Tolerances : ±.005(.13) unless otherwise specified

The used device is 4Mx16 DRAM with EDO mode, TSOP II
DRAM Part No. : M366F0404CT1 - K4E641612C
M366F0484CT1 - K4E661612C