SDRAM Unbuffered Module

168pin Unbuffered Module based on 256Mb J-die

54 TSOP-II with Lead-Free and Halogen-Free

(RoHS compliant)

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Revision History

Revision	Month	Year	History
1.0	November	2007	- Initial Release

168Pin Unbuffered DIMM based on 256Mb J-die (x8, x16)

1.0 Ordering Information

Part Number	Density	Organization	Component Composition	Component Package	Height
M366S1654JUS-C7A	128MB	16M x 64	16M x 16 (K4S561632J) * 4EA	54-TSOP(II)	1,000mil
M366S3253JUS-C7A	256MB	32M x 64	32M x 8 (K4S560832J) * 8EA		1,375mil
M366S6453JUS-C7A	512MB	64M x 64	32M x 8 (K4S560832J) * 16EA		1,375mil

2.0 Operating Frequencies

	7A	
	@CL3	@CL2
Maximum Clock Frequency	133MHz(7.5ns)	100MHz(10ns)
CL-tRCD-tRP(clock)	3 - 3 - 3	2 - 2 - 2

3.0 Feature

- Burst mode operation
- Auto & self refresh capability (8192 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ± 0.3V power supply
- MRS cycle with address key programs Latency (Access from column address)
  Burst length (1, 2, 4, 8 & Full page)
  Data scramble (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial presence detect with EEPROM
- All of 54pin TSOP II components are **Lead-Free, Halogen-Free,** and RoHS compliant package

4.0 Pin Configuration (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V_{SS}	29	DQM1	57	DQ18	85	V_{SS}	113	DQM5	141	DQ50
2	DQ0	30	**$\overline{\text{CS0}}$	58	DQ19	86	DQ32	114	**$\overline{\text{CS1}}$	142	DQ51
3	DQ1	31	DU	59	V_{DD}	87	DQ33	115	$\overline{\text{RAS}}$	143	V_{DD}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{DD}	34	A2	62	*V_{REF}	90	V_{DD}	118	A3	146	*V_{REF}
7	DQ4	35	A4	63	**CKE1	91	DQ36	119	A5	147	NC/REGE
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{DD}	68	V_{SS}	96	V_{SS}	124	V_{DD}	152	V_{SS}
13	DQ9	41	V_{DD}	69	DQ24	97	DQ41	125	**CLK1	153	DQ56
14	DQ10	42	**CLK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	**CKE0	156	DQ59
17	DQ13	45	**$\overline{\text{CS2}}$	73	V_{DD}	101	DQ45	129	**$\overline{\text{CS3}}$	157	V_{DD}
18	V_{DD}	46	DQM2	74	DQ28	102	V_{DD}	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	*A13	160	DQ62
21	NC/CB0	49	V_{DD}	77	DQ31	105	NC/CB4	133	V_{DD}	161	DQ63
22	NC/CB1	50	NC	78	V_{SS}	106	NC/CB5	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	**CLK2	107	V_{SS}	135	NC	163	**CLK3
24	NC	52	NC/CB2	80	NC	108	NC	136	NC/CB6	164	NC
25	NC	53	NC/CB3	81	NC	109	NC	137	NC/CB7	165	SA0
26	V_{DD}	54	V_{SS}	82	SDA	110	V_{DD}	138	V_{SS}	166	SA1
27	$\overline{\text{WE}}$	55	DQ16	83	SCL	111	$\overline{\text{CAS}}$	139	DQ48	167	SA2
28	DQM0	56	DQ17	84	V_{DD}	112	DQM4	140	DQ49	168	V_{DD}

1. * These pins are not used in this module.
2. Pins 82,83,165,166,167 should be NC in the system which does not support SPD.
3. Pins 21,22,52,53,105,106,136,137are used only ECC(x72) Module.
4. ** About these pins, Refer to the Block Diagram of each.

5.0 Pin Description

Pin Description

Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	DQM0 ~ 7	DQM
BA0 ~ BA1	Select bank	V_{DD}	Power supply (3.3V)
DQ0 ~ DQ63	Data input/output	V_{SS}	Ground
CB0 ~ CB7	Check bit (Data-in/data-out)	V_{REF}	Power supply for reference
CLK0 ~ 3	Clock input	REGE	Register enable
CKE0, CKE1	Clock enable input	SDA	Serial data I/O
$\overline{\text{CS0}}$ ~ $\overline{\text{CS3}}$	Chip select input	SCL	Serial clock
$\overline{\text{RAS}}$	Row address strobe	SA0 ~ 2	Address in EEPROM
$\overline{\text{CAS}}$	Colume address strobe	DU	Don't use
$\overline{\text{WE}}$	Write enable	NC	No connection

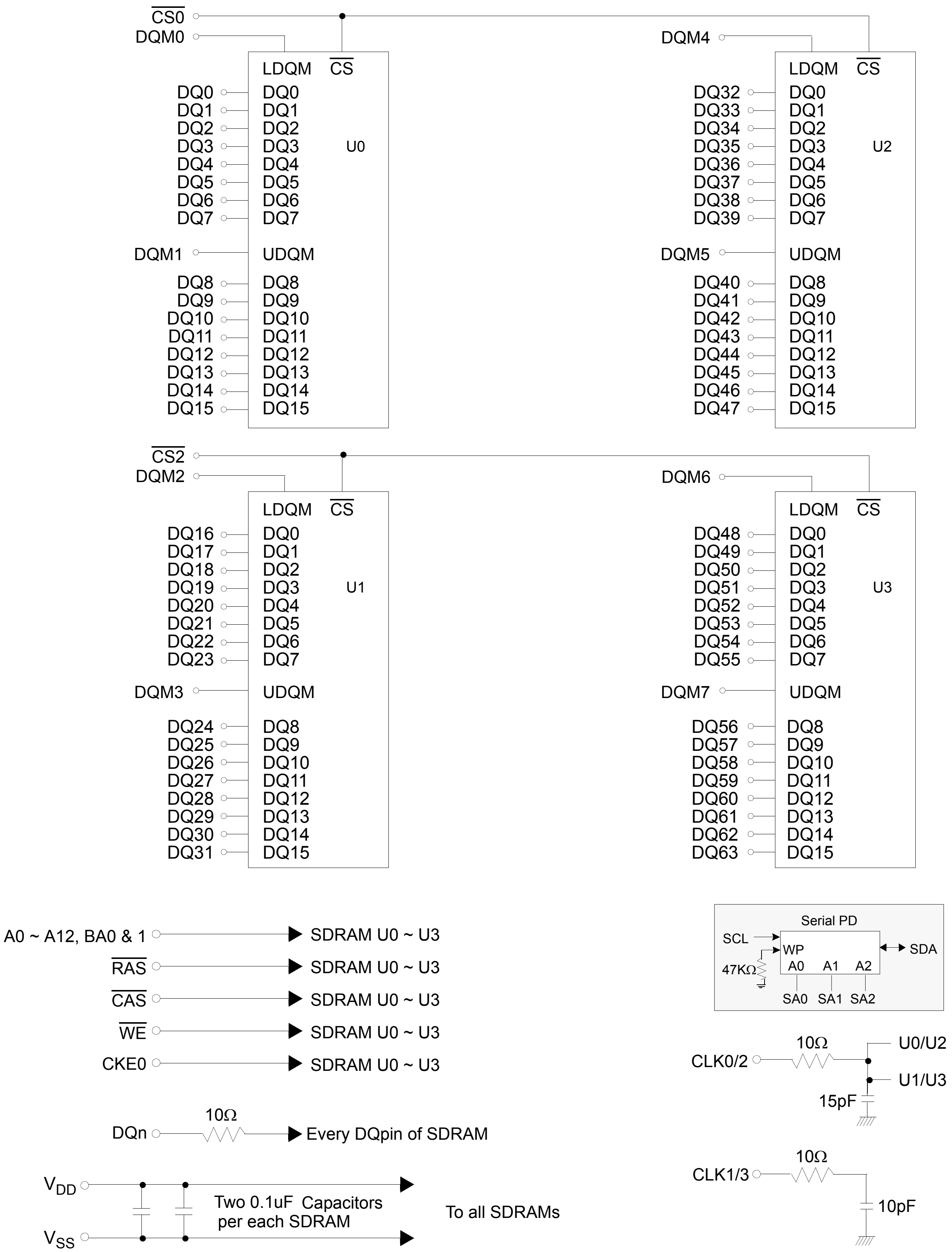
6.0 PIN CONFIGURATION DESCRIPTION

Pin	Name	Input Function
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12 Column address : (x8 : CA0 ~ CA9), (x16 : CA0 ~ CA8)
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM0 ~ 7	*Data input/output mask*	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	*Register enable*	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. the inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to V_{DD} through 10K ohm Resistor on PCB. So if REGE of module is floating, this module will be operated as registered mode.
DQ0 ~ 63	*Data input/output*	Data inputs/outputs are multiplexed on the same pins.
CB0 ~ 7	*Check bit*	Check bits for ECC.
V_{DD}/V_{SS}	*Power supply/ground*	Power and ground for the input buffers and the core logic.

7.0 Functional Block Diagram

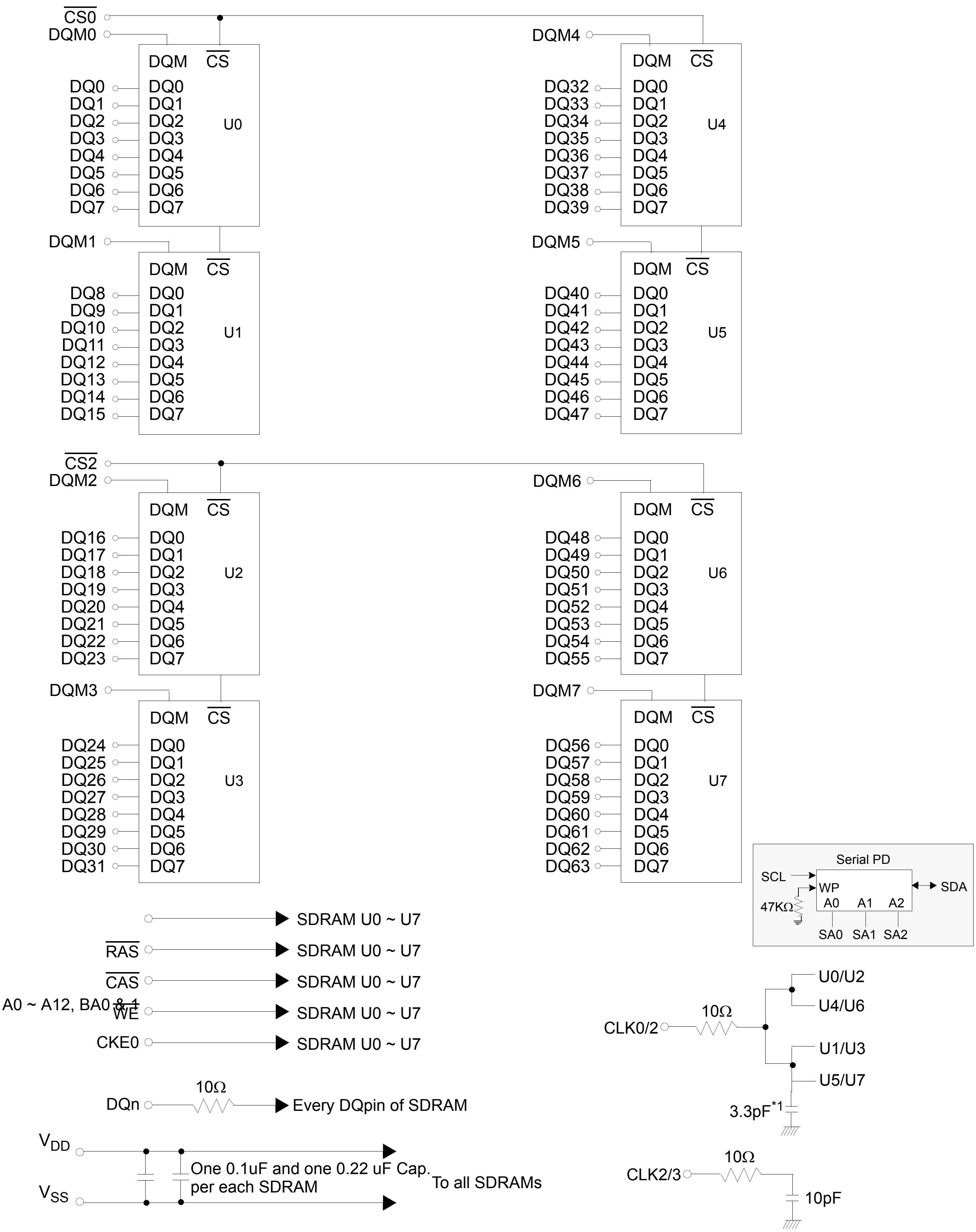
7.1 128MB, 64M x 64 Non-ECC Module (M366S1654JUS)

(Populated as 1 bank of x16 SDRAM Module)



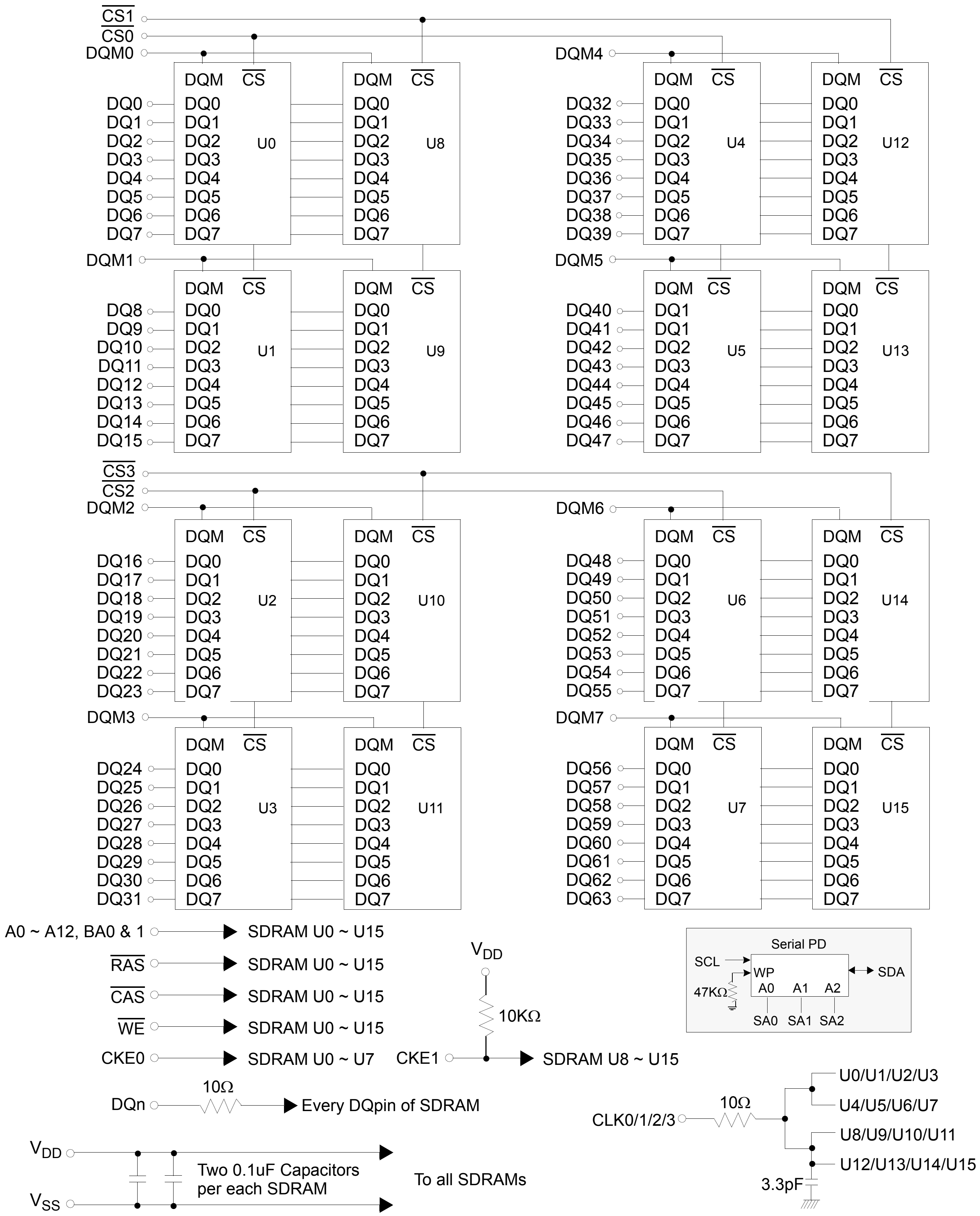
7.2 256MB, 32M x 64 Non-ECC Module (M366S3253JUS)

(Populated as 1 bank of x8 SDRAM Module)



7.3 512MB, 64M x 64 Non-ECC Module (M366S6453JUS)

(Populated as 2 bank of x8 SDRAM Module)



8.0 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	1.0 * # of component	W
Short circuit current	I_{OS}	50	mA

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

9.0 DC Operating Conditions

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current	I_{LI}	-10	-	10	uA	3

Note :
1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is $\leq$ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is $\leq$ 3ns.
3. Any input 0V $\leq V_{IN} \leq V_{DDQ}$. Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

10.0 CAPACITANCE

(V_{DD} = 3.3V, T_A = 23°C, f = 1MHz, V_{REF} = 1.4V $\pm$ 200 mV)

Parameter	Symbol	M366S1654JUS		M366S3253JUS		M366S6453JUS		Unit
		Min	Max	Min	Max	Min	Max	
Input capacitance (A_0 ~ A_{11})	C_{IN1}	15	25	25	45	45	85	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	15	25	25	45	45	85	pF
Input capacitance (CKE)	C_{IN3}	15	25	25	45	25	45	pF
Input capacitance (CLK)	C_{IN4}	10	13	15	21	15	21	pF
Input capacitance ($\overline{CS}$)	C_{IN5}	10	15	15	25	15	25	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	8	10	8	12	10	15	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	9	12	9	12	13	18	pF

11.0 DC CHARACTERISTICS

11.1 M366S1654JUS (16M x 64,128MB Module)

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version 7A	Unit	Note
Operating current (One bank active)	ICC1	Burst length = 1, tRC ≥ tRC(min), IO = 0 mA	280	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ V_{IL}(max), tCC = 10ns	8	mA	
	ICC2PS	CKE & CLK ≤ V_{IL}(max), tCC =∞	8		
Precharge standby current in non power-down mode	ICC2N	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tCC = 10ns Input signals are changed one time during 20ns	60	mA	
	ICC2NS	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tCC =∞ Input signals are stable	40		
Active standby current in power-down mode	ICC3P	CKE ≤ V_{IL}(max), tCC = 10ns	20	mA	
	ICC3PS	CKE & CLK ≤ V_{IL}(max), tCC =∞	20		
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tCC = 10ns Input signals are changed one time during 20ns	112	mA	
	ICC3NS	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tCC =∞ Input signals are stable	80	mA	
Operating current (Burst mode)	ICC4	IO = 0 mA, Page burst, 4Banks activated tCCD = 2CLKs	440	mA	1
Refresh current	ICC5	tRC ≥ tRC(min)	640	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	12	mA	

11.2 M366S3253JUS (32M x 64, 256MB Module)

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version 7A	Unit	Note
Operating current (One bank active)	ICC1	Burst length = 1, tRC ≥ tRC(min), IO = 0 mA	560	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ V_{IL}(max), tCC = 10ns	16	mA	
	ICC2PS	CKE & CLK ≤ V_{IL}(max), tCC =∞	16		
Precharge standby current in non power-down mode	ICC2N	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tCC = 10ns Input signals are changed one time during 20ns	120	mA	
	ICC2NS	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tCC =∞ Input signals are stable	80		
Active standby current in power-down mode	ICC3P	CKE ≤ V_{IL}(max), tCC = 10ns	40	mA	
	ICC3PS	CKE & CLK ≤ V_{IL}(max), tCC =∞	40		
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tCC = 10ns Input signals are changed one time during 20ns	224	mA	
	ICC3NS	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tCC =∞ Input signals are stable	160	mA	
Operating current (Burst mode)	ICC4	IO = 0 mA, Page burst, 4Banks activated tCCD = 2CLKs	880	mA	1
Refresh current	ICC5	tRC ≥ tRC(min)	1,280	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	24	mA	

Note :

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

11.3 M366S6453JUS (64M x 64, 512MB Module)

(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Version 7A	Unit	Note
Operating current (One bank active)	ICC1	Burst length = 1, tRC ≥ tRC(min), IO = 0 mA	784	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ V_{IL}(max), tCC = 10ns	32	mA	
	ICC2PS	CKE & CLK ≤ V_{IL}(max), tCC =∞	32		
Precharge standby current in non power-down mode	ICC2N	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tCC = 10ns Input signals are changed one time during 20ns	240	mA	
	ICC2NS	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tCC =∞ Input signals are stable	160		
Active standby current in power-down mode	ICC3P	CKE ≤ V_{IL}(max), tCC = 10ns	80	mA	
	ICC3PS	CKE & CLK ≤ V_{IL}(max), tCC =∞	80		
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tCC = 10ns Input signals are changed one time during 20ns	448	mA	
	ICC3NS	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tCC =∞ Input signals are stable	320	mA	
Operating current (Burst mode)	ICC4	IO = 0 mA, Page burst, 4Banks activated tCCD = 2CLKs	1,104	mA	1
Refresh current	ICC5	tRC ≥ tRC(min)	1,504	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	48	mA	

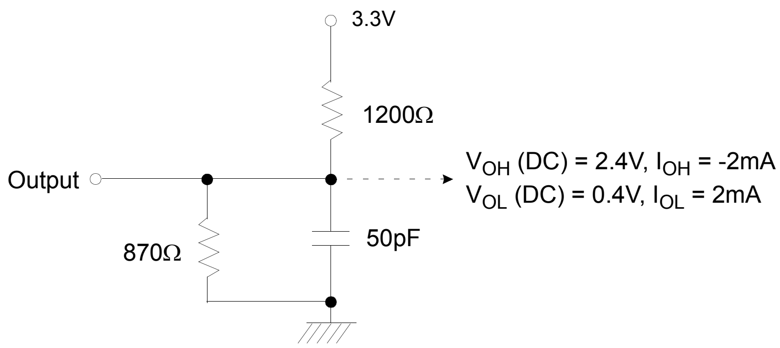
Note :

1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(V_{IH}/V_{IL}=V_{DDQ}/V_{SSQ})

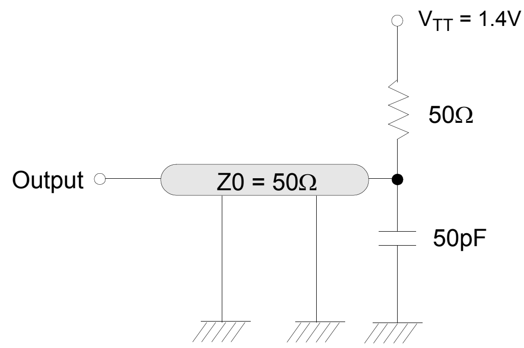
12.0 AC Operating Conditions

(V_{DD} = 3.3V ± 0.3V, T_A = 0 to 70°C)

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

13.0 OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version 7A	Unit	Note
Row active to row active delay		tRRD(min)	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	20	ns	1
Row precharge time		tRP(min)	20	ns	1
Row active time		tRAS(min)	45	ns	1
		tRAS(max)	100	us	
Row cycle time		tRC(min)	65	ns	1
Last data in to row precharge		tRDL(min)	2	CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + tRP	-	5
Last data in to new col. address delay		tCDL(min)	1	CLK	2
Last data in to burst stop		tBDL(min)	1	CLK	2
Col. address to col. address delay		tCCD(min)	1	CLK	3
Number of valid output data	CAS latency=3		2	ea	4
	CAS latency=2		1		

1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.

14.0 AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

REFER TO THE INDIVIDUAL COMPONENET, NOT THE WHOLE MODULE.

Parameter		Symbol	7A		Unit	Note
			Min	Max		
CLK cycle time	CAS latency=3	tCC	7.5	1000	ns	1
	CAS latency=2		10			
CLK to valid output delay	CAS latency=3	tSAC	-	5.4	ns	1,2
	CAS latency=2		-	6		
Output data hold time	CAS latency=3	tOH	3	-	ns	2
	CAS latency=2		3	-		
CLK high pulse width		tCH	2.5	-	ns	3
CLK low pulse width		tCL	2.5	-	ns	3
Input setup time		tSS	1.5	-	ns	3
Input hold time		tSH	0.8	-	ns	3
CLK to output in Low-Z		tSLZ	1	-	ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ	-	5.4	ns	
	CAS latency=2		-	6		

1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns. If tr & tf is longer than 1ns, transient time compensation should be considered, i.e., [(tr + tf)/2-1]ns should be added to the parameter.

15.0 SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

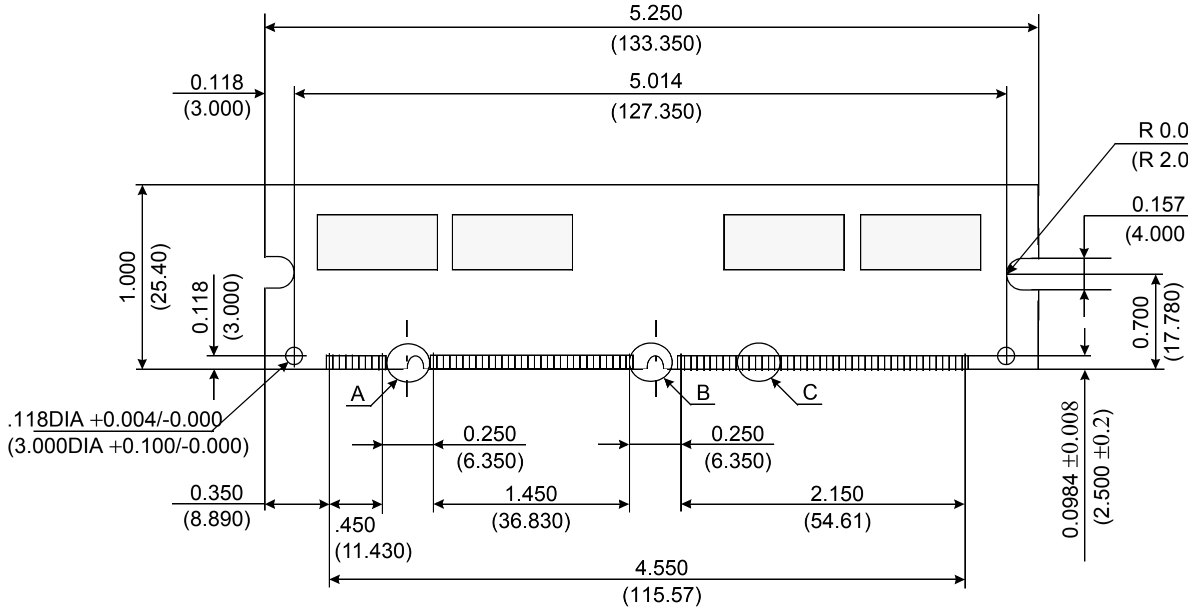
<table>
<tr><th colspan="3">Command</th><th>CKEn-1</th><th>CKEn</th><th>$\overline{CS}$</th><th>$\overline{RAS}$</th><th>$\overline{CAS}$</th><th>$\overline{WE}$</th><th>DQM</th><th>$BA_{0,1}$</th><th>A_{10}/AP</th><th>$A_0 \sim A_9$, A_{11}, A_{12}</th><th>Note</th></tr>
<tr><td>Register</td><td colspan="2">Mode register set</td><td>H</td><td>X</td><td>L</td><td>L</td><td>L</td><td>L</td><td>X</td><td colspan="3">OP code</td><td>1,2</td></tr>
<tr><td rowspan="4">Refresh</td><td colspan="2">Auto refresh</td><td rowspan="2">H</td><td>H</td><td rowspan="2">L</td><td rowspan="2">L</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">X</td><td colspan="3" rowspan="2">X</td><td>3</td></tr>
<tr><td rowspan="3">Self refresh</td><td>Entry</td><td>L</td><td>3</td></tr>
<tr><td rowspan="2">Exit</td><td rowspan="2">L</td><td rowspan="2">H</td><td>L</td><td>H</td><td>H</td><td>H</td><td rowspan="2">X</td><td colspan="3" rowspan="2">X</td><td>3</td></tr>
<tr><td>H</td><td>X</td><td>X</td><td>X</td><td>3</td></tr>
<tr><td colspan="3">Bank active & row addr.</td><td>H</td><td>X</td><td>L</td><td>L</td><td>H</td><td>H</td><td>X</td><td>V</td><td colspan="2">Row address</td><td></td></tr>
<tr><td rowspan="2">Read & column address</td><td colspan="2">Auto precharge disable</td><td rowspan="2">H</td><td rowspan="2">X</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">X</td><td rowspan="2">V</td><td>L</td><td rowspan="2">Column address</td><td>4</td></tr>
<tr><td colspan="2">Auto precharge enable</td><td>H</td><td>4,5</td></tr>
<tr><td rowspan="2">Write & column address</td><td colspan="2">Auto precharge disable</td><td rowspan="2">H</td><td rowspan="2">X</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">L</td><td rowspan="2">L</td><td rowspan="2">X</td><td rowspan="2">V</td><td>L</td><td rowspan="2">Column address</td><td>4</td></tr>
<tr><td colspan="2">Auto precharge enable</td><td>H</td><td>4,5</td></tr>
<tr><td colspan="3">Burst stop</td><td>H</td><td>X</td><td>L</td><td>H</td><td>H</td><td>L</td><td>X</td><td colspan="3">X</td><td>6</td></tr>
<tr><td rowspan="2">Precharge</td><td colspan="2">Bank selection</td><td rowspan="2">H</td><td rowspan="2">X</td><td rowspan="2">L</td><td rowspan="2">L</td><td rowspan="2">H</td><td rowspan="2">L</td><td rowspan="2">X</td><td>V</td><td>L</td><td rowspan="2">X</td><td></td></tr>
<tr><td colspan="2">All banks</td><td>X</td><td>H</td><td></td></tr>
<tr><td colspan="2" rowspan="3">Clock suspend or active power down</td><td rowspan="2">Entry</td><td rowspan="2">H</td><td rowspan="2">L</td><td>H</td><td>X</td><td>X</td><td>X</td><td rowspan="2">X</td><td colspan="3" rowspan="3">X</td><td></td></tr>
<tr><td>L</td><td>V</td><td>V</td><td>V</td><td></td></tr>
<tr><td>Exit</td><td>L</td><td>H</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td></td></tr>
<tr><td colspan="2" rowspan="4">Precharge power down mode</td><td rowspan="2">Entry</td><td rowspan="2">H</td><td rowspan="2">L</td><td>H</td><td>X</td><td>X</td><td>X</td><td rowspan="2">X</td><td colspan="3" rowspan="4">X</td><td></td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td></td></tr>
<tr><td rowspan="2">Exit</td><td rowspan="2">L</td><td rowspan="2">H</td><td>H</td><td>X</td><td>X</td><td>X</td><td rowspan="2">X</td><td></td></tr>
<tr><td>L</td><td>V</td><td>V</td><td>V</td><td></td></tr>
<tr><td colspan="3">DQM</td><td>H</td><td colspan="5"></td><td>V</td><td colspan="3">X</td><td>7</td></tr>
<tr><td colspan="3" rowspan="2">No operation command</td><td rowspan="2">H</td><td rowspan="2">X</td><td>H</td><td>X</td><td>X</td><td>X</td><td rowspan="2">X</td><td colspan="3" rowspan="2">X</td><td></td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>H</td><td></td></tr>
</table>

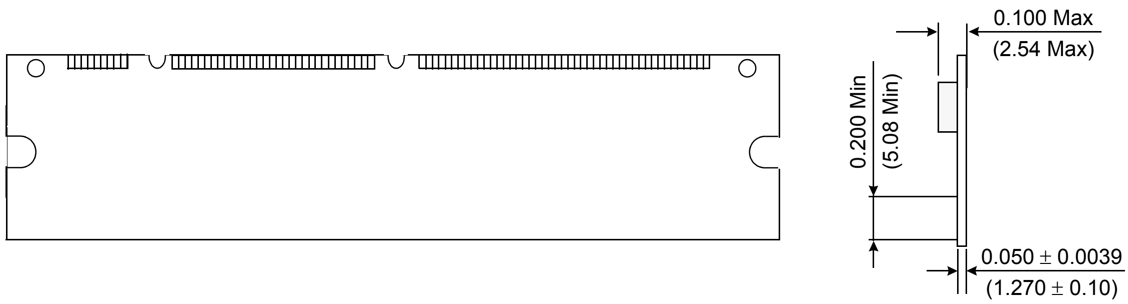
1. OP Code : Operand code
   $A_0 \sim A_{12}$ & $BA_0 \sim BA_1$: Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 clock cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. $BA_0 \sim BA_1$: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

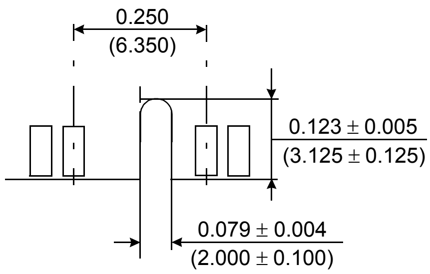
16.0 Physical Dimensions

16.1 16Mx64 (M366S1654JUS)

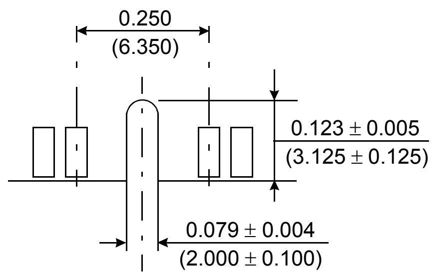
Units : Inches (Millimeters)



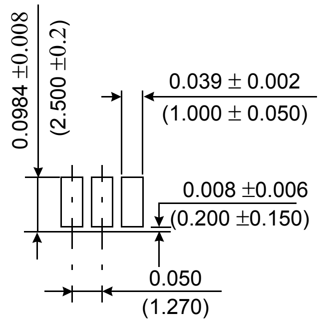




Detail A



Detail B



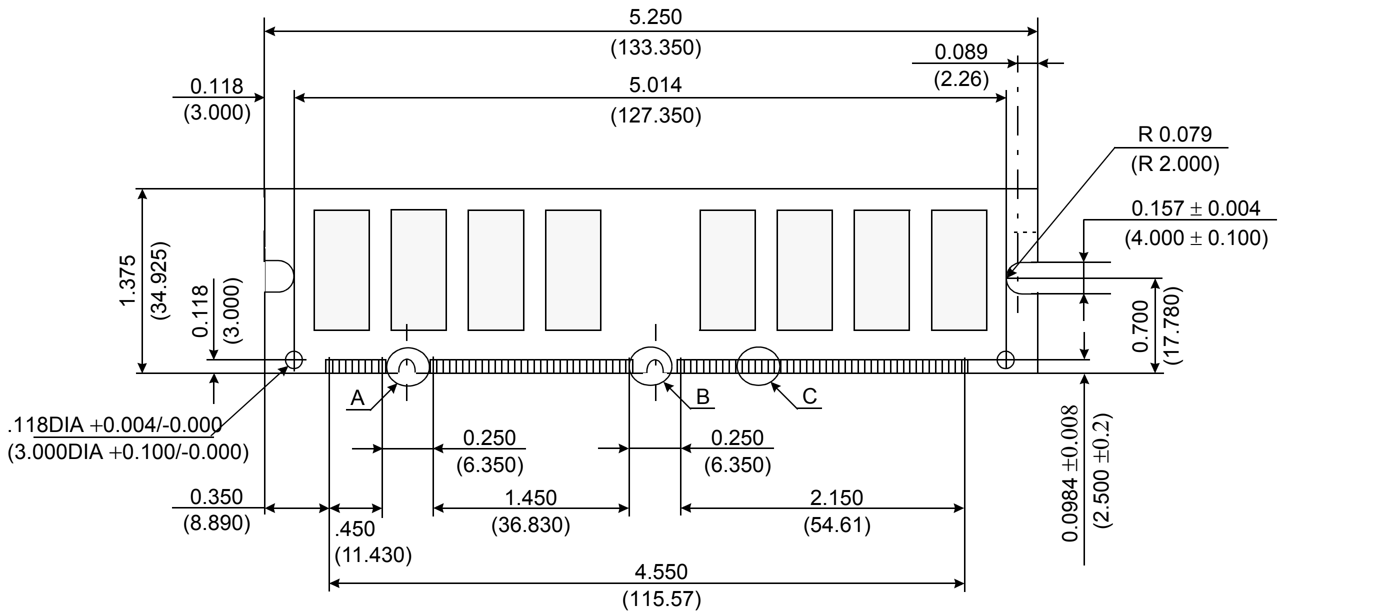
Detail C

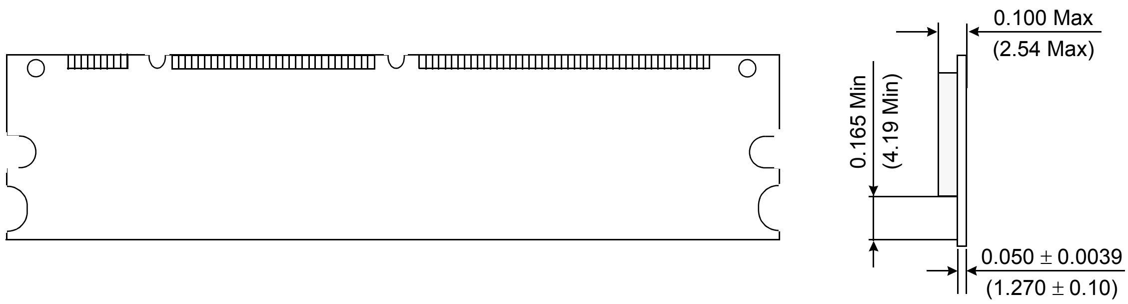
Tolerances : ± .005(.13) unless otherwise specified

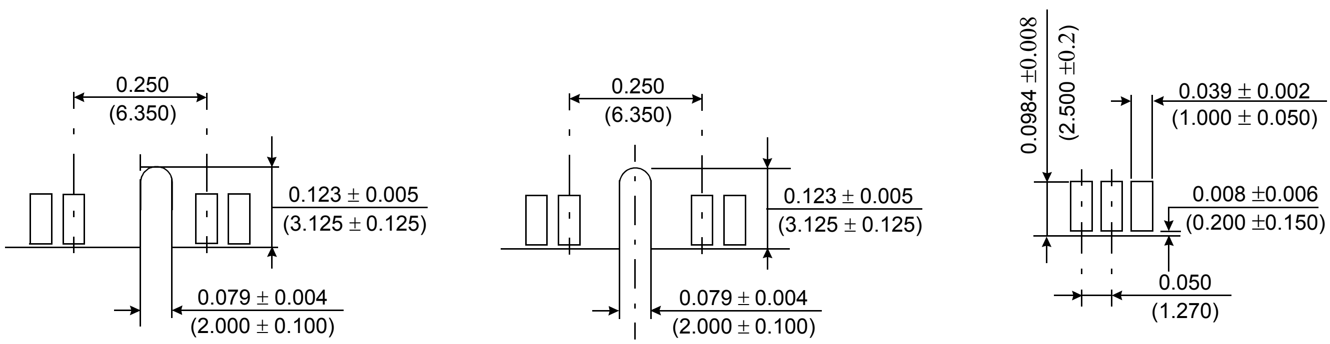
The used device is 16Mx16 SDRAM, TSOPII
SDRAM Part No. : K4S561632J

16.2 32Mx64 (M366S3253JUS)

Units : Inches (Millimeters)







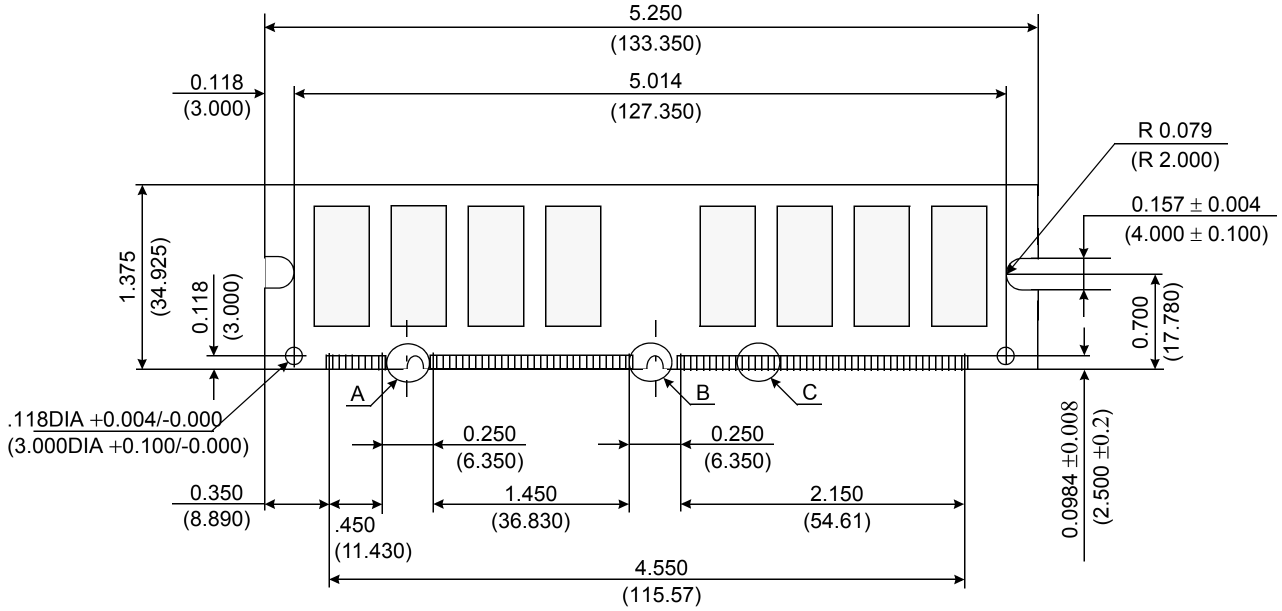
Detail A **Detail B** **Detail C**

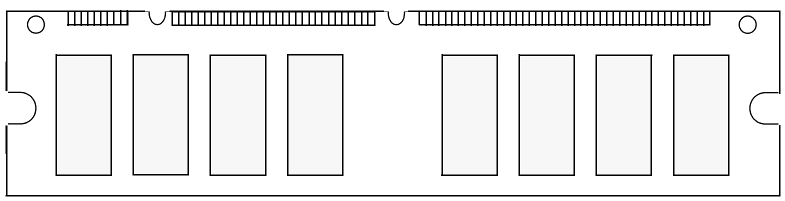
Tolerances : ± .005(.13) unless otherwise specified

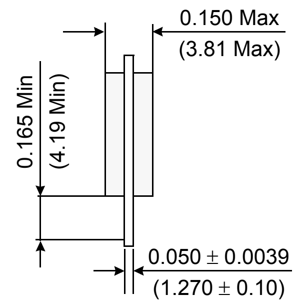
The used device is 32Mx8 SDRAM, TSOPII
SDRAM Part No. : K4S560832J

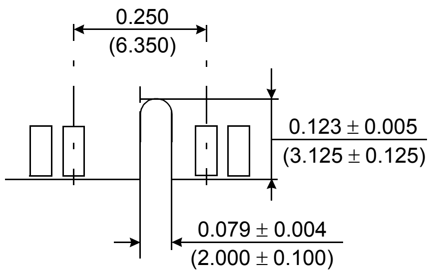
16.3 64Mx64 (M366S6453JUS)

Units : Inches (Millimeters)

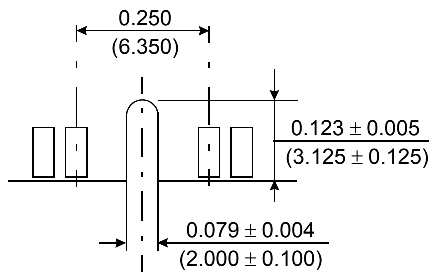




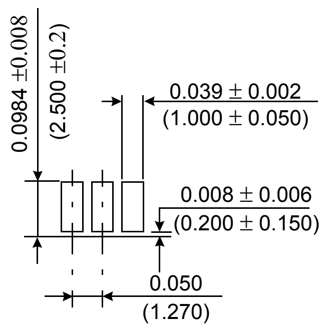




Detail A



Detail B



Detail C

Tolerances : ± .005(.13) unless otherwise specified

The used device is 32Mx8 SDRAM, TSOPII
SDRAM Part No. : K4S560832J