

**M368L3223CT1**

**184pin Unbuffered DDR SDRAM MODULE**

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# 256MB DDR SDRAM MODULE

(32Mx64 based on 32Mx8 DDR SDRAM)

Unbuffered 184pin DIMM  
64-bit Non-ECC/Parity

Revision 0.0

September. 2001

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**Revision History**

**Revision 0 (Sep 2001)**

1. First release for internal usage

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## M368L3223CT1 DDR SDRAM 184pin DIMM

32Mx64 DDR SDRAM 184pin DIMM based on 32Mx8

### GENERAL DESCRIPTION

The Samsung M368L3223CT1 is 32M bit x 64 Double Data Rate SDRAM high density memory modules based on 4th gen of 256Mb DDR SDRAM respectively.

The Samsung M368L3223CT1 consists of eight CMOS 32M x 8 bit with 4banks Double Data Rate SDRAMs in 66pin TSOP-II(400mil) packages mounted on a 184pin glass-epoxy substrate. Four 0.1uF decoupling capacitors are mounted on the printed circuit board in parallel for each DDR SDRAM. The M368L3223CT1 is Dual In-line Memory Modules and intended for mounting into 184pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

### FEATURE

- Performance range

Part No.	Max Freq.	Interface
M368L3223CT1-C(L)B3	167MHz(6.0ns@CL=2.5)	SSTL_2
M368L3223CT1-C(L)A2	133MHz(7.5ns@CL=2)	
M368L3223CT1-C(L)B0	133MHz(7.5ns@CL=2.5)	
M368L3223CT1-C(L)A0	100MHz(10ns@CL=2)	

- Power supply : Vdd: 2.5V ± 0.2V, Vddq: 2.5V ± 0.2V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Differential clock inputs(CK and  $\overline{CK}$ )
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency 2, 2.5 (clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height 1250 (mil), double sided component

### PIN CONFIGURATIONS (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	*/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	*/CS2	102	NC	133	DQ31	163	*/CS3
11	VSS	42	VSS	72	DQ48	103	*A13	134	*CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	*CB5	165	DQ52
13	DQ9	44	*CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	*CB1	75	/CK2	106	DQ13	137	CK0	167	NC
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK0	168	VDD
16	CK1	47	*DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK1	48	A0	78	DQS6	109	DQ14	140	*DM8	170	DQ54
18	VSS	49	*CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	*CKE1	142	*CB6	172	VDDQ
20	DQ11	51	*CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	*BA2	144	*CB7	174	DQ60
22	VDDQ	KEY		83	DQ56	114	DQ20	KEY		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	VSS	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	DQ18	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	VDDQ	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

### PIN DESCRIPTION

Pin Name	Function
A0 ~ A12	Address input (Multiplexed)
BA0 ~ BA1	Bank Select Address
DQ0 ~ DQ63	Data input/output
DQS0 ~ DQS7	Data Strobe input/output
CK0, $\overline{CK0}$ ~ CK2, $\overline{CK2}$	Clock input
CKE0	Clock enable input
CS0	Chip select input
RAS	Row address strobe
$\overline{CAS}$	Column address strobe
WE	Write enable
DM0 ~ DM7	Data - in mask
VDD	Power supply (2.5V)
VDDQ	Power Supply for DQS(2.5V)
VSS	Ground
VREF	Power supply for reference
VDDSPD	Serial EEPROM Power Supply (2.3V to 3.6V)
SDA	Serial data I/O
SCL	Serial clock
SA0 ~ 2	Address in EEPROM
VDDID	VDD identification flag
NC	No connection

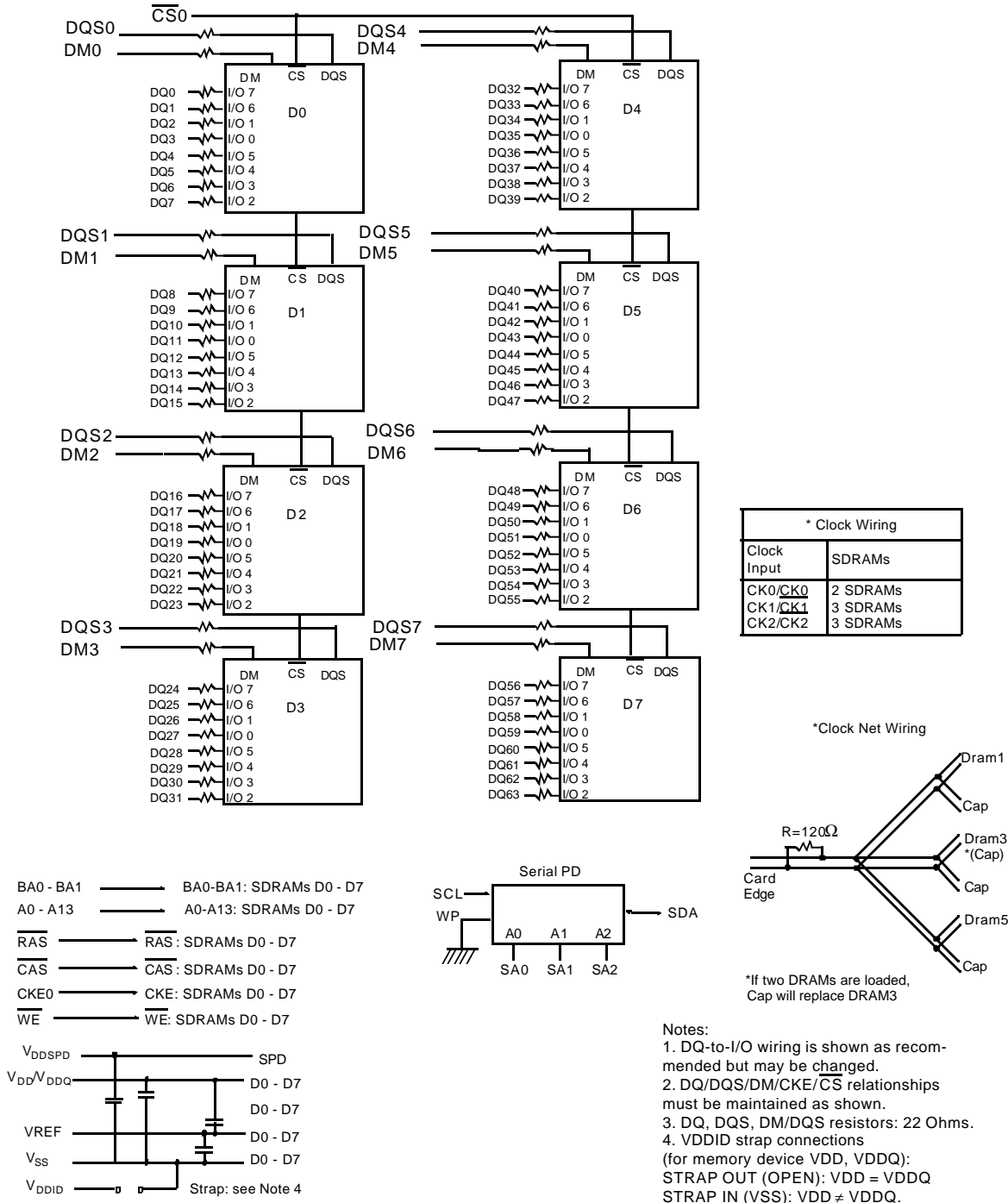
\* These pins are not used in this module.

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Functional Block Diagram



## M368L3223CT1

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### ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 ~ 3.6	V
Voltage on VDD supply relative to Vss	V <sub>DD</sub>	-1.0 ~ 3.6	V
Voltage on VDDQ supply relative to Vss	V <sub>DDQ</sub>	-0.5 ~ 3.6	V
Storage temperature	T <sub>STG</sub>	-55 ~ +150	°C
Power dissipation	P <sub>D</sub>	8	W
Short circuit current	I <sub>OS</sub>	50	mA

**Note :** Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.  
 Functional operation should be restricted to recommended operating condition.  
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

### POWER & DC OPERATING CONDITIONS (SSTL\_2 In/Out)

Recommended operating conditions(Voltage referenced to Vss=0V, TA=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal VDD of 2.5V)	V <sub>DD</sub>	2.3	2.7		
I/O Supply voltage	V <sub>DDQ</sub>	2.3	2.7	V	
I/O Reference voltage	V <sub>REF</sub>	V <sub>DDQ</sub> /2-50mV	V <sub>DDQ</sub> /2+50mV	V	1
I/O Termination voltage(system)	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub> +0.04	V	2
Input logic high voltage	V <sub>IH</sub> (DC)	V <sub>REF</sub> +0.15	V <sub>DDQ</sub> +0.3	V	4
Input logic low voltage	V <sub>IL</sub> (DC)	-0.3	V <sub>REF</sub> -0.15	V	4
Input Voltage Level, CK and $\overline{\text{CK}}$ inputs	V <sub>IN</sub> (DC)	-0.3	V <sub>DDQ</sub> +0.3	V	
Input Differential Voltage, CK and $\overline{\text{CK}}$ inputs	V <sub>ID</sub> (DC)	0.3	V <sub>DDQ</sub> +0.6	V	3
Input crossing point voltage, CK and $\overline{\text{CK}}$ inputs	V <sub>IX</sub> (DC)	1.15	1.35	V	5
Input leakage current	I <sub>I</sub>	-2	2	uA	
Output leakage current	I <sub>OZ</sub>	-5	5	uA	
Output High Current(Normal strength driver) ;V <sub>OUT</sub> = V <sub>TT</sub> + 0.84V	I <sub>OH</sub>	-16.8		mA	
Output High Current(Normal strength driver) ;V <sub>OUT</sub> = V <sub>TT</sub> - 0.84V	I <sub>OL</sub>	16.8		mA	
Output High Current(Half strength driver) ;V <sub>OUT</sub> = V <sub>TT</sub> + 0.45V	I <sub>OH</sub>	-9		mA	
Output High Current(Half strength driver) ;V <sub>OUT</sub> = V <sub>TT</sub> - 0.45V	I <sub>OL</sub>	9		mA	

**Notes**

- Includes ±25mV margin for DC offset on VREF, and a combined total of ±50mV margin for all AC noise and DC offset on VREF, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on VREF and internal DRAM noise coupled TO VREF, both of which may result in VREF noise. VREF should be de-coupled with an inductance of ≤ 3nH.
- V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF
- V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on  $\overline{\text{CK}}$ .
- These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a VREF envelop that has been bandwidth limited to 200MHZ.
- The value of V<sub>IX</sub> is expected to equal 0.5\*V<sub>DDQ</sub> of the transmitting device and must track variations in the dc level of the same.
- These characteristics obey the SSTL-2 class II standards.

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**DDR SDRAM SPEC Items and Test Conditions**

Recommended operating conditions Unless Otherwise Noted, T<sub>A</sub>=0 to 70°C)

Conditions	Symbol	Typical	Worst
<b>Operating current - One bank Active-Precharge;</b> t <sub>RC</sub> =t <sub>RCmin</sub> ;t <sub>CK</sub> =100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	IDD0	-	-
<b>Operating current - One bank operation ;</b> One bank open, BL=4, Reads - Refer to the following page for detailed test condition	IDD1	-	-
<b>Percharge power-down standby current;</b> All banks idle; power - down mode; CKE = <V <sub>IL</sub> (max); t <sub>CK</sub> =100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; V <sub>in</sub> = V <sub>ref</sub> for DQ,DQS and DM	IDD2P	-	-
<b>Precharge Floating standby current;</b> CS# > =V <sub>IH</sub> (min);All banks idle; CKE > = V <sub>IH</sub> (min); t <sub>CK</sub> =100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; Address and other control inputs changing once per clock cycle; V <sub>in</sub> = V <sub>ref</sub> for DQ,DQS and DM	IDD2F	-	-
<b>Precharge Quiet standby current;</b> CS# > = V <sub>IH</sub> (min); All banks idle; CKE > = V <sub>IH</sub> (min); t <sub>CK</sub> = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; Address and other control inputs stable with keeping >= V <sub>IH</sub> (min) or =<V <sub>IL</sub> (max); V <sub>in</sub> = V <sub>ref</sub> for DQ ,DQS and DM	IDD2Q	-	-
<b>Active power - down standby current ;</b> one bank active; power-down mode; CKE=< V <sub>IL</sub> (max); t <sub>CK</sub> = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; V <sub>in</sub> = V <sub>ref</sub> for DQ,DQS and DM	IDD3P	-	-
<b>Active standby current;</b> CS# >= V <sub>IH</sub> (min); CKE>=V <sub>IH</sub> (min); one bank active; active - precharge; t <sub>RC</sub> =t <sub>RASmax</sub> ; t <sub>CK</sub> = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	IDD3N	-	-
<b>Operating current - burst read;</b> Burst length = 2; reads; continguous burst; One bank active; address and control inputs changing once per clock cycle; CL=2 at t <sub>CK</sub> = 100Mhz for DDR200, CL=2 at t <sub>CK</sub> = 133Mhz for DDR266A, CL=2.5 at t <sub>CK</sub> = 133Mhz for DDR266B ; 50% of data changing at every burst; I <sub>out</sub> = 0 m A	IDD4R	-	-
<b>Operating current - burst write;</b> Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL=2 at t <sub>CK</sub> = 100Mhz for DDR200, CL=2 at t <sub>CK</sub> = 133Mhz for DDR266A, CL=2.5 at t <sub>CK</sub> = 133Mhz for DDR266B ; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	IDD4W	-	-
<b>Auto refresh current;</b> t <sub>RC</sub> = t <sub>RFC</sub> (min) - 8*t <sub>CK</sub> for DDR200 at 100Mhz, 10*t <sub>CK</sub> for DDR266A & DDR266B at 133Mhz; distributed refresh	IDD5	-	-
<b>Self refresh current;</b> CKE =< 0.2V; External clock should be on; t <sub>CK</sub> = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B	IDD6	-	-
<b>Orerating current - Four bank operation ;</b> Four bank interleaving with BL=4 -Refer to the following page for detailed test condition	IDD7A	-	-

Typical case: VDD = 2.5V, T = 25' C

Worst case : VDD = 2.7V, T = 10' C

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**DDR SDRAM I<sub>DD</sub> spec table**

Symbol	B3(DDR333@CL=2.5)		A2(DDR266@CL=2)		B0(DDR266@CL=2.5)		A0(DDR200@CL=2)		Unit	Notes	
	typical	worst	typical	worst	typical	worst	typical	worst			
IDD0	TBD	840	TBD	680	TBD	680	TBD	640	mA		
IDD1	TBD	1120	TBD	1000	TBD	1000	TBD	960	mA		
IDD2P	TBD	32	TBD	24	TBD	24	TBD	24	mA		
IDD2F	TBD	256	TBD	216	TBD	216	TBD	184	mA		
IDD2Q	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA		
IDD3P	TBD	296	TBD	256	TBD	256	TBD	240	mA		
IDD3N	TBD	480	TBD	400	TBD	400	TBD	360	mA		
IDD4R	TBD	1360	TBD	1240	TBD	1240	TBD	1080	mA		
IDD4W	TBD	1480	TBD	1120	TBD	1120	TBD	960	mA		
IDD5	TBD	1560	TBD	1320	TBD	1320	TBD	1200	mA		
IDD6	Normal	TBD	24	TBD	24	TBD	24	TBD	24	mA	
	Low power	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA	Optional
IDD7A	TBD	2800	TBD	2360	TBD	2360	TBD	1920	mA		

\* Module I<sub>DD</sub> was calculated on the basis of component I<sub>DD</sub> and can be differently measured according to DQ loading cap.

**< Detailed test conditions for DDR SDRAM IDD1 & IDD7A >**

**IDD1 : Operating current: One bank operation**

1. Typical Case : V<sub>dd</sub> = 2.5V, T=25' C
2. Worst Case : V<sub>dd</sub> = 2.7V, T= 10' C
3. Only one bank is accessed with t<sub>RC</sub>(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I<sub>out</sub> = 0mA
4. Timing patterns
  - DDR200(100Mhz, CL=2) : t<sub>CK</sub> = 10ns, CL2, BL=4, t<sub>RCD</sub> = 2\*t<sub>CK</sub>, t<sub>RAS</sub> = 5\*t<sub>CK</sub>  
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing  
\*50% of data changing at every burst
  - DDR266B(133Mhz, CL=2.5) : t<sub>CK</sub> = 7.5ns, CL=2.5, BL=4, t<sub>RCD</sub> = 3\*t<sub>CK</sub>, t<sub>RC</sub> = 9\*t<sub>CK</sub>, t<sub>RAS</sub> = 5\*t<sub>CK</sub>  
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing  
\*50% of data changing at every burst
  - DDR266A (133Mhz, CL=2) : t<sub>CK</sub> = 7.5ns, CL=2, BL=4, t<sub>RCD</sub> = 3\*t<sub>CK</sub>, t<sub>RC</sub> = 9\*t<sub>CK</sub>, t<sub>RAS</sub> = 5\*t<sub>CK</sub>  
Read : A0 N N R0 N P0 N N A0 N - repeat the same timing with random address changing  
\*50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

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### IDD7A : Operating current: Four bank operation

1. Typical Case : Vdd = 2.5V, T=25' C
2. Worst Case : Vdd = 2.7V, T= 10' C
3. Four banks are being interleaved with tRC(min), Burst Mode, Address and Control inputs on NOP edge are not changing. Iout = 0mA
4. Timing patterns
  - DDR200(100Mhz, CL=2) : tCK = 10ns, CL2, BL=4, tRRD = 2\*tCK, tRCD= 3\*tCK, Read with autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 - repeat the same timing with random address changing  
\*100% of data changing at every burst
  - DDR266B(133Mhz, CL=2.5) : tCK = 7.5ns, CL=2.5, BL=4, tRRD = 2\*tCK, tRCD = 3\*tCK  
Read with autoprecharge  
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing  
\*100% of data changing at every burst
  - DDR266A (133Mhz, CL=2) : tCK = 7.5ns, CL=2, BL=4, tRRD = 2\*tCK, tRCD = 3\*tCK  
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing  
\*100% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

### AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH(AC)	VREF + 0.31		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	VIL(AC)		VREF - 0.31	V	3
Input Differential Voltage, CK and CK inputs	VID(AC)	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and CK inputs	VIX(AC)	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

- Note 1. VID is the magnitude of the difference between the input level on CK and the input on  $\overline{CK}$ .
2. The value of  $V_{IX}$  is expected to equal  $0.5*V_{DDQ}$  of the transmitting device and must track variations in the DC level of the same.
3. These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relative to a Vref envelope that has been bandwidth limited 20MHz.

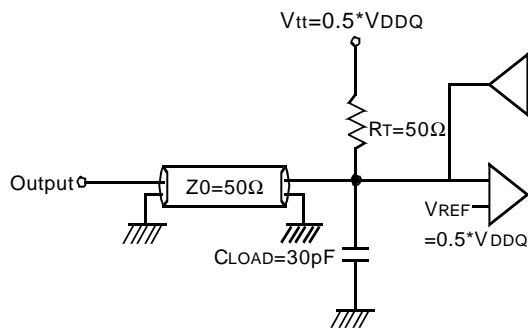


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**AC OPERATING TEST CONDITIONS** ( $V_{DD}=2.5V$ ,  $V_{DDQ}=2.5V$ ,  $T_A=0$  to  $70^{\circ}C$ )

Parameter	Value	Unit	Note
Input reference voltage for Clock	$0.5 * V_{DDQ}$	V	
Input signal maximum peak swing	1.5	V	
Input Levels( $V_{IH}/V_{IL}$ )	$V_{REF}+0.31/V_{REF}-0.31$	V	
Input timing measurement reference level	$V_{REF}$	V	
Output timing measurement reference level	$V_{tt}$	V	
Output load condition	See Load Circuit		



Output Load Circuit (SSTL\_2)

**Input/Output CAPACITANCE** ( $V_{DD}=2.5V$ ,  $V_{DDQ}=2.5V$ ,  $T_A=25^{\circ}C$ ,  $f=1MHz$ )

Parameter	Symbol	Min	Max	Unit
Input capacitance( $A_0 \sim A_{12}$ , $BA_0 \sim BA_1, \overline{RAS}, \overline{CAS}, \overline{WE}$ )	CIN1	49	57	pF
Input capacitance( $\overline{CKE_0}$ )	CIN2	42	50	pF
Input capacitance( $\overline{CS_0}$ )	CIN3	42	50	pF
Input capacitance( $CLK_0, CLK_1, CLK_2$ )	CIN4	22	25	pF
Data & DQS input/output capacitance( $DQ_0 \sim DQ_{63}$ )	COUT	6	8	pF
Input capacitance( $DM_0 \sim DM_8$ )	CIN5	6	8	pF

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**AC Timing Parameters & Specifications (These AC characteristics were tested on the Component)**

Parameter	Symbol	-TCA2(DDR266A)		-TCB0(DDR266B)		-TCA0 (DDR200)		Unit	Note	
		Min	Max	Min	Max	Min	Max			
Row cycle time	tRC	65		65		70		ns		
Refresh row cycle time	tRFC	75		75		80		ns		
Row active time	tRAS	45	120K	45	120K	48	120K	ns		
RAS to CAS delay	tRCD	20		20		20		ns		
Row precharge time	tRP	20		20		20		ns		
Row active to Row active delay	tRRD	15		15		15		ns		
Write recovery time	tWR	2		2		2		tCK		
Last data in to Read command	tCDLR	1		1		1		tCK		
Col. address to Col. address delay	tCCD	1		1		1		tCK		
Clock cycle time	tCK	CL=2.0	7.5	12	10	12	10	12	ns	5
		CL=2.5	7.5	12	7.5	12		12	ns	5
Clock high level width	tCH	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	0.45	0.55	0.45	0.55	tCK		
DQS-out access time from CK/CK	tDQSK	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Output data access time from CK/CK	tAC	-0.75	+0.75	-0.75	+0.75	-0.8	+0.8	ns		
Data strobe edge to output data edge	tDQSQ	-	+0.5	-	+0.5	-	+0.6	ns	5	
Read Preamble	tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	0.4	0.6	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	0.75	1.25	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		0		0		ns	2	
DQS-in hold time	tWPREH	0.25		0.25		0.25		tCK		
DQS falling edge to CK rising-setup time	tDSS	0.2		0.2		0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		0.2		0.2		tCK		
DQS-in high level width	tDQSH	0.35		0.35		0.35		tCK		
DQS-in low level width	tDQSL	0.35		0.35		0.35		tCK		
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	0.9	1.1	tCK		
Address and Control Input setup time	tIS	0.9		0.9		1.1		ns	6	
Address and Control Input hold time	tIH	0.9		0.9		1.1		ns	6	
Data-out high impedance time from CK/CK	tHZ	tACmin - 400ps	tACmax - 400ps	tACmin - 400ps	tACmax - 400ps	tACmin - 400ps	tACmax - 400ps	ps		
Data-out low impedance time from CK/CK	tLZ	tACmin - 400ps	tACmax - 400ps	tACmin - 400ps	tACmax - 400ps	tACmin - 400ps	tACmax - 400ps	ps		
Input Slew Rate(for input only pins)	tSL(I)	0.5		0.5		0.5		V/ns	6	
Input Slew Rate(for I/O pins)	tSL(IO)	0.5		0.5		0.5		V/ns	7	
Output Slew Rate(x4,x8)	tSL(O)	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	10	
Output Slew Rate(x16)	tSL(O)	0.7	5	0.7	5	0.7	5	V/ns	10	
Output Slew Rate Matching Ratio(rise to fall)	tSLMR	0.67	1.5	0.67	1.5	0.67	1.5			

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Parameter	Symbol	-TCA2(DDR266A)		-TCB0(DDR266B)		-TCA0 (DDR200)		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	tMRD	15		15		16		ns	
DQ & DM setup time to DQS	tDS	0.5		0.5		0.6		ns	7,8,9
DQ & DM hold time to DQS	tDH	0.5		0.5		0.6		ns	7,8,9
DQ & DM input pulse width	tDIPW	1.75		1.75		2		ns	
Power down exit time	tPDEX	10		10		10		ns	
Exit self refresh to write command	tXSW	95				116		ns	
Exit self refresh to bank active command	tXSA	75		75		80		ns	4
Exit self refresh to read command	tXSR	200		200		200		Cycle	
Refresh interval time	64Mb, 128Mb	tREF	15.6		15.6		15.6	us	1
	256Mb		7.8		7.8		7.8	us	1
Output DQS valid window	tQH	tHPmin -tQHS	-	tHPmin -tQHS	-	tHPmin -tQHS	-	ns	5
Clock half period	tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.75		0.75		0.8	ns	
DQS write postamble time	tWPST	0.25		0.25		0.25		tCK	3

Note : 1. Maximum burst refresh of 8

2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High\_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.

3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.

4. A write command can be applied with tRCD satisfied after this command.

5. For registered DINNs, tCL and tCH are ≥ 45% of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.

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### 6. Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	$\Delta t_{IS}$	$\Delta t_{IH}$
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase  $t_{IS}/t_{IH}$  in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

### 7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	$\Delta t_{DS}$	$\Delta t_{DH}$
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase  $t_{DS}/t_{DH}$  in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

### 8. I/O Setup/Hold Plateau Derating

I/O Input Level	$\Delta t_{DS}$	$\Delta t_{DH}$
(mV)	(ps)	(ps)
$\pm 280$	+50	+50

This derating table is used to increase  $t_{DS}/t_{DH}$  in the case where the input level is flat below  $V_{REF} \pm 310\text{mV}$  for a duration of up to 2ns.

### 9. I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Delta Rise/Fall Rate	$\Delta t_{DS}$	$\Delta t_{DH}$
(ns/V)	(ps)	(ps)
0	0	0
$\pm 0.25$	+50	+50
$\pm 0.5$	+100	+100

This derating table is used to increase  $t_{DS}/t_{DH}$  in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calated as  $1/\text{SlewRate1}-1/\text{SlewRate2}$ . For example, if slew rate 1 = 5V/ns and slew rate 2 = .4V/ns then the Delta Rise/Fall Rate = -0/5ns/V. Input S/H slew rate based on larger of AC-AC delta rise/fall rate and DC-DC delta rise/fall rate.

### 10. This parameter is fir system simulation purpose. It is guaranteed by design.

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**AC Timing Parameters & Specifications (These AC characteristics were tested on the Component)**

Parameter	Symbol	-TCB3(DDR333)		Unit	Note	
		Min	Max			
Row cycle time	tRC	60		ns		
Refresh row cycle time	tRFC	72		ns		
Row active time	tRAS	42	70K	ns		
RAS to CAS delay	tRCD	18		ns		
Row precharge time	tRP	18		ns		
Row active to Row active delay	tRRD	12		ns		
Write recovery time	tWR	15		ns		
Last data in to Read command	tCDLR	1		tCK		
Clock cycle time	tCK	CL=2.0	7.5	12	ns	4
		CL=2.5	6	12	ns	4
Clock high level width	tCH	0.45	0.55	tCK		
Clock low level width	tCL	0.45	0.55	tCK		
DQS-out access time from CK/ $\overline{\text{CK}}$	tDQSK	-0.6	+0.6	ns		
Output data access time from CK/ $\overline{\text{CK}}$	tAC	-0.7	+0.7	ns		
Data strobe edge to output data edge	tDQSQ	-	0.45	ns	4	
Read Preamble	tRPRE	0.9	1.1	tCK		
Read Postamble	tRPST	0.4	0.6	tCK		
CK to valid DQS-in	tDQSS	0.75	1.25	tCK		
DQS-in setup time	tWPRES	0		ns	2	
Write Preamble	tWPRE	0.25		tCK		
Write Postamble	tWPST	0.4	0.6	tCK	3	
DQS falling edge to CK rising-setup time	tDSS	0.2		tCK		
DQS falling edge from CK rising-hold time	tDSH	0.2		tCK		
DQS-in high level width	tDQSH	0.35		tCK		
DQS-in low level width	tDQSL	0.35		tCK		
Address and Control Input setup/hold time (fast slew rate)	tIS/tIH	0.75		ns		
Address and Control Input setup/hold time (slow slew rate)	tIS/tIH	0.8		ns		
DQ and DM input setup time	tDS	0.45		ns		
DQ and DM input hold time	tDH	0.45		ns		
Data-out high impedance time from CK/ $\overline{\text{CK}}$	tHZ	-0.7	+0.7	ps		
Data-out low impedance time from CK/ $\overline{\text{CK}}$	tLZ	-0.7	+0.7	ps		

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Parameter	Symbol	-TCB3(DDR333)		Unit	Note
		Min	Max		
Mode register set cycle time	tMRD	2		tCK	
Control & Address input pulse width (for each input)	tIPW	2.2		ns	
DQ & DM input pulse width(for each input)	tDIPW	1.75		ns	
Exit self refresh to non read command	tXSNR	75		ns	
Exit self refresh to read command	tXSRD	200		tCK	
Refresh interval time	tREFI	64Mb, 128Mb	15.6	us	1
		256Mb	7.8	us	1
Output DQS valid window	tQH	tHP-tQHS	-	ns	4
Clock half period	tHP	tCLmin or tCHmin	-	ns	
Data hold skew factor	tQHS		0.55	ns	
DQS write postamble time	tRAP	tRCD or tRAS min		ns	3
Auto Precharge Write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		tCK	

1. Maximum burst refresh of 8
2. The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High\_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.
3. The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
4. For registered DIMMs, tCL and tCH are  $\geq 45\%$  of the period including both the half period jitter (tJIT(HP)) of the PLL and the half period jitter due to crosstalk (tJIT(crosstalk)) on the DIMM.

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**Command Truth Table**

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A11, A12 A9 ~ A0	Note	
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X		3	
	Self Refresh	Entry		L							3	
		Exit	L	H	L	H	H	H	X		3	
	H		X	X	X	3						
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable								H	4		
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address (A0~A9)	4
	Auto Precharge Enable									H		4, 6
Burst Stop		H	X	L	H	H	L	X			7	
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		5
Active Power Down	Entry	H	L	H	X	X	X	X				
				L	V	V	V					
	Exit	L	H	X	X	X	X					
Precharge Power Down Mode	Entry	H	L	H	X	X	X	X				
				L	H	H	H					
	Exit	L	H	H	X	X	X					
				L	V	V	V					
DM		H	X					X		8		
No operation (NOP) : Not defined		H	X	H	X	X	X	X		9		
				L	H	H	H			9		

Note : 1. OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)

2. EMRS/ MRS can be issued only at all banks precharge state.

A new command can be issued 2 clock cycles after EMRS or MRS.

3. Auto refresh functions are same as the CBR refresh of DRAM.

The automatical precharge without row precharge command is meant by "Auto".

Auto/self refresh can be issued only at all banks precharge state.

4. BA0 ~ BA1 : Bank select addresses.

If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.

If both BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.

If both BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.

If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.

5. If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.

6. During burst write with auto precharge, new read/write command can not be issued.

Another bank read/write command can be issued after the end of burst.

New row active of the associated bank can be issued at TRP after the end of burst.

7. Burst stop command is valid at every burst length.

8. DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).

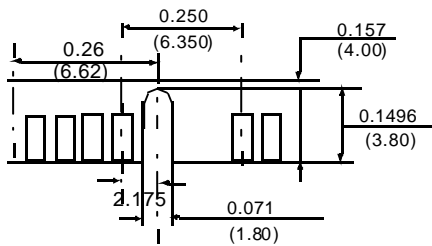
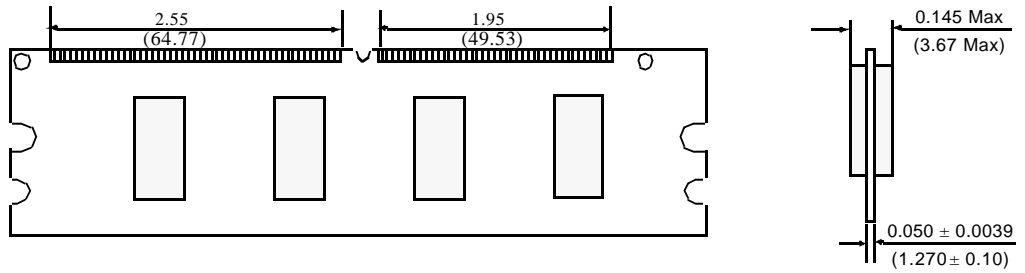
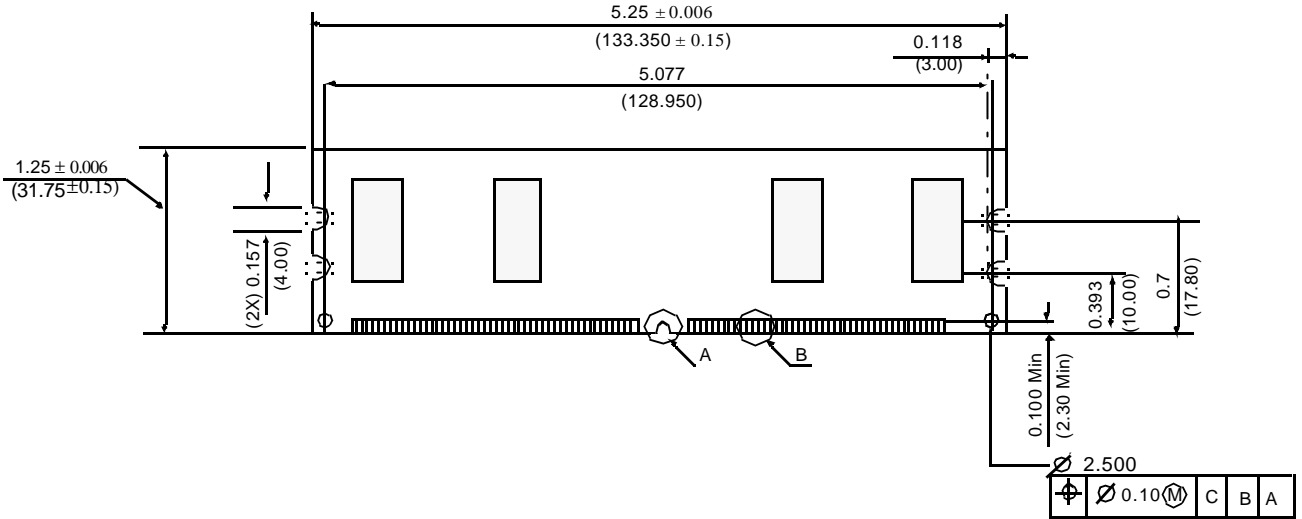
9. This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

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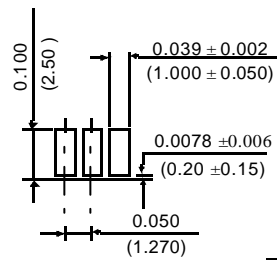
**184pin Unbuffered DDR SDRAM MODULE**

**PACKAGE DIMENSIONS**

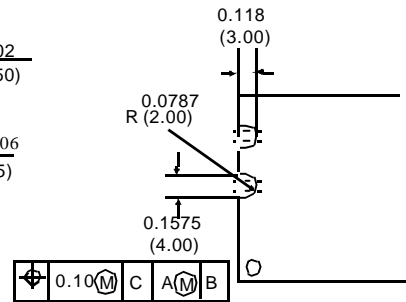
Units : Inches (Millimeters)



Detail A



Detail B



Tolerances : ± 0.005(.13) unless otherwise specified.  
 The used device is 32Mx8 SDRAM, TSOP.  
 SDRAM Part NO : K4H560838C-TC