DDR2 1.55V Fully Buffered DIMM

240pin FBDIMMs based on 2Gb A-die

83FBGA with Lead-Free and Halogen-Free (RoHS compliant)

Table of Contents

Revision History

Revision	Month	Year	History
1.0	April	2008	- Initial release
1.1	August	2008	- Added up 2Rx8 product

1.0 FEATURES

- 240pin fully buffered dual in-line memory module (FB-DIMM)
- 3.2Gb/s, 4.0Gb/s link transfer rate
- 1.55V +/- 0.05V Power Supply for DRAM V_{DD}/V_{DDQ}
- Backward compatible to1.8V +/- 0.1V Power Supply for DRAM V_{DD}/V_{DDQ}
- 1.5V +0.075/-0.045V Power Supply for AMB V_{CC}
- 3.3V +/- 0.3V Power Supply for V_{DDSPD}
- Buffer Interface with high-speed differential point-to-point Link at 1.5 volt
- Channel error detection & reporting
- Channel fail over mode support
- Serial presence detect with EEPROM
- 8 Banks
- Posted CAS
- Programmable CAS Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1, 2, 3, 4
- Automatic DDR2 DRAM bus and channel calibration
- MBIST and IBIST Test functions
- Hot add-on and Hot Remove Capability
- Transparent mode for DRAM test support

Table 1 : Ordering Information

Part Number	Density	Organization	Component Composition	Number of Rank	AMB	Type of Heat Spreader	Height
M395T5263AZ4-YE68	4GB	512M x 72	256Mx8(K4T2G084QA) *18EA	2	IDT L4	Full Module	30.35mm
M395T1K66AZ4-YE68	8GB	1G x 72	st. 1Gx4(K4T4G264QA) *18EA	2			

Note :
1. “Z” of Part number(11th digit) stands for Lead-Free products.
2. “Y” of Part number(14th digit) stands for Low Voltage product.
3. The last digit stands for AMB.

Table 2 : Performance range

	E6(DDR2-667)	Unit
DDR2 DRAM Speed	667	Mbps
CL-tRCD-tRP	5-5-5	CK

Table 3 : Address Configuration

Organization	Row Address	Column Address	Bank Address	Auto Precharge
512Mx4(2Gb) based Module	A0-A14	A0-A9, A11	BA0-BA2	A10
256Mbx8(2Gb) based Module	A0-A14	A0-A9	BA0-BA2	A10

2.0 FBDIMM GENERALS

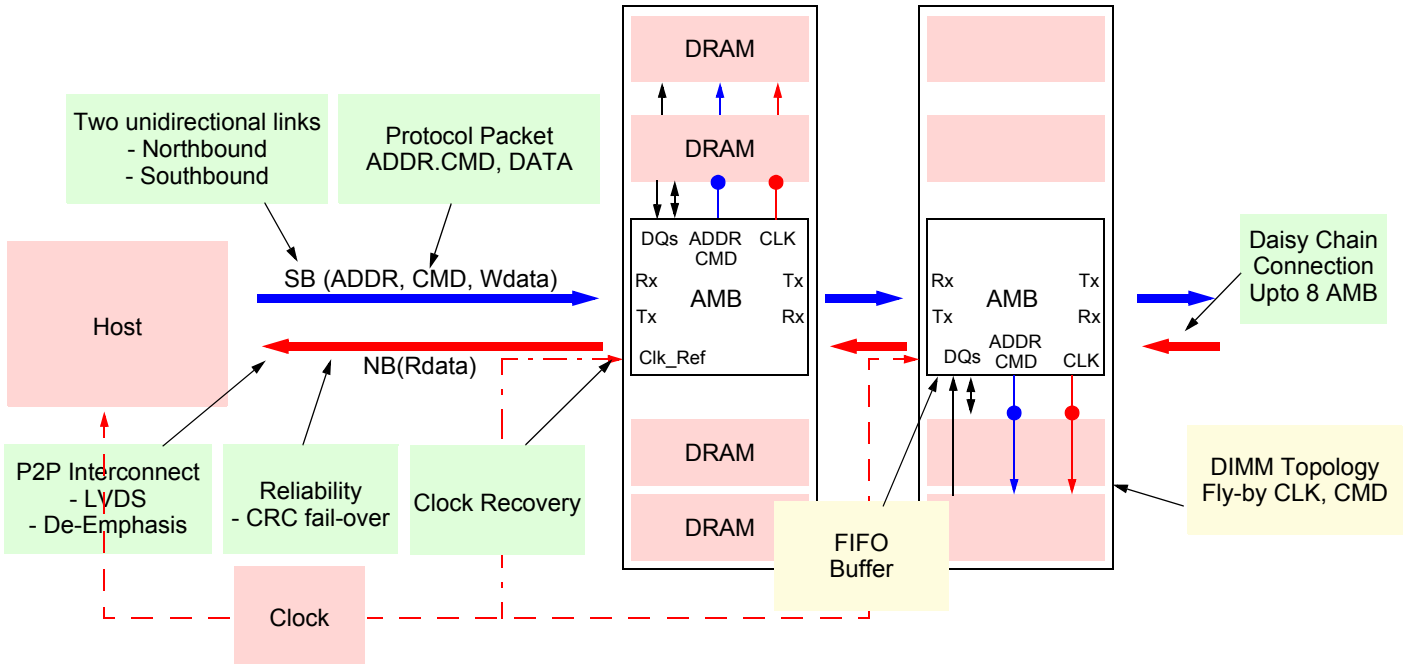
2.1 FB-DIMM Operation Overview

FB-DIMM (Fully Buffered Dual in Line Memory Module) is designed for the applications which require higher data transfer bandwidth and scalable memory capacity. The memory slot access rate per channel decreases as the memory bus speed increases, resulting in limited density build-up as channel speeds increase with memory system having the stub-bus architecture. FB-DIMM solution is intended to eliminate this stub-bus channel bottleneck by using point-to-point links that enable multiple memory modules to be connected serially to a given channel.

Memory system architecture perspective, FB-DIMM is fully differentiated from Registered DIMM and Unbuffered DIMM. A lot of new technologies are integrated into this solution in order to achieve this scalable higher speed memory solution. Serial link interface with packet data format and dedicated read/write paths are key attribute in FB-DIMM protocol. Point to Point interconnect with fully differential signaling and de-emphasis scheme are key attribute in FBD channel link. Clock recovery by using data stream is key attribute in FBD clocking. FB-DIMM supports both clock resync and resampling mode options. CRC (Cyclic Redundancy Check) bits are transferred with data stream for reliability at high speed data transaction. Failover mechanism supports system running with dynamic IO failure. Finally all FB-DIMM is connected in daisy chain manner. Thus, every interconnection between AMB (advanced memory buffer) to AMB, AMB to Host and AMB to DRAM, is point to point interconnection which allows higher data transfer bandwidth.

Figure 1 shows a lot of new technologies integrated with FBD solution.

Figure 1 : FB-DIMM Memory System Overview

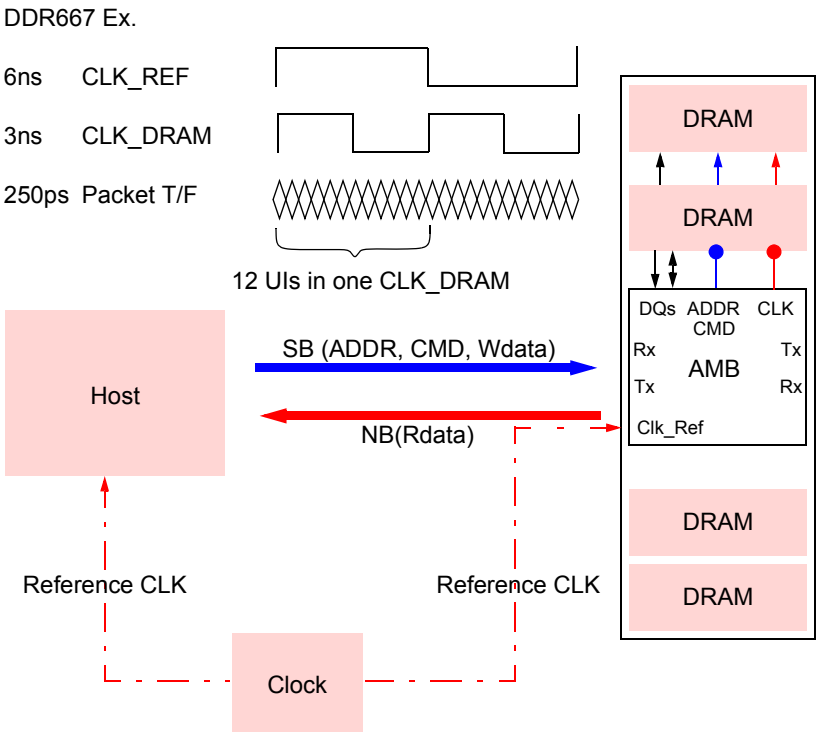


2.2 FB-DIMM Channel Frequency Scaling

There are many frequency parameters including reference clock frequency, DRAM clock frequency, DRAM data transfer rate, channel transfer rate and channel unit interval. All of frequency parameters are scaled with a certain gear ratio. External clock source provides reference clock input to AMB and Host. External clock source is relatively slower than channel and DRAM frequency. Thus, AMB doubles external clock input and generates clock inputs to DRAMs. DRAM use clock input from AMB which is two times faster than reference clock for DRAM operation. DRAM data transfer rate is two times faster than DRAM clock input with nature of double data rate operation and four times faster than external clock source. Channel speed is represented by unit interval - average time interval between voltage transitions of a signal in the FBD channel. It is six times faster than DRAM data transfer rate. For example, external clock source gives 6ns clock (166MHz), AMB doubles it and gives 3ns clock (333MHz) to DRAM and FBD channel communicate with unit interval - 250ps (4.0Gbps transfer rate).

Figure 2 shows frequency scale ratio over frequency parameters in FBD memory system.

Figure 2 : FB-DIMM Speed Scaling

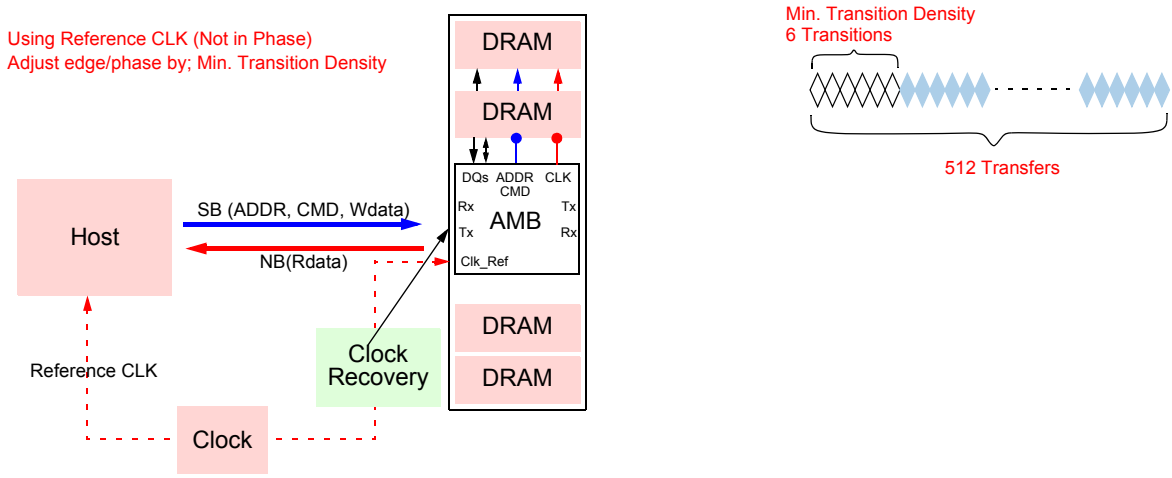


	UI	CLK_DRAM	CLK_REF	Frequency
DDR2-533	312.5ps	266MHz	133MHz	3.2Gb/s
DDR2-667	250ps	333MHz	166MHz	4.0Gb/s
DDR2-800	208.33ps	400MHz	200MHz	4.8Gb/s

2.3 FB-DIMM Clocking Scheme

In FB-DIMM platform design, phase adjustment among reference clock inputs to each individual AMB and host is not taken account. Thus, clock synchronization is made by using both external reference clock and channel data stream in FB-DIMM memory system. Host and each individual AMB has a each individual IO basis clock recovery circuitry for channel data communication. It runs with inputs from PLL inside chip and data stream from the other AMB or Host. Because data stream itself involves data communication process, no signaling switching or data communication may loss clock synchronization between transmitter and receiver. Thus, min transition density is defined for this purpose. In FBD channel, a density of 6 transitions within 512 transfers or unit intervals (UI) on the channel is required for interpolator training.

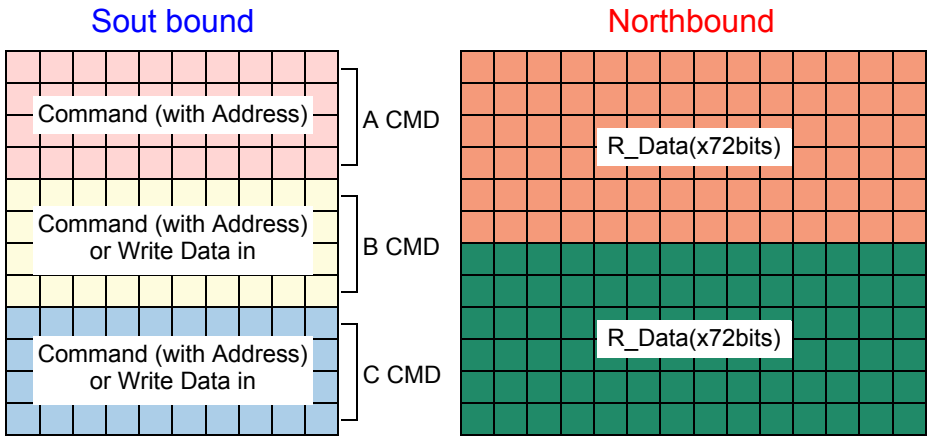
Figure 3 : FB-DIMM Clocking



2.4 FB-DIMM Protocol

FB-DIMM channel has two unidirectional communication paths - south bound and north bound. South bound and north bound use physically different signal path. South and north mean direction of signal transaction. Southbound means direction of signals running from the host controller toward the DIMMs. North is the opposite of south. Due to nature of memory operation, southbound carries information including command to DRAM, address to DRAM and write data to DRAM, while north bound carries read data from DRAM. In channel protocol point of view, southbound and northbound have different data frame formats and frame format size is optimized to ratio of read and write. Data transfer perspective, read data transfer rate of north bound is twice faster than write data transfer. Higher channel utilization achieves with asymmetric read and write data transfer rate.

Figure 4 : Southbound / Northbound Frame format

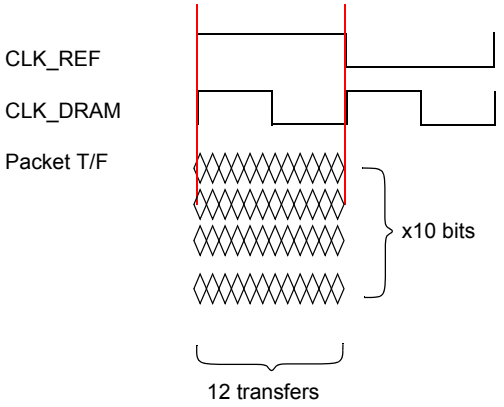


Southbound consists of 10 differential signal pairs (lane), physically 20 signaling line. Southbound Format has 10x12 (10 IO (or Lane) x 12 IO switching) frame format, which deliver 10x12 bit information per one DRAM clock. One south bound frame is divided into three command slot. See figure 5. Command slot A delivers command (with address). Command slot B and C delivers command (with address) or write data into DRAM.

Figure 5 : FBDIMM Command Encoding & SB Frame

Southbound Command Frame Format*

Transfer \ Bit	9	8	7	6	5	4	3	2	1	0	
0	aE0	aE7	aE8	F0=0	aC20	aC16	aC12	aC8	aC4	aC0	A CMD
1	aE1	aE6	aE9	F1=0	aC21	aC17	aC13	aC9	aC5	aC1	
2	aE2	aE5	aE10	aE13	aC22	aC18	aC14	aC10	aC6	aC2	
3	aE3	aE4	aE11	aE12	aC23	aC19	aC15	aC11	aC7	aC3	
4	FE21	0	0	0	bC20	bC16	bC12	bC8	bC4	bC0	B CMD
5	FE20	0	0	0	bC21	bC17	bC13	bC9	bC5	bC1	
6	FE19	0	0	0	bC22	bC18	bC14	bC10	bC6	bC2	
7	FE18	0	0	0	bC23	bC19	bC15	bC11	bC7	bC3	
8	FE17	0	0	0	cC20	cC16	cC12	cC8	cC4	cC0	C CMD
9	FE16	0	0	0	cC21	cC17	cC13	cC9	cC5	cC1	
10	FE15	0	0	0	cC22	cC18	cC14	cC10	cC6	cC2	
11	FE14	0	0	0	cC23	cC19	cC15	cC11	cC7	cC3	
	FE0	FE7	FE11								
	FE1	FE6	FE10								
	FE2	FE5	FE9	FE13							
	FE3	FE4	FE8	FE12							



Note :
1. aE[0~12] : CRC Checksum of the A Command
2. F[0~1] : Frame Type
3. FE[0~21] : CRC Checksum of 72bit data
4. CRC : Cyclic Redundancy Check

DRAM Cmnds	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Activate	DS2	DS1	DS0	1	DRAM Addr		RS	DRAM Bank & Address																
Write	DS2	DS1	DS0	0	1	1	RS	DRAM Bank & Address																
Read	DS2	DS1	DS0	0	1	0	RS	DRAM Bank & Address																
Precharge All	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	1	1	1	X	X	X	X	X	X	X	X	X	X
Precharge Single	DS2	DS1	DS0	0	0	1	RS	DRAM Bank				1	1	0	X	X	X	X	X	X	X	X	X	X
Auto (CBR) Refresh	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	1	0	1	X	X	X	X	X	X	X	X	X	X
Enter Self Refresh	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	1	0	0	X	X	X	X	X	X	X	X	X	X
Exit Self Refresh/ Exit Power Down	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	0	1	1	X	X	X	X	X	X	X	X	X	X
Enter Power Down	DS2	DS1	DS0	0	0	1	RS	X	X	X	X	0	1	0	X	X	X	X	X	X	X	X	X	X
reserved	X	X	X	0	0	1	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X	X	X	X

Note : The values in " X" fields in non-reserved commands above may be driven onto the DRAM device pins.

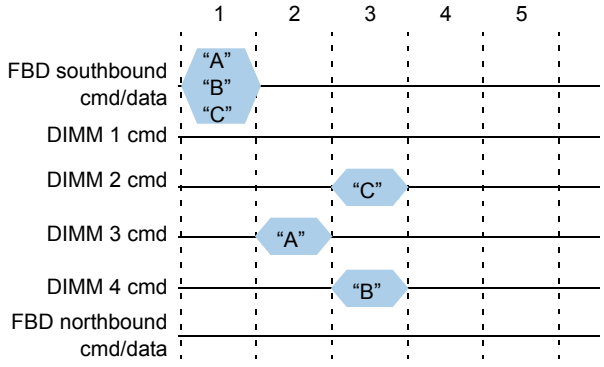
2.5 Southbound Command Delivery

A DRAM command located in the "A" command may be delivered to the DRAM devices as soon as the 14-bit (10-bits in fail-over) CRC is checked. This minimizes DRAM access latency by allowing the command to be delivered after the first 4 transfers of the frame have been received. The "A" command is transferred immediately to the DRAM pins with minimum delay whereas the "B" and "C" command are delivered one DRAM clock later. To minimize memory access latency the read related Activate, Read (if the page is open) and explicit Precharge commands to a rank of DRAM devices should be placed in the "A" command, if possible. Figure 6 illustrates the delivery of the three potential commands in a frame to three separate DRAM channels.

Command "A" is delivered in this case to the DRAM devices on DIMM 3 as soon as the command can traverse the AMB buffer. The "B" and "C" commands are delayed and presented to two other DRAM channels on the following clock. See below figure7~10 for Basic Read & Write Operations

Northbound consists of 14 differential signal pairs (lane), physically 28 signaling line. Southbound Format has 14x12 (14 IO (or Lane) x 12 IO switching) frame format, which deliver 14x12 bit information per one DRAM clock. One north bound frame is divided into two. Both frame deliver read data from DRAM

Figure 6 : FBDIMM Command Delivery Rules



1. CMD A transferred immediately
2. CMD A, B, C cannot target the same DIMM
3. Host is responsible for scheduling CMD

2.6 Basic Timing Diagram

Figure 7 : Basic DRAM Read Data Transfers on FBD

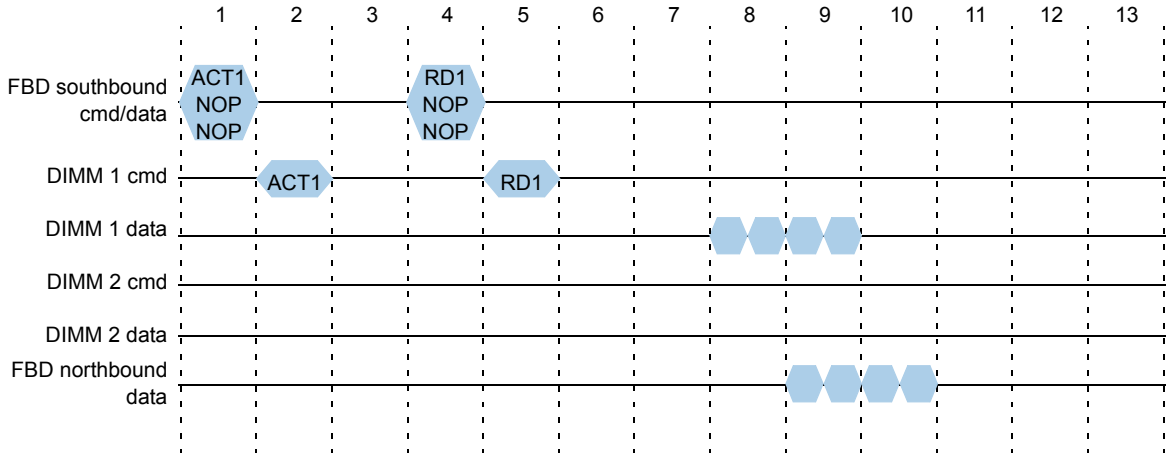


Figure 8 : Back to Back DRAM Read Data Transfers

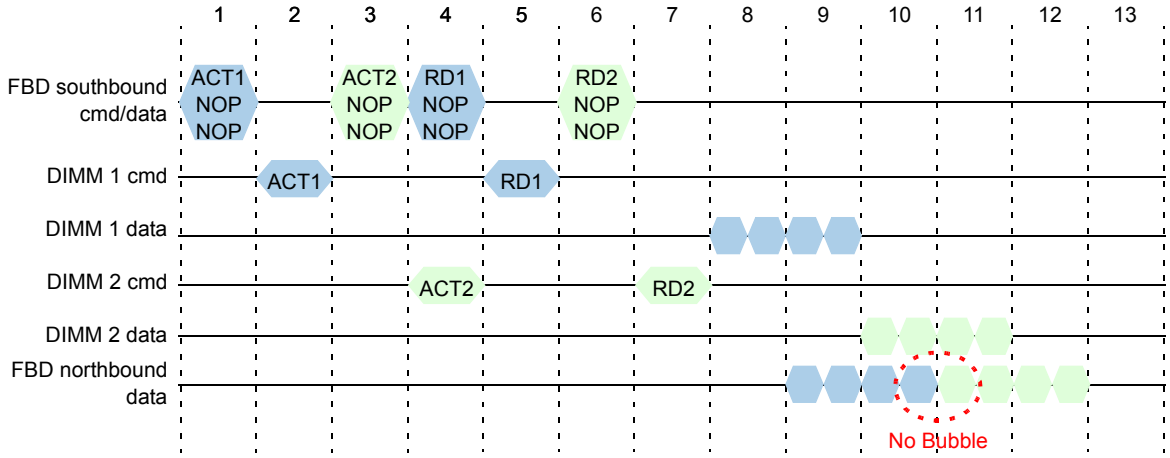


Figure 9 : Basic DRAM Write Data Transfers on FBD

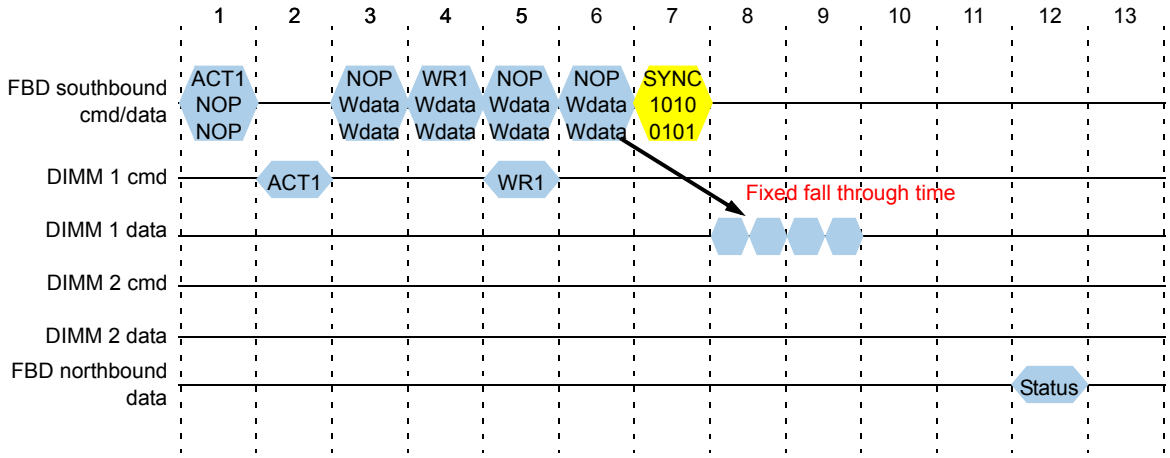
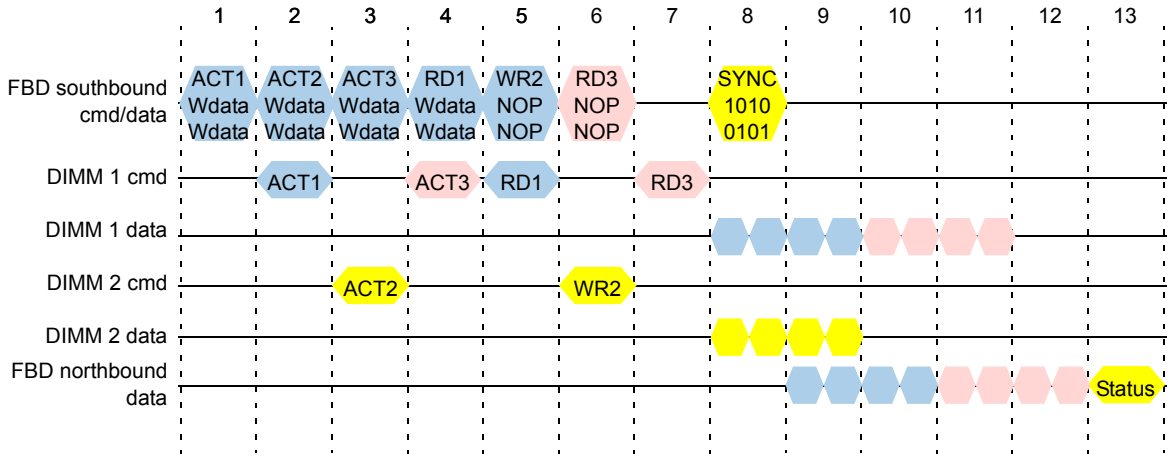
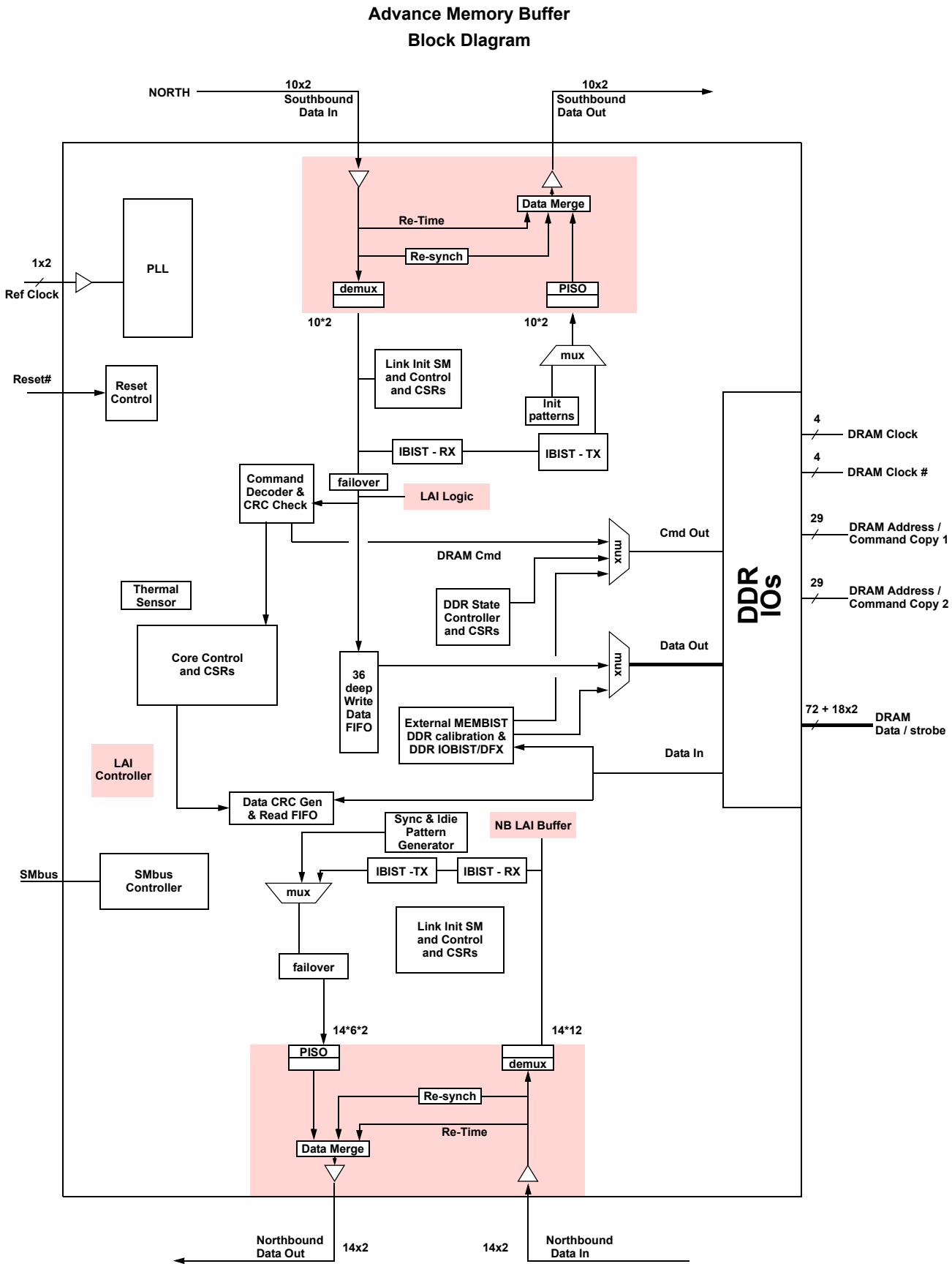


Figure 10 : Simultaneous RD / WR Data TransferS



2.7 Advanced Memory Buffer Block Diagram

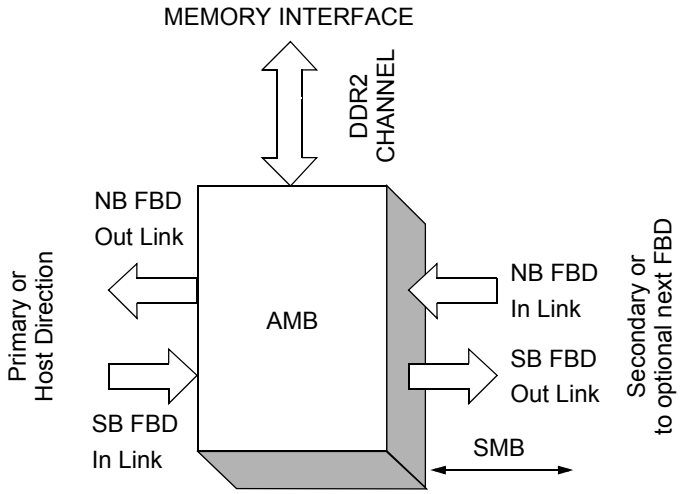
Figure 11 : Advanced Memory Buffer Block Diagram



2.8 Interfaces

Figure12 illustrates the Advanced Memory Buffer and all of its interfaces. They consist of two FBD links, one DDR2 channel and an SM-Bus interface. Each FBD link connects the Advanced Memory Buffer to a host memory controller or an adjacent FBD. The DDR2 channel supports direct connection to the DDR2 SDRAMs on a Fully Buffered DIMM

Figure 12 : Advanced Memory Buffer Interface Block Diagram



The FBDIMM channel uses a daisy-chain topology to provide expansion from a single DIMM per channel to up to 8 DIMMs per channel. The host sends data on the southbound link to the first DIMM where it is received and redriven to the second DIMM. On the southbound data path each DIMM receives the data and again redrives the data to the next DIMM until the last DIMM receives the data. The last DIMM in the chain initiates the transmission of data in the direction of the host (a.k.a. northbound). On the northbound data path each DIMM receives the data and re-drives the data to the next DIMM until the host is reached.

3.0 FBD HIGH-SPEED DIFFERENTIAL POINT TO POINT LINK (at 1.5 V) INTERFACE

The Advanced Memory Buffer supports one FBD Channel consisting of two bidirectional link interfaces using high-speed differential point-to-point electrical signaling.

The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FBD.

The northbound input link is 14 lanes wide and carries read return data or status information from the next FBDIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally.

3.1 DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data signals, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four-transfer bursts are driven on the data and check-bit lines at 800 MHz.

Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using write/read trial and error (or equivalent implementation). Hardware aligns the read data and check-bits to a single core clock.

The Advanced Memory Buffer provides four copies of the command clock phase references (CLK[3:0]) and write data/check-bit.

3.2 SMBus Slave Interface

The Advanced Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the FBD link. The Advanced Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz. SMBus access to the Advanced Memory Buffer may be a requirement to boot a system. This provides a mechanism to set link strength, frequency and other parameters needed to insure robust operation given platform specific configurations. It is also required for diagnostic support when the link is down. The SMBus address straps located on the DIMM connector are used by the Advanced Memory Buffer to get its unique ID.

3.3 FBD Channel Latency

FBD channel latency is measured from the time a read request is driven on the FBD channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller.
When not using the Variable Read Latency capability, the latency for a specific FBDIMM on an FBD channel is always equal to the latency for any other FBDIMM on that channel. However, the latency for each FBDIMM in a specific configuration with some number of FBDIMMs installed may not be equal to the latency for each FBDIMM in a configuration with some different number of FBDIMMs installed.
As more DIMMs are added to the FBD channel, additional latency is required to read from each DIMM on the channel. Because the FBD channel is based on the point-to-point interconnection of buffer components between DIMMs, memory requests are required to travel through N-1 buffers before reaching the Nth buffer. The result is that a four DIMM channel configuration will have greater idle read latency compared to a one DIMM channel configuration.
The Variable Read Latency capability can be used to reduce latency for DIMMs closer to the host.
The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.

3.4 Peak Theoretical Throughput

An FBD channel transfers read completion data on the FBD Northbound data connection. 144 bits of data are transferred for every FBD Northbound data frame. This matches the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 from a single channel or a DRAM burst of four from two lock-stepped channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).
The FBD frame rate matches the DRAM command clock because of the fixed 6:1 ratio of the FBD channel clock to the DRAM command clock. Therefore, the Northbound data connection will exhibit the same peak theoretical throughput as a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Northbound data connection is 4.267 GB/sec.
Write data is transferred on the FBD Southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every FBD Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 transfers from a single channel, or a burst of 4 from two lock-step channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).
When the FBD frame rate matches the DRAM command clock, the Southbound command and data connection will exhibit one half the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Southbound command and data connection is 2.133 GB/sec.
The total peak theoretical throughput for a single FBD channel is defined as the sum of the peak theoretical throughput of the Northbound data connection and the Southbound command and data connection. When the FBD frame rate matches the DRAM command clock, this is equal to 1.5 times the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical throughput of a DDR2 533 channel would be 4.267 GB/sec, while the peak theoretical throughput of an FBD-533 channel would be 6.4 GB/sec

3.5 Hot-add

The FBDIMM channel does not provide a mechanism to automatically detect and report the addition of a new FBDIMM south of the currently active last FBDIMM. It is assumed the system will be notified through some means of the addition of one or more new FBDIMMs so that specific commands can be sent to the host controller to initialize the newly added FBDIMM(s) and perform a hot-add reset to bring them into the channel timing domain. It should be noted that the power to the FBDIMM socket must be removed before a hot-add FBDIMM is inserted or removed. Applying or removing the power to a FBDIMM socket is a system platform function.

3.6 Hot remove

In order to accomplish removal of FBDIMMs, the host must perform a fast reset sequence targeted at the last FBDIMM that will be retained on the channel. The fast reset re-establishes the appropriate last FBDIMM so that the southbound transmission outputs of the last active FBDIMM and the southbound and northbound outputs of the FBDIMMs beyond the last active FBDIMM are disabled. Once the appropriate outputs are disabled, the system can coordinate the procedure to remove power in preparation for physical removal of the FBDIMM if needed. Note that the power to the FBDIMM socket must be removed before a hot-add FBDIMM is inserted or removed. Applying or removing the power to a FBDIMM socket is a system platform function.

3.7 Hot replace

Hot replace of FBDIMM is accomplished through combining the hot-remove and hotadd processes.

4.0 PIN CONFIGUREATION

Table 4 : DDR2 240 Pin FBDIMM Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{DD}	121	V_{DD}	31	PN3	151	SN3	61	$\overline{PN9}$	181	SN9	91	$\overline{PS9}$	211	$\overline{SS9}$
2	V_{DD}	122	V_{DD}	32	$\overline{PN3}$	152	$\overline{SN3}$	62	V_{SS}	182	V_{SS}	92	V_{SS}	212	V_{SS}
3	V_{DD}	123	V_{DD}	33	V_{SS}	153	V_{SS}	63	PN10	183	SN10	93	PS5	213	SS5
4	V_{SS}	124	V_{SS}	34	PN4	154	SN4	64	$\overline{PN10}$	184	$\overline{SN10}$	94	$\overline{PS5}$	214	$\overline{SS5}$
5	V_{DD}	125	V_{DD}	35	$\overline{PN4}$	155	$\overline{SN4}$	65	V_{SS}	185	V_{SS}	95	V_{SS}	215	V_{SS}
6	V_{DD}	126	V_{DD}	36	V_{SS}	156	V_{SS}	66	PN11	186	SN11	96	PS6	216	SS6
7	V_{DD}	127	V_{DD}	37	PN5	157	SN5	67	$\overline{PN11}$	187	$\overline{SN11}$	97	$\overline{PS6}$	217	$\overline{SS6}$
8	V_{SS}	128	V_{SS}	38	$\overline{PN5}$	158	$\overline{SN5}$	68	V_{SS}	188	V_{SS}	98	V_{SS}	218	V_{SS}
9	V_{CC}	129	V_{CC}	39	V_{SS}	159	V_{SS}	KEY				99	PS7	219	SS7
10	V_{CC}	130	V_{CC}	40	PN13	160	SN13	69	V_{SS}	189	V_{SS}	100	$\overline{PS7}$	220	$\overline{SS7}$
11	V_{SS}	131	V_{SS}	41	$\overline{PN13}$	161	$\overline{SN13}$	70	PS0	190	SS0	101	V_{SS}	221	V_{SS}
12	V_{CC}	132	V_{CC}	42	V_{SS}	162	V_{SS}	71	$\overline{PS0}$	191	$\overline{SS0}$	102	PS8	222	SS8
13	V_{CC}	133	V_{CC}	43	V_{SS}	163	V_{SS}	72	V_{SS}	192	V_{SS}	103	$\overline{PS8}$	223	$\overline{SS8}$
14	V_{SS}	134	V_{SS}	44	RFU*	164	RFU*	73	PS1	193	SS1	104	V_{SS}	224	V_{SS}
15	V_{TT}	135	V_{TT}	45	RFU*	165	RFU*	74	$\overline{PS1}$	194	$\overline{SS1}$	105	RFU**	225	RFU**
16	VID1	136	VID0	46	V_{SS}	166	V_{SS}	75	V_{SS}	195	V_{SS}	106	RFU**	226	RFU**
17	$\overline{RESET}$	137	DNU/M_Test	47	V_{SS}	167	V_{SS}	76	PS2	196	SS2	107	V_{SS}	227	V_{SS}
18	V_{SS}	138	V_{SS}	48	PN12	168	SN12	77	$\overline{PS2}$	197	$\overline{SS2}$	108	V_{DD}	228	SCK
19	RFU**	139	RFU**	49	$\overline{PN12}$	169	$\overline{SN12}$	78	V_{SS}	198	V_{SS}	109	V_{DD}	229	$\overline{SCK}$
20	RFU**	140	RFU**	50	V_{SS}	170	V_{SS}	79	PS3	199	SS3	110	V_{SS}	230	V_{SS}
21	V_{SS}	141	V_{SS}	51	PN6	171	SN6	80	$\overline{PS3}$	200	$\overline{SS3}$	111	V_{DD}	231	V_{DD}
22	PN0	142	SN0	52	$\overline{PN6}$	172	$\overline{SN6}$	81	V_{SS}	201	V_{SS}	112	V_{DD}	232	V_{DD}
23	$\overline{PN0}$	143	$\overline{SN0}$	53	V_{SS}	173	V_{SS}	82	PS4	202	SS4	113	V_{DD}	233	V_{DD}
24	V_{SS}	144	V_{SS}	54	PN7	174	SN7	83	$\overline{PS4}$	203	$\overline{SS4}$	114	V_{SS}	234	V_{SS}
25	PN1	145	SN1	55	$\overline{PN7}$	175	$\overline{SN7}$	84	V_{SS}	204	V_{SS}	115	V_{DD}	235	V_{DD}
26	$\overline{PN1}$	146	$\overline{SN1}$	56	V_{SS}	176	V_{SS}	85	V_{SS}	205	V_{SS}	116	V_{DD}	236	V_{DD}
27	V_{SS}	147	V_{SS}	57	PN8	177	SN8	86	RFU*	206	RFU*	117	V_{TT}	237	V_{TT}
28	PN2	148	SN2	58	$\overline{PN8}$	178	$\overline{SN8}$	87	RFU*	207	RFU*	118	SA2	238	V_{DDSPD}
29	$\overline{PN2}$	149	$\overline{SN2}$	59	V_{SS}	179	V_{SS}	88	V_{SS}	208	V_{SS}	119	SDA	239	SA0
30	V_{SS}	150	V_{SS}	60	PN9	180	SN9	89	V_{SS}	209	V_{SS}	120	SCL	240	SA1
								90	PS9	210	SS9				

RFU = Reserved Future Use.
* These pin positions are reserved for forwarded clocks to be used in future module implementations
** These pin positions are reserved for future architecture flexibility

1. The following signals are CRC bits and thus appear out of the normal sequence : PN12/$\overline{PN12}$, SN12/$\overline{SN12}$, PN13/$\overline{PN13}$, SN13/$\overline{SN12}$, PS9/$\overline{PS9}$, SS9/$\overline{SS9}$.

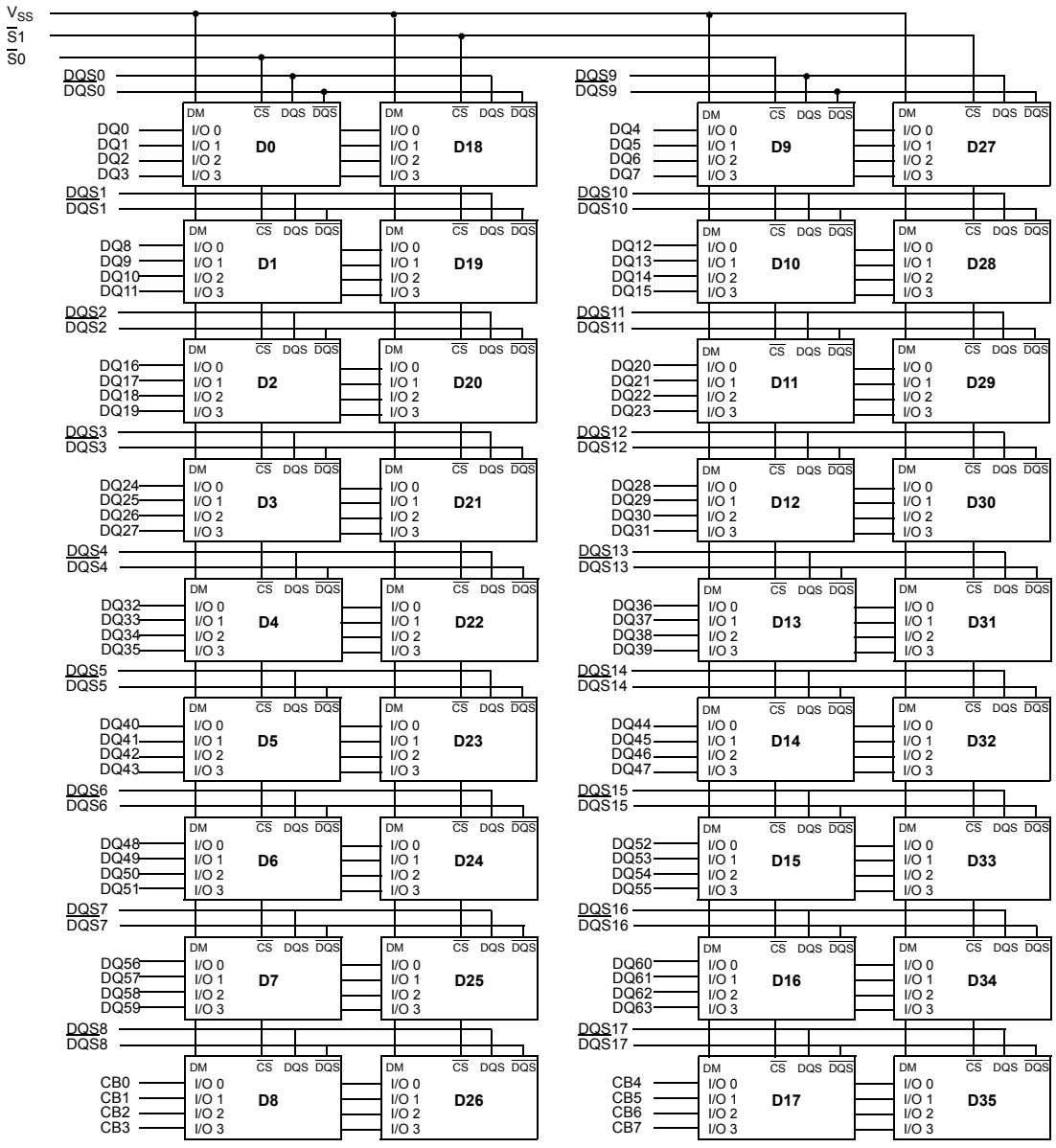
Table 5 : Pin Description

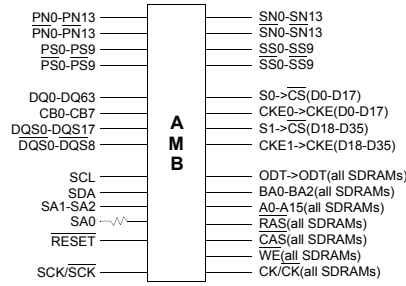
Pin Name	Type	Pin Description	Pin Numbers
SCK	Input	System Clock Input, positive line	228
$\overline{SCK}$	Input	System Clock Input, negative line	229
PN[13:0]	Output	Primary northbound Data, positive lines	22, 25, 28, 31, 34, 37, 40, 48, 51, 54, 57, 60, 63, 66
$\overline{PN}$[13:0]	Output	Primary northbound Data, negative lines	23, 26, 29, 32, 35, 38, 41, 49, 52, 55, 58, 61, 64, 67
PS[9:0]	Input	Primary Southbound Data, positive lines	70, 73, 76, 79, 82, 90, 93, 96, 99, 102
$\overline{PS}$[9:0]	Input	Primary Southbound Data, negative lines	71, 74, 77, 80, 83, 91, 94, 97, 100, 103
SN[13:0]	Output	Secondary Northbound Data, positive lines	142, 145, 148, 151, 154, 157, 160, 168, 171, 174, 177, 180, 183, 186
$\overline{SN}$[13:0]	Output	Secondary Northbound Data, negative lines	143, 146, 149, 152, 155, 158, 161, 16, 172, 175, 178, 181, 184, 187
SS[9:0]	Input	Secondary Southbound Data, positive lines	190, 193, 196, 199, 202, 210, 213, 216, 219, 222
$\overline{SS}$[9:0]	Input	Secondary Southbound Data, negative lines	191, 194, 197, 200, 203, 211, 214, 217, 220, 223
SCL	Input	Serial Presence Detect (SPD) Clock Input	120
SDA	Input	SPD Data Input / Output	119
SA[2:0]	Input	SPD Address Inputs, also used to slelect the DIMM number in the AMB	118, 239, 240
V_{ID}[1:0]	NC	Voltage ID : These pins must be unconnected for DDR2 - based Fully Buffered DIMMs V_{ID}[0] is V_{DD} value : OPEN = 1.55 V, GND = 1.5 V ; V_{ID}[1] is V_{CC} value : OPEN = 1.5V, GND = 1.2V	16, 136
RESET	Input	AMB reset signal	17
RFU	RFU	Reserved for Future Use	19, 20, 44, 45, 86, 87, 105, 106, 139, 140, 164, 165, 206, 207, 225, 226
V_{CC}	PWR	AMB Core Power and AMB Channel Interface Power (1.5 Volt)	9, 10, 12, 13, 129, 130, 132, 133
V_{DD}	PWR	DRAM Power and AMB DRAM I/O Power (1.55Volt)	1, 2, 3, 5, 6, 7, 108, 109, 111, 112, 113, 115, 116, 121, 122, 123, 125, 126, 127, 231, 232, 233, 235, 236
V_{TT}	PWR	DRAM Address/Command/Clcok Termination Power(V_{DD}/2)	15, 117, 135, 237
V_{DDSPD}	PWR	SPD Power	238
V_{SS}	GND	Ground	4, 8, 11, 14, 18, 21, 24, 27, 30, 33, 36, 39, 42, 43, 46, 47, 50, 53, 56, 59, 62, 65, 68, 69, 72, 75, 78, 81, 84, 85, 88, 89, 92, 95, 98, 101, 104, 107, 110, 114, 124, 128, 131, 134, 138, 141, 144, 147, 150, 153, 156, 159, 162, 163, 166, 167, 170, 173, 176, 179, 182, 185, 188, 189, 192, 195, 198, 201, 204, 205, 208, 209, 212, 215, 218, 221, 224, 227, 230, 234
DNU/M_Test	DNU	The DNU/M_Test pin provides an external connection R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.	137

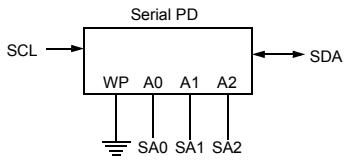
5.0 FBDIMM FUNCTIONAL BLOCK DIAGRAM

5.1 8GB, 1Gx72 Module - M395T1K66AZ4

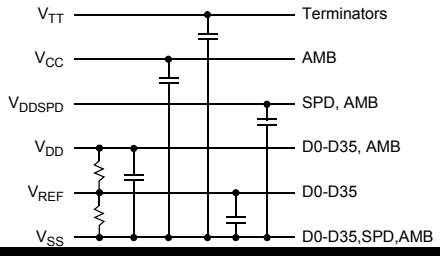
(populated as 2 rank of x4 DDR2 SDRAMs)







All address/command/control/clock ——∿∿— V_{TT}



Note :
1. DQ-to I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock.
3. There are four physical copies of each clock.

6.0 ELECTRICAL CHARACTERISTICS

Table 6 : Absolute Maximum Ratings

Parameter	Symbol	MIN	MAX	Units	Note
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.3	1.75	V	1
Voltage on V_{CC} pin relative to V_{SS}	V_{CC}	-0.3	1.75	V	1
Voltage V_{DD} pin relative to V_{SS}	V_{DD}	-0.5	2.3	V	1
Voltage on V_{TT} pin relative to V_{SS}	V_{TT}	-0.5	2.3	V	1
Storage temperature	T_{STG}	-55	100	°C	1
DDR2 SDRAM device operating temperature(Ambient)	T_{CASE}	0	85	°C	1,2
		85	95		
AMB device operating temperature (Ambient)	T_{CASE}	0	110	°C	1,2

Note : 1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.
2. DDR2 SDRAMs of FBDIMM should require this specification.

Parameter	Symbol		DRAM	Units
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85°C	7.8	µs
		85 °C < T_{CASE} ≤ 95°C	3.9	µs

Table 7 : Input DC Operating Conditions

Parameter	Symbol	MIN	Nom	MAX	Units	Notes
AMB supply voltage	V_{CC}	1.455	1.50	1.575	V	
DDR2 SDRAM supply voltage	V_{DD}	1.5	1.55	1.6	V	
Termination voltage	V_{TT}	0.48 x V_{DD}	0.50 x V_{DD}	0.52 x V_{DD}	V	
EEPROM supply voltage	V_{DDSPD}	3.0	3.3	3.6	V	
SPD Input HIGH (logic 1) voltage	V_{IH}(DC)	2.1		V_{DDSPD}	V	1
SPD Input LOW (logic 0) voltage	V_{IL}(DC)			0.8	V	1
RESET Input HIGH (logic 1) voltage	V_{IH}(DC)				V	2
RESET Input LOW (logic 0) voltage	V_{IL}(DC)			0.5	V	1
Leakage Current (RESET)	I_L	-90		90	uA	2
Leakage Current (link)	I_L	-5		5	uA	3

Note : 1. Applies for SMB and SPD bus signals.
2. Applies for AMB CMOS signal $\overline{\text{RESET}}$.
3. For all other AMB related DC parameters, please refer to the high-speed differential link interface specification.
4. Backward compatible to 1.8V +/-0.1V Power supply for DRAM V_{DD}/V_{DDQ}

Table 8 : Timing Parameters

Parameter	Symbol	MIN	Typ.	Max.	Units	Notes
EI Assertion Pass-Thru Timing	tEI Propagatet			4	clks	-
EI Deassertion Pass-Thru Timing	tEID			Bitlock	clks	2
EI Assertion Duration	tEI	100			clks	1,2
FBD Cmd to DDR Clk out that latches Cmd			8.1		ns	3
FBD Cmd to DDR Write			TBD		ns	
DDR Read to FBD (last DIMM)			5.0		ns	4
Resample Pass-Thru time			1.075		ns	
ResynchPass-Thru time			2.075		ns	
Bit Lock Interval	tBitLock			119	frames	1
Frame Lock Interval	tFrameLock			154	frames	1

Note : 1. Defined in FB-DIMM Architecture and Protocol Spec
2. Clocks defined as core clocks = 2x SCK input
3. @DDR2-667 - measured from beginning of frame at southbound input to DDR clock output that latches the first command of a frame to the DRAMs
4. @ DDR2-667 - measured from latest DQS input AMB TO start of matching data frame at northbound FB-DIMM outputs.

Table 9 : Power specification parameter and test condition

Symbol	Conditions	Power Supply	Units
Icc_Idle_0	Idle Current, single or last DIMM L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	mA
Idd_Idle_0		@1.55V	mA
Idd_Idle_0 Total Power			W
Icc_Idle_1	Idle Current, first DIMM L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	mA
Idd_Idle_1		@1.55V	mA
Idd_Idle_1 Total Power			W
Icc_Active_1	Active Power L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V	mA
Idd_Active_1		@1.55V	mA
Idd_Active_1 Total Power			W
Icc_Active_2	Active Power, data pass through L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	mA
Idd_Active_2		@1.55V	mA
Idd_Active_2 Total Power			W
Idd_Training (for AMB spec, Not in SPD)	Training Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V	mA
Idd_Training (for AMB spec, Not in SPD)		@1.55V	mA
Idd_Training Total Power			W

Table 10 : Power specification (Vdd Max = 1.600V, Vcc Max = 1.575V)

Symbol	8GB(M395T1K66AZ4)	Notes	Unit
	YE68		
	(PC2-5300)		
Icc_Idle_0	2600	@1.5V	mA
Idd_Idle_0	2395	@1.55V	mA
P_idle_0	7.93		W
Icc_Idle_1	3400	@1.5V	mA
Idd_Idle_1	2395	@1.55V	mA
P_idle_1	9.19		W
Icc_active_1	3900	@1.5V	mA
Idd_active_1	5065	@1.55V	mA
P_active_1	14.25		W
Icc_active_2	3700	@1.5V	mA
Idd_active_2	2395	@1.55V	mA
P_active_2	9.66		W
Icc_training	4000	@1.5V	mA
Idd_training	2395	@1.55V	mA
P_training	10.13		W

Note :
1. FBDIMM Power was calculated on the basis of DRAM and AMB Values in datasheet.

Table 11 : V_{TT} Currents

Description	Symbol	Typ	MAX	Units
Idle current, DDR2 SDRAM device power down	ITT1	500	700	mA
Active power, 50% DDR2 SDRAM BW	ITT2	500	700	mA

Table 12 : Reference Clock Input Specifications

Parameter	Symbol	Values		Units	Note
		MIN	MAX		
Reference clock frequency @3.2 Gb/s (nominal 133.33 MHz)	fRefclk-3.2	126.67	133.40	MHz	1.2
Reference clock frequency @4.0 Gb/s (nominal 166.67 MHz)	fRefclk-4.0	158.33	166.75	MHz	1.2
Rise time, fall time	$T_{SCK-RISE}$, $T_{SCK-FALL}$	175	700	ps	3
Voltage high	$V_{SCK-HIGH}$	660	850	mV	
Voltage low	$V_{SCK-LOW}$	-150		mV	
Absolute crossing point	$V_{CROSS-ABS}$	250	550	mV	4
Relative crossing	$V_{CROSS-REL}$	calculated	calculated		4,5
Percent mismatch between rise and fall times	$T_{SCK-RISE-FALL-MATCH}$	-	10	%	
Duty cycle of reference clock	$T_{SCK-DUTYCYCLE}$	40	60	%	
Clock leakage current	I_{I-CK}	-10	10	uA	6,7
Clock input capacitance	C_{I-CK}	0.5	2	pF	7
Clock input capacitance delta	$C_{I\_CK(D)}$	-0.25	0.25	pF	8
Transport delay	T1		5	ns	9, 10
Phase jitter sample size	NSAMPLE	10^{16}		Periods	11
Reference clock jitter, filtered	$T_{REF-JITTER}$		40	ps	12,13
Reference clock deterministic jitter	T_{REF-DJ}		TBD	ps	

Note :

1. 133MHz for PC2-4200 and 166MHz for PC2-5300.
2. Measured with SSC disabled.
3. Measured differentially through the range of 0.175V to 0.525V.
4. The crossing point must meet the absolute and relative crossing point specification simultaneously.
5. $V_{CROSS\_REL\_(MIN)}$ and $V_{CROSS\_REL(MAX)}$ are derived using the following calculation : Min = $0.5(V_{havg}-0.710)+0.250$;and Max=$0.5(V_{havg}-0.710)+0.550$, where Vhavg is the average of $V_{SCK-HIGHM}$.
6. Measured with a single-ended input voltage of 1V.
7. Applies to reference clocks SCK and $\overline{SCK}$.
8. Difference between SCK and $\overline{SCK}$ input.
9. T1 = [Tdatapath-Tclockpath](excluding PLL loop delays). This parameter is not a direct clock output parameter but in indirectly determines the clock output parameter $T_{REF-JITTER}$.
10. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data dampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. The path delays are caused by copper trace routes. on-chip routing, on-chip buffering, etc. They include the time-of flight of interpolators or other clock adjustment mechanisms. They do not include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.
11. Direct measurement of phase jitter records over 1016 periods is impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at 10^{16} samples extrapolated from an estimate of the sigma of the random jitter components.
12. Measured with SSC enabled on reference clock generator.
13. As measured after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRXTotal - MIN parameters.

Table 13 : Differential Transmitter Output Specifications

Parameter	Symbol	Values		Units	Comments
		MIN	MAX		
Differential peak-to-peak output voltage for large voltage swing	$V_{TX-DIFFp-p\_L}$	900	1,300	mV	EQ1, Note1
Differential peak-to -peak output voltage for regular voltage swing	$V_{TX-DIFFPp-p\_R}$	800		mV	EQ1, Note1
Differential peak-to-peak output voltage for small votage swing	$V_{TX-DIFFp-p\_S}$	520		mV	EQ1, Note1
DC common code output voltage for large voltage swing	V_{TX-CM_L}		375	mV	EQ2, Note1
DC common code output voltage for small voltage swing	V_{TX-CM_S}	135	280	mV	EQ2, Note1,2
De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	$V_{TX-DE-3.5-Ratio}$	-3.0	-4.0	dB	1,3,4
De-emphasized differential output voltage ratio for -6.0 dB de-emphasis	$V_{TX-DE-6.0-Ratio}$	-5.0	-7.0	dB	1,2,3
AC peak-to-peak common mode output voltage for large swing	$V_{TX-CM-ACp-p-L}$		90	mV	EQ7, Note1,5
AC peak-to-peak common mode output voltage for regular swing	$V_{TX-CM-ACp-p-R}$		80	mV	EQ7, Note1,5
AC peak-to-peak common mode output voltage for small swing	$V_{TX-CM-ACp-p-S}$		70	mV	EQ7, Note1,5
Maximum single-ended voltage in EI condition DC+AC	$V_{TX-IDLE-SE}$		50	mV	6
Maximum single-ended voltage in EI condition DC+AC	$V_{TX-IDLE-SE-DC}$		20	mV	6
Maximum peak-to-peak differential voltage in EI condition	$V_{TX-IDLE-DIFFp-p}$		40	mV	
Single-ended voltage (w.r.t. VSS) on D+/D-	V_{TX-SE}	-75	750	mV	1,7
Mimimum TX eye width, 3.2 and 4.0 Gb/s	$T_{TX-Eye-MIN}$			UI	1,8
Mimimum TX eye width 4.8 Gb/s	$T_{TX-EYE-MIN4.8}$			UI	1,8
Maximum TX deterministic jitter, 3.2 and 4.8Gb/s	$T_{TX-DJ-DD}$		02	UI	1,8,9
Maximum TX deterministic jitter, 4.8 Gb/s	$T_{TX-DJ-DD-4.8}$		TBD	UI	1,8,9
Insantaneous pulse width	$T_{TX-PULSE}$	0.85		UI	10
Differential TX output rise/fall time	$T_{TX-RISE}$ $T_{TX-FALL}$	30	90	ps	20-80% voltage, Note1
Mismatch between rise and fall times	$T_{TX-RF-MISMATCH}$		20	ps	
Differential return loss	$RL_{TTX-DIFF}$	8		dB	1 GHz-2.4 GHz, Note 11
Common mode return loss	RL_{TX-CM}	6		dB	1 GHz-2.4 GHz, Note 11
Transmitter termination impender	R_{TX}	41	55		12
D+/D-TX Impedance difference	$R_{TX-MATCH-DC}$		4	%	EQ 4, Boundaries are applied separately to high and low output voltage states
Lane-to lane skew at TX	$L_{TX-SKEW1}$		100+3UI	ps	13, 15
Lane-to lane skew at TX	$L_{TX-SKEW2}$		100=2UI	ps	14, 15

Table 14 : Differential Receiver Input Specifications

Parameter	Symbol	Values		Units	Comments
		MIN	MAX		
Differential peak-to-peak input voltage for large voltage swing	$V_{RX-DIFFp-p}$	170	TBD	mV	EQ 5, Note1
Maximum single-ended voltage in EI condition	$V_{RX-IDLE-SE}$		75	mV	2,3
Maximum single-ended voltage in Ei condition (DC only)	$V_{RX-IDLE-SE-DC}$		50	mV	2,3
Maximum peak-to-peak differential voltage in EI condition	$V_{RX-IDLE-DIFFp-p}$		65	mV	3
Single-ended voltage (w.r.t. V_{SS}) on D+/D-	V_{RX-SE}	-300	900	mV	4
Single-pulse peak differential input voltage	$V_{RX-DIFF-PULSE}$	85		mV	4,5
Amplitude ratio between adjacent symbols	$V_{RX-DIFF-ADJ-RATIO}$		TBD		4,6
Maximum RX inherent timing error, 3.2 and 4.0 Gb/x	$T_{RX-TJ-MAX}$		0.4	UI	4,7,8
Maximum RX inherent deterministic timing eror, 3.2 and 4.8 Gb/s	$T_{RX-TJ-MAX4.8}$		TBD	UI	4,7,8
Single-pulse width as zero-voltage crossing	$V_{RX-DJ-DD}$		0.3	UI	4,7,8,9
Single-pulse width at minimum-level crossing	$V_{RX-DJ-DD-4.8}$		TBD	UI	4,7,8,9
Differential RX input rise/fall time	$T_{RX-PW-ZC}$	0.55		UI	4,5
Common mode fo the input voltage	$T_{RX-PW-ML}$	0.2		UI	4.5
Differential RX output rise/fall time	$T_{RX-RISE}$ $T_{RX-FALL}$	50		ps	20~80% voltage
Common mode of input voltage	V_{RX-CM}	120	400	mV	EQ 6, Note1, 10
AC peak-to-peak common mode of input voltage	$V_{RX-CM-ACp-p}$		270	mV	EQ 7, Note 1
Ratio of $V_{RX-CM-ACp-p}$ to minimum $V_{RX-DIFFp-p}$	$V_{RX-CM-EH-RATOP}$		45	%	11
Differential return loss	$RL_{RX-DIFF}$	9		dB	1GHz-2.4 GHz, Note 12
Common mode return loss	RL_{RX-CM}	6		dB	1GHz-2.4 GHz, Note 12
RX termination impedance	R_{RX}	41	55	Ω	13
D+/D- RX Impedance difference	$R_{RX-MATCH-DC}$		4	%	EQ 8
Lane-to lane PCB skew at RX	$L_{RX-PCB-SKEW}$		6	UI	Lane-to-lane skew at the receiver that must be tolerated. Note 14
Minimum RX drift tolerance	$T_{RX-DRIFT}$	400		ps	15
Minim data tracking 3dB bandwidth	F_{TRK}	0.2		MHz	16
Electrical idle entry detect time	$T_{EI-ENTRY-DETECT}$		60	ns	17
Electrical idle exit detect time	$T_{EI-EXIT-DETECT}$		30	ns	
Bit Error Ratio	BER		10^{-12}		18

Note :
1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D-are interpreted as the Electrical Idle condition. Worst-case margins are determined for the case with transmitter using small voltage swing.
3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.
4. Specified at the package pins into a timing and voltage compliance test setup.
5. The single-pulse mask provides suffcient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eyemask.
6. The relative amplitude ratio limit between adjacent symbols prevents excessive intersymbol interference in the RX. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
7. This number does not include the effects of SSC or reference clock jitter.
8. This number includes setup and hold of the RX sampling flop.
9. Defined as the dual-dirac deterministic timing error.
10. Allows for 15 mV DC offset between transmit and receive devices.

11. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peaktopeak common mode specification. For example, if $V_{RX\text{-}DIFFp\text{-}p}$ is 200 mV, the maximum AC peak-to peak common mode is the lesser of (200 mV*0.45=90 mV)and $V_{RX\text{-}CM\text{-}AC\text{-}p\text{-}p}$.
12. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
13. The termination small signal resistance; tolerance across voltage from 100 mV to 400 mV shall not exceed +/-5 W with regard to the average of the values measured at 100 mV and at 400 mV for that pin.
14. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component of the end-to-end channel skew in the AMB specification.
15. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
16. This bandwidth number assume the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI,
17. The specified time includes the time required to forward the EI entry condition.
18. BER per differential lane.

$V_{RX\text{-}DIFFp\text{-}p} = 2x[V_{RX\text{-}D+} - V_{RX\text{-}D-}]$ (EQ5)

($V_{RX\text{-}CM}$ = DC(avg) of $[V_{RX\text{-}D+} + V_{RX\text{-}D-}]$ /2) (EQ 6)

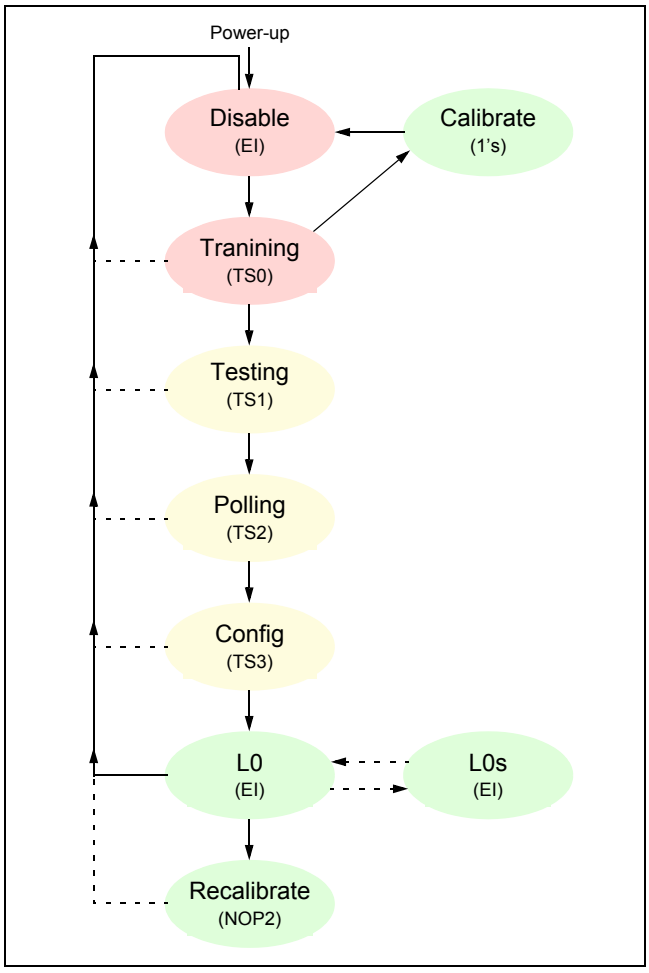
$V_{RX\text{-}CM\text{-}AC}=((Max[V_{RX\text{-}D+} + V_{RX\text{-}D})/2)((Min\ [V_{RX\text{-}D+} + V_{RX\text{-}D-})/2)$ (EQ 7)

$R_{RX\text{-}MATCH\text{-}DC} = 2x((R_{RX\text{-}D+} - R_{RX\text{-}D-})/(R_{RX\text{-}D+} + R_{RX\text{-}D-})$ (EQ 8)

7.0 CHANNEL INITIALIZATION

This chapter defines the process of initializing the FBD channel. The FBD initialzation process generally follows the top to bottom sequence of state transitions shown in the high level AMB Initialization Flow diagram in Figure The host must sequence the AMB devices through the Disable, (back to Disable), Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state. The value in parenthesis in each state bubble indicates the condition/activity of the links during these states.

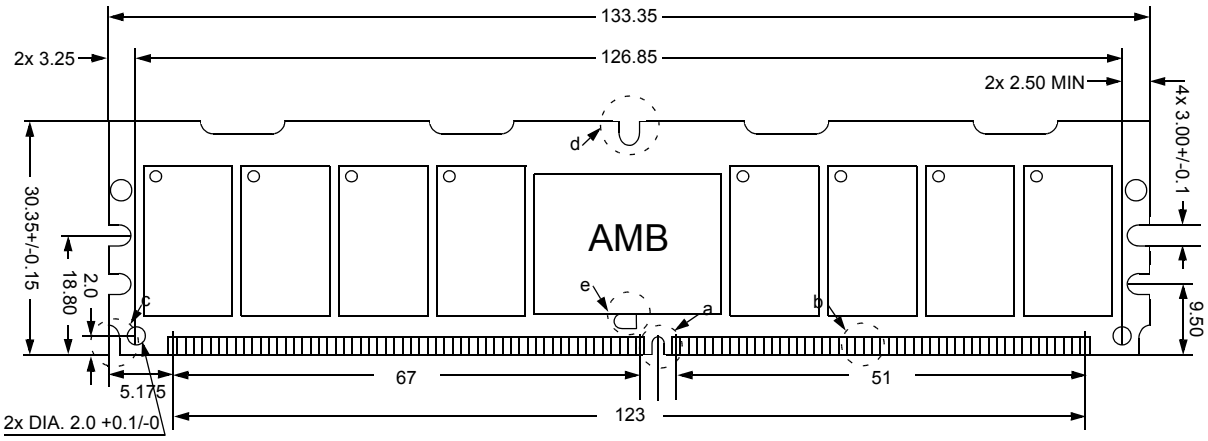
Figure 13 : AMB Initialization Flow Diagram

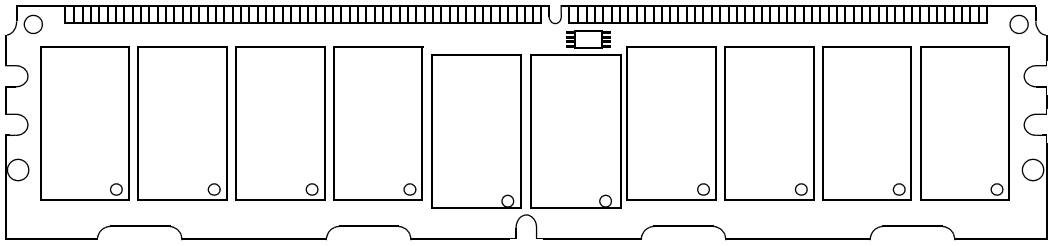


The states in the AMB Initialization Flow diagram are :
Disable - The channel is inactive and the interface signals are in a low power Electrical Idle condition.
Training - The initial bit alignment and frame alignment training is done in this state.
Testing - Each bit lane is individually tested in this state.
Polling - The channel capabilities of the individual AMB devices are communicated in this state.
Config - The channel width configuration is communicated to the AMB devices in this state.
L0 - The channel is active and frames of information are flowing between the host and the AMB devices.
Recalibrate - The channel is momentarily idled to allow TX and Rx circuits to be recalibrated.
L0s - The channel is in a low-latency power saving condition. (Optional)

Each bit lane is initialized (mosly) independently to support fault tolerance. The transitions in the figure represent the transitions of the AMB core logic state machine and are taken when the transition event is detected on the minimum required number of southound bit lanes. The chain of FBD links connecting the host the AMBs must each be initialized to esabish the timing for broadcasting data frames in the southbound direction and for merging data frame in the northbound direction. The AMBs on the channel are generally initialized as a group but because each AMB is individually addressable many altemate may altemate initialization sequences may be employed.

Figure 14 : FBDIMM Physical Dimension -1 (For PCB) : 512Mbx4 based 1Gx72 Module (2Rank)
M395T1K66AZ4





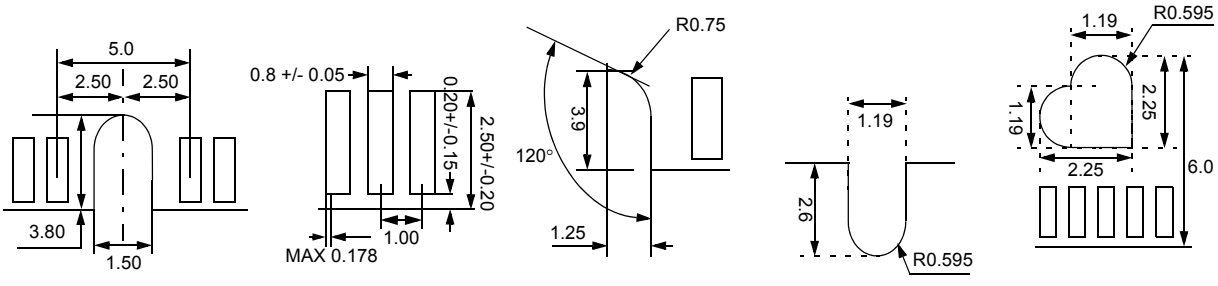


Figure 15 : FBDIMM Physical Dimension -2 (For Heat Spreader) : 512Mbx4 based 1Gx72 Module (2Rank)
M395T1K66AZ4