

## DDR SDRAM Unbuffered SODIMM

200pin Unbuffered SODIMM based on 512Mb F-die

**66 TSOP-II & 54 sTSOP-II with Lead-Free and Halogen-Free  
(RoHS compliant)**

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**Table of Contents**

**1.0 Ordering Information .....2**

**2.0 Operating Frequencies .....2**

**3.0 Feature .....2**

**4.0 Pin Configuration (Front side/back side) .....3**

**5.0 Pin Description .....3**

**6.0 Functional Block Diagram .....4**

    6.1 512MB, 64M x 64 Non ECC Module (M470L6524FL0) .....4

    6.2 1GB, 128M x 64 Non ECC Module (M470L2923F60) .....5

**7.0 Absolute Maximum Ratings .....6**

**8.0 DC Operating Conditions .....6**

**9.0 DDR SDRAM IDD spec table .....7**

    9.1 M470L6524FL0 [ (64M x 64) 512MB Module ] .....7

    9.2 M470L2923F60 [ (128M x 64) 1GB Module ] .....7

**10.0 AC Operating Conditions .....8**

**11.0 Input/Output Capacitance .....8**

**12.0 AC Timing Parameters & Specifications .....9**

**13.0 System Characteristics for DDR SDRAM .....10**

**14.0 Component Notes .....11**

**15.0 System Notes: .....12**

**16.0 Command Truth Table .....13**

**17.0 Physical Dimensions .....14**

    17.1 64Mx64 (M470L6524FL0) .....14

    17.2 128Mx64 (M4702923F60) .....15

**Revision History**

Revision	Month	Year	History
1.0	August	2008	- Initial Release
1.01	August	2008	- Typo correction
1.1	December	2008	- Changed operation frequency and AC timing parameter table

**200Pin Unbuffered SODIMM based on 512Mb F-die (x8, x16)****1.0 Ordering Information**

Part Number	Density	Organization	Component Composition	Height
M470L6524FL0-C(L)B3	512MB	64M x 64	32Mx16 (K4H511638F) * 8EA	1,250mil
M470L2923F60-C(L)B3	1GB	128M x 64	64Mx8 (K4H510838F) * 16EA	1,250mil

Note:

1. "L" and "6" of part number(11th digit) stand for Lead-Free, Halogen-Free, and RoHS compliant products.

**2.0 Operating Frequencies**

	B3(DDR333@CL=2.5)
Speed @CL2	133MHz
Speed @CL2.5	166MHz
Speed @CL3	-
CL-tRCD-tRP	2.5-3-3

**3.0 Feature**

- $V_{DD}$  : 2.5V  $\pm$  0.2V,  $V_{DDQ}$  : 2.5V  $\pm$  0.2V for DDR333
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe [DQ] (x4,x8) & [L(U)DQS] (x16)
- Differential clock inputs(CK and  $\overline{CK}$ )
- DLL aligns DQ and DQS transition with CK transition
- Programmable Read latency : DDR333(2.5 Clock)
- Programmable Burst length (2, 4, 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto & Self refresh, 7.8us refresh interval(8K/64ms refresh)
- Serial presence detect with EEPROM
- PCB : Height - 512MB/1GB(non ECC DS, 1250mil, ECC DS, 1400mil)
- SSTL\_2 Interface
- 66pin TSOP II & 54pin sTSOP II package
- All of products are Lead-Free, Halogen-Free, and RoHS compliant

4.0 Pin Configuration (Front side/back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V <sub>REF</sub>	67	DQ27	135	DQ34	2	V <sub>REF</sub>	68	DQ31	136	DQ38
3	V <sub>SS</sub>	69	V <sub>DD</sub>	137	V <sub>SS</sub>	4	V <sub>SS</sub>	70	V <sub>DD</sub>	138	V <sub>SS</sub>
5	DQ0	71	CB0	139	DQ35	6	DQ4	72	CB4	140	DQ39
7	DQ1	73	CB1	141	DQ40	8	DQ5	74	CB5	142	DQ44
9	V <sub>DD</sub>	75	V <sub>SS</sub>	143	V <sub>DD</sub>	10	V <sub>DD</sub>	76	V <sub>SS</sub>	144	V <sub>DD</sub>
11	DQS0	77	DQS8	145	DQ41	12	DM0	78	DM8	146	DQ45
13	DQ2	79	CB2	147	DQS5	14	DQ6	80	CB6	148	DM5
15	V <sub>SS</sub>	81	V <sub>DD</sub>	149	V <sub>SS</sub>	16	V <sub>SS</sub>	82	V <sub>DD</sub>	150	V <sub>SS</sub>
17	DQ3	83	CB3	151	DQ42	18	DQ7	84	CB7	152	DQ46
19	DQ8	85	DU	153	DQ43	20	DQ12	86	*DU/(RESET)	154	DQ47
21	V <sub>DD</sub>	87	V <sub>SS</sub>	155	V <sub>DD</sub>	22	V <sub>DD</sub>	88	V <sub>SS</sub>	156	V <sub>DD</sub>
23	DQ9	89	CK2	157	V <sub>DD</sub>	24	DQ13	90	V <sub>SS</sub>	158	CK1
25	DQS1	91	CK2	159	V <sub>SS</sub>	26	DM1	92	V <sub>DD</sub>	160	CK1
27	V <sub>SS</sub>	93	V <sub>DD</sub>	161	V <sub>SS</sub>	28	V <sub>SS</sub>	94	V <sub>DD</sub>	162	V <sub>SS</sub>
29	DQ10	95	CKE1	163	DQ48	30	DQ14	96	CKE0	164	DQ52
31	DQ11	97	DU	165	DQ49	32	DQ15	98	*DU(BA2)	166	DQ53
33	V <sub>DD</sub>	99	A12	167	V <sub>DD</sub>	34	V <sub>DD</sub>	100	A11	168	V <sub>DD</sub>
35	CK0	101	A9	169	DQS6	36	V <sub>DD</sub>	102	A8	170	DM6
37	CK0	103	V <sub>SS</sub>	171	DQ50	38	V <sub>SS</sub>	104	VSS	172	DQ54
39	V <sub>SS</sub>	105	A7	173	V <sub>SS</sub>	40	V <sub>SS</sub>	106	A6	174	V <sub>SS</sub>
KEY		107	A5	175	DQ51	KEY		108	A4	176	DQ55
41	DQ16	109	A3	177	DQ56	42	DQ20	110	A2	178	DQ60
43	DQ17	111	A1	179	V <sub>DD</sub>	44	DQ21	112	A0	180	V <sub>DD</sub>
45	V <sub>DD</sub>	113	V <sub>DD</sub>	181	DQ57	46	V <sub>DD</sub>	114	V <sub>DD</sub>	182	DQ61
47	DQS2	115	A10/AP	183	DQS7	48	DM2	116	BA1	184	DM7
49	DQ18	117	BA0	185	V <sub>SS</sub>	50	DQ22	118	RAS	186	V <sub>SS</sub>
51	V <sub>SS</sub>	119	WE	187	DQ58	52	V <sub>SS</sub>	120	CAS	188	DQ62
53	DQ19	121	CS0	189	DQ59	54	DQ23	122	CS1	190	DQ63
55	DQ24	123	*DU(A13)	191	V <sub>DD</sub>	56	DQ28	124	DU	192	V <sub>DD</sub>
57	V <sub>DD</sub>	125	V <sub>SS</sub>	193	SDA	58	V <sub>DD</sub>	126	V <sub>SS</sub>	194	SA0
59	DQ25	127	DQ32	195	SCL	60	DQ29	128	DQ36	196	SA1
61	DQS3	129	DQ33	197	V <sub>DDSPD</sub>	62	DM3	130	DQ37	198	SA2
63	V <sub>SS</sub>	131	V <sub>DD</sub>	199	V <sub>DDID</sub>	64	V <sub>SS</sub>	132	V <sub>DD</sub>	200	DU
65	DQ26	133	DQS4			66	DQ30	134	DM4		

Note :

- \* : These pins are not used in this module.
- Pins 71, 72, 73, 74, 77, 78, 79, 80, 83, 84 are not used on x64(M470~) module, & used on x72(M485~) module.
- Pins 95,122 are NC for 1Row module & used for 2Row module.

5.0 Pin Description

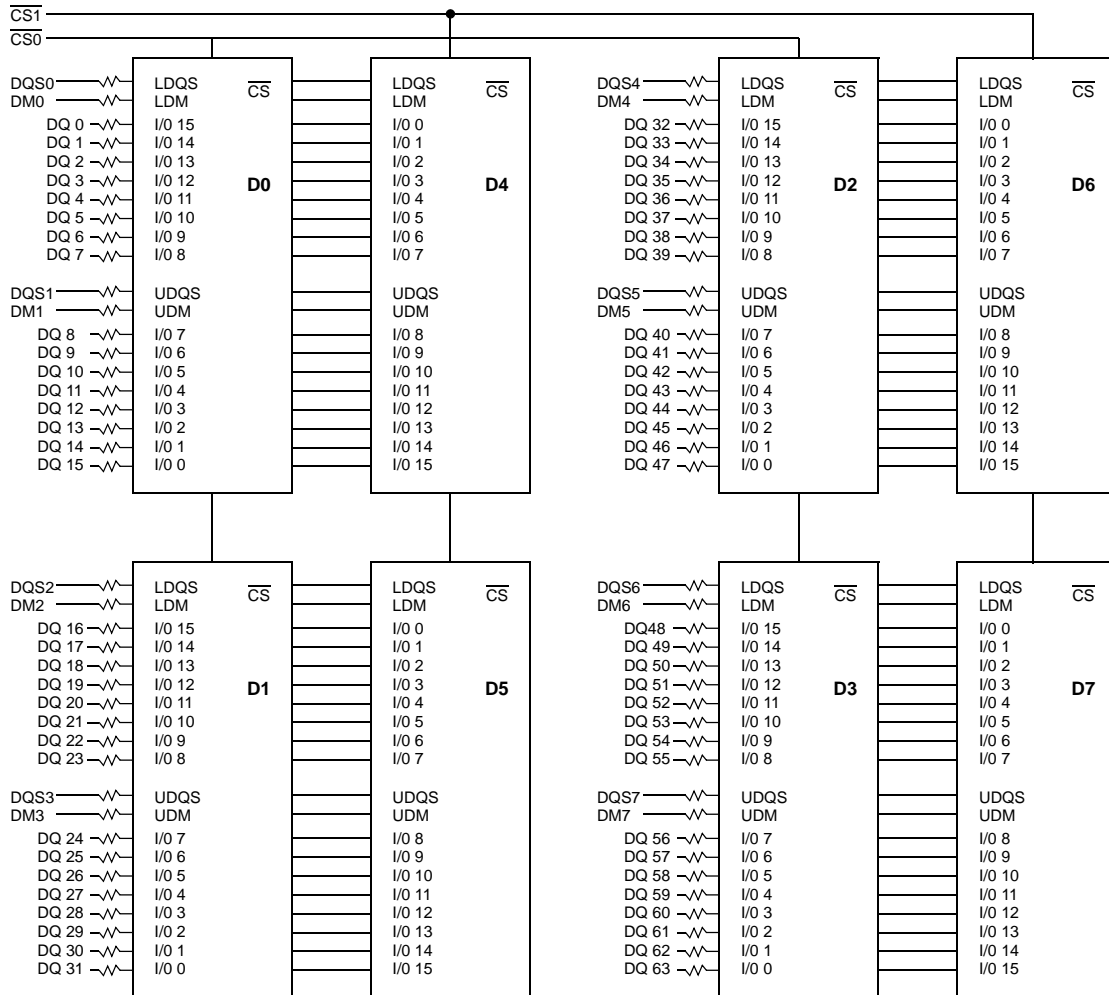
Pin Name	Function	Pin Name	Function
A0 ~ A12	Address input (Multiplexed)	DM0 ~7,8(for ECC)	Data - in mask
BA0 ~ BA1	Bank Select Address	V <sub>DD</sub>	Power supply (2.5V for DDR333, 2.6V for DDR400)
DQ0 ~ DQ63	Data input/output	V <sub>DDQ</sub>	Power Supply for DQS (2.5V for DDR333, 2.6V for DDR400)
DQS0 ~ DQS8	Data Strobe input/output	V <sub>SS</sub>	Ground
CK0,CK0 ~ CK2, CK2	Clock input	V <sub>REF</sub>	Power supply for reference
CKE0, CKE1(for double rank)	Clock enable input	V <sub>DDSPD</sub>	Serial EEPROM Power/Supply ( 2.3V to 3.6V )
CS0, CS1(for double rank)	Chip select input	SDA	Serial data I/O
RAS	Row address strobe	SCL	Serial clock
CAS	Column address strobe	SA0 ~ 2	Address in EEPROM
WE	Write enable	V <sub>DDID</sub>	V <sub>DD</sub> , V <sub>DDQ</sub> level detection
CB0 ~ CB7(for x72 module)	Check bit(Data-in/data-out)	NC	No connection

Note : V<sub>DDID</sub> defines relationship of V<sub>DD</sub> and V<sub>DDQ</sub>, and the default status of it is open (V<sub>DD</sub>=V<sub>DDQ</sub>)

6.0 Functional Block Diagram

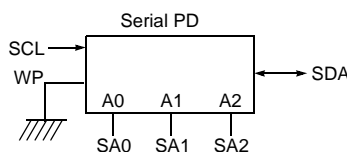
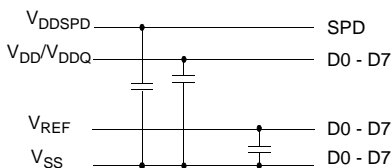
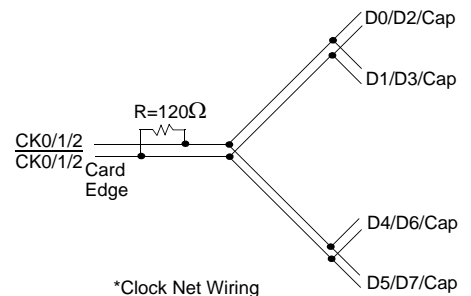
6.1 512MB, 64M x 64 Non ECC Module (M470L6524FL0)

(Populated as 2 bank of x16 DDR SDRAM Module)



- BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D7
- A0 - A12 → A0-A12: DDR SDRAMs D0 - D7
- $\overline{\text{RAS}}$  →  $\overline{\text{RAS}}$ : SDRAMs D0 - D7
- $\overline{\text{CAS}}$  →  $\overline{\text{CAS}}$ : SDRAMs D0 - D7
- CKE0 → CKE: SDRAMs D0 - D3
- CKE1 → CKE: SDRAMs D4 - D7
- $\overline{\text{WE}}$  →  $\overline{\text{WE}}$ : SDRAMs D0 - D7

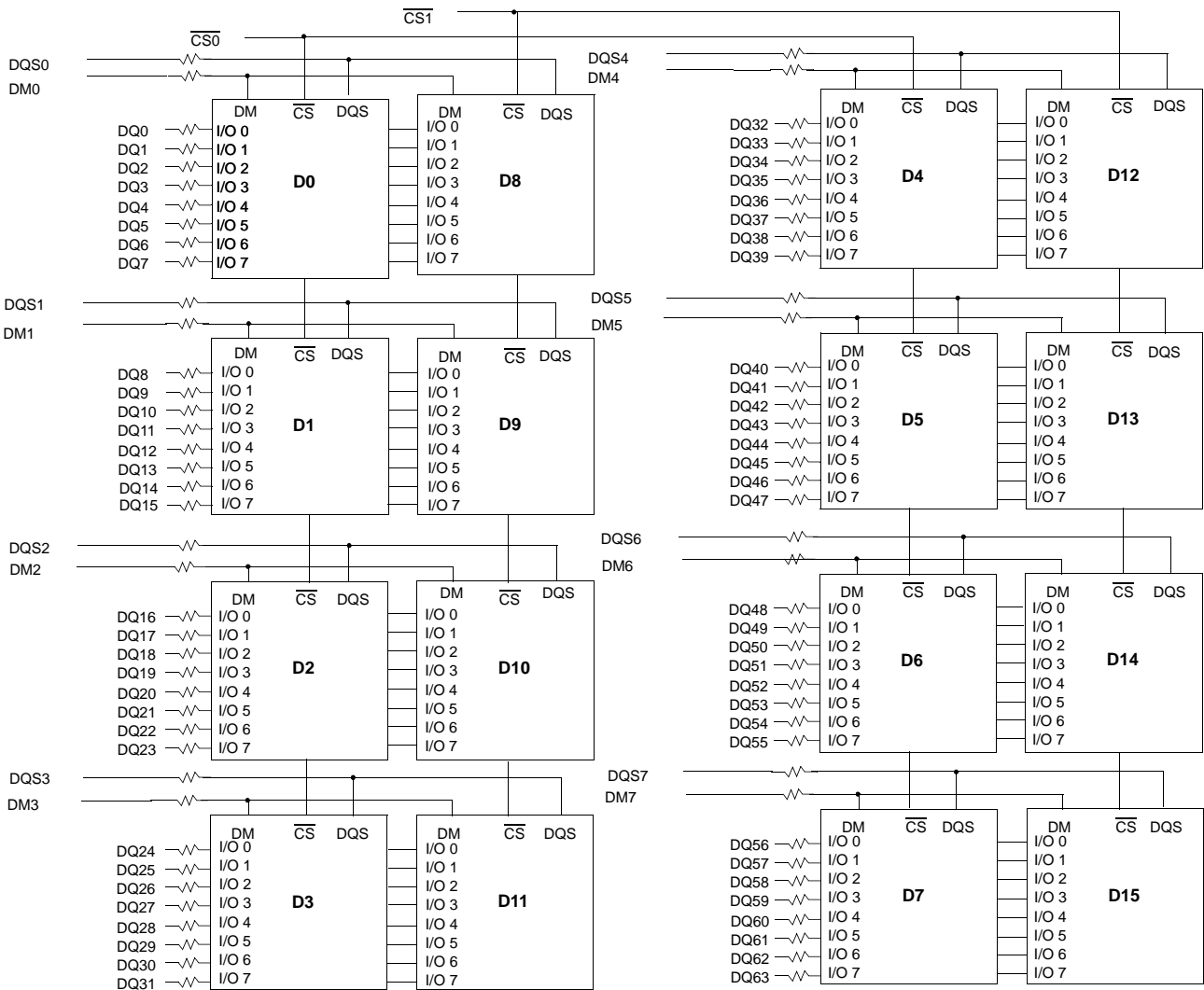
Clock Wiring	
Clock Input	SDRAMs
CK0/CK0	4 SDRAMs
CK1/CK1	4 SDRAMs
CK2/CK2	NC



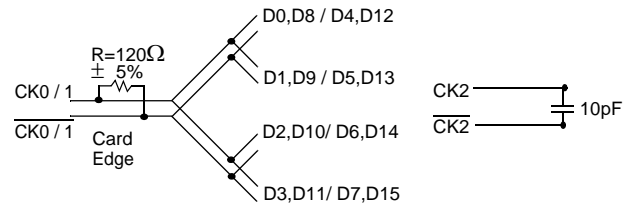
- Note :
1. DQ-to-I/O wiring is shown as recommended but may be changed.
  2. DQ/DQS/DM/CKE/ $\overline{\text{CS}}$  relationships must be maintained as shown.
  3. DQ, DQS, DM/DQS resistors: 22 Ohms.

6.2 1GB, 128M x 64 Non ECC Module (M470L2923F60)

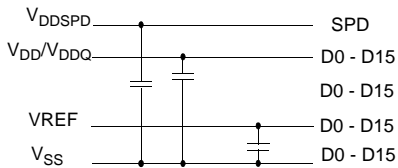
(Populated as 2 bank of x8 DDR SDRAM Module)



- BA0 - BA1 → BA0-BA1: DDR SDRAMs D0 - D15
- A0 - A12 → A0-A12 : DDR SDRAMs D0 - D15
- RAS → RAS : DDR SDRAMs D0 - D15
- CAS → CAS : DDR SDRAMs D0 - D15
- CKE1 → CKE : DDR SDRAMs D8 - D15
- CKE0 → CKE : DDR SDRAMs D0 - D7
- WE → WE : DDR SDRAMs D0 - D15



\*Clock Net Wiring



Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/QDS/DM/CKE/CS relationships must be maintained as shown
3. DQ, QDS, DM/QDS resistors: 22 Ohm.

### 7.0 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 ~ 3.6	V
Voltage on $V_{DD}$ & $V_{DDQ}$ supply relative to $V_{SS}$	$V_{DD}, V_{DDQ}$	-1.0 ~ 3.6	V
Storage temperature	$T_{STG}$	-55 ~ +150	°C
Short circuit current	$I_{OS}$	50	mA

Note :

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
2. Functional operation should be restricted to recommended operating condition.
3. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

### 8.0 DC Operating Conditions

Recommended operating conditions(Voltage referenced to  $V_{SS}=0V$ ,  $T_A=0$  to  $70^{\circ}C$ )

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal $V_{DD}$ of 2.5V for DDR333)	$V_{DD}$	2.3	2.7	V	
I/O Supply voltage(for device with a nominal $V_{DD}$ of 2.5V for DDR333)	$V_{DDQ}$	2.3	2.7	V	
I/O Reference voltage	$V_{REF}$	$0.49 \cdot V_{DDQ}$	$0.51 \cdot V_{DDQ}$	V	1
I/O Termination voltage(system)	$V_{TT}$	$V_{REF}-0.04$	$V_{REF}+0.04$	V	2
Input logic high voltage	$V_{IH}(DC)$	$V_{REF}+0.15$	$V_{DDQ}+0.3$	V	
Input logic low voltage	$V_{IL}(DC)$	-0.3	$V_{REF}-0.15$	V	
Input Voltage Level, CK and $\overline{CK}$ inputs	$V_{IN}(DC)$	-0.3	$V_{DDQ}+0.3$	V	
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID}(DC)$	0.36	$V_{DDQ}+0.6$	V	3
V-I Matching: Pullup to Pulldown Current Ratio	$V_I(\text{Ratio})$	0.71	1.4	-	4
Input leakage current	$I_I$	-2	2	uA	
Output leakage current	$I_{OZ}$	-5	5	uA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} + 0.84V$	$I_{OH}$	-16.8		mA	
Output High Current(Normal strength driver) ; $V_{OUT} = V_{TT} - 0.84V$	$I_{OL}$	16.8		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} + 0.45V$	$I_{OH}$	-9		mA	
Output High Current(Half strength driver) ; $V_{OUT} = V_{TT} - 0.45V$	$I_{OL}$	9		mA	

Note :

1.  $V_{REF}$  is expected to be equal to  $0.5 \cdot V_{DDQ}$  of the transmitting device, and to track variations in the dc level of same. Peak-to peak noise on  $V_{REF}$  may not exceed +/-2% of the dc value.
2.  $V_{TT}$  is not applied directly to the device.  $V_{TT}$  is a system supply for signal termination resistors, is expected to be set equal to  $V_{REF}$  and must track variations in the DC level of  $V_{REF}$ .
3.  $V_{ID}$  is the magnitude of the difference between the input level on CK and the input level on  $\overline{CK}$ .
4. The ratio of the pullup current to the pulldown current is specified for the same temperature and voltage, over the entire temperature and voltage range, for device drain to source voltages from 0.25V to 1.0V. For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation. The full variation in the ratio of the maximum to minimum pullup and pulldown current will not exceed 1.7 for device drain to source voltages from 0.1 to 1.0.



**9.0 DDR SDRAM IDD spec table****9.1 M470L6524FL0 [ (64M x 64) 512MB Module ]**(V<sub>DD</sub>=2.7V, T = 10°C)

Symbol		B3(DDR333@CL=2.5)	Unit	Notes
IDD0		640	mA	
IDD1		740	mA	
IDD2P		40	mA	
IDD2F		240	mA	
IDD2Q		200	mA	
IDD3P		240	mA	
IDD3N		360	mA	
IDD4R		860	mA	
IDD4W		920	mA	
IDD5		1000	mA	
IDD6	Normal	40	mA	
	Low power	24	mA	Optional
IDD7A		1700	mA	

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**9.2 M470L2923F60 [ (128M x 64) 1GB Module ]**(V<sub>DD</sub>=2.7V, T = 10°C)

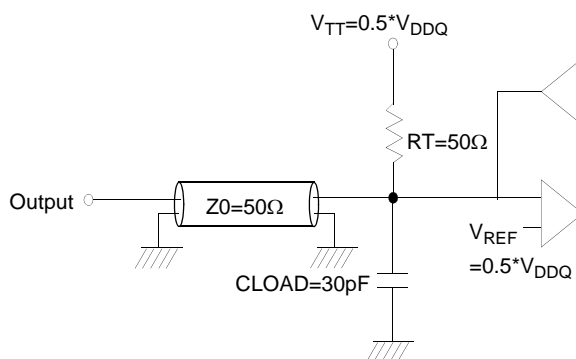
Symbol		B3(DDR333@CL=2.5)	Unit	Notes
IDD0		1200	mA	
IDD1		1440	mA	
IDD2P		80	mA	
IDD2F		480	mA	
IDD2Q		400	mA	
IDD3P		480	mA	
IDD3N		720	mA	
IDD4R		1480	mA	
IDD4W		1560	mA	
IDD5		2000	mA	
IDD6	Normal	80	mA	
	Low power	48	mA	Optional
IDD7A		3240	mA	

\* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

10.0 AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	$V_{IH(AC)}$	$V_{REF} + 0.31$		V	3
Input Low (Logic 0) Voltage, DQ, DQS and DM signals.	$V_{IL(AC)}$		$V_{REF} - 0.31$	V	3
Input Differential Voltage, CK and $\overline{CK}$ inputs	$V_{ID(AC)}$	0.7	$V_{DDQ}+0.6$	V	1
Input Crossing Point Voltage, CK and $\overline{CK}$ inputs	$V_{IX(AC)}$	$0.5 \cdot V_{DDQ}-0.2$	$0.5 \cdot V_{DDQ}+0.2$	V	2

- Note :
- $V_{ID}$  is the magnitude of the difference between the input level on CK and the input on  $\overline{CK}$ .
  - The value of  $V_{IX}$  is expected to equal  $0.5 \cdot V_{DDQ}$  of the transmitting device and must track variations in the DC level of the same.
  - These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. the AC and DC input specifications are relation to a  $V_{REF}$  envelope that has been bandwidth limited 20MHz.



Output Load Circuit (SSTL\_2)

11.0 Input/Output Capacitance

(  $T_A= 25^{\circ}C, f=100MHz$ )

Parameter	Symbol	M470L6524FL0		M470L2923F60		Unit
		Min	Max	Min	Max	
Input capacitance(A0 ~ A12, BA0 ~ BA1, RAS, CAS, WE )	CIN1	49	57	65	81	pF
Input capacitance(CKE0, CKE1)	CIN2	42	50	42	50	pF
Input capacitance( $\overline{CS0}, \overline{CS1}$ )	CIN3	42	50	42	50	pF
Input capacitance( CLK0, CLK1, CLK2)	CIN4	25	30	28	34	pF
Input capacitance(DM0~DM7)	CIN5	6	7	10	12	pF
Data & DQS input/output capacitance(DQ0~DQ63)	Cout1	6	7	10	12	pF

12.0 AC Timing Parameters & Specifications

Parameter	Symbol	B3 (DDR333@CL=2.5)		Unit	Note
		Min	Max		
Row cycle time	tRC	60		ns	
Refresh row cycle time	tRFC	72		ns	
Row active time	tRAS	42	70K	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay	tRCD	18		ns	
Row precharge time	tRP	18		ns	
Row active to Row active delay	tRRD	12		ns	
Write recovery time	tWR	15		ns	
Last data in to Read command	tWTR	1		tCK	
Clock cycle time	tCK	CL=2.0	7.5	12	ns
		CL=2.5	6	12	
		CL=3.0	-	-	
Clock high level width	tCH	0.45	0.55	tCK	
Clock low level width	tCL	0.45	0.55	tCK	
DQS-out access time from CK/ $\overline{\text{CK}}$	tDQSCK	-0.6	+0.6	ns	
Output data access time from CK/ $\overline{\text{CK}}$	tAC	-0.7	+0.7	ns	
Data strobe edge to output data edge	tDQSQ	-	0.45	ns	22
Read Preamble	tRPRE	0.9	1.1	tCK	
Read Postamble	tRPST	0.4	0.6	tCK	
CK to valid DQS-in	tDQSS	0.75	1.25	tCK	
DQS-in setup time	tWPRES	0		ns	13
DQS-in hold time	tWPREH	0.25		tCK	
DQS falling edge to CK rising-setup time	tDSS	0.2		tCK	
DQS falling edge from CK rising-hold time	tDSH	0.2		tCK	
DQS-in high level width	tDQSH	0.35		tCK	
DQS-in low level width	tDQSL	0.35		tCK	
Address and Control Input setup time(fast)	tIS	0.75		ns	15, 17-19
Address and Control Input hold time(fast)	tIH	0.75		ns	15, 17-19
Address and Control Input setup(slow)	tIS	0.8		ns	16-19
Address and Control Input hold time(slow)	tIH	0.8		ns	16-19
Data-out high impedance time from CK/ $\overline{\text{CK}}$	tHZ	-0.7	+0.7	ns	11
Data-out low impedance time from CK/ $\overline{\text{CK}}$	tLZ	-0.7	+0.7	ns	11
Mode register set cycle time	tMRD	12		ns	
DQ & DM setup time to DQS	tDS	0.45		ns	j, k
DQ & DM hold time to DQS	tDH	0.45		ns	j, k
Control & Address input pulse width	tIPW	2.2		ns	18
DQ & DM input pulse width	tDIPW	1.75		ns	18
Exit self refresh to non-Read command	tXSNR	75		ns	
Exit self refresh to read command	tXSRD	200		tCK	
Refresh interval time	tREFI		7.8	us	14
Output DQS valid window	tQH	tHP -tQHS	-	ns	21
Clock half period	tHP	tCLmin or tCHmin	-	ns	20, 21
Data hold skew factor	tQHS		0.55	ns	21
DQS write postamble time	tWPST	0.4	0.6	tCK	12
Active to Read with Auto precharge command	tRAP	18			
Autoprecharge write recovery + Precharge time	tDAL	(tWR/tCK) + (tRP/tCK)		tCK	23

13.0 System Characteristics for DDR SDRAM

The following specification parameters are required in systems using DDR333 devices to ensure proper system performance. these characteristics are for system simulation purposes and are guaranteed by design.

Table 1 : Input Slew Rate for DQ, DQS, and DM

AC CHARACTERISTICS PARAMETER	SYMBOL	DDR333		Units	Notes
		MIN	MAX		
DQ/DM/DQS input slew rate measured between $V_{IH}(DC)$ , $V_{IL}(DC)$ and $V_{IL}(DC)$ , $V_{IH}(DC)$	DCSLEW	0.5	4.0	V/ns	a, l

Table 2 : Input Setup & Hold Time Derating for Slew Rate

Input Slew Rate	$\Delta tIS$	$\Delta tIH$	Units	Notes
0.5 V/ns	0	0	ps	i
0.4 V/ns	+50	0	ps	i
0.3 V/ns	+100	0	ps	i

Table 3 : Input/Output Setup & Hold Time Derating for Slew Rate

Input Slew Rate	$\Delta tDS$	$\Delta tDH$	Units	Notes
0.5 V/ns	0	0	ps	k
0.4 V/ns	+75	+75	ps	k
0.3 V/ns	+150	+150	ps	k

Table 4 : Input/Output Setup & Hold Derating for Rise/Fall Delta Slew Rate

Delta Slew Rate	$\Delta tDS$	$\Delta tDH$	Units	Notes
+/- 0.0 V/ns	0	0	ps	j
+/- 0.25 V/ns	+50	+50	ps	j
+/- 0.5 V/ns	+100	+100	ps	j

Table 5 : Output Slew Rate Characteristic (X4, X8 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	1.0	4.5	b,c,d,f,g,h

Table 6 : Output Slew Rate Characteristic (X16 Devices only)

Slew Rate Characteristic	Typical Range (V/ns)	Minimum (V/ns)	Maximum (V/ns)	Notes
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	a,c,d,f,g,h
Pulldown slew	1.2 ~ 2.5	0.7	5.0	b,c,d,f,g,h

Table 7 : Output Slew Rate Matching Ratio Characteristics

AC CHARACTERISTICS PARAMETER	DDR333		Notes
	MIN	MAX	
Output Slew Rate Matching Ratio (Pullup to Pulldown)	0.67	1.5	e, l

## 14.0 Component Notes

1. All voltages referenced to  $V_{SS}$ .
2. Tests for ac timing,  $I_{DD}$ , and electrical, ac and dc characteristics, may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Figure 1 represents the timing reference load used in defining the relevant timing parameters of the part. It is not intended to be either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers will correlate to their production test conditions (generally a coaxial transmission line terminated at the tester electronics).

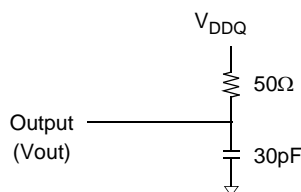


Figure 1 : Timing Reference Load

4. AC timing and  $I_{DD}$  tests may use a  $V_{IL}$  to  $V_{IH}$  swing of up to 1.5 V in the test environment, but input timing is still referenced to  $V_{REF}$  (or to the crossing point for  $CK/\overline{CK}$ ), and parameter specifications are guaranteed for the specified ac input levels under normal use conditions. The minimum slew rate for the input signals is 1 V/ns in the range between  $V_{IL}(AC)$  and  $V_{IH}(AC)$ .
5. The ac and dc input level specifications are as defined in the SSTL\_2 Standard (i.e., the receiver will effectively switch as a result of the signal crossing the ac input level and will remain in that state as long as the signal does not ring back above (below) the dc input LOW (HIGH) level.
6. Inputs are not recognized as valid until  $V_{REF}$  stabilizes. Exception: during the period before  $V_{REF}$  stabilizes,  $CKE \leq 0.2V_{DDQ}$  is recognized as LOW.
7. Enables on-chip refresh and address counters.
8.  $I_{DD}$  specifications are tested after the device is properly initialized.
9. The  $CK/\overline{CK}$  input reference level (for timing referenced to  $CK/\overline{CK}$ ) is the point at which  $CK$  and  $\overline{CK}$  cross; the input reference level for signals other than  $CK/\overline{CK}$ , is  $V_{REF}$ .
10. The output timing reference voltage level is  $V_{TT}$ .
11. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level but specify when the device output is no longer driving (HZ), or begins driving (LZ).
12. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
13. The specific requirement is that DQS be valid (HIGH, LOW, or at some point on a valid transition) on or before this CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. when no writes were previously in progress on the bus, DQS will be transitioning from High-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.
14. A maximum of eight AUTO REFRESH commands can be posted to any given DDR SDRAM device.
15. For command/address input slew rate  $\geq 1.0$  V/ns
16. For command/address input slew rate  $\geq 0.5$  V/ns and  $< 1.0$  V/ns
17. For  $CK$  &  $\overline{CK}$  slew rate  $\geq 1.0$  V/ns
18. These parameters guarantee device timing, but they are not necessarily tested on each device. They may be guaranteed by device design or tester correlation.
19. Slew Rate is measured between  $V_{OH}(AC)$  and  $V_{OL}(AC)$ .
20. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)....For example, tCL and tCH are = 50% of the period, less the half period jitter (tJIT(HP)) of the clock source, and less the half period jitter due to crosstalk (tJIT(crosstalk)) into the clock traces.
21.  $t_{QH} = t_{HP} - t_{QHS}$ , where:  
tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCH, tCL). tQHS accounts for 1) The pulse duration distortion of on-chip clock circuits; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p channel to n-channel variation of the output drivers.
22. tDQSQ - Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.
23.  $t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK})$   
For each of the terms above, if not already an integer, round to the next highest integer. Example: For DDR266B at CL=2.5 and tCK=7.5ns  $t_{DAL} = (15 \text{ ns} / 7.5 \text{ ns}) + (20 \text{ ns} / 7.5 \text{ ns}) = (2) + (3) \text{ } t_{DAL} = 5 \text{ clocks}$

15.0 System Notes:

a. Pullup slew rate is characterized under the test conditions as shown in Figure 2.

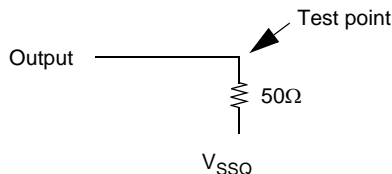


Figure 2 : Pullup slew rate test load

b. Pulldown slew rate is measured under the test conditions shown in Figure 3.

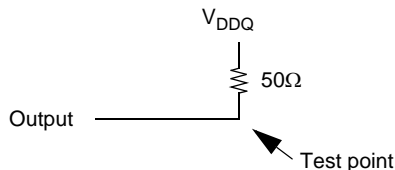


Figure 3 : Pulldown slew rate test load

c. Pullup slew rate is measured between ( $V_{DDQ}/2 - 320 \text{ mV} \pm 250 \text{ mV}$ )

Pulldown slew rate is measured between ( $V_{DDQ}/2 + 320 \text{ mV} \pm 250 \text{ mV}$ )

Pullup and Pulldown slew rate conditions are to be met for any pattern of data, including all outputs switching and only one output switching.

Example : For typical slew rate, DQ0 is switching

For minimum slew rate, all DQ bits are switching from either high to low, or low to high.

The remaining DQ bits remain the same as for previous state.

d. Evaluation conditions

Typical : 25 °C (T Ambient),  $V_{DDQ} = 2.5\text{V}$ (for DDR266/333) and 2.6V(for DDR400), typical process

Minimum : 70 °C (T Ambient),  $V_{DDQ} = 2.3\text{V}$ (for DDR266/333) and 2.5V(for DDR400), slow - slow process

Maximum : 0 °C (T Ambient),  $V_{DDQ} = 2.7\text{V}$ (for DDR266/333) and 2.7V(for DDR400), fast - fast process

e. The ratio of pullup slew rate to pulldown slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range.  
For a given output, it represents the maximum difference between pullup and pulldown drivers due to process variation.

f. Verified under typical conditions for qualification purposes.

g. TSOP11 package devices only.

h. Only intended for operation up to 266 Mbps per pin.

i. A derating factor will be used to increase tIS and tIH in the case where the input slew rate is below 0.5V/ns as shown in Table 2. The Input slew rate is based on the lesser of the slew rates determined by either  $V_{IH}(AC)$  to  $V_{IL}(AC)$  or  $V_{IH}(DC)$  to  $V_{IL}(DC)$ , similarly for rising transitions.

j. A derating factor will be used to increase tDS and tDH in the case where DQ, DM, and DQS slew rates differ, as shown in Tables 3 & 4. Input slew rate is based on the larger of AC-AC delta rise, fall rate and DC-DC delta rise, Input slew rate is based on the lesser of the slew rates determined by either  $V_{IH}(AC)$  to  $V_{IL}(AC)$  or  $V_{IH}(DC)$  to  $V_{IL}(DC)$ , similarly for rising transitions. The delta rise/fall rate is calculated as:  $\{1/(\text{Slew Rate1})\} - \{1/(\text{Slew Rate2})\}$

For example : If Slew Rate 1 is 0.5 V/ns and slew Rate 2 is 0.4 V/ns, then the delta rise, fall rate is - 0.5ns/V . Using the table given, this would result in the need for an increase in tDS and tDH of 100 ps.

k. Table 3 is used to increase tDS and tDH in the case where the I/O slew rate is below 0.5 V/ns. The I/O slew rate is based on the lesser of the AC - AC slew rate and the DC- DC slew rate. The input slew rate is based on the lesser of the slew rates determined by either  $V_{IH}(AC)$  to  $V_{IL}(AC)$  or  $V_{IH}(DC)$  to  $V_{IL}(DC)$ , and similarly for rising transitions.

l. DQS, DM, and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

16.0 Command Truth Table

(V=Valid, X=Don't Care, H=Logic High, L=Logic Low)

COMMAND		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0,1	A10/AP	A0 ~ A9 A11, A12	Note	
Register	Extended MRS	H	X	L	L	L	L	OP CODE			1, 2	
Register	Mode Register Set	H	X	L	L	L	L	OP CODE			1, 2	
Refresh	Auto Refresh		H	H	L	L	L	H	X		3	
	Self Refresh	Entry		L					H	H	H	X
		Exit	L	H	L	H	H	H	X		3	
					H	X	X	X			3	
Bank Active & Row Addr.		H	X	L	L	H	H	V	Row Address (A0~A9, A11,A12)			
Read & Column Address	Auto Precharge Disable		H	X	L	H	L	H	V	L	Column Address	4
	Auto Precharge Enable								H			4
Write & Column Address	Auto Precharge Disable		H	X	L	H	L	L	V	L	Column Address	4
	Auto Precharge Enable								H			4, 6
Burst Stop		H	X	L	H	H	L	X			7	
Precharge	Bank Selection		H	X	L	L	H	L	V	L	X	
	All Banks								X	H		
Active Power Down		Entry	H	L	H	X	X	X	X			
					L	V	V	V				
Precharge Power Down Mode		Entry	H	L	H	X	X	X	X			
					L	H	H	H				
		Exit	L	H	H	X	X	X				
					L	V	V	V				
DM		H	X					X			8	
No operation (NOP) : Not defined		H	X	H	X	X	X	X			9	
				L	H	H	H				9	

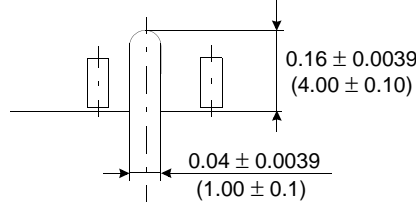
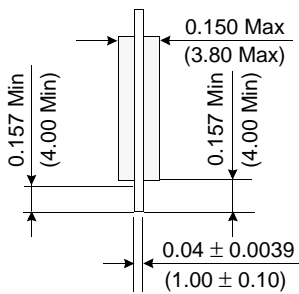
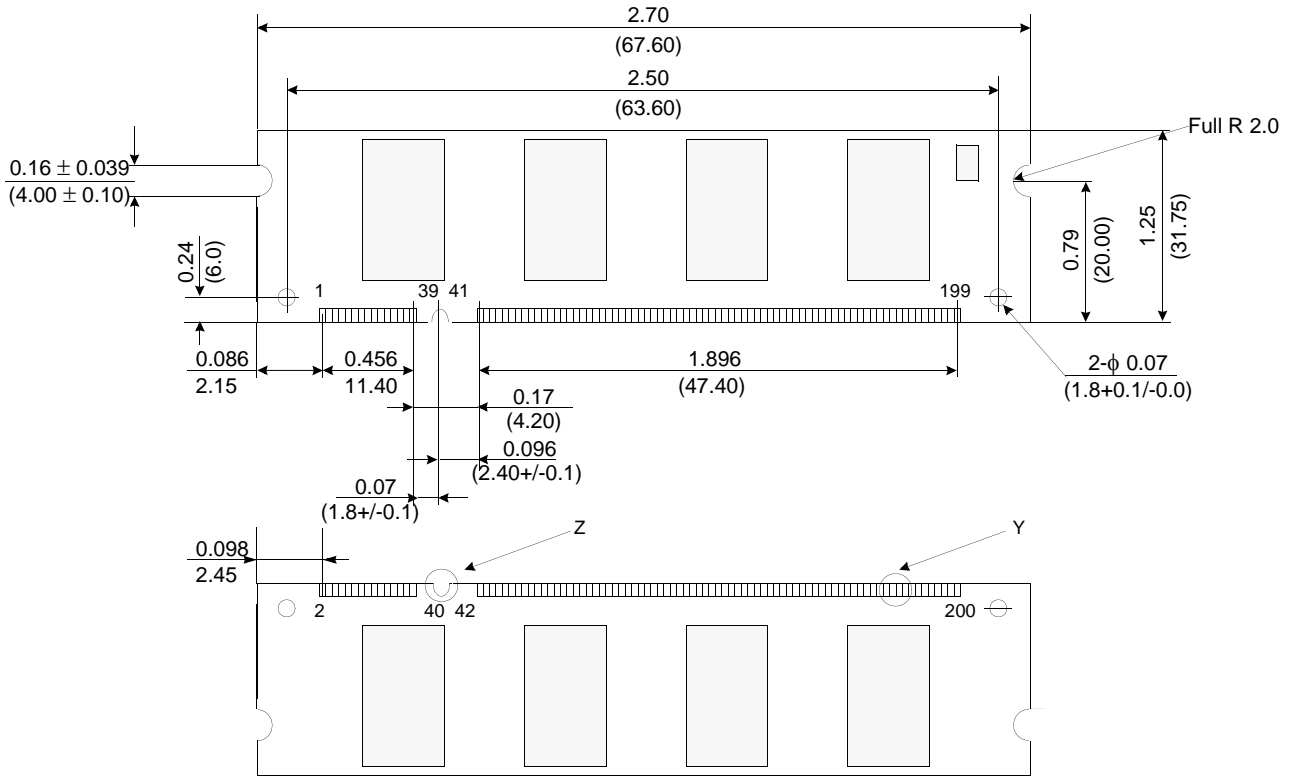
Note :

- OP Code : Operand Code. A0 ~ A12 & BA0 ~ BA1 : Program keys. (@EMRS/MRS)
- EMRS/ MRS can be issued only at all banks precharge state. A new command can be issued 2 clock cycles after EMRS or MRS.
- Auto refresh functions are same as the CBR refresh of DRAM.  
The automatical precharge without row precharge command is meant by "Auto".  
Auto/self refresh can be issued only at all banks precharge state.
- BA0 ~ BA1 : Bank select addresses.  
If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.  
If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.  
If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.  
If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
- If A10/AP is "High" at row precharge, BA0 and BA1 are ignored and all banks are selected.
- During burst write with auto precharge, new read/write command can not be issued.  
Another bank read/write command can be issued after the end of burst.  
New row active of the associated bank can be issued at tRP after the end of burst.
- Burst stop command is valid at every burst length.
- DM sampled at the rising and falling edges of the DQS and Data-in are masked at the both edges (Write DM latency is 0).
- This combination is not defined for any function, which means "No Operation(NOP)" in DDR SDRAM.

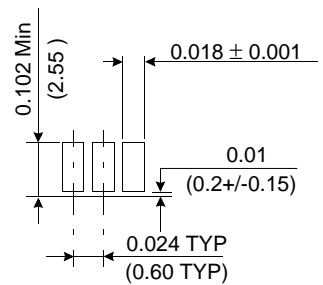
17.0 Physical Dimensions

17.1 64Mx64 (M470L6524FL0)

Units : Inches (Millimeters)



Detail Z



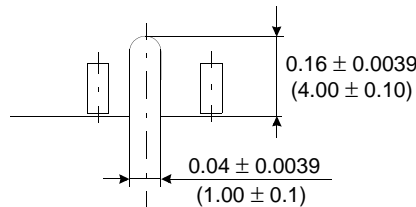
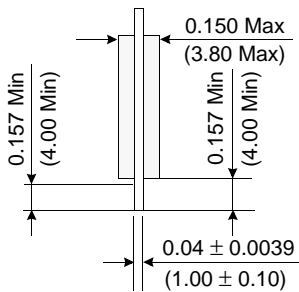
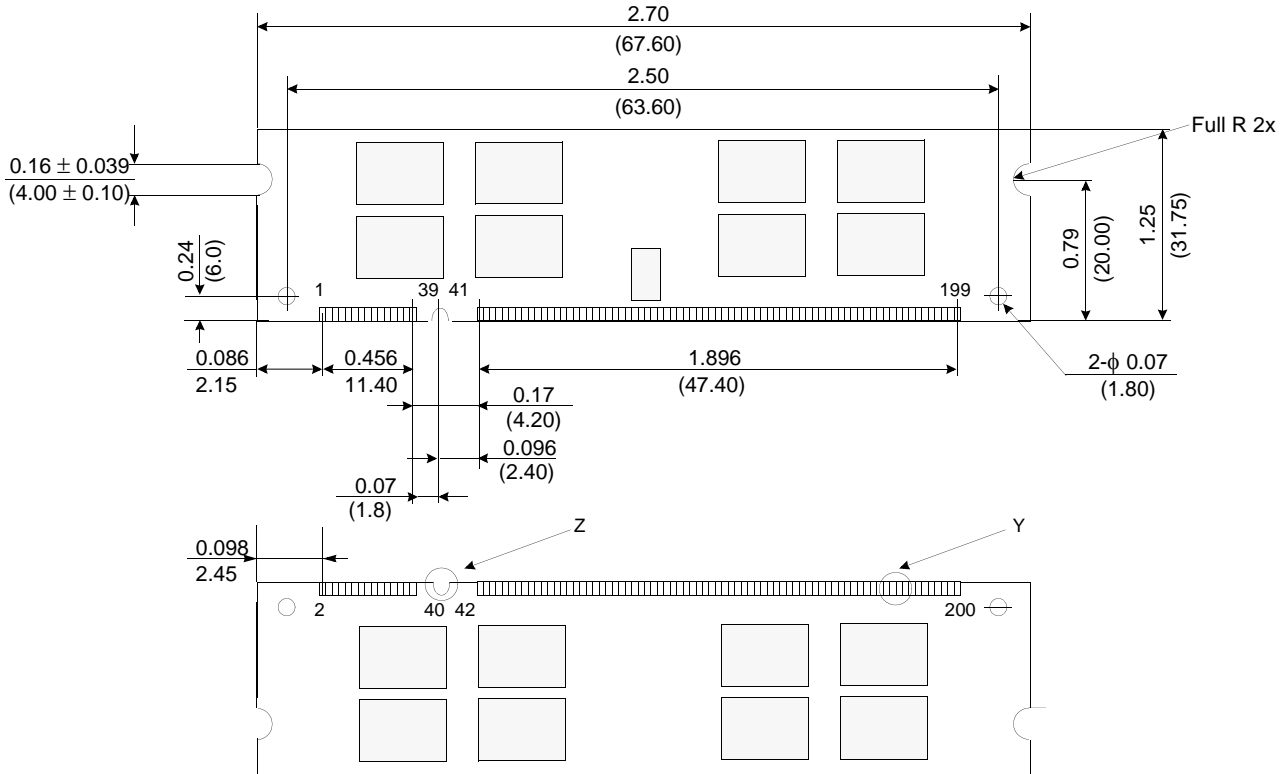
Detail Y

Tolerances : ±.006(.15) unless otherwise specified  
The used device is 32Mx16 SDRAM, TSOPII  
SDRAM Part No. : K4H511638F-L\*\*\*

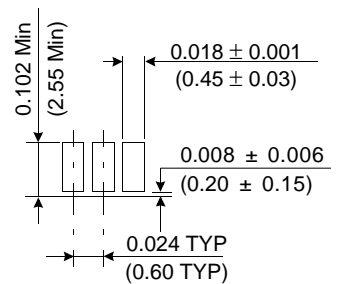


17.2 128Mx64 (M4702923F60)

Units : Inches (Millimeters)



Detail Z



Detail Y

Tolerances :  $\pm 0.006(.15)$  unless otherwise specified  
 The used device is 64Mx8 DDR SDRAM, sTSP0II-300mil  
 SDRAM Part No. : K4H510838F-6\*\*\*