

#### **DATA SHEET**

### **CX77105 Power Amplifier Module for CDMA/AMPS** (824–849 MHz)

#### Applications

- Digital cellular (CDMA)
- Analog cellular (AMPS)
- Wireless local loop (WLL)

#### Features

- Low voltage positive bias supply
  - 3.2 V to 4.2 V, typical
- Good linearity
- · High efficiency
- Dual mode operation
- Large dynamic range
- 10-pad package
  4 x 4 x 1.5 mm
- · Power down control
- Low power-state control

Skyworks offers lead

friendly" packaging

for the Restriction of Hazardous Substances).

that is RoHS compliant (European Parliament

(Pb)-free "environmentally

InGaP

NFW

• IS 95/CDMA2000

#### Description

The CX77105, a dual-mode, Code Division Multiple Access (CDMA) / Advanced Mobile Phone Service (AMPS) Power Amplifier Module (PAM), is a fully matched, 10-pad surface mount module developed for cellular handsets and wireless local loop applications. This small and efficient power amplifier module packs a full 824–849 MHz bandwidth coverage into a single compact package. The device meets the stringent IS95 CDMA linearity requirements to and exceeding 28 dBm output power, and can be driven to levels beyond 31 dBm for high efficiency in FM mode operation. A low current digital pad (VCONT) provides improved efficiency for the low RF power range of operation.

The single Gallium Arsenide (GaAs) Microwave Monolithic Integrated Circuit (MMIC) contains all active circuitry in the module. The MMIC contains on-board bias circuitry, as well as input and interstage matching circuits. Output match into a 50  $\Omega$  load is realized off-chip and within the module package to optimize efficiency and power performance. This device is manufactured with Skyworks' GaAs Heterojunction Bipolar Transistor (HBT) process that provides for all positive voltage DC supply operation while maintaining high efficiency and good linearity. Primary bias to the CX77105 is supplied directly from a three-cell Ni-Cd, a single-cell Li-Ion, or other suitable battery with an output in the 3 to 4 volt range. Power down is accomplished by setting the voltage on the low current reference pad to zero volts. No external supply side switch is needed as typical "off" leakage is a few microamperes with full primary voltage supplied from the battery.

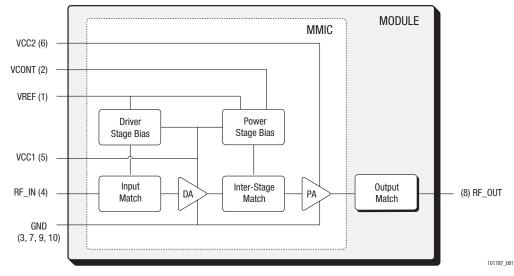


Figure 1. CX77105 Functional Block Diagram

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### **Electrical Specifications**

The following tables list the electrical characteristics of the CX77105 Power Amplifier. Table 1 lists the absolute maximum ratings and Table 2 lists the recommended operating conditions

for achieving the electrical performance listed in Table 4. Table 3 is a truth table for the CX77105 Power Amplifier.

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
RF Input Power		Pin	_	4.0	7.0	dBm
Supply Voltage		Vcc	_	3.4	6.0	Volts
Reference Voltage		VREF	_	3.0	3.1	Volts
Case Temperatures	Operating	Tc	-30	25	+110	°C
base remperatures	Storage	Tstg	-55	_	+125	°C

#### Table 1. Absolute Maximum Ratings<sup>1</sup>

<sup>1</sup> No damage assuming only one parameter is set at limit at a time with all other parameters set at nominal value.

#### **Table 2. Recommended Operating Conditions**

Parameter		Symbol	Minimum	Nominal	Maximum	Unit
Supply Voltage		Vcc	3.2	3.4	4.2	Volts
Reference Voltage	PA On	VREF	2.95	3.0	3.05	Volts
nererence voltage	PA Off	VIILI	—	—	0.5	1010
Mode Input Impedance >2.5 kW	High Bias	VCONT	0.0	_	0.5	Volts
	Low Bias	VCONT	2.5	—	3.0	VOID
Operating Frequency		Fo	824.0	836.5	849.0	MHz
Case Operating Temperature		Тс	-30	_	+85	°C

#### Table 3. Power Range Truth Table

Power Mode	Vref	VCONT	Range
High Power	3.0 V	0.0–0.5 V	16 dBm-31 dBm
Low Power	3.0 V	2.5–3.0 V	$\leq$ 16 dBm
Shut Down	0.0 V	0.0 V	—

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Characteristi	ics	Symbol	Condition	Minimum	Typical	Maximum	Unit
	Digital Mode	Glow		25.0	27.0	28.0	
Gain conditions	Digital mode	Gніgh	$\label{eq:Vcont} \begin{array}{l} \text{Vcont} \leq 0.5 \text{ V} \\ \text{Po} = 28 \text{ dBm} \end{array}$	28.5	29.0	31.0	dB
	Analog Mode	Gp	$\label{eq:Vcont} \begin{array}{l} \text{Vcont} \leq 0.5 \text{ V} \\ \text{Po} = 31 \text{ dBm} \end{array}$	27.5	29.0	31.0	
	Digital Mode	PAELOW	$\begin{array}{l} \text{VCONT} \geq 2.5 \text{ V} \\ \text{Po} = 16 \text{ dBm} \end{array}$	7.6	8.5	_	
Power Added Efficiency	Digital Mode	РАЕнідн	$\begin{array}{l} \text{VCONT} \leq 0.5 \text{ V} \\ \text{Po} = 28 \text{ dBm} \end{array}$	37.0	40.0	_	%
	Analog Mode	ΡΑΕΑ	$\label{eq:Vcont} \begin{array}{l} \text{Vcont} \leq 0.5 \text{ V} \\ \text{Po} = 31 \text{ dBm} \end{array}$	48.0	55.0	_	
Total Supply Current		Icc_low	Po = 16 dBm	_	137	153	mA
		Ісс_нідн	Po = 28 dBm	—	490	500	IIIA
Quiescent Current		Iq_low	$V_{CONT} \geq 2.5 \text{ V}$	40			mA
		Іо_нісн	$V_{CONT} \le 0.5 \ V$	60	55	75	
Reference Current		IREF	—	—	2.5	5.0	mA
Control Current		Ictrl	Vcont = 2.5 V	200	235	500	μA
Total Supply current in Power-do	own Mode	IPD	Vcc = 3.4 V Vref = 0 V	_	3.0	5.0	μA
	885 kHz offset	ACP1LOW	$\label{eq:Vcont} \begin{array}{l} \text{Vcont} \geq 2.5 \text{ V} \\ \text{Po} \leq 16 \text{ dBm} \end{array}$	-	-49.0	-47.3	
Adjacent Channel Power <sup>2,3</sup>	000 KH2 011361	ACP1HIGH	$\label{eq:VCONT} \begin{array}{l} V \text{CONT} \leq 0.5 \text{ V} \\ P_0 \leq 28 \text{ dBm} \end{array}$	_	-50.0	-47.0	dBc
Aujacent Gnamer i Gwer	1.98 MHz offset	ACP2Low	$\label{eq:Vcont} \begin{array}{l} \text{Vcont} \geq 2.5 \text{ V} \\ \text{Po} \leq 16 \text{ dBm} \end{array}$	-	-65.0	-59.0	ubc
		АСР2нідн	$\label{eq:VCONT} \begin{array}{l} \text{Vcont} \leq 0.5 \text{ V} \\ \text{Po} \leq 28 \text{ dBm} \end{array}$	_	-60.0	-57.4	
Harmonic Suppression	Second	fo2	$P_0 \le 28 \text{ dBm}$	—	-38.0	-35.0	dBc
namonic ouppiession	Third	fo3	$P_0 \le 28 \text{ dBm}$	—	-59.0	-45.0	UDU
Noise Power in RX Band 869-89	4 MHz	RxBN	$P_0 \le 28 \text{ dBm}$	_	-137	_	dBm/Hz
Noise Figure		NF	—	—	4.6	5.0	dB
Input Voltage Standing Wave Rat	tio	VSWR	—	—		1.9:1	—
Stability (Spurious output)		S	5:1 VSWR all phases		_	-60.0	dBc
Ruggedness—No damage4		Ru	$P_0 \le 28 \text{ dBm}$	10:1	_	_	VSWR

Table 4. Electrical Specifications for CDMA / AMPS Nominal Operating Conditions<sup>1</sup>

<sup>1</sup> VCC = +3.4 V, VREF = +3.0 V, Freq = 836.5 MHz, TC = 25 °C, unless otherwise specified.

<sup>2</sup> ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

<sup>3</sup> CDMA2000 is configured as DCCH = 9600, SCH0 = 9600, PCH (Walsh 0) = - 3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For CDMA2000, 0.5 dB back-off in output power is required.

<sup>4</sup> All phases, time = 10 seconds.

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Table 5. Liecultal specifications for Obmet / Amr 5 neconfinenced operating conditions						
Characteristics	6	Symbol	Condition	Minimum	Maximum	Unit
	Digital Mode	Glow	$ \begin{array}{l} \text{VCONT} \geq 2.5 \text{ V} \\ \text{Po} = 16 \text{ dBm} \end{array} $	24.0	28.5	
Gain conditions		Gніgh	$\begin{array}{l} \text{Vcont} \leq 0.5 \text{ V} \\ \text{Po} = 28 \text{ dBm} \end{array}$	27.1	32.4	dB
	Analog Mode	Gp	$ \begin{array}{l} \text{Vcont} \leq 0.5 \text{ V} \\ \text{Po} = 31 \text{ dBm} \end{array} $	24.0	33.0	
	1.25 MHz offset	ACP1LOW	$\begin{array}{l} \text{Vcont} \geq 2.5 \text{ V} \\ \text{Po} \leq 16 \text{ dBm} \end{array}$	_	-44	
Adjacent Channel Power <sup>2,3</sup>		ACP1HIGH	$\begin{array}{l} \text{Vcont} \leq 0.5 \text{ V} \\ \text{Po} \leq 28 \text{ dBm} \end{array}$	_	-44	dBc
	1.98 MHz offset	ACP2LOW	$ \begin{array}{l} \text{VCONT} \geq 2.5 \text{ V} \\ \text{Po} \leq 16 \text{ dBm} \end{array} \end{array}                                 $	_	-56	
		ACP2HIGH	$\begin{array}{l} \text{Vcont} \leq 0.5 \text{ V} \\ \text{Po} \leq 28 \text{ dBm} \end{array}$	_	-56	
Harmonic Suppression	Second	fo2	$P_0 \le 28 \text{ dBm}$	—	-30	dBc
	Third	fo3	$P_0 \le 28 \text{ dBm}$	—	-40	
Noise Power in RX Band 869-894 I	MHz	RxBN	$P_0 \le 28 \text{ dBm}$	—	-134.0	dBm/Hz
Noise Figure		NF	—	—	7.0	dB
Input Voltage Standing Wave Ratio	(VSWR)	VSWR	_		2.0:1	—
Stability (Spurious output)		S	5:1 VSWR All phases	_	-60.0	dBc
Ruggedness – No damage <sup>4</sup>		Ru	$P_0 \leq 28 dBm$	10:1		VSWR

Table 5. Electrical Specifications for CDMA / AMPS Recommended Operating Conditions <sup>1</sup>

<sup>1</sup> Per Table 2, unless otherwise specified.

<sup>2</sup> ACP is specified per IS95 as the ratio of the total in-band power (1.23 MHz BW) to adjacent power in a 30 kHz BW.

<sup>3</sup> CDMA2000 is configured as DCCH = 9600, SCH0 = 9600, PCH (Walsh 0) = -3.75 dB, and Peak-to-Average Ratio (CCDF = 1%) = 4.5 dB. For CDMA2000, 0.5 dB back-off in output power is required.

<sup>4</sup> All phases, time = 10 seconds.

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#### **Characterization Data**

The following graphs illustrate the characteristics of a typical CX77105 power amplifier designed for operation in the cellular frequency band (824–849 MHz). This amplifier was selected by characterizing a group of devices and then selecting a part with average electrical performance for both nominal and the full range of recommended operating conditions, including worst case limits. Figure 2 through Figure 8 illustrate the digital signal

characteristics of the CX77105. Shown are power sweep characteristics for key performance parameters, over temperature and frequency, up to 28.5 dBm output power. The data was taken up to and including 16 dBm output power with the bias mode control pad setting of  $V_{CONT} = 2.5$  volts. Beyond 16 dBm output power, the  $V_{CONT}$  was set to zero volts.

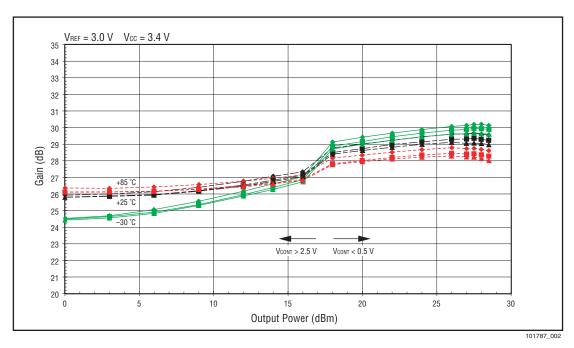


Figure 2. Digital Mode Gain vs. Output Power

Legend		
— <b>◆</b> — 824 @ −30 °C	— 🔶 - · 824 @ +25 °C	<b>◆</b> 824 @ +85 ℃
— <b>■</b> — 837 @ –30 °C	—- <b>—</b> · 837 @ +25 ℃	<b> 837 @ +85</b> °C
— <b>▲</b> — 849 @ –30 °C	— 🛧 -· 849 @ +25 ℃	<b>▲</b> 849 @ +85 ℃

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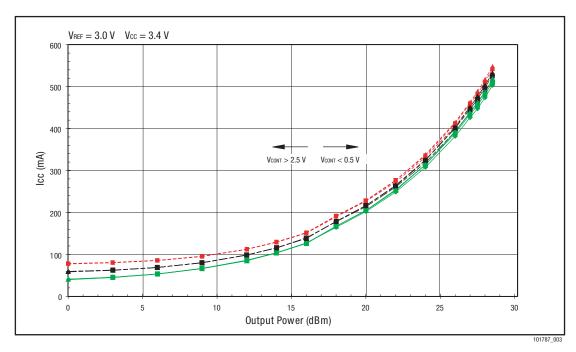


Figure 3. Primary Bias Current vs. Output Power

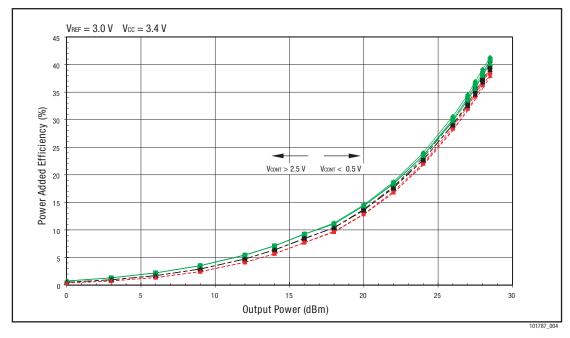


Figure 4. Power Added Efficiency vs. Output Power

Legend		
— <b>◆</b> — 824 @ −30 °C	— ◆ - · 824 @ +25 °C	<b>◆</b> 824 @ +85 ℃
— <b>■</b> — 837 @ –30 °C	—- <b>—</b> 837 @ +25 ℃	<b></b> 837 @ +85 °C
— <b>▲</b> — 849 @ −30 °C	— <del>▲</del> -· 849 @ +25 °C	<b>▲</b> 849 @ +85 ℃

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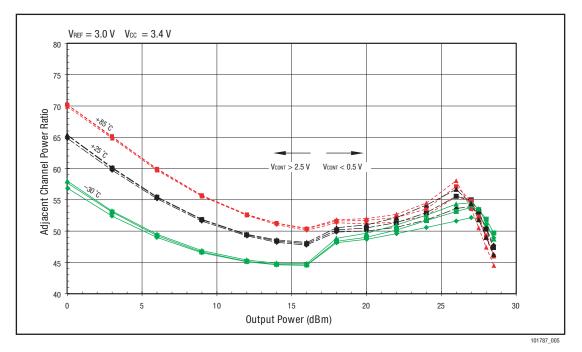


Figure 5. Channel Power for 885 kHz Offset Current vs. Output Power

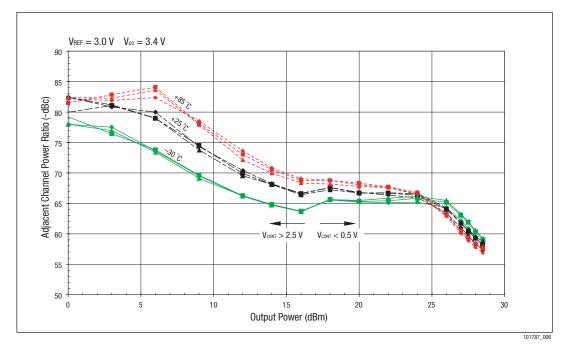


Figure 6. Adjacent Channel Power for 1.98 MHz Offset vs. Output Power

Legend		
— <b>◆</b> — 824 @ −30 °C	— ◆ -· 824 @ +25 °C	◆ 824 @ +85 °C
— <b>■</b> — 837 @ –30 °C	— 📥 - · 837 @ +25 °C	<b></b> 837 @ +85 °C
— <b>▲</b> — 849 @ −30 °C	— 🛧 -· 849 @ +25 ℃	<b>▲</b> 849 @ +85 ℃

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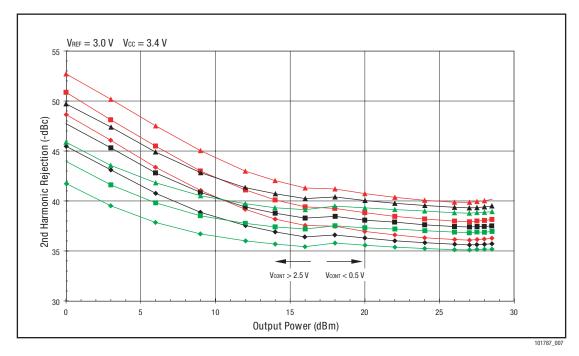


Figure 7. Second Harmonic Rejection vs. Output Power

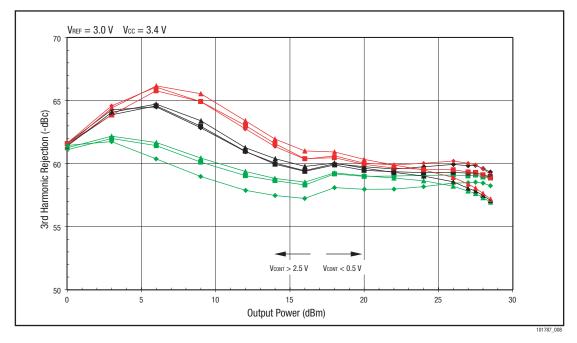


Figure 8. Third Harmonic Rejection vs. Output Power

Legend		
— <b>◆</b> — 824 @ −30 °C	— ◆ - · 824 @ +25 °C	◆ 824 @ +85 °C
— <b>■</b> — 837 @ –30 °C	— — 837 @ +25 °C	<b></b> 837 @ +85 °C
— <b>▲</b> — 849 @ −30 °C	— <del>▲</del> - · 849 @ +25 °C	<b>▲</b> 849 @ +85 ℃

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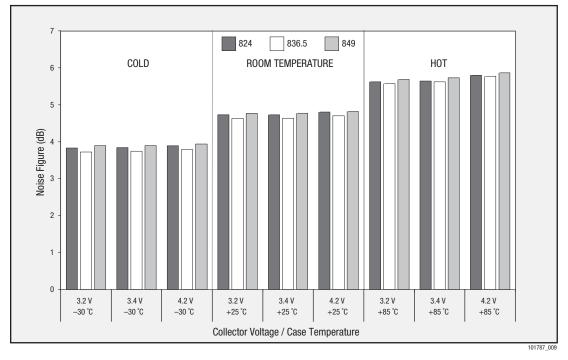


Figure 9. Noise Figure as Function of Operating Conditions

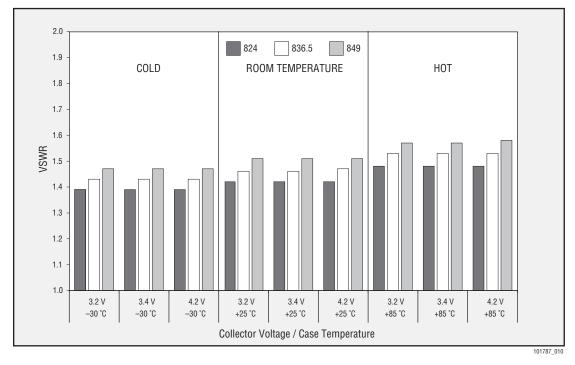


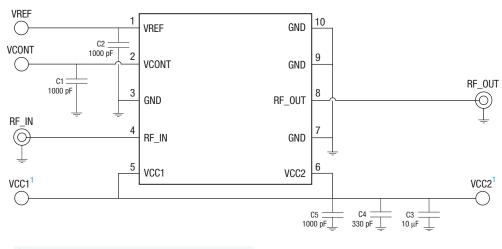
Figure 10. Input VSWR as Function of Operating Conditions

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### **Evaluation Board Description**

The evaluation board is a platform for testing and interfacing design circuitry. To accommodate the interface testing of the CX77105, the evaluation board schematic and diagrams are

included for preliminary analysis and design. Figure 11 shows the basic schematic of the board for the 824 MHz to 849 MHz range.



<sup>1</sup>All supply pins may be connected together at the supply.

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Figure 11. CX77105 Evaluation Board Schematic

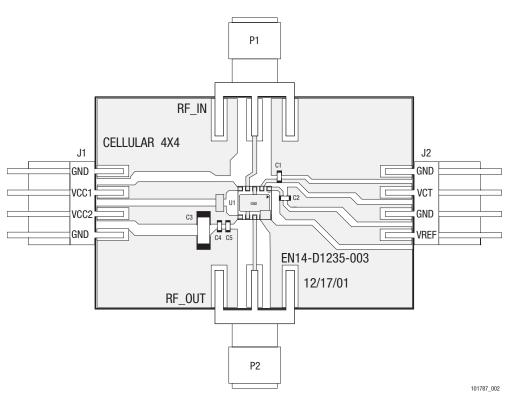
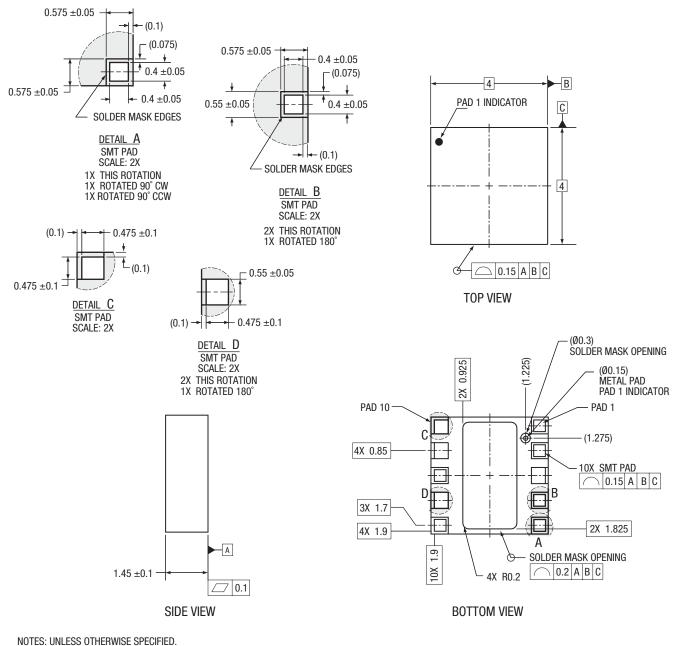


Figure 12. Evaluation Board Assembly Diagram

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#### **Package Dimensions and Pin Descriptions**

The CX77105 is a multi-layer laminate base, overmold encapsulated modular package designed for surface mount solder attachment to a printed circuit board. Figure 13 is a mechanical drawing of the pad layout for this package. Figure 14 provides a recommended phone board layout footprint for the PAM to help the designer attain optimum thermal conductivity, good grounding, and minimum RF discontinuity for the 50-ohm terminals. The pad numbering convention starts with pad 1 in the upper left, as indicated in Figure 15, and increments counter-clockwise around the package. Figure 16 illustrates typical case markings.



1. Dimensioning and Tolerancing in accordance with ASME Y14.5M-1994.

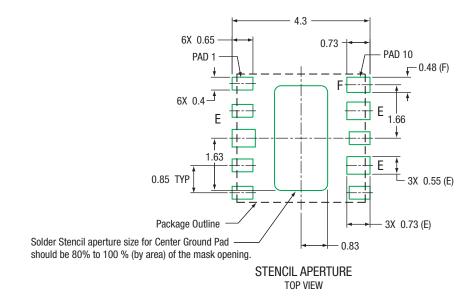
2. All dimensions are in millimeters.

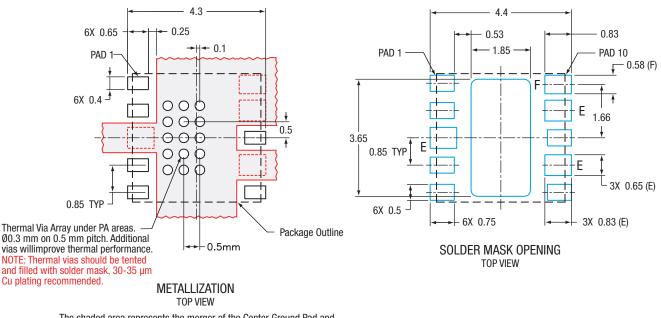
3. Pads are solder mask and metal defined.

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#### Figure 13. Dimensional Drawing for 4 x 4 x 1.5 mm, 10-Pad Package – CX77105 Specific

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The shaded area represents the merger of the Center Ground Pad and 4 individual I/O pads thus reducing the number of places dimensioned.

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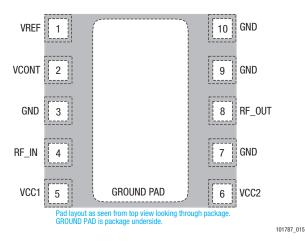


Figure 15. CX77105 Pin Configuration (Top View)

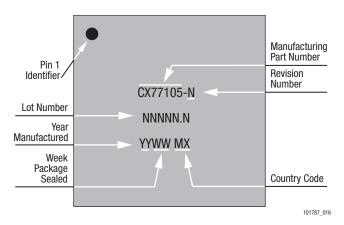


Figure 16. Typical Case Markings (Top View)

### **Package and Handling Information**

Because of its sensitivity to moisture absorption, this device package is baked and vacuum-packed prior to shipment. Instructions on the shipping container label must be followed regarding exposure to moisture after the container seal is broken, otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The CX77105 is capable of withstanding an MSL3/240 °C solder reflow. Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. If the part is attached in a reflow oven, the temperature ramp rate should not exceed 3 °C per second; maximum temperature should not exceed 240 °C. If the part is manually attached, precaution should be taken to insure that the part is not subjected to temperatures exceeding 240 °C for more than 10 seconds. For details on both attachment techniques, precautions, and handling procedures recommended by Skyworks, please refer to Skyworks

Application Note: *PCB Design and SMT Assembly/Rework,* Document Number 101752. Additional information on standard SMT reflow profiles can also be found in the *JEDEC Standard J-STD–020.* 

Production quantities of this product are shipped in the standard tape-and-reel format. For packaging details, refer to Skyworks Application Note: *Tape and Reel Information – RF Modules,* Document Number 101568.

#### **Electrostatic Discharge Sensitivity**

The CX77105 is a Class I device. Figure 17 lists the Electrostatic Discharge (ESD) immunity level for each non-ground pad of the CX77105 product. The numbers in Figure 17 specify the ESD threshold level for each pad where the I-V curve between the pad and ground starts to show degradation.

The ESD testing was performed in compliance with MIL-STD-883E Method 3015.7 using the Human Body Model. If ESD damage threshold magnitude is found to consistently exceed 2000 volts on a given pad, this so is indicated. If ESD damage threshold below 2000 volts is measured for either polarity, numbers are indicated that represent worst case values observed in product characterization.

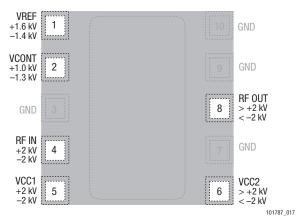


Figure 17. ESD Sensitivity Areas (Top View)

Various failure criteria can be utilized when performing ESD testing. Many vendors employ relaxed ESD failure standards, which fail devices only after "the pad fails the electrical specification limits" or "the pad becomes completely non-functional". Skyworks employs most stringent criteria and fails devices as soon as the pad begins to show any degradation on a curve tracer.

To avoid ESD damage, both latent and visible, it is very important that the product assembly and test areas follow the Class-1 ESD handling precautions listed in. Table 6

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	Wrist Straps		
Personnel Grounding	Conductive Smocks, Gloves and Finger Cots		
	Antistatic ID Badges		
Facility	Relative Humidity Control and Air Ionizers		
raciiity	Dissipative Floors (less than $10^9 \Omega$ to GND)		
	Dissipative Table Tops		
	Protective Test Equipment (Properly Grounded)		
Protective Workstation	Grounded Tip Soldering Irons		
	Conductive Solder Suckers		
	Static Sensors		
	Bags and Pouches (Faraday Shield)		
	Protective Tote Boxes (Conductive Static Shielding)		
Protective Packaging & Transportation	Protective Trays		
	Grounded Carts		
	Protective Work Order Holders		

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#### **Ordering Information**

Model Number	Manufacturing Part Number	Product Revision	Package	Operating Temperature
CX77105	CX77105-16P	16	MCM 4x4LM-10	−30 °C to +85 °C

#### **Revision History**

Revision	Level	Date	Description
A		December 10, 2002	Initial Release
В		April 20, 2005	Revise: Figure 1, 11, 12; Table 1 Add: Figure 14
С		January 6, 2006	Add: Lead-free statement (p1) Revise: Figures 13, 14; section Package and Handling Information: changes solder flow temperature ramp rate to 3 °C/sec

#### References

Application Note: PCB Design and SMT Assembly/Rework, Document Number 101752. Application Note: Tape and Reel Information – RF Modules, Document Number 101568 JEDEC Standard J–STD–020.

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