

# SKY13290-000/099: 20 MHz-2.5 GHz, 10 W pHEMT SPDT Switch

## Applications

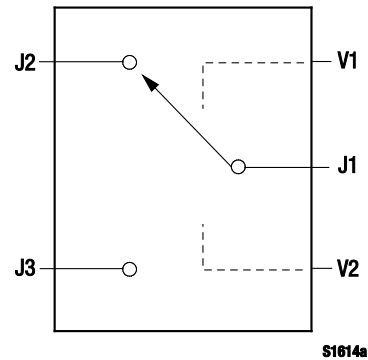
- Transmit/receive switching for telematic systems at elevated power levels

## Features

- Broadband frequency range: 20 MHz to 2.5 GHz
- Very low insertion loss, 0.4 dB typical @ 0.9 GHz
- High isolation: 26 dB typical @ 0.9 GHz
- High input power compression: 0.1 dB @ > +40 dBm
- Low current consumption: <100  $\mu$ A @ 3 V
- Bare pHEMT die: 1355 x 830 x 200  $\mu$ m
- Chips supplied on Gel-Pak® or singulated wafers on film frame



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**Figure 1. SKY13290-000 Block Diagram**

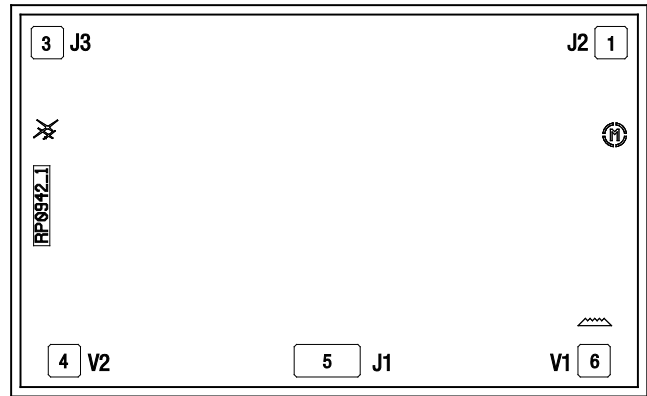
## Description

The SKY13290-000/099 is a high power, pHEMT Single Pole Double Throw (SPDT) switch. The switch is designed for use in systems operating from 20 MHz to 2.5 GHz for which low loss, high isolation, low control voltage, and chip scale size are required.

The device is controlled with positive, negative, or a combination of both voltages. The RF signal paths within the device are fully bilateral.

The SKY13290-000/099 is provided as a bare die in an ultra-compact 1355 x 830 x 200  $\mu$ m design. Chips are shipped in quantities of 100 per 2 x 2 inch Gel-Pak (use part number SKY13290-000). For high volume orders, chips can be supplied on a film frame (use part number SKY13290-099).

A functional block diagram is shown in Figure 1. The pin configuration is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.



Pin 2 is ground pad on backside of chip

S2439

**Figure 2. SKY13290-000/099 Pinout –6-Pin QFN (Top View)**

**Table 1. SKY13290-000/099 Signal Descriptions**

Pin #	Name	Description	Pin #	Name	Description
1	J2	RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J1 using a low insertion loss path or isolated from J1 (Note 1).	4	V2	DC control voltage input #2. The logic voltage applied to this pin, along with the voltage level applied to the V1 pin, determines the states of the RF paths between J1/J2 and J1/J3.
2	GND	Ground. Backside of chip. Mount with conductive or non-conductive epoxy.	5	J1	RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J2 or to J3 using a low insertion loss path and isolated from the other RF port (Note 1).
3	J3	RF input/output. According to the logic voltage levels applied to the V1 and V2 pins, this port is either connected to J1 using a low insertion loss path or isolated from J1 (Note 1).	6	V1	DC control voltage input #1. The logic voltage applied to this pin, along with the voltage level applied to the V2 pin, determines the states of the RF paths between J1/J2 and J1/J3.

**Note 1:** A 47 pF blocking capacitor is required for >500 MHz operation. Use larger value capacitors for lower frequency operation.

### Technical Description

The SKY13290-000/099 is controlled using two voltage inputs, V1 and V2 (pins 6 and 4, respectively). Depending on the voltage level applied to these pins, the common RF port (J1) is connected to one of two RF ports (J2 or J3) using a low insertion loss path, while the path between J1 and the other RF port is in its isolation state.

When the control voltages are toggled, the states between J1 and J2, as well as J1 and J3, are also toggled.

### Electrical and Mechanical Specifications

The absolute maximum ratings of the SKY13290-000/099 are provided in Table 2. Electrical specifications are provided in Table 3 and the operating characteristics are specified in Table 4.

Typical performance characteristics of the SKY13290-000/099 are illustrated in Figures 3 through 6.

The state of the SKY13290-000/099 is determined by the logic provided in Table 5.

**Table 2. SKY13290-000/099 Absolute Maximum Ratings**

Parameter	Symbol	Minimum	Maximum	Units
Control voltage	V <sub>CTL</sub>	0	+10	V
RF input power (V <sub>CTL</sub> > 0.9 GHz)	P <sub>IN</sub>		+43.5	dBm
Operating temperature	T <sub>OP</sub>	-40	+85	°C
Storage temperature	T <sub>STG</sub>	-65	+150	°C

**Note:** Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value.

**CAUTION:** Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.

**Table 3. SKY13290-000/099 Electrical Specifications (Note 1)**

(V<sub>CTL</sub> = 0-3 V, T<sub>OP</sub> = +25 °C, P<sub>IN</sub> = 0 dBm, Characteristic Impedance = 50 Ω, Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Insertion loss		0.02 to 1.0 GHz		0.40	0.50	dB
		1.0 to 2.0 GHz		0.45	0.60	dB
		2.0 to 2.5 GHz		0.55	0.70	dB
Isolation		0.02 to 1.0 GHz	23	26		dB
		1.0 to 2.0 GHz	17	20		dB
		2.0 to 2.5 GHz	15	18		dB
Return loss (Note 2)		0.02 to 1.0 GHz		20		dB
		1.0 to 2.5 GHz		20		dB
Switching characteristics: Rise/fall On/off		10/90% or 90/10% RF		650		ns
		50% V <sub>CTL</sub> to 90/10% RF		800		ns
0.1 dB Input Compression Point	IPO.1dB	@ 48 MHz		+37.6		dBm
		@ 900 MHz		+40.5		dBm
Thermal resistance				45		°C/W
Control voltage: Low (@ 20 μA max) High (@100 μA max) High (@ 200 μA max)	V <sub>CTL_L</sub>		0			V
	V <sub>CTL_H</sub>				2.7	V
	V <sub>CTL_H</sub>				10.0	V

**Note 1:** Performance is guaranteed only under the conditions listed in this Table.

**Note 2:** Return loss state. Lower frequency return loss is dependent on value of the DC blocking capacitors.

### Typical Performance Characteristics

( $V_{CTL} = 0-3\text{ V}$ ,  $T_{OP} = +25\text{ }^{\circ}\text{C}$ ,  $P_{IN} = 0\text{ dBm}$ , Characteristic Impedance  $[Z_0] = 50\ \Omega$ ,  $C_{BL} = 100\text{ pF}$ , Unless Otherwise Noted)

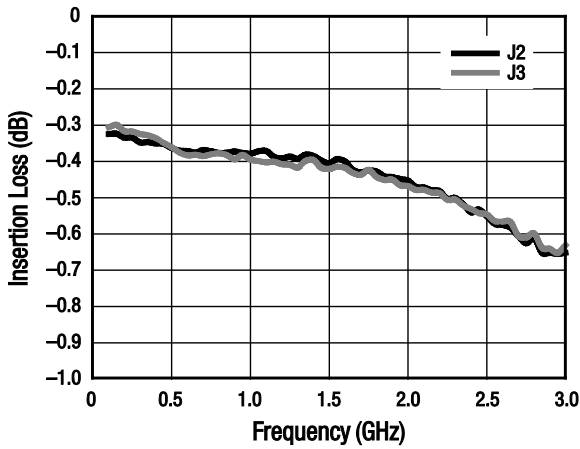


Figure 3. Insertion Loss vs Frequency

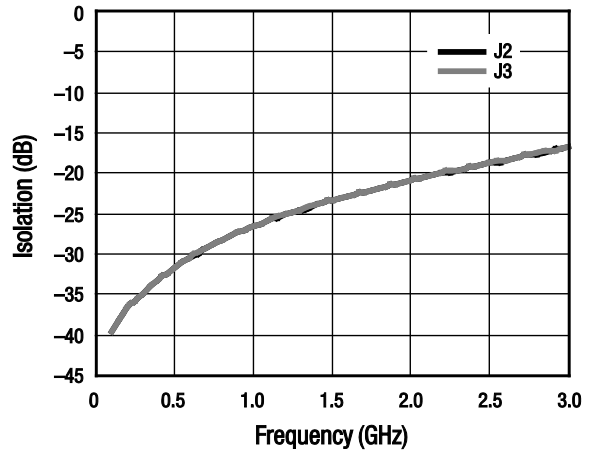


Figure 4. Isolation vs Frequency

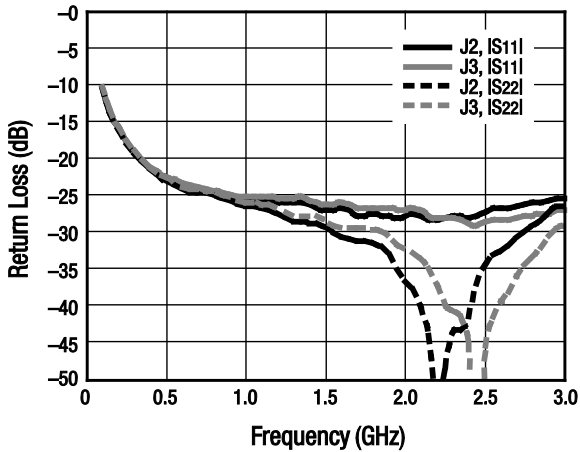


Figure 5. Return Loss vs Frequency (Insertion Loss State)

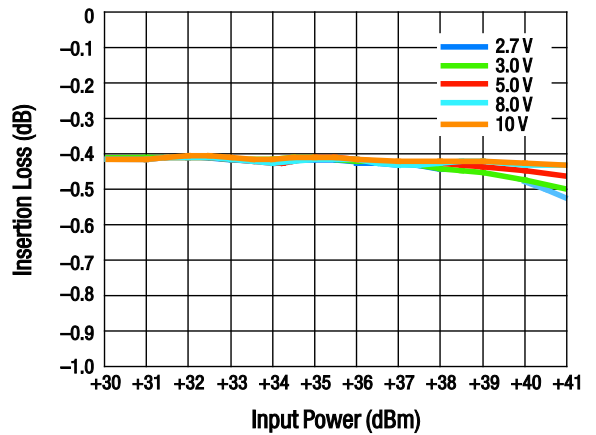


Figure 6. Insertion Loss vs Input Power (@ 900 MHz)

**Table 4. Truth Table (V<sub>HIGH</sub> = 2 to 5 V)**

V1	V2	J1-J2	J1-J3
V <sub>LOW</sub>	V <sub>HIGH</sub>	Isolation	Insertion loss
V <sub>HIGH</sub>	V <sub>LOW</sub>	Insertion loss	Isolation

**Note:** V<sub>LOW</sub> = 0 to 0.2 V, V<sub>HIGH</sub> = 2.7 to 10 V. Any state other than described in this Table places the device in an undefined state. An undefined state does not damage the device.

**Evaluation Board Description**

The SKY13290-000/099 is evaluated in a plastic package format to determine its performance characteristics. An Evaluation Board schematic diagram is provided in Figure 7. An assembly drawing for the Evaluation Board is shown in Figure 8.

**Chip Dimensions**

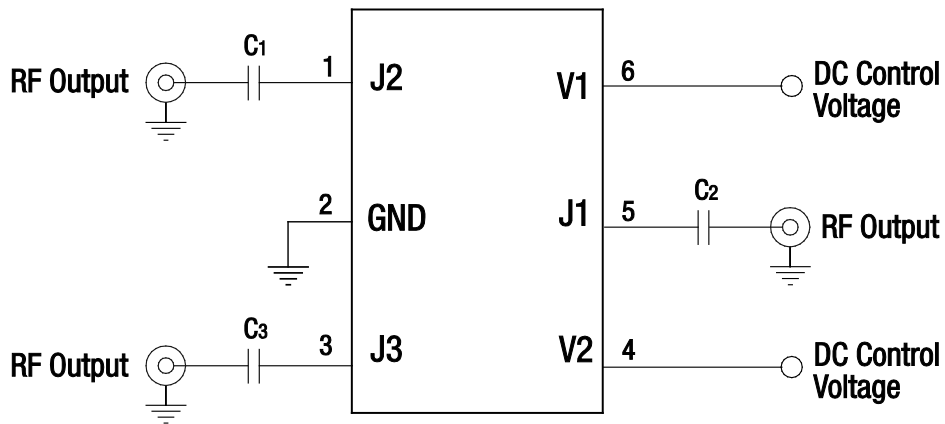
Chip dimensions are shown in Figure 9.

**Package and Handling Information**

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The SKY13290-000 chips are shipped in Gel-Paks. The SKY13290-099 wafers are shipped on film frames (see singulated wafer format dimensions in Figure 10).

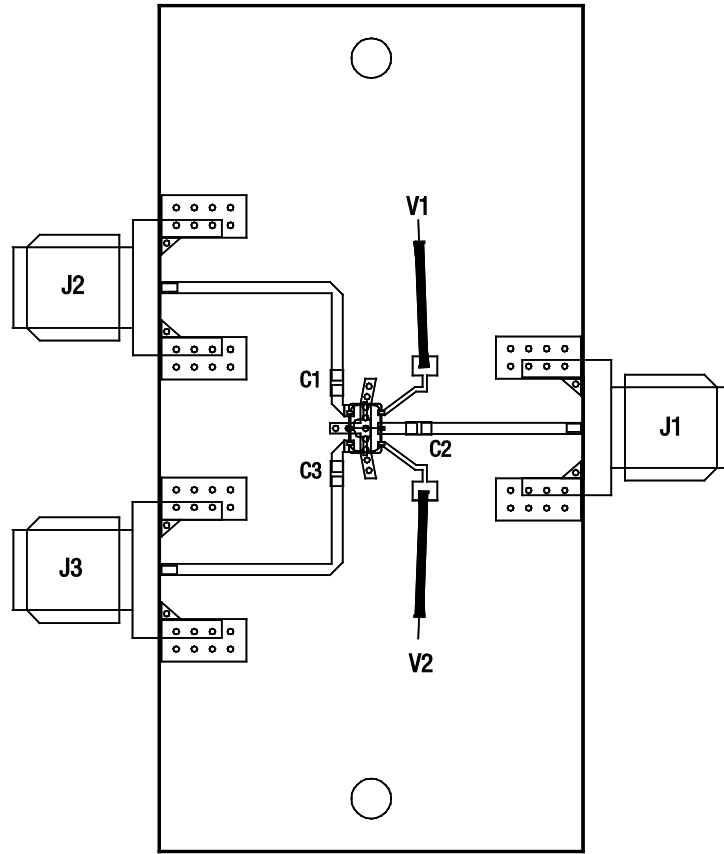
The SKY13290-000/099 has no backside metal and must be attached using conductive or non-conductive epoxy.



*Note: Use 47 pF blocking capacitors (C1, C2, C3) for >500 MHz operation. Higher values recommended for lower frequency operation. Exposed paddle must be grounded.  
Use 10 nF blocking capacitors (C1, C2, C3) for <50 MHz operation.*

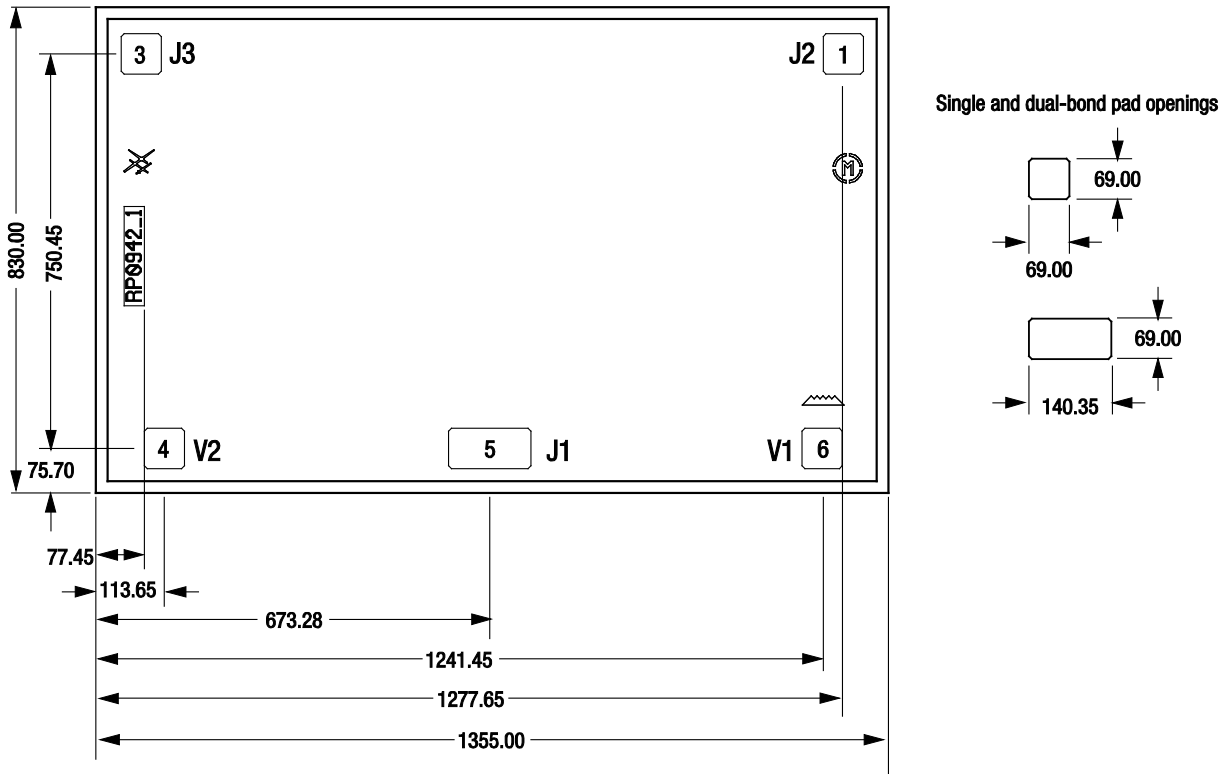
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**Figure 7. SKY13290-000/099 Evaluation Board Schematic**



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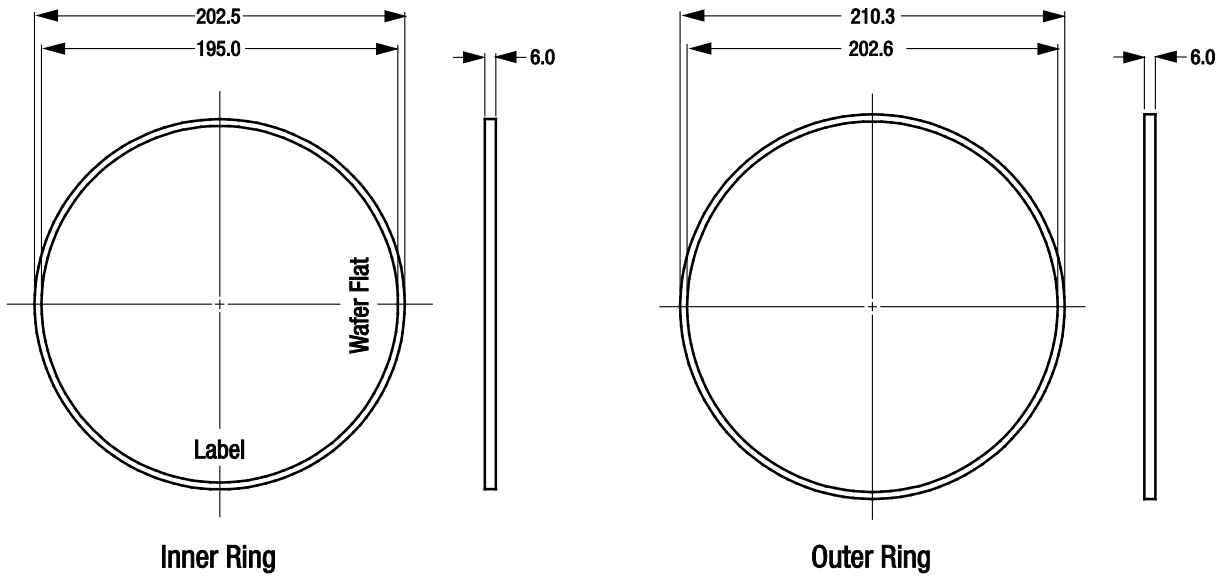
Figure 8. SKY13290-000/099 Evaluation Board Assembly Diagram



Notes: All dimensions are in microns.  
 Pin 2 is ground pad on backside of chip.  
 Bond pads are gold metalized.  
 Chip backside metalization: none.  
 Chip thickness: 200 microns

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Figure 9. SKY13290-000/099 Chip Dimensions



Grip Ring Number: GRP-2620-6

- Notes:  
1. All dimensions in millimeters.  
2. Tape material: unexposed UV tape.

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Figure 10. SKY13290-099 (Singulated Wafer Format)



**Ordering Information**

Model Name	Manufacturing Part Number	Evaluation Board Part Number
SKY13290 SPDT Switch	SKY13290-000 (100 chips per 2 x 2 inch Gel-Pak)	SKY13290-000-EVB
	SKY13290-099 (singulated wafers on film frame)	

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