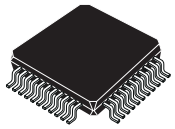
STA011

L-band RF front-end for digital radio

Preliminary Data

Features

- Single chip receiver for satellite and terrestrial digital radio
- Super-heterodyne tuner with low IF output
- High input intercept point
- Low noise IC
- RF image rejection mixer
- Adjustable RF and IF gain
- 54 dB IF VGA gain range
- Integrated RF and IF VCOs
- Integrated synthesizers
- Low cost external components
- I^2C-bus slave control interface
- Unregulated 2.7 to 3.3V supply voltage



TQFP44

Description

The STA011 is an RF IC using STMicroelectronics BiCMOS6G high speed technology for one chip solution for the digital satellite radio receiver. The STA011 is assembled in a TQFP44 package. The front-end architecture is a double conversion receiver (see block diagram). The chip includes all the RF functions up to low IF and it manages the signals going to and coming from the base-band.

Table 1. Device summary

Order code	Package	Packing
STA011	TQFP44 (10x10x1.4mm)(1)	Tube

1. ECOPACK® (see *Chapter 8*).

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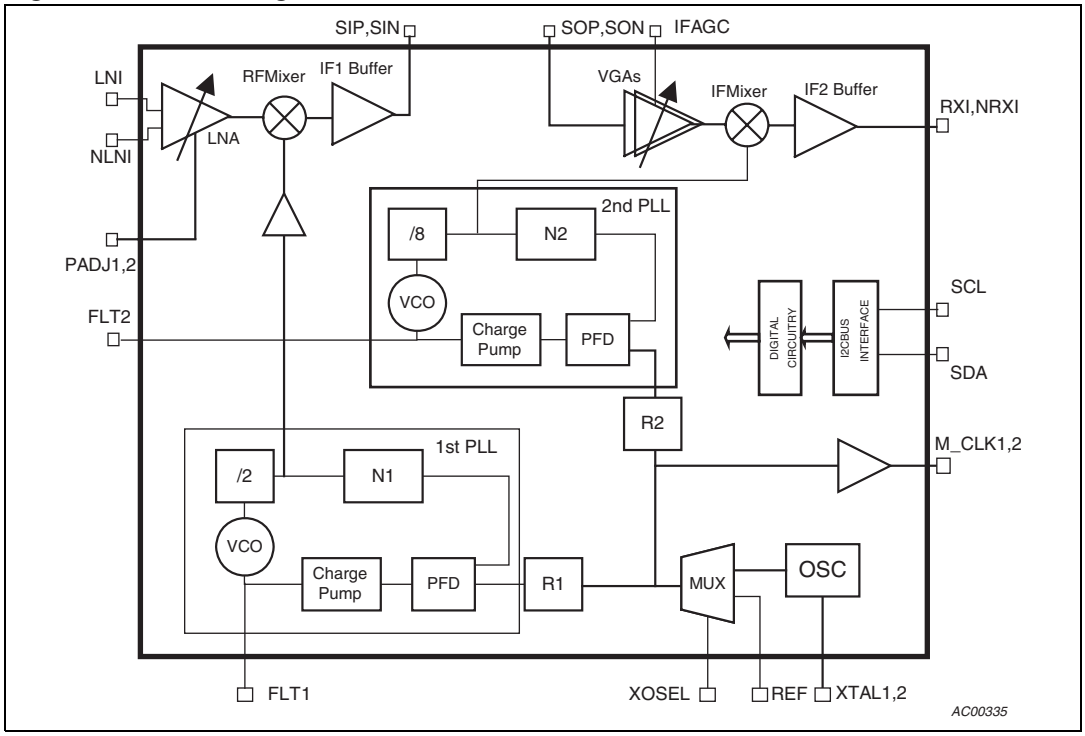
1 Block diagram

Figure 1. Block diagram



2 Pins description

Figure 2. Pins connection (top view)

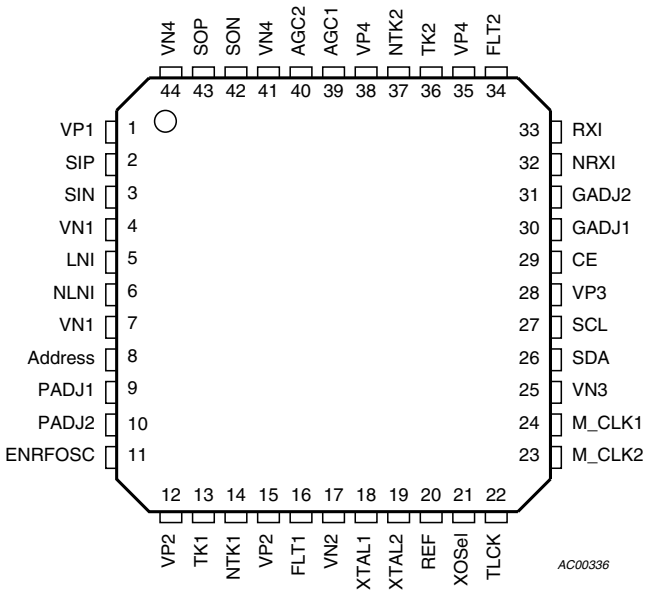


Table 2. Pins description

N.	Name	Function
1	VP1	Positive supply 1
2	SIP	SAW filter input connection
3	SIN	SAW filter input connection
4	VN1	Negative supply1
5	LNI	RF input
6	NLNI	RF input
7	VN1	Negative supply 1
8	Address	Device address selection
9	PADJ1	RF gain adjust connection1
10	PADJ2	RF gain adjust connection2
11	ENRFOSC	RF oscillator hardware enable
12	VP2	Positive supply 2
13	TK1	External LO1 connection1
14	NTK1	External LO1 connection2
15	VP2	Positive supply 2
16	FLT1	1st PLL loop filter connection
17	VN2	Negative supply 2

Table 2. Pins description (continued)

N.	Name	Function
18	XTAL1	Quartz oscillator connection 1
19	XTAL2	Quartz oscillator connection 2
20	REF	External optional TCXO input
21	XOSel	Internal/external XO selection
22	TLCK	Lock detector output
23	M_CLK2	Master Clock differential output2
24	M_CLK1	Master Clock differential output1
25	VN3	Negative supply 3
26	SDA	Data Serial Input
27	SCL	Clock Input
28	VP3	Positive supply 3
29	CE	Chip Enable
30	GADJ1	IF gain adjust connection 1
31	GADJ2	IF gain adjust connection 2
32	NRXI	Low IF Signal output 2
33	RXI	Low IF Signal output 1
34	FLT2	2^{nd} PLL loop filter connection
35	VP4	Positive supply 4
36	TK2	External LO2 connection1
37	NTK2	External LO2 connection2
38	VP4	Positive supply 4
39	AGC1	VGA control pin 1
40	AGC2	VGA control pin 2
41	VN4	Negative supply 4
42	SON	SAW filter negative output connection 2
43	SOP	SAW filter output connection 1
44	VN4	Negative supply 4

3 Electrical specifications

3.1 Absolute maximum/minimum ratings

Table 3. Absolute maximum/minimum ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{stg}	Storage temperature	-40		125	°C
T_{op}	Operating ambient temperature	-40	25	85	°C
V_{Max}	Maximum voltage on each pin			3.6	V
V_{Min}	Minimum voltage on each pin	GND-0.3			V
V_{pmax}	Minimum/Maximum power supply Between $VP_{1,2,3,4}$ and $VN_{1,2,3,4}$	-0.3		3.6	
$V_{ESD,HBM}$	Electrostatic discharge Voltage (ESD, Human Body Model)			2	kV

3.2 Operating conditions

Table 4. Operating conditions

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
VP	Operating supply voltage		2. 7		3.3	V
T_j	Junction temperature				125	°C

3.3 Thermal data

Table 5. Thermal data

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
$R_{th\ j\text{-}amb}$	Thermal resistance junction to ambient	According to JEDEC specification on a layers board		45		°C/W

3.4 Electrical characteristics

Table 6. Supply currents, (T_{amb} = 25°C, VP-VN = 3V)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
I_{CC1}	Current supplied by VP1	Powered circuits: LNA, RFMixer, IF buffer	12.5	17	21.5	mA
I_{CC2}	Current supplied by VP2	Powered circuits: RFVCO, divider by 2 and LO buffer Powered circuits: external LO1, divider by 2 and LO buffer	5.5 11.5	9 15	12.5 18.5	mA
I_{CC3}	Current supplied by VP3	Powered circuits: Digital cells, Crystal oscillator (XOSel high) Powered circuits: Digital cells, external REF (XOSel low)	5.5 3.5	7 6	11.5 8	mA
I_{CC4}	Current supplied by VP4	Powered circuits: VGAs, IFMixer, output buffer, IFPLL VAGC1=VAGC2=1.2V, IFgain=75dB	8.5	13	17.5	mA
I_{CCTOT}	I_{CC1+} I_{CC2+} I_{CC3+} I_{CC4}	CE = high, XOSel high, RFVCO enabled	36	46	56	mA
$I_{CCTOT,SB}$	Standby current	CE = low			20	µA

Table 7. LNA, RF mixer and IF1 buffer, (T_{amb} = 25°C, VP-VN = 3V)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
BWi	Input signal BW		1452		1492	MHz
BW0	Output signal BW		114		116.5	MHz
G_V	Voltage gain	Input LNI, NLNI pins; output SIP, SIN pins. R_L = 200Ω, PADj1,2 pins floating	26	30	34	dB
$G_{V,trim}$	Voltage gain	Input LNI, NLNI pins; output SIP,SIN pins. R_L=200Ω, R_{ext}=0	19	25	29	dB
ΔG_V	Voltage gain variation	Programmable via software mode		2.5		dB
Z_i	Input impedance	Balanced @ LNi, NLNI pins, R//C		75 0.2		Ω pF
Z_o	Output impedance	Balanced @ SIP, SIN pins		50		Ω
γ	Return loss	LNI,NLNI pins		14		dB
NF	Noise figure	Measurements condition: Input LNI, NLNI pins; output SIP,SIN pins,R_L=200Ω, PADj1,2 pins floating, R_s=50Ω		5	7	dB

Table 7. LNA, RF mixer and IF1 buffer, (T_{amb} = 25°C, VP-VN = 3V) (continued)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
NF_{trim}	Noise figure @ minimum gain	Measurements condition: Input LNI, NLNI pins; output SIP,SIN pins,R_L=200Ω, R_{ext}=0, R_s=50Ω		6.5	8.5	dB
IIP3	Input IP3	Input LNI, NLNI pins; output SIP,SIN pins. R_L=200Ω, PADj1,2 pins floating	-21	-17	-12	dBm
$IIP3_{trim}$	Input IP3 @ minimum gain	Input LNI, NLNI pins; output SIP,SIN pins. R_L=200Ω, R_{ext}=0	-18	-14.5	-7	dBm
1dB C.P.	1dB compression point	Input LNI, NLNI pins; output SIP,SIN pins. R_L=200Ω,PADj1,2 pins floating	-29	-26		dBm
$1dB\ C.P._{trim}$	1dB compression point	Input LNI, NLNI pins; output SIP,SIN pins. R_L=200Ω, R_{ext}=0	-27	-24		dBm
IR	Image rejection	RFin = LO-IF	15			dB
$REXT_{trim}$	REXT usable range	Connected between PADJ1 and PADJ2, to obtain intermediate gain between min and max	10		100	kΩ
$IF1_{leak}$	LO1 to IF1 leakage				-24	dBm
RF_{leak}	LO1 to RF leakage				-29	dBm
$V_{DC,RFin}$	LNI,NLNI common mode DC voltage	AC coupled to the balun	VP-1.3	VP-1.1	VP-0.9	V
$V_{DC,IFout}$	SIP,SIN common mode DC voltage	AC coupled to the SAW filter	VP-1.45	VP-1.2	VP-0.95	V

Table 8. IFVGA amplifiers, IF mixer and output buffer (T_{amb} = 25°C, VP-VN = 3V)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
BWi	Input signal BW		114		116.5	MHz
BWo	Output BW		0.6		3.1	MHz
G_{min}	Minimum gain	Input SOP, SON pins; output RXI,RXIN pins, RLoad high impedance, $VAGC_{1,2}$ = 0V		32	38	dB
G_{max}	Maximum gain	Input SOP, SON pins; output RXI,RXIN pins, RLoad high impedance, $VAGC_{1,2}$ = 3V	80	86		dB
I_{AGC}	Input current in AGC pin				10	µA
Z_{AGC}	AGC input impedance		150	600		kΩ

Table 8. IFVGA amplifiers, IF mixer and output buffer (T_{amb} = 25°C, VP-VN = 3V) (continued)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
NF	Noise Figure	Measurements condition: Input SOP, SON pins; output RXI, NRXI pins, R_S=50Ω, Double Side Band, IFGain=65dB		9	12	dB
1dB cp	1dB compression point	Gain=65dB	-53	-50		dBm
1dB $cp_{,fg}$	1dB compression point, full gain	Gain=81dB	-69	-66		dBm
IIP3	Input IP3	Gain=65dB	-45	-41		dBm
$IIP3_{,fg}$	Input IP3	Gain=81dB	-61	-57		dBm
Z_{in}	Input impedance	Balanced @ SOP, SON,		50		Ω
Z_{out}	Output impedance	Balanced @ RXI, RXIN Corresponding to 1.75mA in each emitter follower		50		Ω
$V_{DC,IFin}$	SIP, SIN common mode DC voltage	AC coupled to the SAW filter	VP-1.3	VP-1.1	VP-0.9	V
$V_{DC,RXout}$	RXI,NRXI common mode DC voltage	AC coupled to the base-band	VP-2.1	VP-1.8	VP-1.65	V
$V_{DC,PADJ}$	PADJ1,2 common mode DC voltage		VP-0.3	VP-0.12	VP-0.5	V
Z_{adj}	Gain adjustment pins impedance	Balanced GADJ1, GADJ2 pins	650	800	950	W
BB_{leak}	LO2 to BB leakage	Obtained by using low pass filter at the output		-49	-30	dBm
$IF2_{leak}$	LO2 to IF1 leakage	Obtained by using SAW filter at the input		-44	-30	dBm

Figure 3. Typical IF overall gain vs control voltage

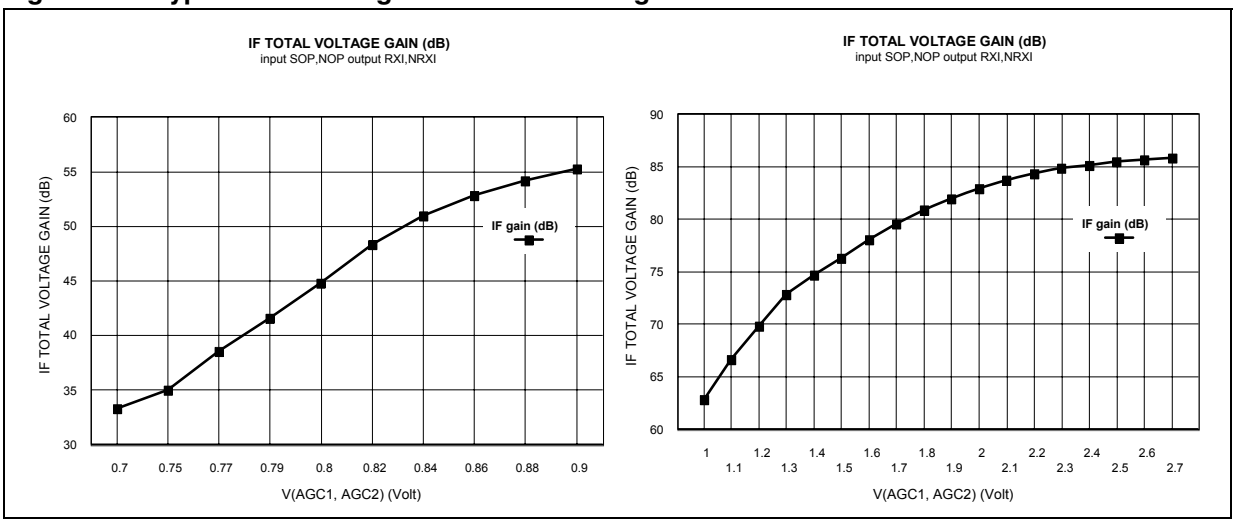


Table 9. Base-band output performance

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
R_{load}	Baseband Output load resistance	The output resistance the IC is loaded SE to GND	5			KΩ
C_{load}	Baseband output load capacitance	The output capacitance the IC is loaded SE to GND			10	pF

Table 10. Crystal oscillator, (T=25°C, VP-VN=3V)(1)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
f_{XTAL1}	Quartz frequency	Resonance mode: series Using 14.72		14.72		MHz
f_{XTAL2}	Quartz frequency	Resonance mode: series Using 14.725		14.725		MHz
Pn	Phase Noise	Δf=1kHz		-120	-118	dBc
$VDC_{,XTAL}$	XTAL1,2 common mode voltage		VP-1.1	VP-.9	VP-.7	V

1. A 18pF capacitor connected from XTAL1 pin to gnd is suggested for start-up robustness (see *Figure 4*).

Figure 4. System clock input/output

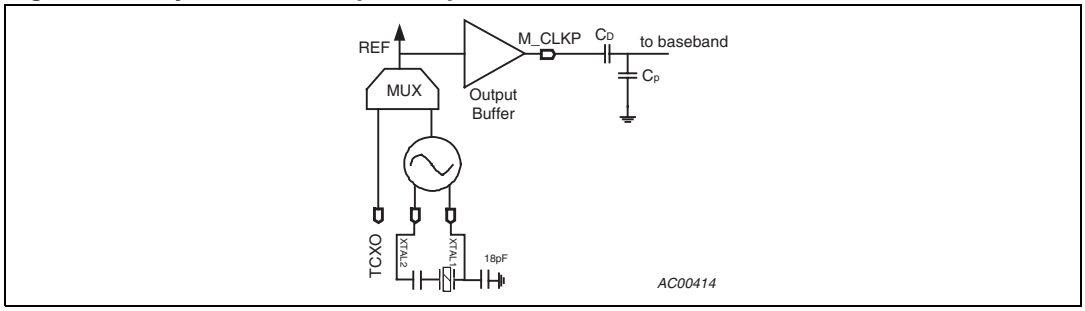


Table 11. PLLs, Synthesizers, (T_{amb} = 25°C, VP-VN = 3V)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
t_s	RF pll loop setting time			1	10	msec
P_n	Total phase noise contribution	100Hz<Δf<1.84MHz			1.8	°rms
f_{REF1}	RF pll comparison frequency	Programmable via software mode	0.92	3.68	14.72	MHz
f_{REF2}	IF pll comparison frequency	Programmable via software mode		113.23		KHz
P_{SP}	Spurious power level	RFPLL, Δf=n*460KHz IFPLL, Δf=113.23KHz			-50 -50	dBc

Table 11. PLLs, Synthesizers, (T_{amb} = 25°C, VP-VN = 3V) (continued)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
N_{prog1}	RF PLL selectable division ratios	From REF1 to LO1, f_{comp}=3.68MHz	360.75 (363.625 1st used)		376.5 (373.75 last used)	
N_{prog2}	IF PLL selectable division ratios	f_{comp}=113.23KHz	987	1034	1081	
N_{REF1}	REF1 division ratio	Programmable via software mode	1	4	16	
N_{REF2}	REF2 division ratio	Programmable via software mode		130		

Table 12. RF VCO, (T_{amb} = 25°C°C, VP-VN = 3V)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
f_{osc}	VCO frequency oscillation		2676.28		2750.8	MHz
F_{LO1_1}	LO1 frequency range	after divider by 2, by using 14.72MHz crystal	1338.14		1375.4	MHz
F_{LO1_2}	LO1 frequency range	after divider by 2, by using 14.725MHz crystal	1338.134375 to 1375.407031			MHz
V_{FLT1}	Freq control voltage range	FLT1 pin	VN+0.2		VP-0.2	V

Table 13. IF VCO, (T_{amb} = 25°C, VP-VN = 3V)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
f_{osc}	VCO frequency oscillation		894.08	936.64	979.2	MHz
f_{LO2_1}	LO2 frequency range	after divider by 8, by using 14.72MHz crystal	111.76	117.08	122.4	MHz
f_{LO2_2}	LO2 frequency range	after divider by 8, by using 14.725MHz crystal	111.8	117.12	122.44	MHz
V_{FLT2}	Frequency control voltage range	FLT2 pin	VN+0.2		VP-0.2	V

Table 14. Digital interface to MP (SCL,SDA,TLCK), ENRFOSC and XOSEL interface
(T_{amb} = 25°C, VP-VN = 3V)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
Input parameters (SCL, SDA, ENRFOSC, XOSEL)						
V_{IH}	Digital input signals	High	VP-.7		VP	V
V_{IL}		Low	VN		VN+.7	V
T_t	Input edge transition				0.1	µs/V
R_{in}	Input resistance			10		MΩ

Table 14. Digital interface to MP (SCL,SDA,TLCK), ENRFOSC and XOSEL interface (continued)
(T_{amb} = 25°C, VP-VN = 3V)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
Output parameter (TLCK)						
V_{OH}	Digital output signals	High	VP-.7		VP	V
V_{OL}		Low	VN		VN+.7	V
t_r	Rise time	C=5pF		0.4	0.6	µs/V
t_f	Fall time	C=5pF		0.4	0.6	µs/V
Differential digital interface (M_CLK1, M_CLK2)						
V_{OH}	Digital output signals, V(M_CLK1)-V(M_CLK2)	High		0.3		V
V_{OL}		Low		-0.3		V
$VDC_{,M\_CLK}$	M_CLK1,2 Common mode voltage		VP-1.65	VP-1.4	VP-1.2	
t_r	Rise time	Cl=5pF each pin		10	12	ns
t_f	Fall time	C=5pF		10	12	ns
Z_{out}	Output impedance	balanced		500		Ω
F_{M_CLK1}	M_CLK frequency	Using a 14.72MHz quartz		14.72		MHz
F_{M_CLK2}	M_CLK frequency	Using a 14.725MHz quartz		14.725		MHz

Table 15. Additional optional interface (REF)

Symbol	Parameter	Test conditions/notes	Min.	Typ.	Max.	Unit
P_{REF}	External reference input power	It must be AC coupled to REF, XOSel low	-2	0		dBm
VDC	REF DC voltage	XOSel low	VP-1.2	VP-1.35	VP-1.6	V
R_{in}	Input resistance			70		kΩ

4 Functional description

4.1 Receiver chain

The receiver chain transforms the RF frequency signals to an IF signal at 1.84 MHz carrier directly usable by the channel decoder. In front of the STA011 IC there it must be an external LNA and a band-pass filter; the band-pass filter limits the input bandwidth and guarantees a suitable rejection to the image frequency. The STA011 input stage is a LNA working in the 1452-1492 MHz band. The RF signal is down-converted, using an active mixer, to a first IF of 115.244 MHz. The first LO is tunable with a frequency step of 460 KHz. The RF gain can be reduced by 5dB by using an external trimmer/resistor connected between the PADJ1 and PADJ2 pins, and it can also be reduced by 7.5dB (2.5 step) via thesoftware mode.

A 54 dB typical gain range is guaranteed at IF level. By connecting an external trimmer/resistor to pins GADJ1, GADJ2, the IF output signal level can be decreased to the desired value.

Moreover, the IF chain can be configured to have a fixed gain by fixing statically control voltages on AGC1 and AGC2 pins (i.e. V(AGC1)=VCC and V(AGC2)=GND), and trimming the gain by connecting an external resistor between GADJ1 and GADJ2.

By using an 800 Ohm resistor connected between GADJ1 and GADJ2, for example, a typical 56 dBs IF static gain is obtained. The first IF signal, having a bandwidth of 2.5 MHz, shaped by an external SAW filter, is down-converted to a second IF of 1.84 MHz.

A differential clock output of 14.72 MHz is available for use from the base-band.

4.2 Synthesizers, PLL, charge pump and VCOs

The first voltage controlled oscillator is controlled by an integrated PLL, and it's able to cover a frequency range of 37 MHz with a step size of 460 KHz.

The second voltage controlled oscillator produces a fixed 8 x 117.08MHz frequency, scaled by a divider by 8, and controlled by a second integrated PLL. Moreover, the 2nd PLL is able cover the frequency range from 111.76MHz to 122.4MHz, suitable for anapplication test.

The other components of the first PLL synthesizer are a low frequency programmable divider and a dual modulus prescaler; a fixed divider is instead used to synthesize the second VCO fre-quency. Other internal programmable dividers are used to obtain the comparison frequencies of both loops.

Channel selection is made through the I^2CBUS interface, directly from the µP.

4.3 Power supplies

The chip operates from an unregulated power supply of 2.7 to 3.3 Volts. All interface circuits to the base-band chips are operate between these supplies unless otherwise specified.

4.4 Interface specification

All the interface voltage levels to the micro controller are referenced to the supply voltage of the interface power supply (GND). The interface voltage levels are therefore fully compatible with the base-band circuits. The digital levels are all CMOS threshold compatible with the ex-ception of M_CLK1, M_CLK2 pins (ECL type). For a total solution all other interface signals are also included.

5 I²C-bus interface

Data transmission from the microprocessor to the STA011 takes place through the 2 wires (SDA and SCL) of the I²C-bus interface. The STA011 is always a slave device.

5.1 I²C-bus specifications

The I²C-bus protocol defines any device that sends data to the bus as a transmitter, and any device that reads the data as a receiver. The device that controls the data transfer is known as the Master and the others as the slave. The master will always initiate the transfer and will provide the serial clock for synchronization.

5.1.1 Power ON reset

The device at Power ON is able to configure itself to a fixed configuration, with all the circuitry ON and the RFPLL output frequency set to 1356.54MHz (fcomp=3.68MHz, N=368.625)

5.1.2 Data validity

Data changes on the SDA line must only occur when the SCL is LOW. SDA transitions while the clock is HIGH are used to identify START or STOP condition.

5.1.3 Start condition

Start is identified by a HIGH to LOW transition of the data bus SDA while the clock signal SCL is stable in the HIGH state. A Start condition must precede any command for data transfer.

5.1.4 Stop condition

A LOW to HIGH transition of the data bus SDA identifies a stop while the clock signal SCL is stable in the HIGH state. A STOP condition terminates communications between the STA011 and the Bus Master.

5.1.5 Byte format

Every byte transferred on the SDA line must contain bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

5.1.6 Acknowledge

An acknowledge bit is used to indicate a successful data transfer. The bus transmitter, either master or slave, will release the SDA bus after sending 8 bits of data.

During the 9th clock pulse the receiver pulls the SDA low to acknowledge the receipt of 8 bits of data.

5.1.7 Transmission without acknowledge

To avoid detecting an acknowledge from the STA011, the µP can use a simpler transmission: simply it waits one clock period without checking the STA011 acknowledging, and sends the new data. This approach of course is less protected from data corruption.

5.1.8 Device addressing

To start the communication between the master and the STA011, the master must initiate with a start condition. Following this, the master sends onto the SDA line 8 bits (MSB first) corre-sponding to the device select address and read or write mode.

The first 7 MSB`s are the device address identifier, corresponding to the I²C-bus definition. For the STA011 these are fixed as 110000A. The A bit is reset to 0 internally by a pull-down re-sistor but it can be changed through the corresponding external pin Address. In this way if the Address pin is floating the address is fixed to the previous configuration (110000), otherwise if the pin is set high the address is fixed to 1100001.

The 8th bit (LSB) is the read or write operation bit (RW; set to 1 in read mode and to 0 in write mode). After a START condition the STA011 identifies on the Bus the device address and, if matched, it will acknowledge the identification on the SDA bus during the 9th clock pulse.

The following byte after the device identification byte, is the internal sub-address byte that provides access to any of the internal registers.

5.1.9 Write operation (single byte write)

Following a START (S) condition the master sends a device select code with the RW bit set to 0. The I²C gives the acknowledgement and waits for the 1 byte of internal sub address.

This byte provides access to any of the internal registers.

After the reception of the internal byte sub address the I²C again responds with an acknowl-edgement. The master terminates the transfer by generating a STOP (P) condition.

A single byte write with sub-address 00H would affect DATA_OUT[119:112], so a single byte write with sub-address 02H would affect DATA_OUT[103:96] and so on

A single byte address with sub-address out of ranges 00H - 0FH produces illegal_subaddress signal to go high and DATA_OUT[119:0] will not change until a successive write operation request with the correct range for sub-address will be made.

For example if the sub-address is 15H will be produced illegal_subaddress = '1' and DATA_OUT will no change.

S	110000A	R/W 0	ack	Sub-address byte	ack	DATA IN	ack	P

5.1.10 Write operation (multibyte write)

The multi-byte write mode can start from any internal sub address (the same as a single byte write).

Following a START (S) condition the master sends a device select code with the RW bit set to 0. The I²C gives the acknowledgement and waits for 1 byte from the internal sub address.

This byte provides the starting byte of the internal registers.

The master sends the data and each byte isacknowledged by the I²C. The master terminates the transfer by generating a STOP (P) condition.

The sub-address decides the starting byte. A Multi-byte with sub-address 00H and 5 DATA_IN bytes would affect the bytes starting from DATA_OUT [119:112] to DATA_OUT [87:80] and so on. A Multi byte with sub-address from the ranges 00H - 0FH produces illegal sub-address signal to go high, and DATA_OUT[119:0] will not change until a successive write operation request, with the correct range for sub-address will be made.

S	110000A	R/W 0	ack	Sub-address byte	ack	DATA IN	ack	.....	DATA IN	ack	P

5.1.11 Read operation

Current byte address read

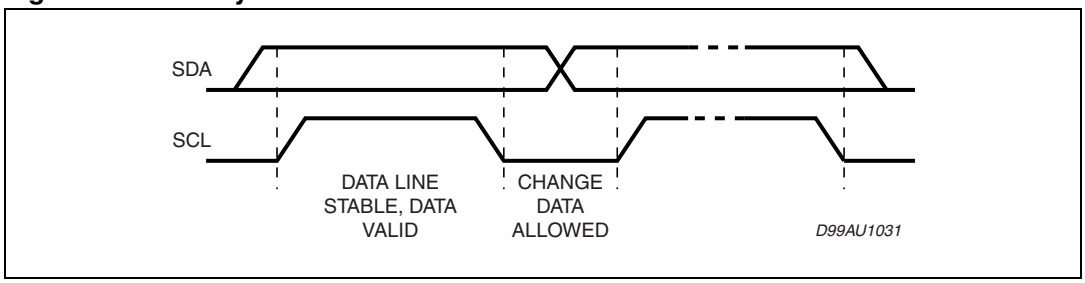
For the I²C of STA011 this is the only read mode operation implemented. In the current byte address read mode, following a START condition, the master sends the device address with the RW bit set to 1. The I²C acknowledges this and outputs the byte data by reading from the internal byte address counter. The master does not acknowledge the received byte, but terminates the transfer with a STOP condition.

S	110000A	R/W 1	ack	DATA	No ack	P

This method operation is not used.

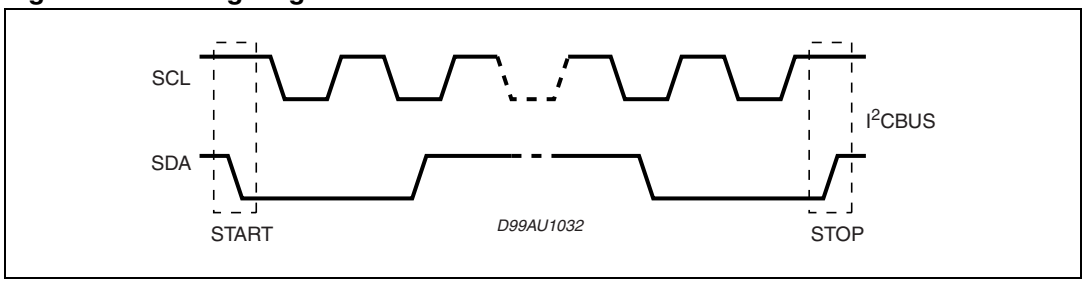
Data validity

Figure 5. Validity on I²C-bus



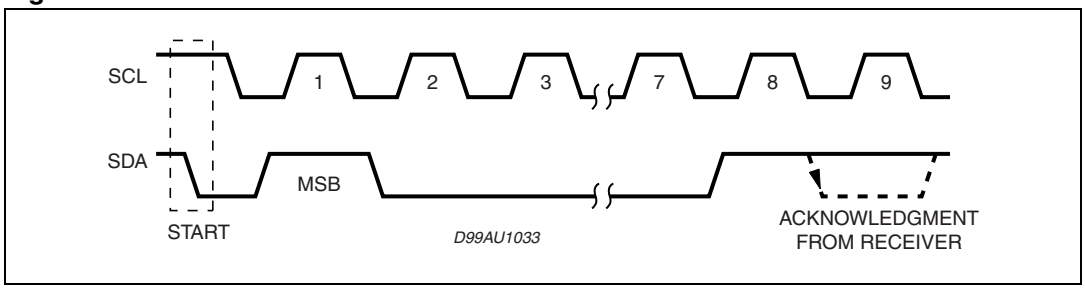
Timing diagram of the I²C-bus:

Figure 6. Timing diagram of the I²C-bus



Acknowledge on the I²C-bus:

Figure 7. Ack on I²Cbus



5.1.12 Timing specification

Figure 8. Data and clock

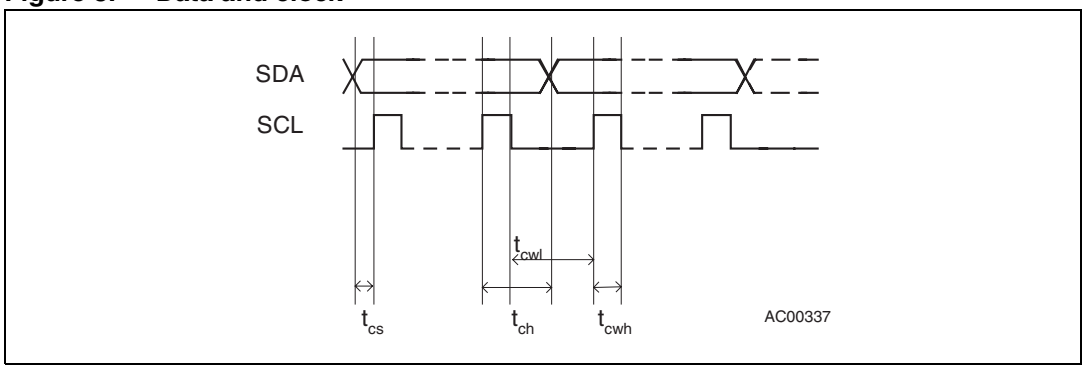


Table 16. Timing electrical characteristics

Symbol	Parameter	Minimum time (ns)
t_{cs}	Data to clock set up time	100
t_{ch}	Data to clock hold time	50
t_{cwh}	Clock pulse width high	100
t_{cwl}	Clock pulse width low	100

5.1.13 Start and stop

Figure 9. Start and stop

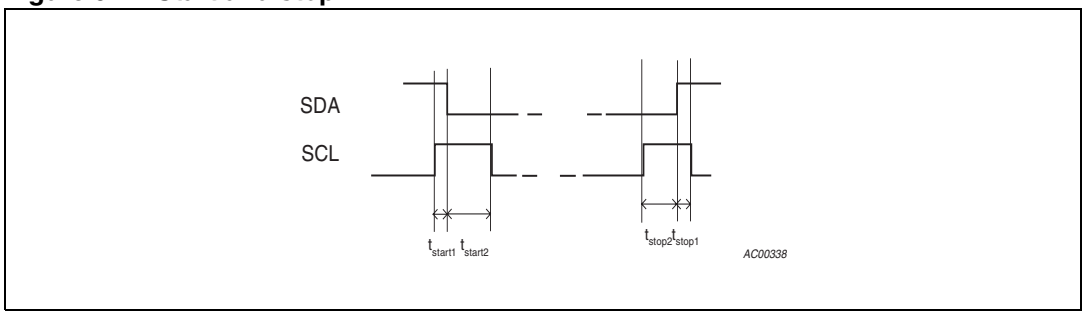


Table 17. Start and stop electrical characteristics

Symbol	Parameter	Minimum time (ns)
$T_{start1,2}$	Clock to data start time	100
$T_{stop1,2}$	Data to clock down stop time	100

5.1.14 ACK

Figure 10. ACK

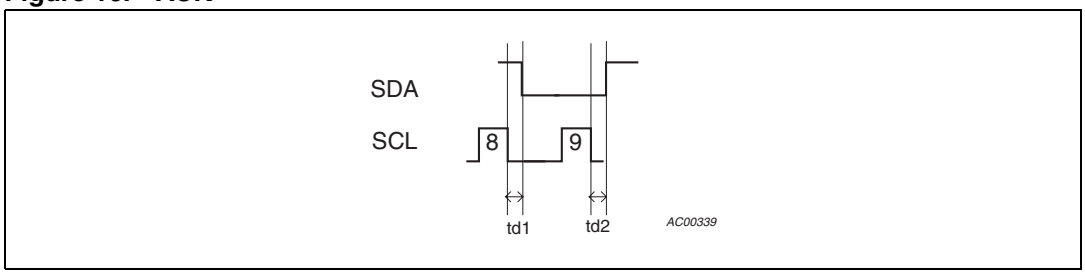


Table 18. ACK electrical characteristics

Symbol	Parameter	Maximum time (ns)
t_{d1}	Ack begin delay	200
t_{d2}	Ack end delay	200

5.2 Software specification

5.2.1 Write mode (multibyte write)

MSB	device address						LSB		MSB	sub-address byte							LSB	
S	1	1	0	0	0	0	A	0	ack	S7	S6	S5	S4	S3	S2	S1	S0	ack

MSB	1st data byte							LSB		MSB	2nd data byte							LSB	
D119	D118	D117	D116	D115	D114	D113	D112	ack		D111	D110	D109	D108	D107	D106	D105	D104	ack	

MSB	3rd data byte							LSB		MSB	4th data byte							LSB	
D103	D102	D101	D100	D99	D98	D97	D96	ack		D95	D94	D93	D92	D91	D90	D89	D88	ack	

MSB	5th data byte							LSB		MSB	6th data byte							LSB	
D87	D86	D85	D84	D83	D82	D81	D80	ack		D79	D78	D77	D76	D75	D74	D73	D72	ack	

MSB	7th data byte							LSB		MSB	8th data byte							LSB	
D71	D70	D69	D68	D67	D66	D65	D64	ack		D63	D62	D61	D60	D59	D58	D57	D56	ack	

MSB	9th data byte							LSB		MSB	10th data byte							LSB	
D55	D54	D53	D52	D51	D50	D49	D48	ack		D47	D46	D45	D44	D43	D42	D41	D40	ack	

MSB	11th data byte							LSB		MSB	12th data byte							LSB	
D39	D38	D37	D36	D35	D34	D33	D32	ack		D31	D30	D29	D28	D27	D26	D25	D24	ack	

MSB	13th data byte							LSB		MSB	14th data byte							LSB	
D23	D22	D21	D20	D19	D18	D17	D16	ack		D15	D14	D13	D12	D11	D10	D9	D8	ack	

MSB	13th data byte						LSB		
D7	D6	D5	D4	D3	D2	D1	D0	ack	P

ack = Acknowledge

S = Start

P = Stop

Bits description

1st data byte

RFPLL							
Loop divider							
M counter							
D119	D118	D117	D116	D115	D114	D113	D112

2nd data byte

RF PLL							
Loop divider							
Loop divider A counter			K (fractional)				
D111	D110	D109	D108	D107	D106	D105	D104

3rd data byte

RF PLL							
Reference divider					Div 2 Enable	Loop div Enable	CP Enable
Division ratio							
D103	D102	D101	D100	D99	D98	D97	D96

4th data byte

RFPLL							
VCO Enable	ext LO Enable	VCO output voltage setting		Prescaler Enable	Charge Pump current setting		
D95	D94	D93	D92	D91	D90	D89	D88

5th data byte

RF PLL							
Phase frequency detector							
PFD setting					Down ASYM enable	Down Split enable	DAC Enable
D87	D86	D85	D84	D83	D82	D81	D80

Table 19. 6th data byte

RFPLL							
DAC current adjustment					Down Asym delay setting		Not used
D79	D78	D77	D76	D75	D74	D73	D72

7th data byte

RF path						IFpath	
LNA enable	RF Mixer enable	RF Gain Setting		IF Buffer enable	IF Buffer Current setting	Pre VGA enable	VGA1 enable
D71	D70	D69	D68	D67	D66	D65	D64

8th data byte

IF path			IFPLL				
VGA2 enable	IF Mixer enable	IF2 amp enable	Lock detector setting			VCO Enable	ext LO Enable
D63	D62	D61	D60	D59	D58	D57	D56

9th data byte

IF PLL							
PFD setting					CP enable	Ref div Division ratio	
D55	D54	D53	D52	D51	D50	D49	D48

10th data byte

IF PLL							
Reference divider division ratio							Loop div ratio
D47	D46	D45	D44	D43	D42	D41	D40

11th data byte

IF PLL							
Loop divider Division ratio							
D39	D38	D37	D36	D35	D34	D33	D32

12th data byte

IF PLL		XTAL					
Loop divider division ratio		M_CLK output disable	Double/ single ended	Cut-off frequency setting		Loop gain setting	Not used
D31	D30	D29	D28	D27	D26	D25	D24

Not used	Not used	Not used	Not used	Not used	…	…	.
D31	D30	…	…	…	…	….	….

5.3 Read mode

Current byte address read

MSB			chip address					R/W		MSB			data byte				LSB	
S	1	1	0	0	0	0	A	1	ack	B7	B6	B5	B4	B3	B2	B1	B0	P

ack = acknowledge

s = start

p = stop

5.3.1 Bits description

In read mode, only one byte is provided to the master.

PLL's Lock	Not used	Not used	Not used	Not used	Not used	Not used	Not used
B7	B6	B5	B4	B3	B2	B1	B0

The last six not used bits are fixed to 0.

6 Programming specifications

6.1 RFPLL

6.1.1 Loop divider division ratio

M counter								Notes
D119	D118	D117	D116	D115	D114	D113	D112	
…	…	…	…	…	…	…	…	
0	**0**	**1**	**0**	**1**	**1**	**1**	**0**	**M=46, startup configuration**
…	…	…	…	…	…	…	…	
0	0	1	1	1	0	0	0	
…	…	…	…	…	…	…	…	

A counter			K (fractional)					Description
D111	D110	D109	D108	D107	D106	D105	D104	N=M*P+A+K/32 (P=8)
1	0	1	1	1	0	0	1	
…	…	…	…	…	…	…	…	
0	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**N=368.625, LO1=368.625x3.68= 1356.54 MHz, startup configuration**
…	…	…	…	…	…	…	…	
1	1	0	0	0	1	1	1	
…	…	…	…	…	…	…	…	
1	0	1	1	1	0	0	1	

6.1.2 Reference divider division ratio

Table 20. Reference divider division ratio

D103	D102	D101	D100	D99	Description	Notes
0	0	0	0	1	R=1	XTAL or TCXO=14.72MHz f_{comp}=14. 72MHz,
0	0	0	1	0	R=2	…
…	…	…	…	…	…	
0	0	1	0	0	R=4	XTAL=14.72MHz f_{comp}=3.68MHzKHz, startup configuration
…	…	…	…	…		
0	1	0	0	0	R=8	f_{comp}=1.84MHz
…	…	…	…	…		
1	0	0	0	0	R=16	f_{comp}=.92MHz

6.1.3 Blocks enable

Table 21. Blocks enable

	Description	Notes
D98		
0	Divider by 2 OFF	
1	Divider by 2 ON	**Startup configuration**
D97		
0	Loop Divider OFF	
1	Loop Divider ON	**Startup configuration**
D96		
0	Charge Pump OFF	
1	Charge Pump ON	**Startup configuration**
D91		
0	Prescaler OFF	
1	Prescaler ON	**Startup configuration**

6.1.4 VCO enable

Table 22. VCO enable

D95	D94	Description	Notes
1	**0**	Internal RFVCO	**Startup configuration**
1	1	External RFLO	

The internal RFVCO can also be enabled via hardware mode through the ENRFOSC pin.

With the ENRFOSC pin high the software mode is disabled and the RFVCO is turned ON; with the ENRFOSC pin low the software mode is enabled, depending on the truth table described above .

6.1.5 VCO output voltage

Table 23. VCO output voltage

D93	D92	Description	Notes
0	**0**	Vout=1Vpp	**Startup configuration**
0	1	Vout=2Vpp	
1	0	Vout=3Vpp	
1	1	Vout=4Vpp	

6.1.6 Charge pump current setting

Table 24. Charge pump current

D90	D89	D88	Description	Notes
0	0	0	I_{CP}=300uA	
…	…	…	…….	
0	**1**	**1**	I_{CP}=400uA	**Startup configuration**
.			…….	
1	1	1	I_{CP}=600uA	

6.1.7 PFD programming

Table 25. Frequency phase detector setting

D87	D86	D85	D84	D83	Description	Notes
x	x	1	x	1	Normal operation	Default configuration
x	x	1	0	0	Reference divider test, available @Lock	Synthesizer test reserved configuration
x	x	1	1	0	Loop divider test available @ Lock	Synthesizer test reserved configuration
0	0	0	x	x	Charge pump test, high impedance state	Synthesizer test reserved configuration
0	1	0	x	x	Charge pump test, DEC active	Synthesizer test reserved configuration
1	0	0	x	x	Charge pump test, INC active	Synthesizer test reserved configuration
1	1	0	x	x	Charge pump test, DEC&INC active	Synthesizer test reserved configuration
D82					Down ASYM	
0					UP and DOWN sym	**Startup configuration**
1					UP and DOWN asym	
D81						
0					Down Split disabled	
1					Down Split enabled	**Startup configuration**

6.1.8 Fractional spurious compensation

Table 26. Fractional spurious compensation

D80	Description	Notes
0	DAC OFF	
1	DAC ON	**Startup configuration**

Table 27. DAC current adjustment

D79	D78	D77	D76	D75	Description	Notes
0	0	1	1	1	N=7	startup configuration

Table 28. Down Asym delay setting

D74	D73	Description	Notes
0	**0**	Minimum delay	**Startup configuration**
..	..		
1	1	Maximum delay	

6.2 RF path

6.2.1 Blocks enable

Table 29. Blocks enable

	Description	Notes
D71		
0	LNA OFF	
1	LNA ON	**Startup configuration**
D70		
0	Mixer OFF	
1	Mixer ON	**Startup configuration**
D67		
0	Buffer OFF	
1	Buffer ON	**Startup configuration**

6.2.2 RF gain setting

Table 30. RF gain setting

D69	D68	Description	Notes
1	1	High Gain	
1	**0**	**Medium1**	**Startup configuration**
0	1	Medium2	
0	0	Low Gain	

6.2.3 IF buffer setting

Table 31. IF Buffer setting

D66	Description	Notes
0	Itail=3mA	lower output linearity
1	**Itail=4mA**	**Higher output linearity, startup configuartion**

6.3 IF path

6.3.1 Blocks disable

Table 32. Blocks disable

D65	Description	Notes
D65		
0	preVGA OFF	
1	preVGA ON	**Startup configuration**
D64		
0	VGA1 OFF	
1	VGA1 ON	**Startup configuration**
D63		
0	VGA2 OFF	
1	VGA2 ON	**Startup configuration**
D62		
0	Mixer OFF	
1	Mixer ON	**Startup configuration**
D61		
0	IF2Amp OFF	
1	IF2Amp ON	**Startup configuration**

6.4 Lock detector setting

Table 33. Lock detector setting

D60	D59	D58	Description	Notes
0	0	0	Lock test on RF PLL	Test condition
0	0	1	Lock test on IF PLL	Test condition
1	**0**	**0**	**Lock test on RF PLL and IF PLL**	**Startup configuration**
x	1	0	Test on RF PLL dividers	Test condition
x	1	1	Test on IF PLL dividers	Test condition

6.5 IF PLL

6.5.1 IFVCO enable

Table 34. IFVCO enable

D57	D56	Description	Notes
1	**0**	**Internal IFVCO**	**Startup configuration**
1	1	External IFLO	Test condition

6.5.2 PFD programming

Table 35. Frequency phase detector setting

D55	D54	D53	D52	D51	Description	Notes
x	**x**	**1**	**x**	**1**	**Normal operation**	**Default configuration**
x	x	1	0	0	Reference divider test, available @Lock	Synthesizer test reserved configuration
x	x	1	1	0	Loop divider test available @ Lock	Synthesizer test reserved configuration
0	0	0	x	x	Charge pump test, high impedance state	Synthesizer test reserved configuration
0	1	0	x	x	Charge pump test, DEC active	Synthesizer test reserved configuration
1	0	0	x	x	Charge pump test, INC active	Synthesizer test reserved configuration
1	1	0	x	x	Charge pump test, DEC&INC active	Synthesizer test reserved configuration

6.5.3 Charge pump enable

Table 36. Charge pump enable

D50	Description	Notes
0	Charge Pump OFF	
1	**Charge Pump ON**	**Startup configuration**

6.5.4 Reference divider division ratio

Table 37. Reference divider division ratio

D49	D48	D47	D46	D45	D44	D43	D42	D41	Description	Notes
0	1	0	0	0	0	0	1	0	R=130	f_{comp}=113.23KHz startup configuration

6.5.5 Loop divider division ratio

Table 38. Loop divider division ratio

D40	D39	D38	D37	D36	D35	D34	D33	D32	D31	D30	Description	Notes
…	…	…	…	…	…	…	…	…	…	…		
0	1	1	1	1	0	1	1	0	1	1	N=987	
…	…	…	…	…	…	…	…	…	…	…		
1	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**N=1034**	**Startup configuration**
…	…	…	…	…	…	…	…	…	…	…		
1	0	0	0	0	1	1	1	0	0	1	N=1081	
…	…	…	…	…	…	…	…	…	…	…		

6.6 XTAL

Table 39. XTAL

		Description	Notes
D29			
0		M_CLK output buffer ON	**Startup configuration**
1		M_CLK output buffer OFF	
D28			
0		M_CLK double ended output	**Startup configuration**
1		M_CLK single ended output	
Cut-off frequency setting			
D27	**D26**		
0	0	Maximum cut-off frequency	
0	1	Intermediate 1	
1	**0**	**Intermediate 2**	**Startup configuration**
1	1	Minimum cut-off frequency	
D25			
0		open loop gain set low	
1		open loop gain set high	**Startup configuration**

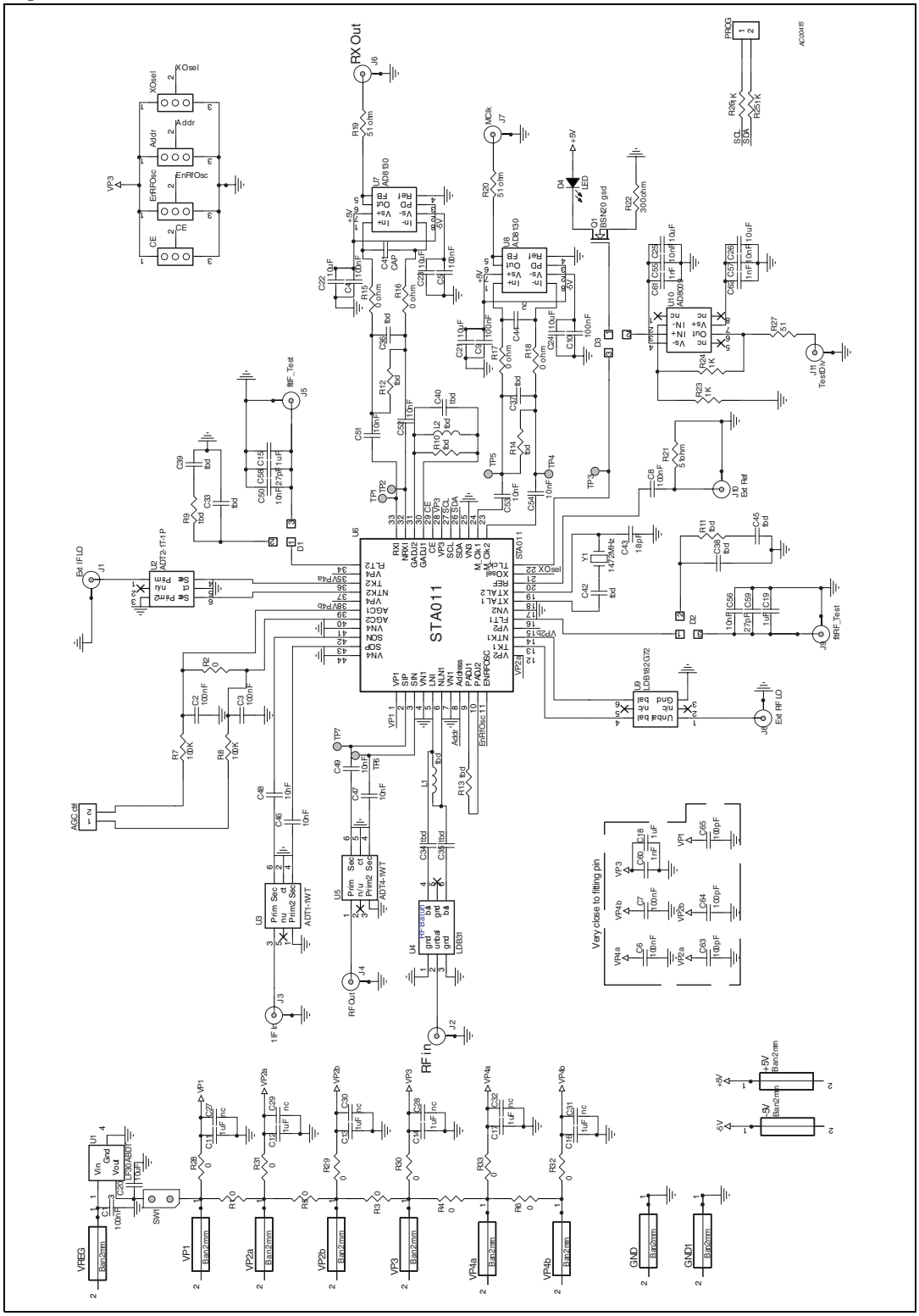
6.7 Startup configuration

Table 40. Startup configuration

Data Byte	Binary	Dec Value
1	00101110	46
2	00010100	20
3	00100111	39
4	10001011	139
5	00101011	43
6	00111000	80
7	11101111	239
8	11110010	242
9	00101101	45
10	00000101	5
11	00000010	2
12	10001010	140

7 Evaluation board

Figure 11. Evaluation board schematic



8 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

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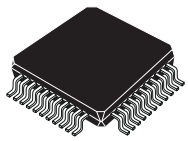
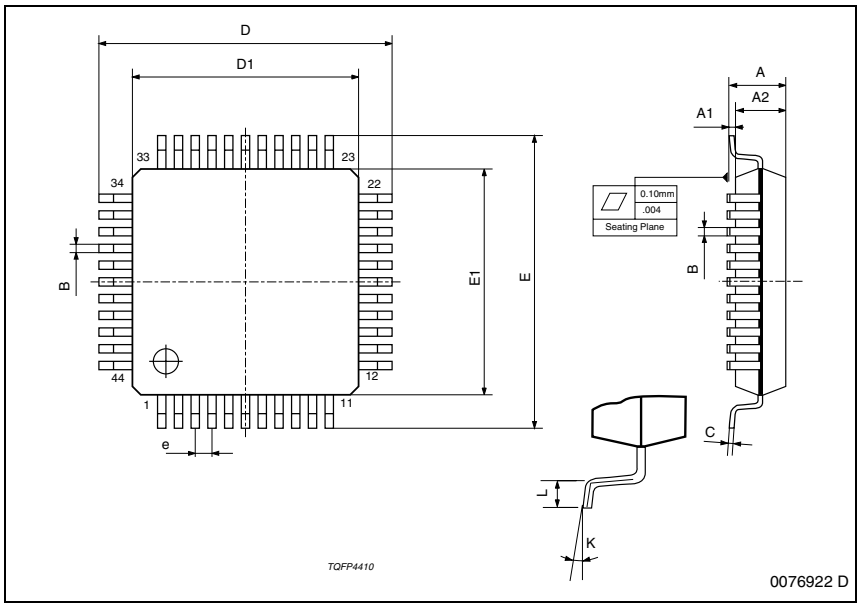
Figure 12. TQFP44 mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		8.00			0.315	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
k	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10 x 1.4mm)



9 Revision history

Table 41. Document revision history

Date	Revision	Changes
21-Nov-2007	1	Initial release.

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