



# STP8NM50 STP8NM50FP

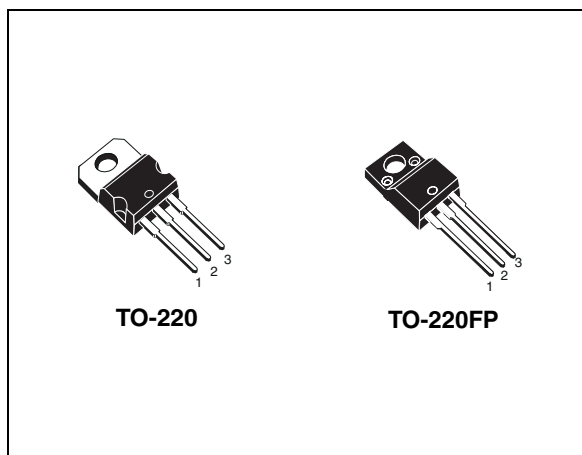
N-channel 550V @ Tjmax - 0.7Ω - 8A - TO-220 - TO-220FP  
MDmesh™ Power MOSFET

## General features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub>	I <sub>D</sub>
STP8NM50	550V	<0.8Ω	8A
STP8NM50FP	550V	<0.8Ω	8A <sup>(1)</sup>

1. Limited only by maximum temperature allowed

- 100% avalanche tested
- High dv/dt and avalanche capabilities
- Low gate input resistance
- Low input capacitance and gate charge



## Description

The MDmesh™ is a new revolutionary Power MOSFET technology that associates the multiple drain process with the company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

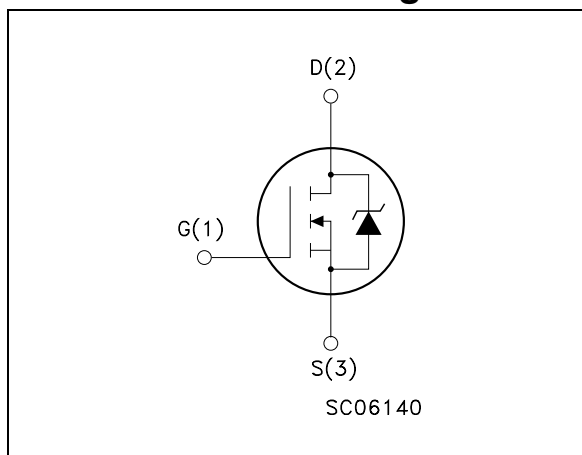
## Applications

- Switching application

## Order codes

Part number	Marking	Package	Packaging
STP8NM50	P8NM50	TO-220	Tube
STP8NM50FP	P8NM50FP	TO-220FP	Tube

## Internal schematic diagram



## Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220	TO-220FP	
$V_{GS}$	Gate-source voltage	± 30		V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	8	8 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	5	5 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	32	32 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	100	25	W
	Derating factor	0.8		W/°C
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15		V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{s}; T_C=25^\circ\text{C}$ )	--	2500	V
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-65 to 150		°C

1. Limited only by maximum temperature allowed
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 8\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 2. Thermal data**

Symbol	Parameter	TO-220	TO-220FP	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.25	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb max	62.5		°C/W
$T_l$	Maximum lead temperature for soldering purpose	300		°C

**Table 3. Avalanche characteristics**

Symbol	Parameter	Max value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	2.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$ , $I_D=I_{AR}$ , $V_{DD}=50\text{V}$ )	200	mJ

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\mu A, V_{GS} = 0$	500			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 30 V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 2.5 A$		0.7	0.8	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 2.5 A$		2.4		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		415 88 12		pF pF pF
$C_{oss eq.}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0V \text{ to } 400V$		50		pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400V, I_D = 5A$ $V_{GS} = 10V$ <i>(see Figure 16)</i>		13 4 6		nC nC nC
$R_G$	Gate input resistance	$f = 1MHz$ Gate DC Bias = 0 Test signal level = 20mV Open drain		3		$\Omega$

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%
2.  $C_{oss eq.}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=250\text{ V}$ , $I_D=2.5\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ (see Figure 15)		16		ns
$t_r$	Rise time			8		ns
$t_{r(Voff)}$	Off-voltage rise time	$V_{DD}=400\text{ V}$ , $I_D=5\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=10\text{ V}$ (see Figure 15)		14		ns
$t_f$	Fall time			6		ns
$t_c$	Cross-over time			13		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$I_{SD}$	Source-drain current				8	A
$I_{SDM}$	Source-drain current (pulsed)				32	A
$V_{SD}$	Forward on voltage	$I_{SD}=10\text{ A}$ , $V_{GS}=0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=100\text{ V}$ , $T_j=25^\circ\text{C}$ (see Figure 20)		185		ns
$Q_{rr}$	Reverse recovery charge			1.1		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			11.5		A
$t_{rr}$	Reverse recovery time	$I_{SD}=5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD}=100\text{ V}$ , $T_j=150^\circ\text{C}$ (see Figure 20)		270		ns
$Q_{rr}$	Reverse recovery charge			1.6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			12		A

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

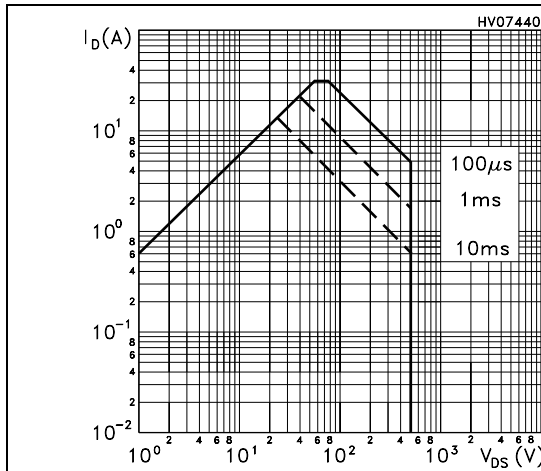


Figure 2. Thermal impedance for TO-220

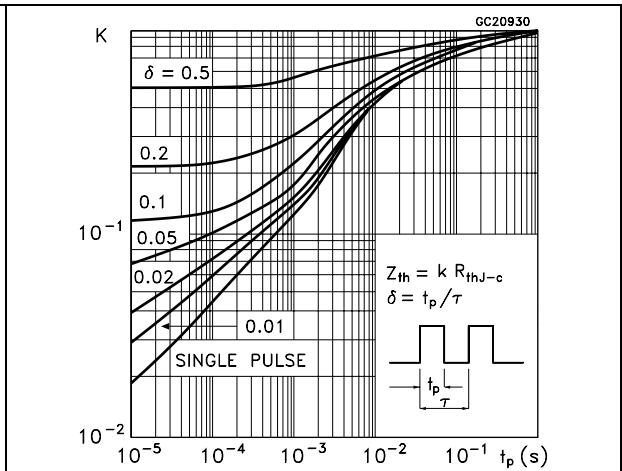


Figure 3. Safe operating area for TO-220FP

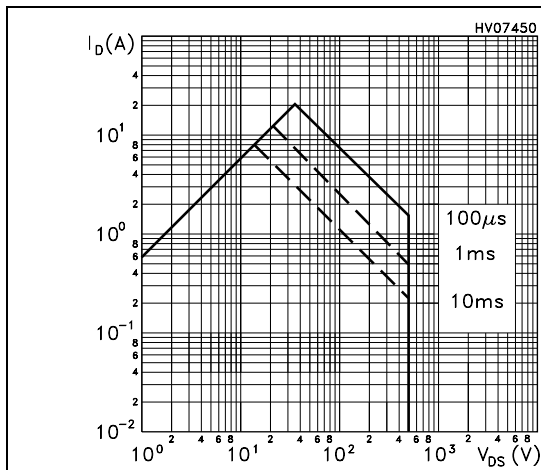


Figure 4. Safe operating area for TO-220FP

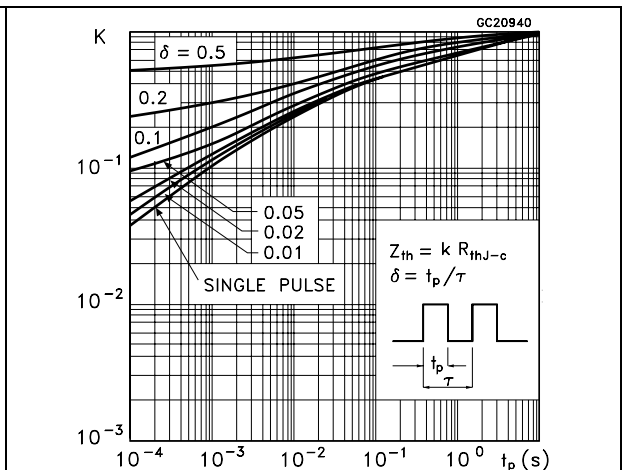


Figure 5. Output characteristics

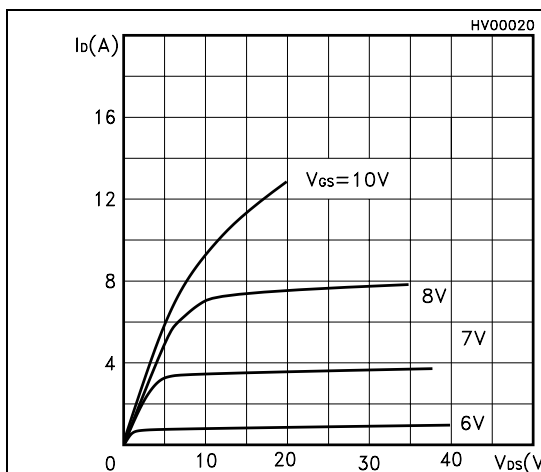


Figure 6. Transfer characteristics

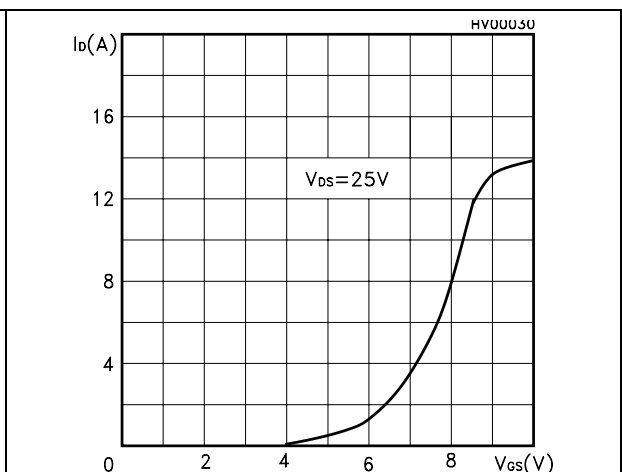


Figure 7. Transconductance

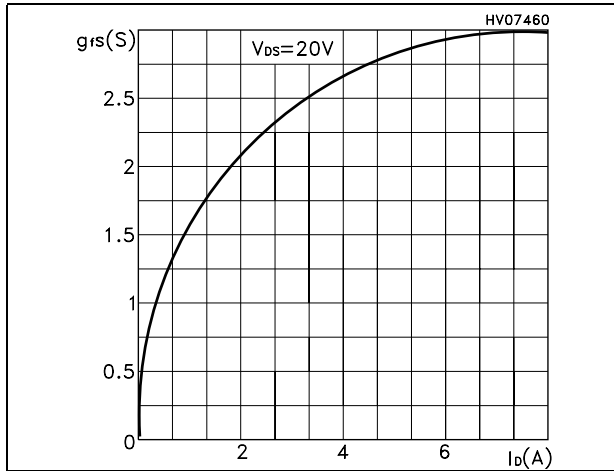


Figure 8. Static drain-source on resistance

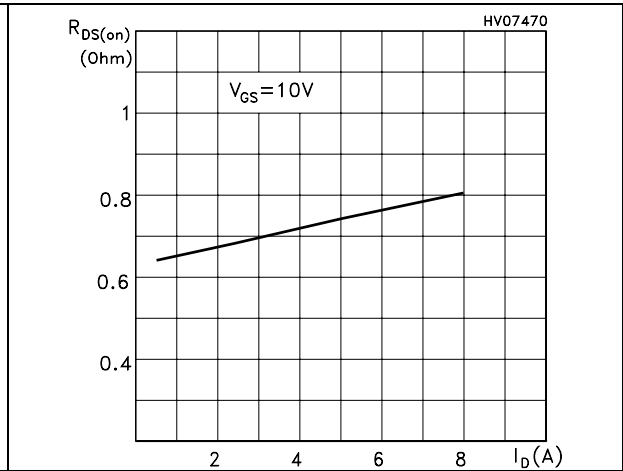


Figure 9. Gate charge vs gate-source voltage Figure 10. Capacitance variations

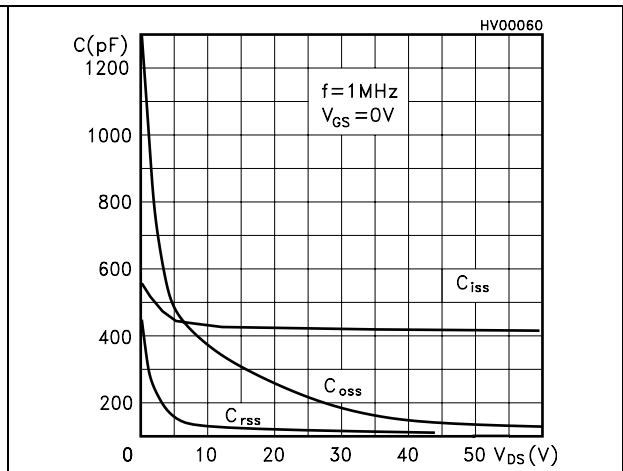
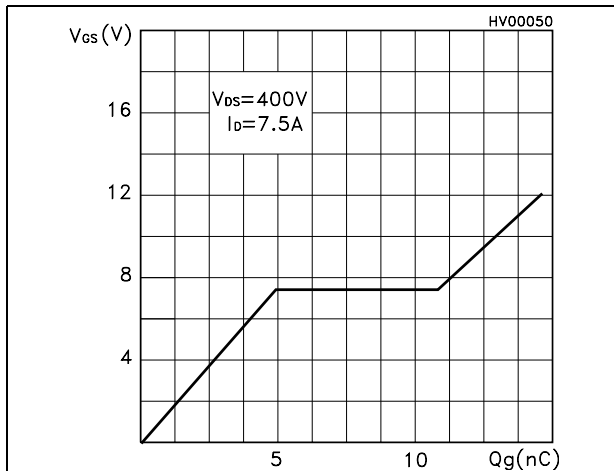


Figure 11. Normalized gate threshold voltage vs temperature

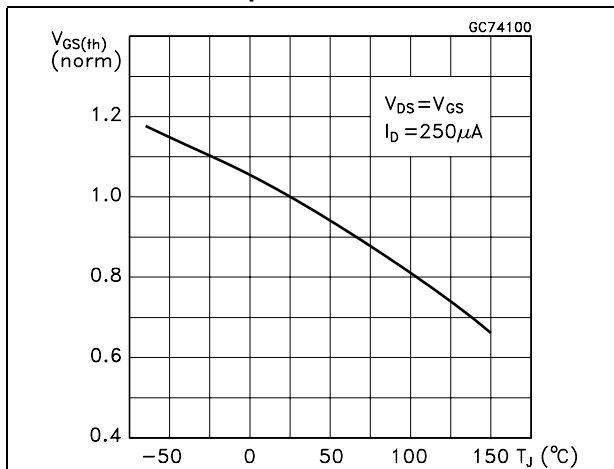


Figure 12. Normalized on resistance vs temperature

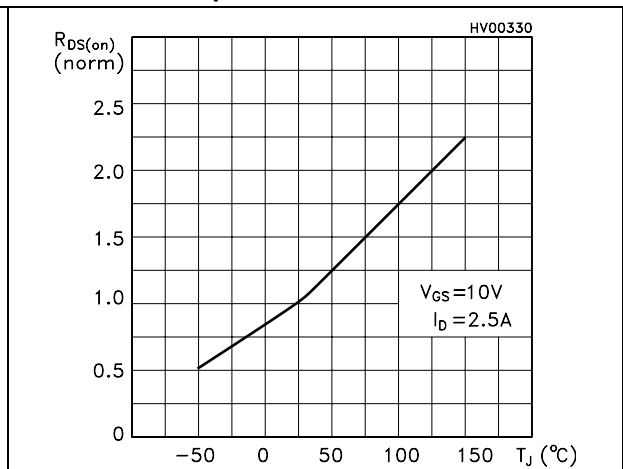


Figure 13. Source-drain diode forward characteristics

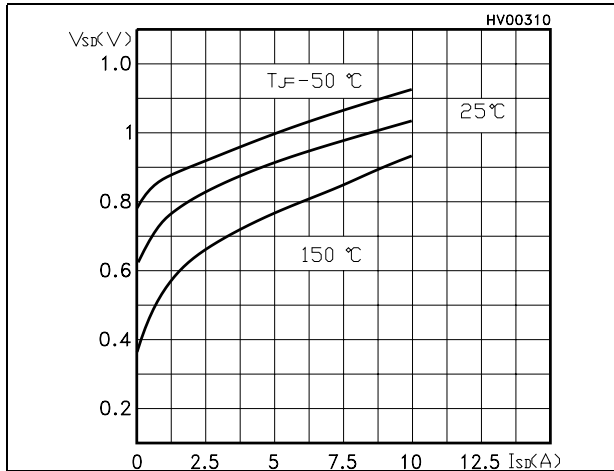
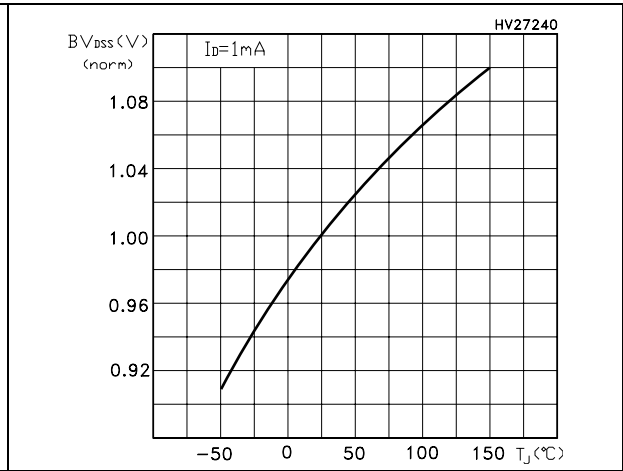


Figure 14. Normalized  $B_{VDSS}$  vs temperature





### 3 Test circuit

Figure 15. Switching times test circuit for resistive load

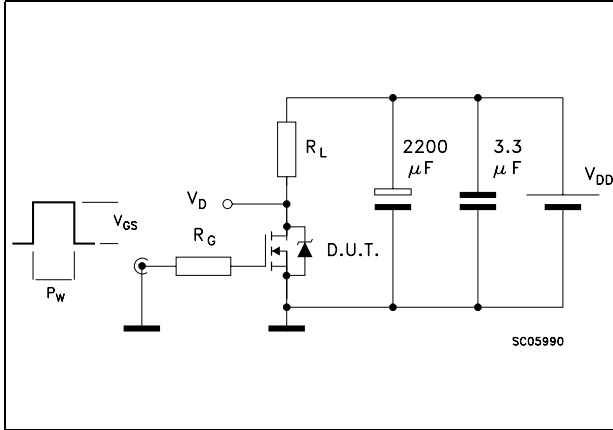


Figure 16. Gate charge test circuit

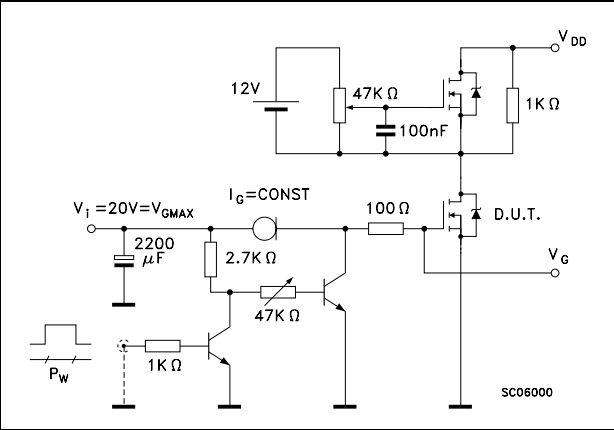


Figure 17. Test circuit for inductive load switching and diode recovery times

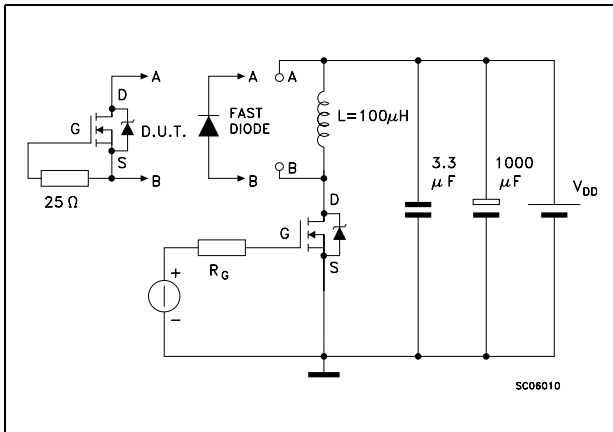


Figure 18. Unclamped Inductive load test circuit

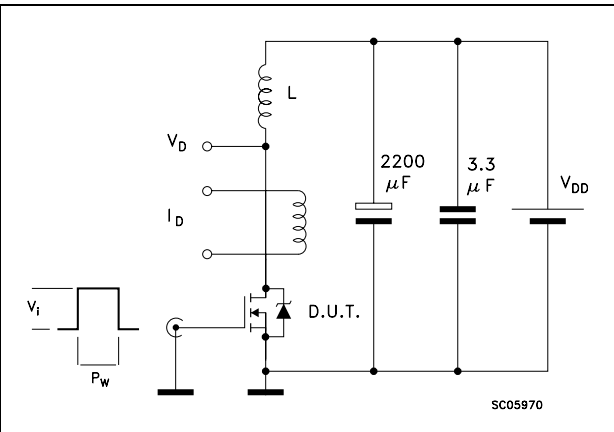


Figure 19. Unclamped inductive waveform

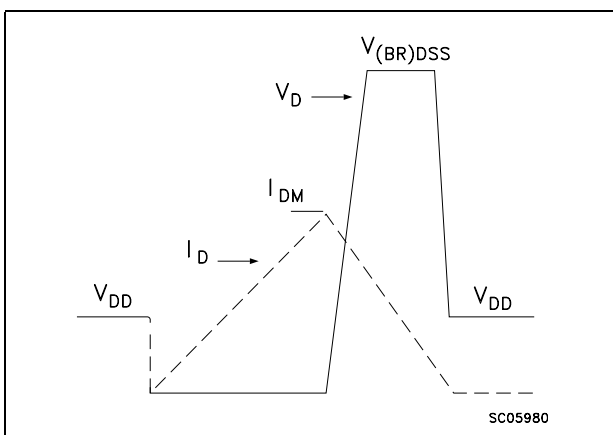
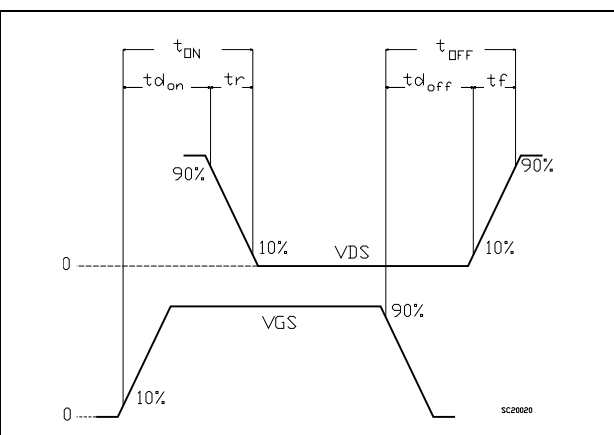


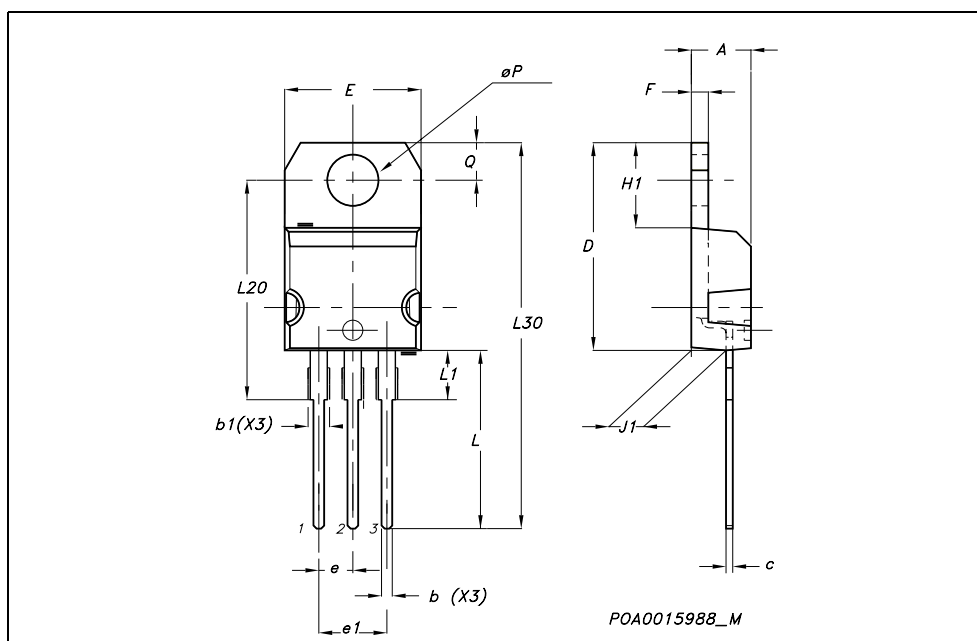
Figure 20. Switching time waveform



## 4 Package mechanical data

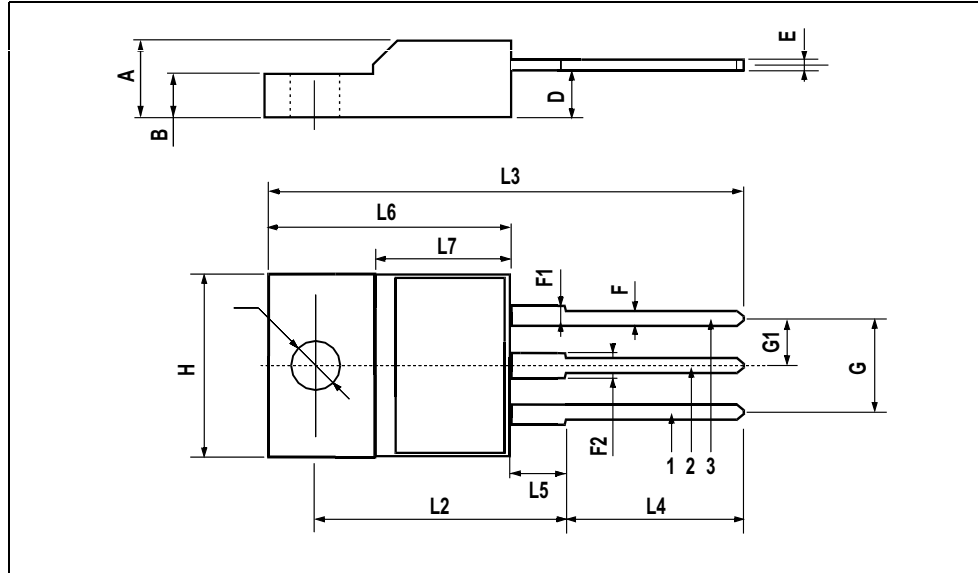
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



## 5 Revision history

**Table 8. Revision history**

Date	Revision	Changes
09-Sep-2004	4	Title changed
11-Aug-2006	5	New template
22-Sep-2006	6	Some value change in <a href="#">Table 4: On/off states</a>
18-Oct-2006	7	Updated <a href="#">Note 3 on page 3</a>

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