



## STS5DNF20V

N-channel 20 V, 0.030  $\Omega$ , 5 A SO-8  
2.7 V, drive STripFET™ II Power MOSFET

### Features

Order code	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STS5DNF20V	20 V	< 0.040 $\Omega$ @ 4.5 V < 0.045 $\Omega$ @ 2.7 V	5 A

- Ultra low threshold gate drive (2.7 V)
- Standard outline for easy automated surface mount assembly

### Applications

Switching application

### Description

The STS5DNF20V is a N-channel STripFET™ II. This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

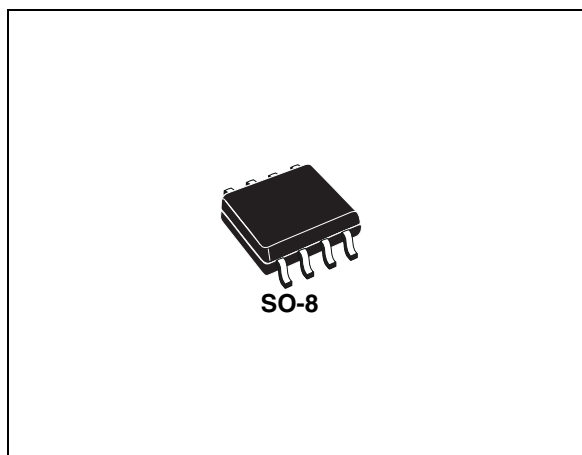


Figure 1. Internal schematic diagram

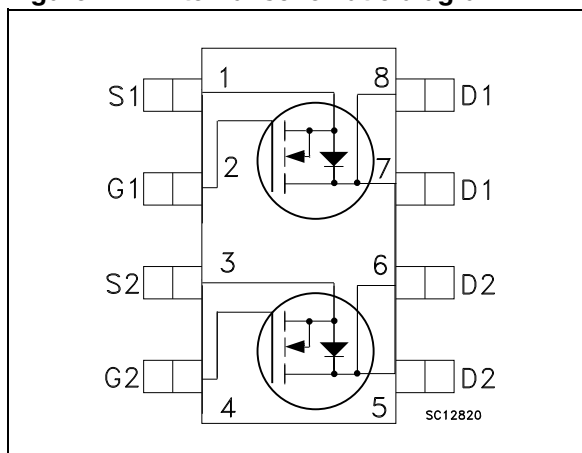


Table 1. Device summary

Order code	Marking	Package	Packaging
STS5DNF20V	5DNF20V	SO-8	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	20	V
$V_{GS}$	Gate-source voltage	$\pm 12$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (dual operation)	1.6	W
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ (single operation)	2	W

1. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-a}$	Thermal resistance junction-ambient single operation	62.5	$^\circ\text{C/W}$
	Thermal resistance junction-ambient dual operation	78	$^\circ\text{C/W}$
$T_J$	Max. operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	20			V
$I_{DSS}$	Zero gate voltage Drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 12\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	0.6			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5\text{ V}$ , $I_D = 2.5\text{ A}$ $V_{GS} = 2.7\text{ V}$ , $I_D = 2.5\text{ A}$		0.030 0.037	0.040 0.045	$\Omega$ $\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance			460		pF
$C_{oss}$	Output capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	200		pF
$C_{rss}$	Reverse transfer capacitance			50		pF
$Q_g$	Total gate charge	$V_{DD} = 16\text{ V}$ , $I_D = 5\text{ A}$ ,		8.5	11.5	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 4.5\text{ V}$	-	1.8		nC
$Q_{gd}$	Gate-drain charge	(see <a href="#">Figure 13</a> )		2.4		nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=10\text{ V}$ , $I_D=2.5\text{ A}$ , $R_G=4.7\Omega$ , $V_{GS}=4.5\text{ V}$ (see <a href="#">Figure 12</a> )	-	7	-	ns
				33		ns
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time			27		ns
				10		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5\text{ A}$ , $V_{GS} = 0$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $V_{DD} = 10\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 14</a> )	-	26		ns
$Q_{rr}$	Reverse recovery charge			13		nC
$I_{RRM}$	Reverse recovery current			1		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

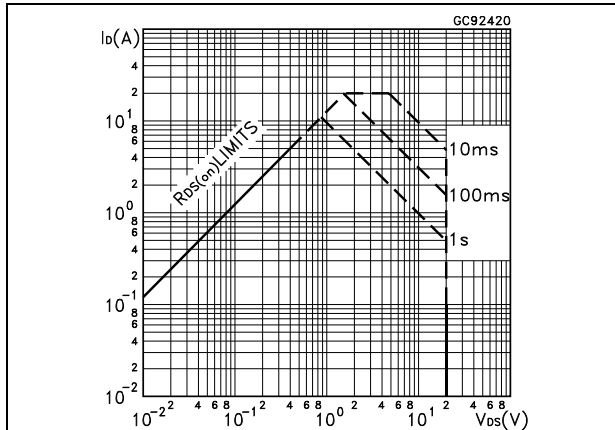


Figure 3. Thermal impedance

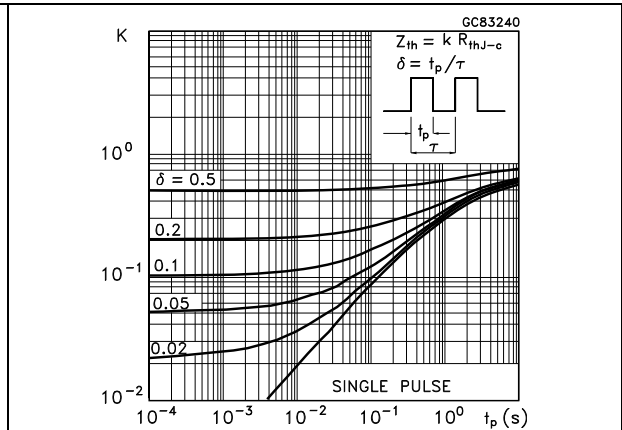


Figure 4. Output characteristics

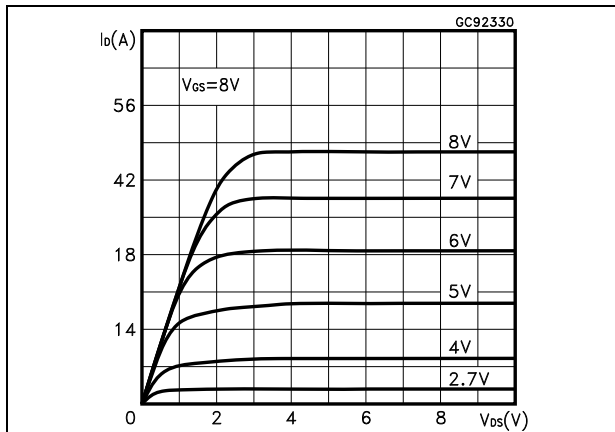


Figure 5. Transfer characteristics

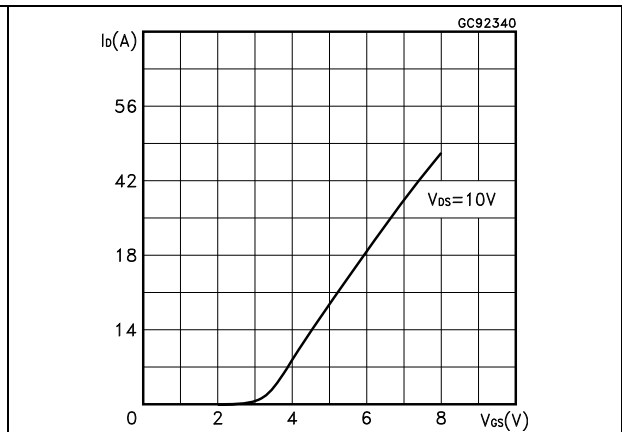


Figure 6. Source-drain diode forward characteristics

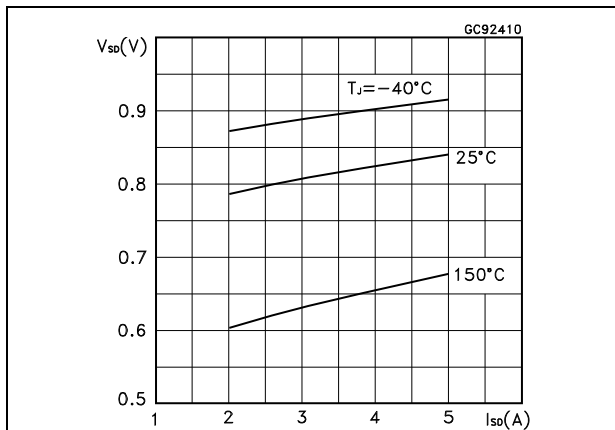


Figure 7. Static drain-source on resistance

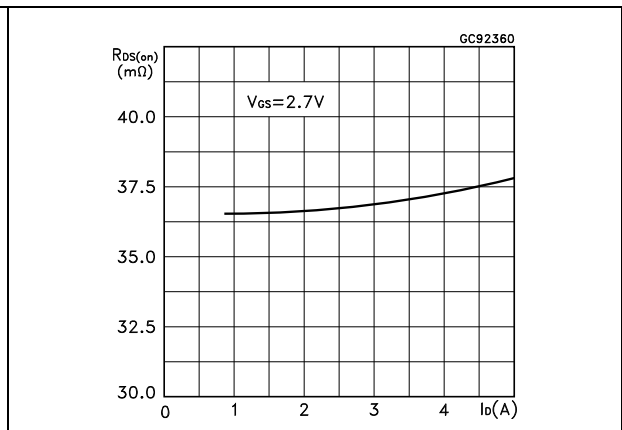


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

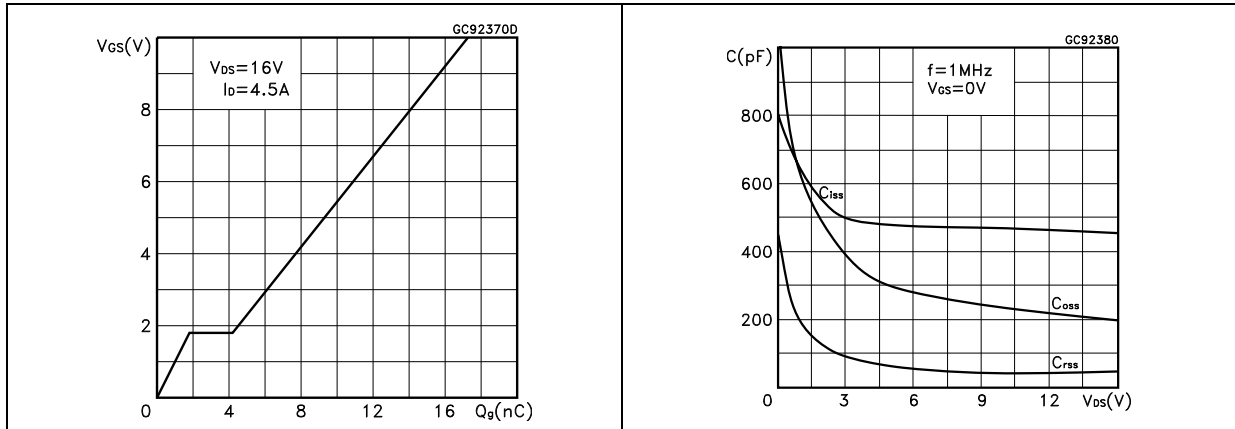


Figure 10. Normalized gate threshold voltage vs temperature

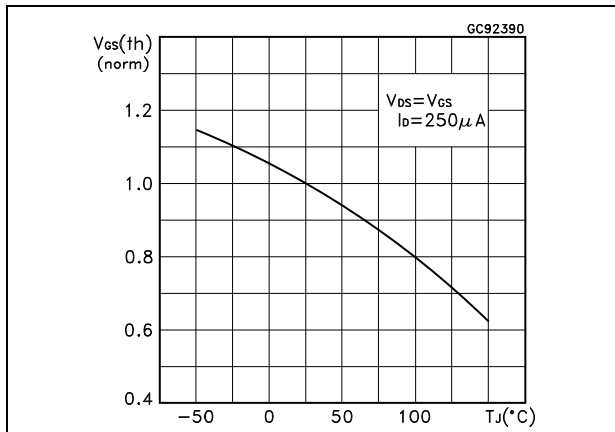
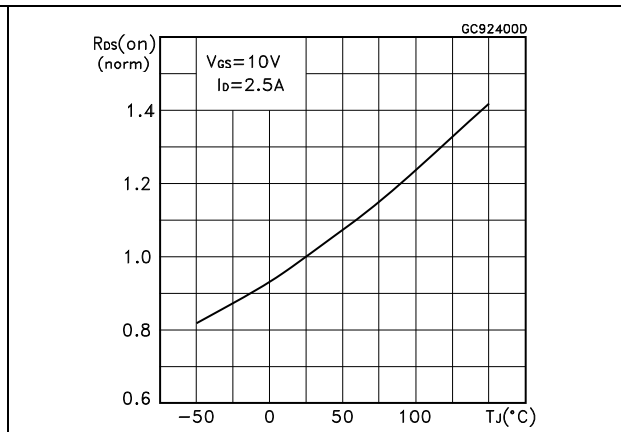
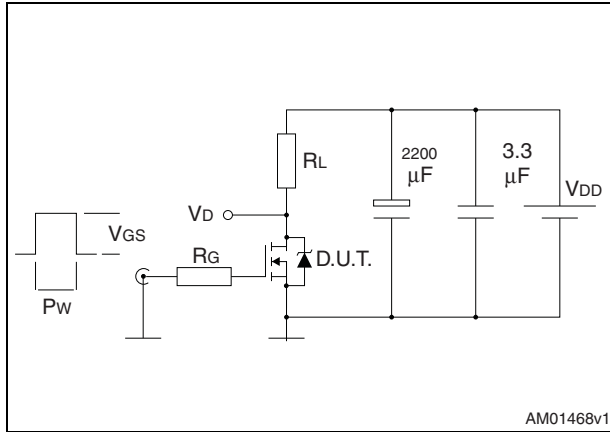


Figure 11. Normalized on resistance vs temperature

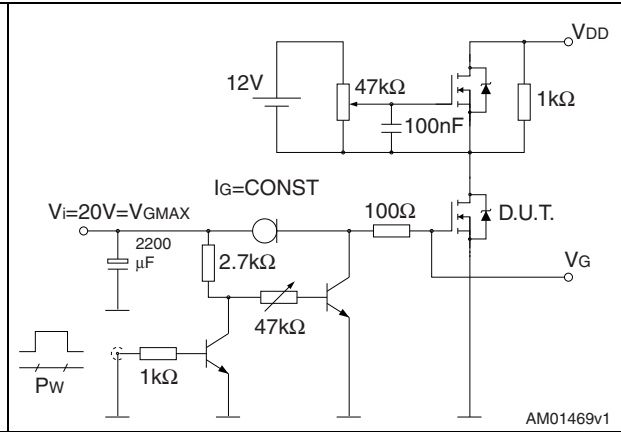


### 3 Test circuit

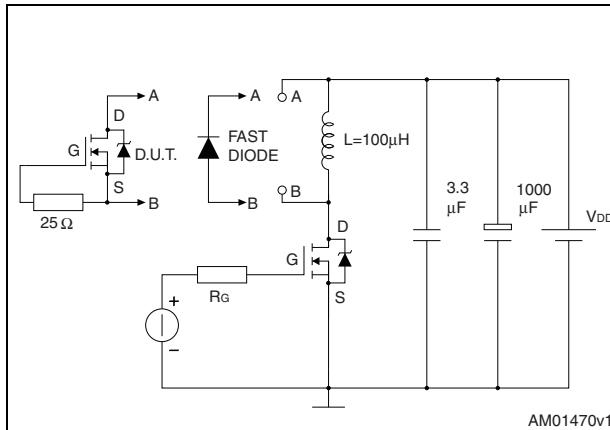
**Figure 12. Switching times test circuit for resistive load**



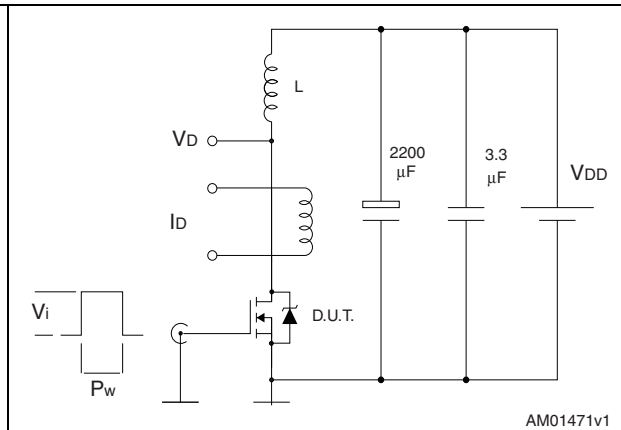
**Figure 13. Gate charge test circuit**



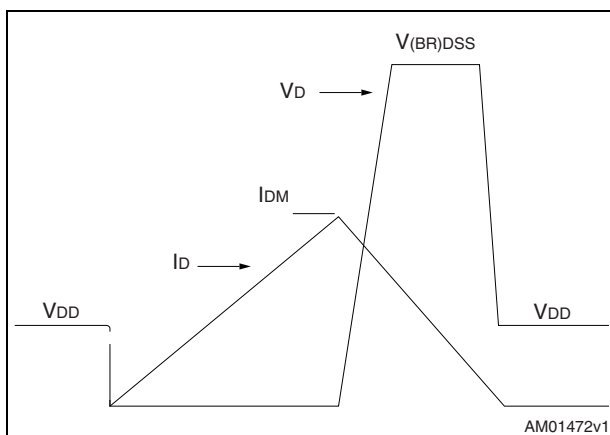
**Figure 14. Test circuit for inductive load switching and diode recovery times**



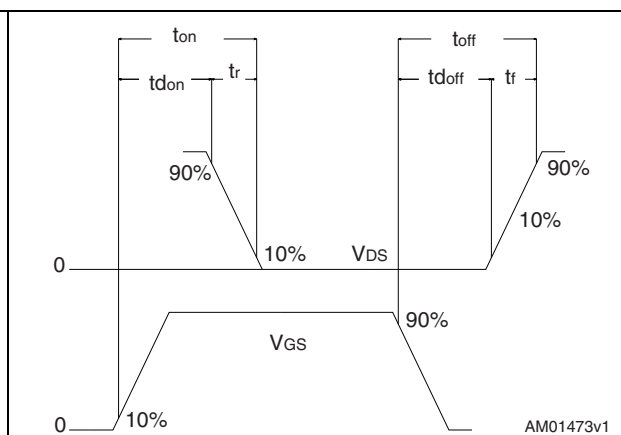
**Figure 15. Unclamped Inductive load test circuit**



**Figure 16. Unclamped inductive waveform**



**Figure 17. Switching time waveform**





## 4 Package mechanical data

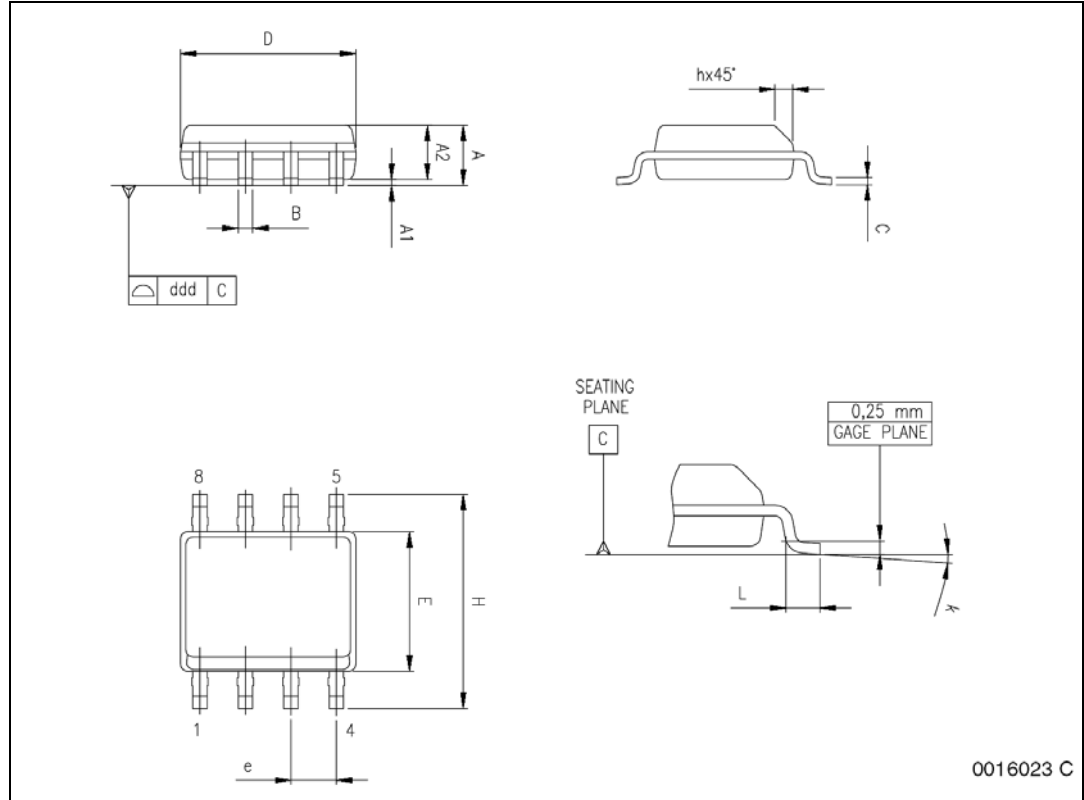
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Table 1. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 18. Package dimensions



0016023 C

## 5 Revision history

**Table 8. Revision history**

Date	Revision	Changes
21-Jun-2004	4	Complete document
13-Nov-2006	5	The document has been reformatted
02-May-2011	6	<a href="#">Table 1: Device summary</a> has been corrected

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