STW56NM60ND

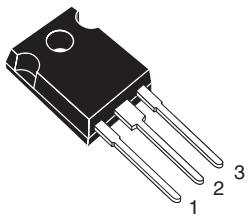
N-channel 600 V, 0.047 Ω typ., 50 A FDmesh™ II Power MOSFET in TO-247 package

Datasheet — preliminary data

Features

Order code	V_{DSS} @ T_{JMAX}	$R_{DS(on)}$ max	I_D
STW56NM60ND	650 V	< 0.06 Ω	50 A

- The worldwide best $R_{DS(on)}$ * area amongst the fast recovery diode devices
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Extremely high dv/dt and avalanche capabilities



TO-247

Applications

- Switching applications

Description

This FDmesh™ II Power MOSFET with intrinsic fast-recovery body diode is produced using the second generation of MDmesh™ technology. Utilizing a new strip-layout vertical structure, this revolutionary device features extremely low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.

Figure 1. Internal schematic diagram

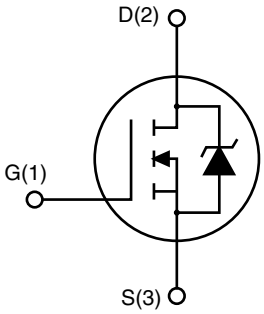


Table 1. Device summary

Order code	Marking	Package	Packaging
STW56NM60ND	56NM60ND	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	50	A
I_D	Drain current (continuous) at T_C = 100 °C	32	A
I_{DM} (1)	Drain current (pulsed)	200	A
P_{TOT}	Total dissipation at T_C = 25 °C	390	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	10	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AS}, V_{DD}=50 V)	TBD	mJ
dv/dt (2)	Peak diode recovery voltage slope	40	V/ns
T_{stg}	Storage temperature	- 55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤50 A, di/dt ≤400 A/µs, V_{DS} peak ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.32	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	50	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS} = 0)	I_D = 1 mA,	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 600 V V_{DS} = 600 V, T_C = 125 °C			1 150	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 25 V			±150	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 25 A		0.047	0.06	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	5000 245 10	-	pF pF pF
$C_{oss\ eq.}$ (1)	Output capacitance	V_{GS} = 0, V_{DS} = 0 to 480 V	-	TBD	-	pF
R_g	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV Open drain	-	1.7	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 200 V, I_D = 25 A, V_{GS} = 10 V, *(see Figure 3)*	-	TBD TBD TBD	-	nC nC nC

1. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$ $t_{r(v)}$ $t_{f(i)}$ $t_{c(off)}$	Voltage delay time Voltage rise time Current fall time Crossing time	V_{DD} = 325 V, I_D = 25 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 2)*	-	TBD TBD TBD TBD	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		50 200	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 50 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 50 A, di/dt = 100 A/µs V_{DD} = 60 V *(see Figure 4)*	-	TBD TBD TBD		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 50A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C *(see Figure 4)*	-	TBD TBD TBD		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

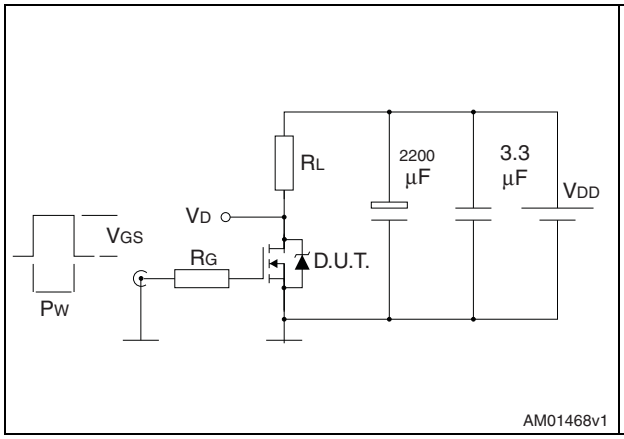


Figure 3. Gate charge test circuit

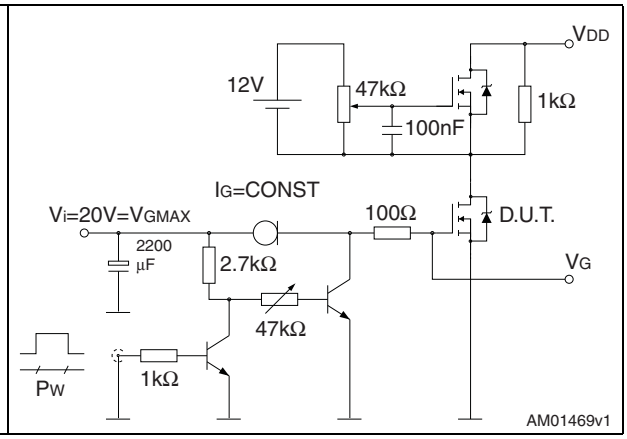


Figure 4. Test circuit for inductive load switching and diode recovery times

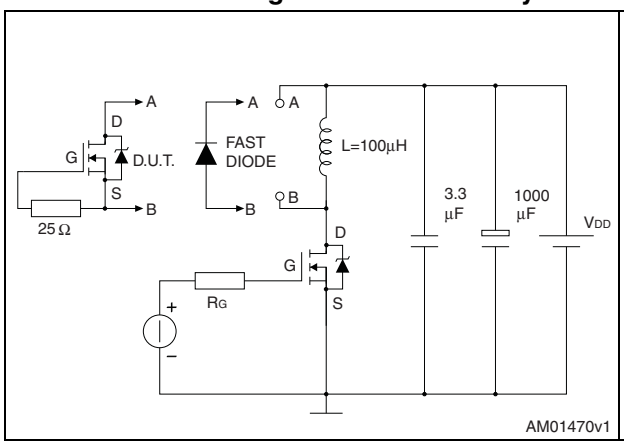


Figure 5. Unclamped inductive load test circuit

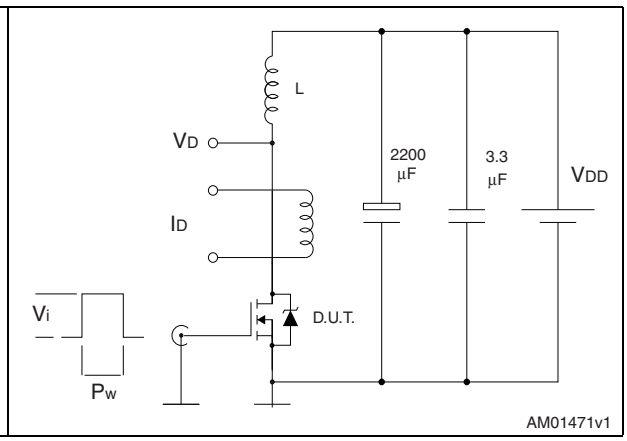


Figure 6. Unclamped inductive waveform

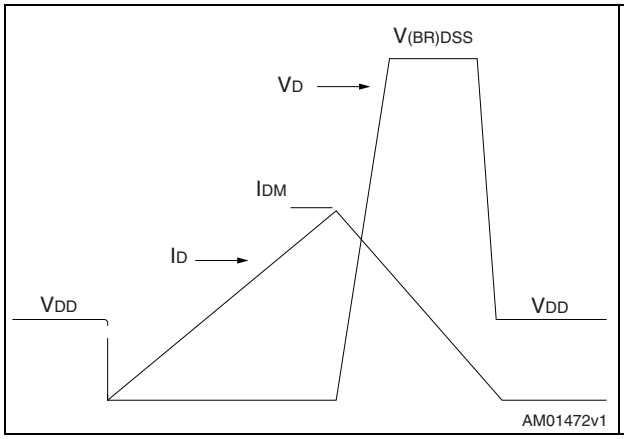
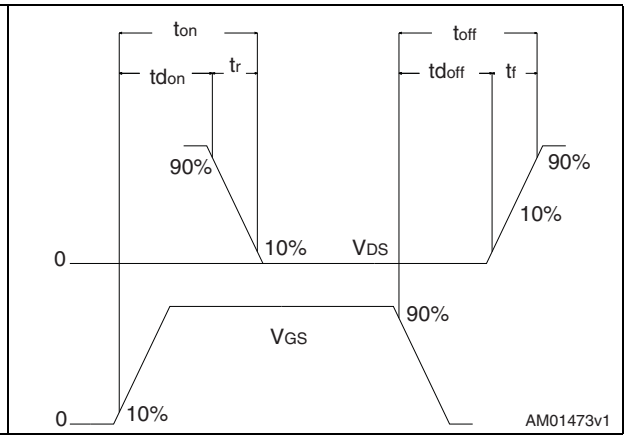


Figure 7. Switching time waveform



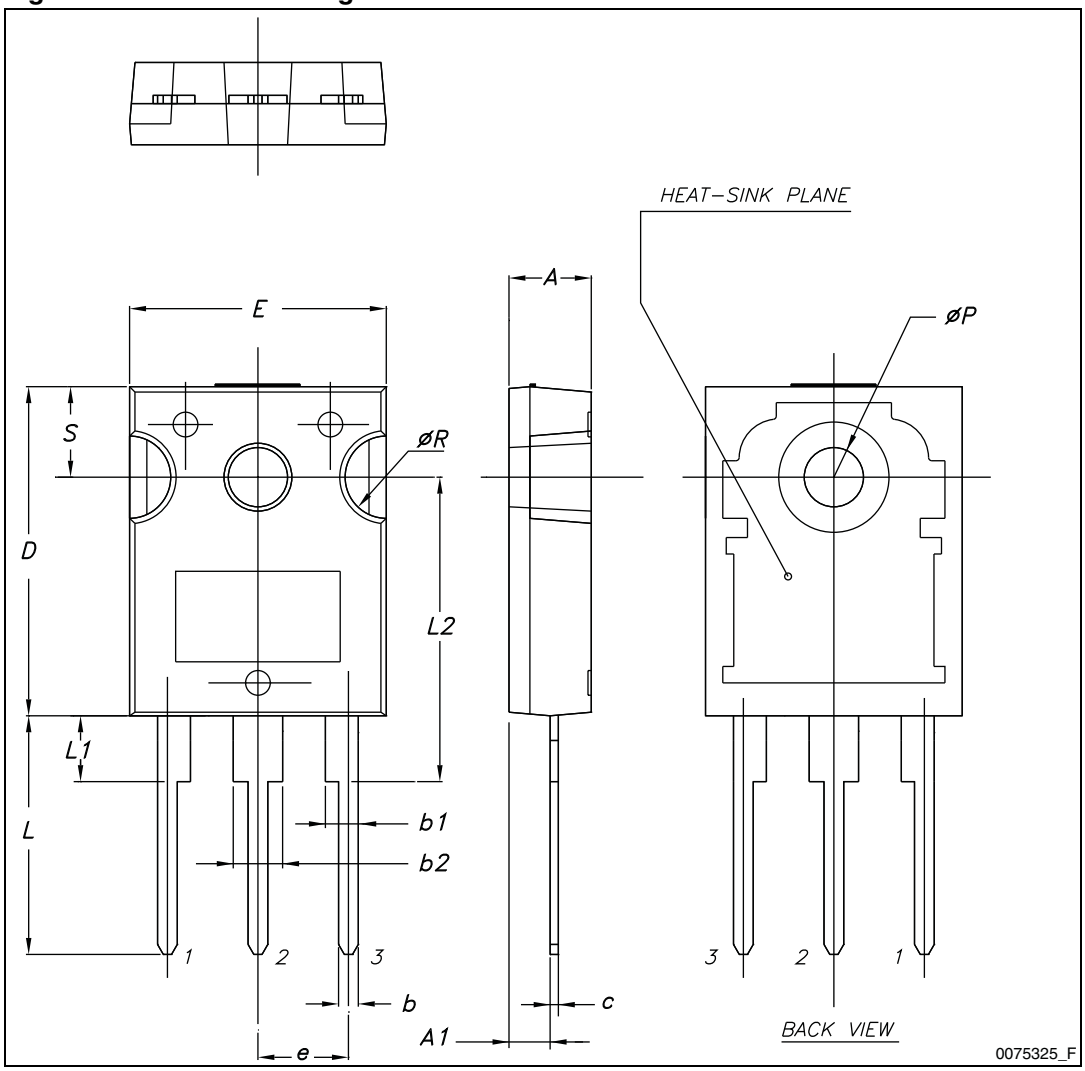
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK is an ST trademark.

Table 8. TO-247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
∅P	3.55		3.65
∅R	4.50		5.50
S		5.50	

Figure 8. TO-247 drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
13-Jul-2012	1	First release

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