



VND5004A-E VND5004ASP30-E

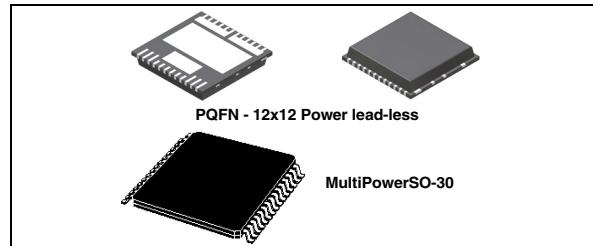
Double 4mΩ high side driver with analog current sense
for automotive applications

Features

| | | |
|-----------------------------------|-------------------|---------------------|
| Max transient supply voltage | V _{CC} | 41V |
| Operating voltage range | V _{CC} | 4.5 to 27V |
| Max On-State resistance (per ch.) | R _{ON} | 4 mΩ |
| Current limitation (typ) | I _{LIMH} | 100A |
| Off state supply current | I _S | 2 μA ⁽¹⁾ |

1. Typical value with all loads connected

- General
 - Inrush current active management by power limitation
 - Very low stand-by current
 - 3.0V CMOS compatible input
 - Optimized electromagnetic emission
 - Very low electromagnetic susceptibility
 - In compliance with the 2002/95/EC European directive
- Diagnostic functions
 - Proportional load current sense
 - Current sense disable
 - Thermal shutdown indication
- Protection
 - Undervoltage shut-down
 - Overvoltage clamp
 - Load current limitation
 - Thermal shut down
 - Self limiting of fast thermal transients
 - Protection against loss of ground and loss of V_{CC}
 - Reverse battery protection with self switch on of the PowerMOS (see [Application schematic on page 18](#))
 - Electrostatic discharge protection



Application

- All types of resistive, inductive and capacitive loads
- Suitable for power management applications

Description

The VND5004ATR-E and VND5004ASP30-E are devices made using STMicroelectronics VIPower technology. They are intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp and load dump protection circuit protect the devices against transients on the V_{CC} pin (see ISO7637 transient compatibility table). These devices integrate an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS_DIS is driven low or left open. When CS_DIS is driven high, the CURRENT SENSE pin is high impedance. Output current limitation protects the devices in overload condition. In case of long duration overload, the devices limit the dissipated power to a safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as a fault condition disappears.

Table 1. Devices summary

| Package | Order codes | | |
|----------------------------|----------------|------------------|------------|
| | Tube | Tape and Reel | Tray |
| PQFN-12x12 Power lead-less | - | VND5004ATR-E | VND5004A-E |
| MultiPowerSO-30 | VND5004ASP30-E | VND5004ASP30TR-E | - |

Contents

| | | |
|----------|--|-----------|
| 1 | Block diagram and pin configurations | 5 |
| 2 | Electrical specifications | 7 |
| 2.1 | Absolute maximum ratings | 7 |
| 2.2 | Thermal data | 8 |
| 2.3 | Electrical characteristics | 9 |
| 2.4 | Electrical characteristics curves | 15 |
| 3 | Application information | 18 |
| 3.1 | MCU I/Os protection | 18 |
| 3.2 | Load dump protection | 18 |
| 3.3 | Maximum demagnetization energy (VCC = 13.5V) | 19 |
| 4 | Package and PC board thermal data | 20 |
| 4.1 | MultiPowerSO-30 thermal data | 20 |
| 4.2 | PQFN - 12x12 Power lead-less thermal data | 23 |
| 5 | Package and packing information | 26 |
| 5.1 | ECOPACK [®] packages | 26 |
| 5.2 | MultiPowerSO-30 mechanical data | 26 |
| 5.3 | PQFN - 12x12 Power lead-less mechanical data | 28 |
| 5.4 | MultiPowerSO-30 packing information | 30 |
| 5.5 | PQFN - 12x12 Power lead-less packing information | 31 |
| 6 | Revision history | 33 |

List of tables

| | | |
|-----------|---|----|
| Table 1. | Devices summary | 1 |
| Table 2. | Pin functions | 5 |
| Table 3. | Suggested connections for unused and n.c. pins | 6 |
| Table 4. | Absolute maximum ratings | 7 |
| Table 5. | Thermal data | 8 |
| Table 6. | Power section | 9 |
| Table 7. | Switching (VCC = 13V; Tj = 25°C) | 9 |
| Table 8. | Logic input | 10 |
| Table 9. | Protection and diagnostics | 10 |
| Table 10. | Current sense (8V<VCC<16V) | 11 |
| Table 11. | Truth table | 12 |
| Table 12. | Electrical transient requirements | 13 |
| Table 13. | Thermal parameters for MultiPowerSO-30 | 22 |
| Table 14. | Thermal parameters for PQFN - 12x12 Power lead-less | 25 |
| Table 15. | MultiPowerSO-30 mechanical data | 27 |
| Table 16. | PQFN - 12x12 Power lead-less mechanical data | 29 |
| Table 17. | Document revision history | 33 |

List of figures

| | | |
|------------|---|----|
| Figure 1. | Block diagram | 5 |
| Figure 2. | Configuration diagram (not in scale) | 6 |
| Figure 3. | Current and voltage conventions | 7 |
| Figure 4. | Current sense delay characteristics | 11 |
| Figure 5. | Switching characteristics | 12 |
| Figure 6. | Waveforms | 14 |
| Figure 7. | Off state output current | 15 |
| Figure 8. | High level input current | 15 |
| Figure 9. | Input clamp voltage | 15 |
| Figure 10. | Input low level | 15 |
| Figure 11. | Input high level | 15 |
| Figure 12. | Input hysteresis voltage | 15 |
| Figure 13. | On state resistance vs. T_{case} | 16 |
| Figure 14. | On state resistance vs. V_{CC} | 16 |
| Figure 15. | Undervoltage shutdown | 16 |
| Figure 16. | Turn-On voltage slope | 16 |
| Figure 17. | I_{LIMH} vs. T_{case} | 16 |
| Figure 18. | Turn-Off voltage slope | 16 |
| Figure 19. | CS_DIS high level voltage | 17 |
| Figure 20. | CS_DIS clamp voltage | 17 |
| Figure 21. | CS_DIS low level voltage | 17 |
| Figure 22. | Application schematic | 18 |
| Figure 23. | Maximum turn off current versus inductance | 19 |
| Figure 24. | MultiPowerSO-30 PC board | 20 |
| Figure 25. | $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON) | 20 |
| Figure 26. | MultiPowerSO-30 thermal impedance junction ambient single pulse (one channel ON) | 21 |
| Figure 27. | Thermal fitting model of a double channel HSD in MultiPowerSO-30 | 21 |
| Figure 28. | 12x12 Power lead-less package PC board | 23 |
| Figure 29. | $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON) | 23 |
| Figure 30. | PQFN - 12x12 Power lead-less package thermal impedance junction ambient single pulse (one channel ON) | 24 |
| Figure 31. | Thermal fitting model of a double channel HSD in PQFN - 12x12 Power lead-less | 24 |
| Figure 32. | MultiPowerSO-30 outline | 26 |
| Figure 33. | PQFN - 12x12 Power lead-less outline | 28 |
| Figure 34. | MultiPowerSO-30 tube shipment (no suffix) | 30 |
| Figure 35. | MultiPowerSO-30 tape and reel shipment (suffix "TR") | 30 |
| Figure 36. | PQFN - 12x12 Power lead-less tray shipment (no suffix) | 31 |
| Figure 37. | PQFN - 12x12 Power lead-less tape and reel shipment (suffix "TR") | 32 |

1 Block diagram and pin configurations

Figure 1. Block diagram

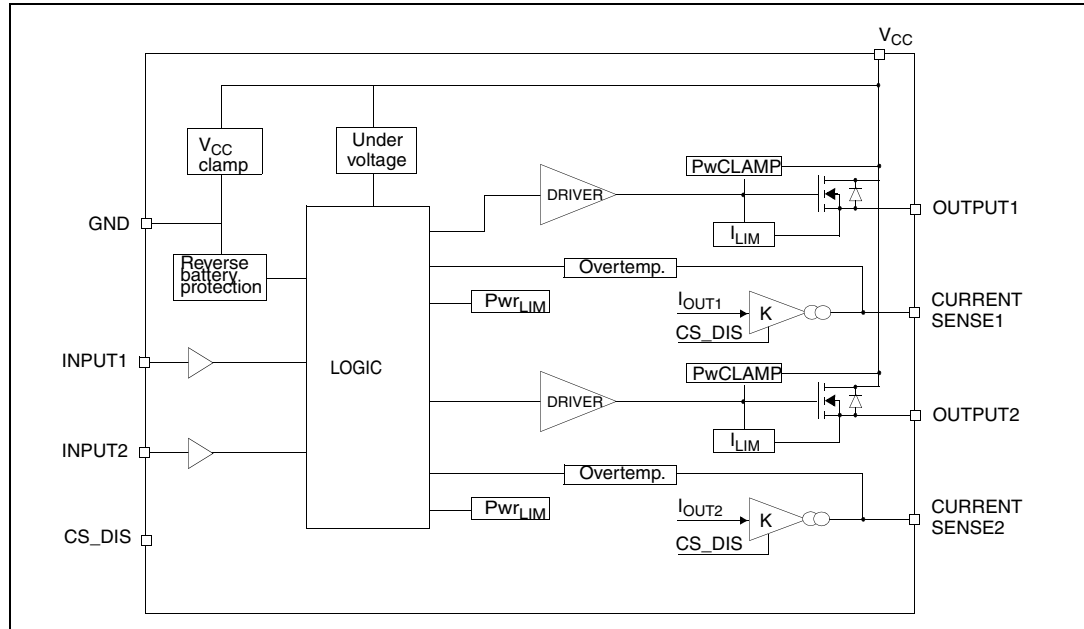


Table 2. Pin functions

| Name | Function |
|------------------|---|
| VCC | Battery connection |
| OUTPUT1,2 | Power output |
| GND | Ground connection |
| INPUT1,2 | Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state |
| CURRENT SENSE1,2 | Analog current sense pin, delivers a current proportional to the load current |
| CS_DIS | Active high CMOS compatible pin, to disable the current sense pins |

Figure 2. Configuration diagram (not in scale)

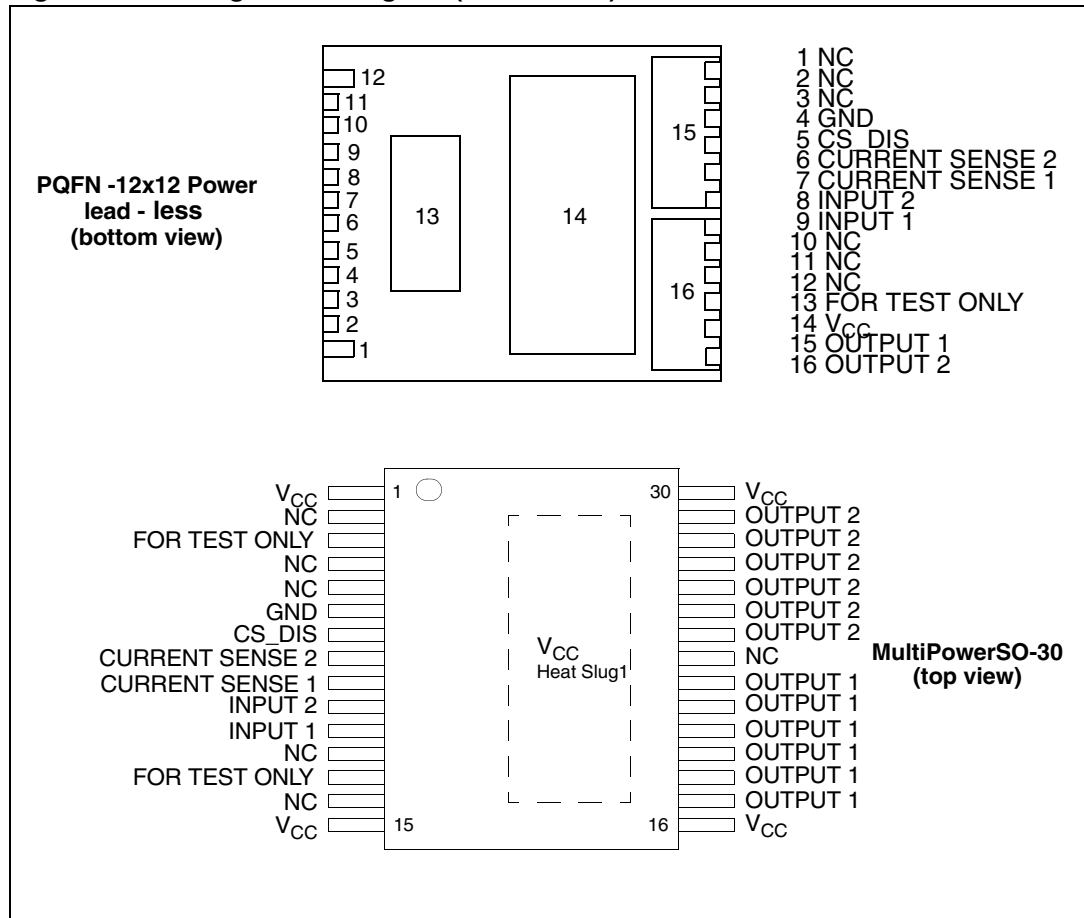


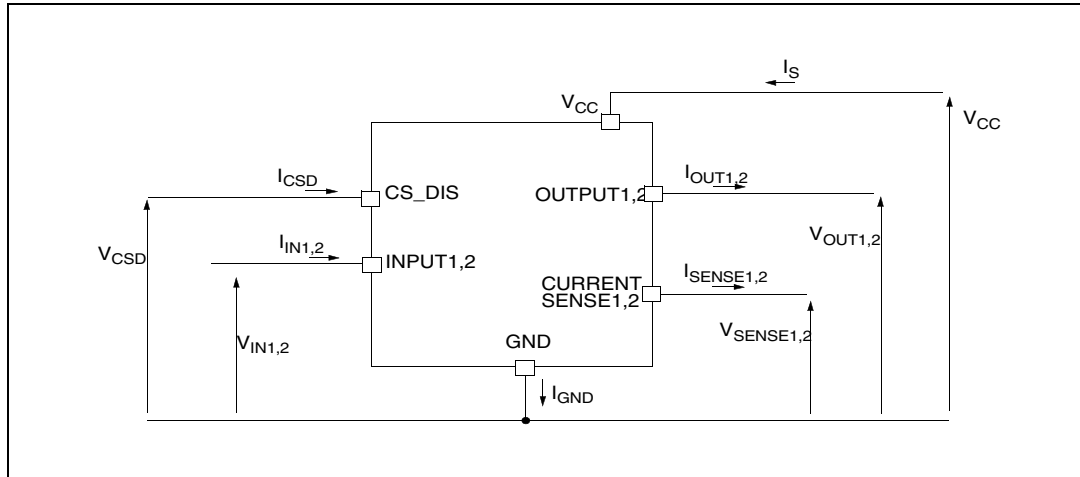
Table 3. Suggested connections for unused and n.c. pins

| Connection / Pin | Current Sense | N.C. | Output | Input | CS_DIS | For test only |
|------------------|----------------------|------|--------|-----------------------|-----------------------|---------------|
| Floating | N.R. ⁽¹⁾ | X | X | X | X | X |
| To ground | Through 1kΩ resistor | X | N.R. | Through 10kΩ resistor | Through 10kΩ resistor | N.R. |

1. Not recommended.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “Absolute maximum ratings” tables may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in this section for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------|---|----------------------------|--------|
| V_{CC} | DC supply voltage | 27 | V |
| V_{CCPK} | Transient supply voltage ($T < 400\text{ms}$, $R_{load} > 0.5\Omega$) | 41 | V |
| $-V_{CC}$ | Reverse DC supply voltage | 16 | V |
| I_{OUT} | DC output current | Internally limited | A |
| $-I_{OUT}$ | Reverse DC output current | 70 | A |
| I_{IN} | DC input current | -1 to 10 | mA |
| I_{CSD} | DC current sense disable input current | -1 to 10 | mA |
| $V_{CSSENSE}$ | Current sense maximum voltage ($V_{CC} > 0V$) | $V_{CC} - 41$ $+V_{CC}$ | V V |
| E_{MAX} | Maximum switching energy (single pulse) ($L = 0.3\text{mH}$; $R_L = 0\Omega$; $V_{bat} = 13.5V$; $T_{jstart} = 150^\circ\text{C}$; $I_{OUT} = I_{limL}(Typ.)$) | 342 | mJ |
| V_{ESD} | Electrostatic discharge (Human Body Model: $R = 1.5k\Omega$; $C = 100\text{pF}$) | 2000 | V |
| V_{ESD} | Charge device model (CDM-AEC-Q100-011) | 750 | V |

Table 4. Absolute maximum ratings (continued)

| Symbol | Parameter | Value | Unit |
|-----------|--------------------------------|------------|------|
| T_j | Junction operating temperature | -40 to 150 | °C |
| T_{STG} | Storage temperature | -55 to 150 | °C |

2.2 Thermal data

Table 5. Thermal data

| Symbol | Parameter | Value | | Unit |
|----------------|---|-------------------|-------------------|------|
| | | MultiPowerSO-30 | 12x12 PLLP | |
| $R_{thj-case}$ | Thermal resistance junction-case (MAX) (with one channel ON) | 0.35 | 0.35 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient (MAX) | 58 ⁽¹⁾ | 39 ⁽²⁾ | °C/W |

1. PCB FR4 area 58mmX58mm , PCB thickness 2mm, Cu thickness 35 μ m, minimum pad layout.
2. PCB FR4 area 78mmX78mm , PCB thickness 2mm, Cu thickness 35 μ m, minimum pad layout.

2.3 Electrical characteristics

Values specified in this section are for $8V < V_{CC} < 24V$, $-40^{\circ}C < T_j < 150^{\circ}C$, unless otherwise stated.

Table 6. Power section

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|---|--|------|------------------|------------------|------------|
| V_{CC} | Operating supply voltage | | 4.5 | 13 | 27 | V |
| V_{USD} | Undervoltage shutdown | | | 3.5 | 4.5 | V |
| $V_{USDhyst}$ | Undervoltage shut-down hysteresis | | | 0.5 | | V |
| R_{ON} | On-state resistance ⁽¹⁾ | $I_{OUT}=15A; T_j=25^{\circ}C$ | | | 4 | m Ω |
| | | $I_{OUT}=15A; T_j=150^{\circ}C$ | | | 8 | m Ω |
| | | $I_{OUT}=15A; V_{CC}=5V; T_j=25^{\circ}C$ | | | 6 | m Ω |
| $R_{ON REV}$ | R_{dson} in reverse battery condition | $V_{CC}=-13V; I_{OUT}=-15A; T_j=25^{\circ}C$ | | | 4 | m Ω |
| V_{clamp} | V_{CC} clamp voltage | $I_{CC}=20 mA; I_{OUT1,2}=0A$ | 41 | 46 | 52 | V |
| I_S | Supply current | Off state; $V_{CC}=13V; T_j=25^{\circ}C;$ $V_{IN}=V_{OUT}=V_{SENSE}=V_{CSD}=0V$ | | 2 ⁽²⁾ | 5 ⁽²⁾ | μA |
| | | On state; $V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A$ | | 3.5 | 6 | mA |
| $I_{L(off)}$ | Off-state output current ⁽¹⁾ | $V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=25^{\circ}C$ | 0 | 0.01 | 3 | μA |
| | | $V_{IN}=V_{OUT}=0V; V_{CC}=13V; T_j=125^{\circ}C$ | 0 | | 5 | μA |

1. For each channel.
2. PowerMOS leakage included.

Table 7. Switching ($V_{CC} = 13V; T_j = 25^{\circ}C$)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------|---|---|------|--------------------------------|------|------------|
| $t_{d(on)}$ | Turn-on delay time | $R_L=0.87\Omega$ (see Figure 5.) | | 25 | | μs |
| $t_{d(off)}$ | Turn-off delay time | $R_L=0.87\Omega$ (see Figure 5.) | | 35 | | μs |
| $(dV_{OUT}/dt)_{on}$ | Turn-on voltage slope | $R_L=0.87\Omega$ | | See Figure 16. | | V/ μs |
| $(dV_{OUT}/dt)_{off}$ | Turn-off voltage slope | $R_L=0.87\Omega$ | | See Figure 18. | | V/ μs |
| W_{ON} | Switching energy losses during t_{won} | $R_L=0.87\Omega$ (see Figure 5.) | | 5.4 | | mJ |
| W_{OFF} | Switching energy losses during t_{woff} | $R_L=0.87\Omega$ (see Figure 5.) | | 2.3 | | mJ |

Table 8. Logic input

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------------|---------------------------|---------------------------------|------|------|------|---------|
| $V_{IL1,2}$ | Input low level voltage | | | | 0.9 | V |
| $I_{IL1,2}$ | Low level input current | $V_{IN}=0.9V$ | 1 | | | μA |
| $V_{IH1,2}$ | Input high level voltage | | 2.1 | | | V |
| $I_{IH1,2}$ | High level input current | $V_{IN}=2.1V$ | | | 10 | μA |
| $V_{I(hyst)1,2}$ | Input hysteresis voltage | | 0.25 | | | V |
| $V_{ICL1,2}$ | Input clamp voltage | $I_{IN}=1mA$ $I_{IN}=-1mA$ | 5.5 | -0.7 | 7 | V V |
| V_{CSDL} | CS_DIS low level voltage | | | | 0.9 | V |
| I_{CSDL} | Low level CS_DIS current | $V_{CSD}=0.9V$ | 1 | | | μA |
| V_{CSDH} | CS_DIS high level voltage | | 2.1 | | | V |
| I_{CSDH} | High level CS_DIS current | $V_{CSD}=2.1V$ | | | 10 | μA |
| $V_{CSD(hyst)}$ | CS_DIS hysteresis voltage | | 0.25 | | | V |
| V_{CSCL} | CS_DIS clamp voltage | $I_{CSD}=1mA$ $I_{CSD}=-1mA$ | 5.5 | -0.7 | 7 | V V |

Table 9. Protection and diagnostics⁽¹⁾

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------|--|-------------------------------------|-------------|-------------|-------------|-------------|
| I_{limH} | Short circuit current | $V_{CC}=13V$ $5V < V_{CC} < 24V$ | 70 | 100 | 140 140 | A A |
| I_{limL} | Short circuit current during thermal cycling | $V_{CC}=13V; T_R < T_J < T_{TSD}$ | | 40 | | A |
| T_{TSD} | Shutdown temperature | | 150 | 175 | 200 | $^{\circ}C$ |
| T_R | Reset temperature | | $T_{RS}+1$ | $T_{RS}+5$ | | $^{\circ}C$ |
| T_{RS} | Thermal reset of STATUS | | 135 | | | $^{\circ}C$ |
| T_{HYST} | Thermal hysteresis ($T_{TSD}-T_R$) | | | 7 | | $^{\circ}C$ |
| V_{DEMAG} | Turn-off output voltage clamp | $I_{OUT}=2A; V_{IN}=0; L=6mH$ | $V_{CC}-27$ | $V_{CC}-30$ | $V_{CC}-33$ | V |

1. To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles.

Table 10. Current sense (8V<VCC<16V)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|--|---|----------------|----------------|----------------|--------------------|
| K_1 | I_{OUT}/I_{SENSE} | $I_{OUT}=15A$; $V_{SENSE}=4V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C$ $T_j=25^{\circ}C...150^{\circ}C$ | 11530 12730 | 16000 16000 | 19340 19270 | |
| K_2 | I_{OUT}/I_{SENSE} | $I_{OUT}=30A$; $V_{SENSE}=4V$; $V_{CSD}=0V$; $T_j=-40^{\circ}C$ $T_j=25^{\circ}C...150^{\circ}C$ | 13430 14500 | 16150 16150 | 17880 17880 | |
| I_{SENSE0} | Analog sense current | $I_{OUT}=0A$; $V_{SENSE}=0V$; $V_{CSD}=5V$; $V_{IN}=0V$; $T_j=-40^{\circ}C$ to $150^{\circ}C$ $V_{CSD}=0V$; $V_{IN}=5V$; $T_j=-40^{\circ}C$ to $150^{\circ}C$ | 0 0 | | 5 400 | μA μA |
| V_{SENSE} | Max analog sense output voltage | $I_{OUT}=45A$; $V_{CSD}=0V$; $R_{SENSE}=3.9k\Omega$ | 5 | | | V |
| V_{SENSEH} | Analog sense output voltage in overtemperature condition | $V_{CC}=13V$; $R_{SENSE}=3.9k\Omega$ | | 9 | | V |
| I_{SENSEH} | Analog sense output current in overtemperature condition | $V_{CC}=13V$; $V_{SENSE}=5V$ | | 8 | | mA |
| $t_{DSENSE1H}$ | Delay response time from falling edge of CS_DIS pin | $V_{SENSE}<4V$, $5A<I_{OUT}<30A$ $I_{SENSE}=90\%$ of $I_{SENSE\ max}$ (see Figure 4.) | | 50 | 100 | μs |
| $t_{DSENSE1L}$ | Delay response time from rising edge of CS_DIS pin | $V_{SENSE}<4V$, $5A<I_{OUT}<30A$ $I_{SENSE}=10\%$ of $I_{SENSE\ max}$ (see Figure 4.) | | 5 | 20 | μs |
| $t_{DSENSE2H}$ | Delay response time from rising edge of INPUT pin | $V_{SENSE}<4V$, $5A<I_{OUT}<30A$ $I_{SENSE}=90\%$ of $I_{SENSE\ max}$ (see Figure 4.) | | 270 | 600 | μs |
| $t_{DSENSE2L}$ | Delay response time from falling edge of INPUT pin | $V_{SENSE}<4V$, $5A<I_{OUT}<30A$ $I_{SENSE}=10\%$ of $I_{SENSE\ max}$ (see Figure 4.) | | 100 | 250 | μs |

Figure 4. Current sense delay characteristics

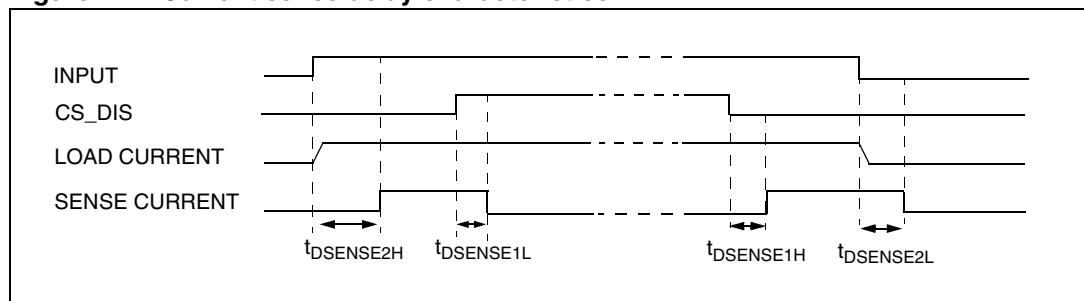


Table 11. Truth table

| Conditions | INPUTn | OUTPUTn | SENSEn ($V_{CSD}=0V$) ⁽¹⁾ (see Figure 3.) |
|--|--------|---------|--|
| Normal operation | L | L | 0 |
| | H | H | Nominal |
| Overtemperature | L | L | 0 |
| | H | L | V_{SENSEH} |
| Undervoltage | L | L | 0 |
| | H | L | 0 |
| Short circuit to GND ($R_{sc} \leq 10 \text{ m}\Omega$) | L | L | 0 |
| | H | L | 0 if $T_j < T_{TSD}$ |
| | H | L | V_{SENSEH} if $T_j > T_{TSD}$ |
| Short circuit to V_{CC} | L | H | 0 |
| | H | H | < Nominal |
| Negative output voltage clamp | L | L | 0 |

1. If V_{CSD} is high, the SENSE output is at a high impedance. Its potential depends on leakage currents and the external circuit.

Figure 5. Switching characteristics

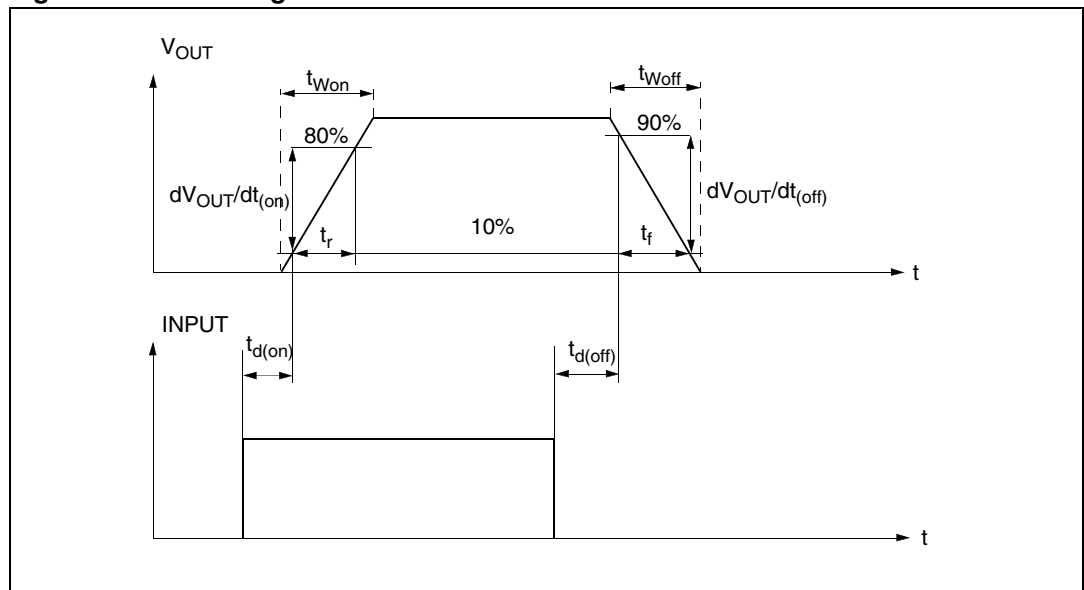


Table 12. Electrical transient requirements

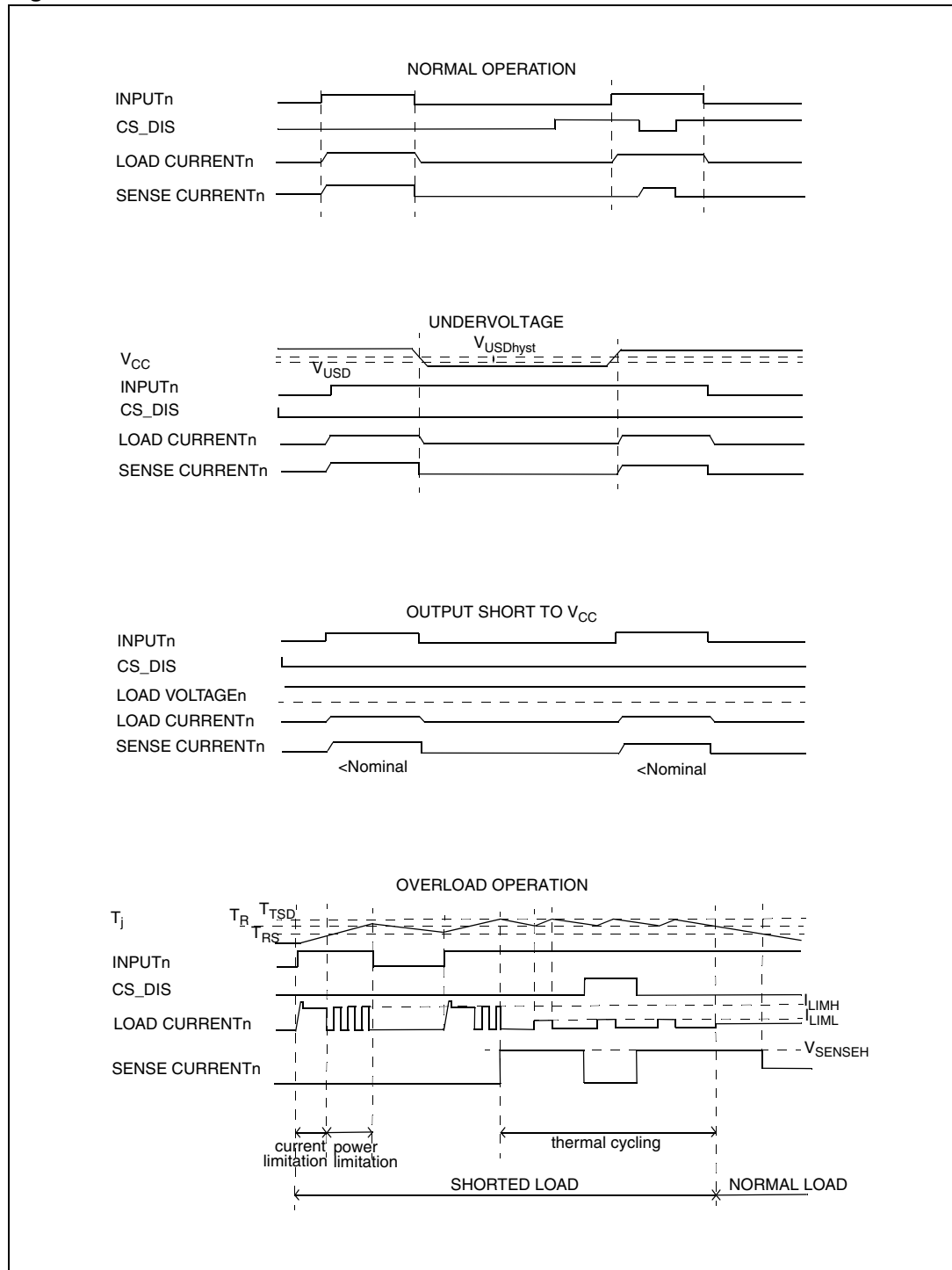
| ISO 7637-2: 2004(E) Test pulse | Test levels ⁽¹⁾ | | Number of pulses or test times | Burst cycle/pulse repetition time | | Delays and Impedance |
|--------------------------------------|----------------------------|--------|--------------------------------------|--------------------------------------|--------|--------------------------|
| | III | IV | | | | |
| 1 | -75 V | -100 V | 5000 pulses | 0.5 s | 5 s | 2 ms, 10 Ω |
| 2a | +37 V | +50 V | 5000 pulses | 0.2 s | 5 s | 50 μ s, 2 Ω |
| 3a | -100 V | -150 V | 1h | 90 ms | 100 ms | 0.1 μ s, 50 Ω |
| 3b | +75 V | +100 V | 1h | 90 ms | 100 ms | 0.1 μ s, 50 Ω |
| 4 | -6 V | -7 V | 1 pulse | | | 100 ms, 0.01 Ω |
| 5b ⁽²⁾ | +65 V | +87 V | 1 pulse | | | 400 ms, 2 Ω |

| ISO 7637-2: 2004(E) Test pulse | Test level results ⁽¹⁾ | |
|--------------------------------------|-----------------------------------|----|
| | III | IV |
| 1 | C | C |
| 2a | C | C |
| 3a | C | C |
| 3b | C | C |
| 4 | C | C |
| 5b ⁽²⁾ ⁽³⁾ | C | C |

1. The above test levels must be considered referred to $V_{cc} = 13.5V$ except for pulse 5b
2. Valid in case of external load dump clamp: 40V maximum referred to ground.
3. Suppressed load dump (pulse 5b) is withstood with a minimum load connected as specified in [Table 4.](#): *Absolute maximum ratings.*

| Class | Contents |
|-------|--|
| C | All functions of the device are performed as designed after exposure to disturbance. |
| E | One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device. |

Figure 6. Waveforms



2.4 Electrical characteristics curves

Figure 7. Off state output current

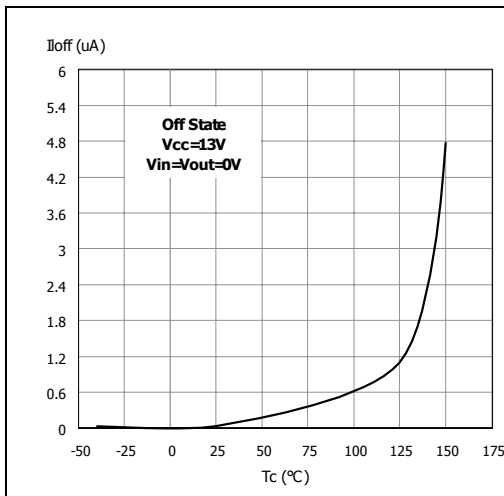


Figure 8. High level input current

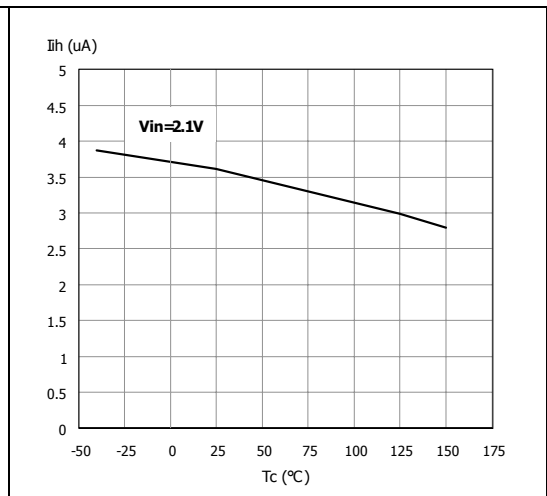


Figure 9. Input clamp voltage

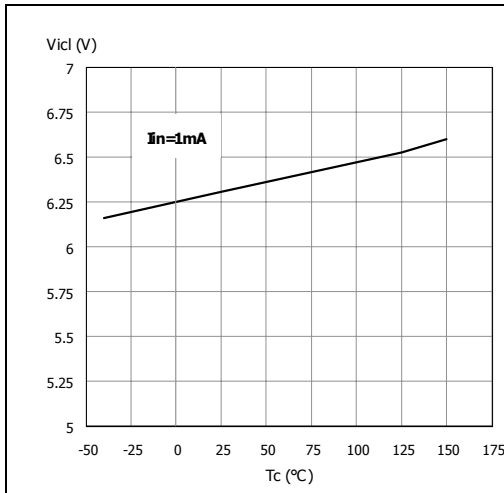


Figure 10. Input low level

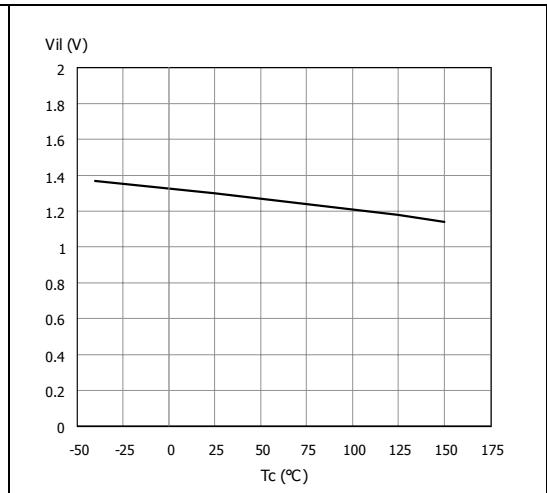


Figure 11. Input high level

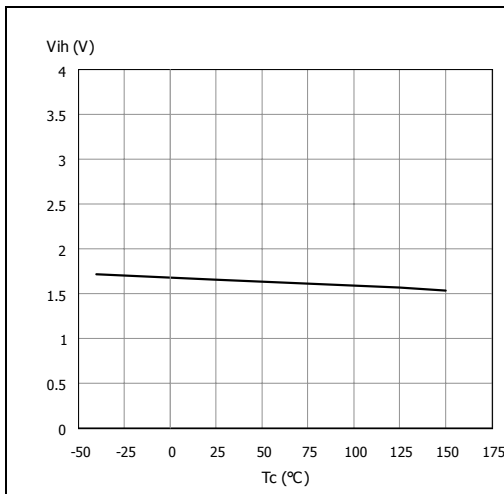


Figure 12. Input hysteresis voltage

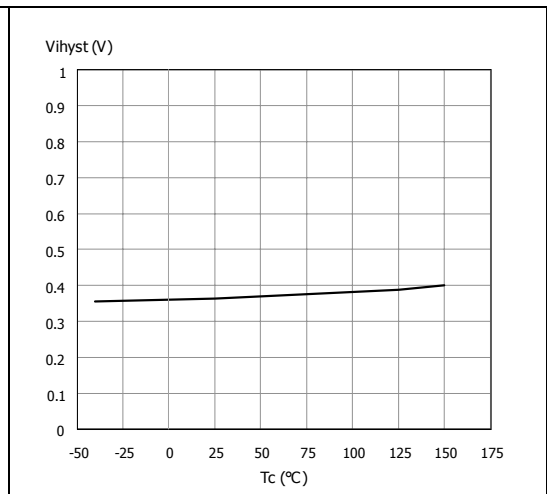


Figure 13. On state resistance vs. T_{case}

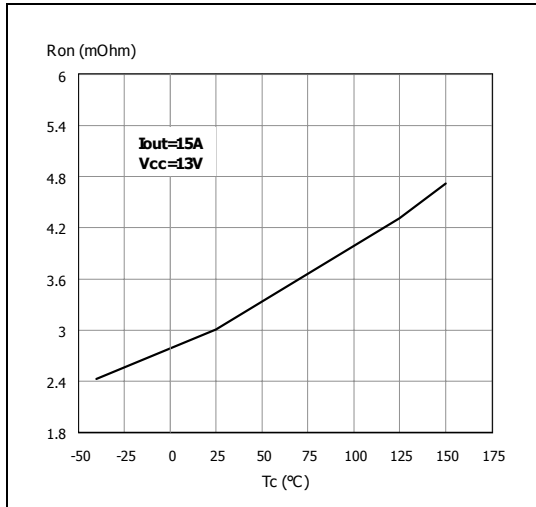


Figure 14. On state resistance vs. V_{CC}

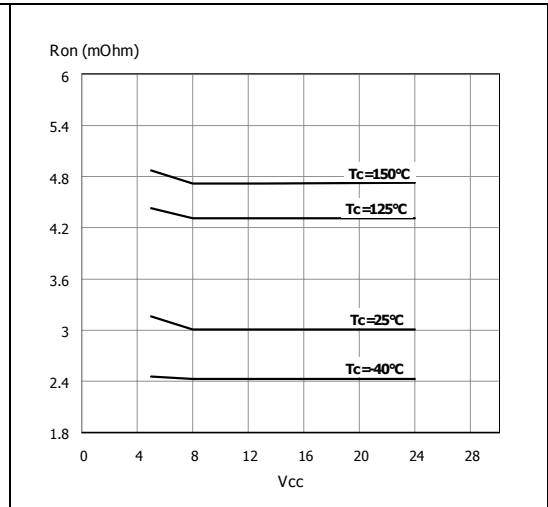


Figure 15. Undervoltage shutdown

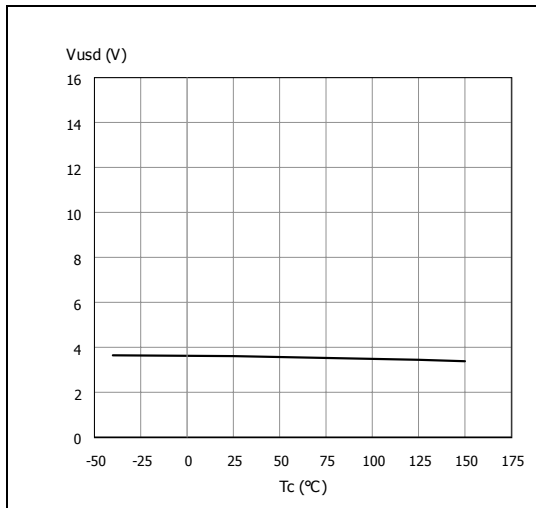


Figure 16. Turn-On voltage slope

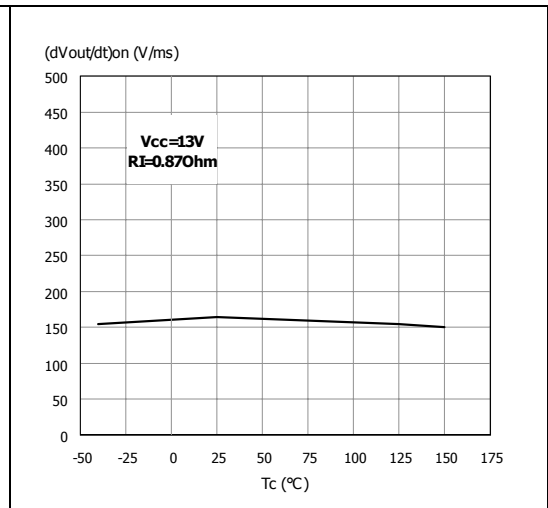


Figure 17. I_{LIMH} vs. T_{case}

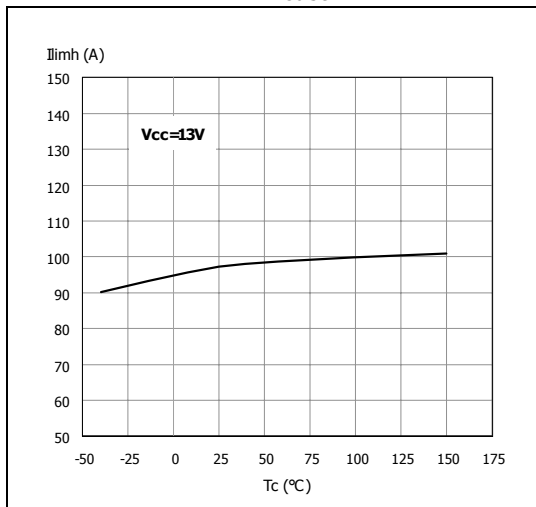


Figure 18. Turn-Off voltage slope

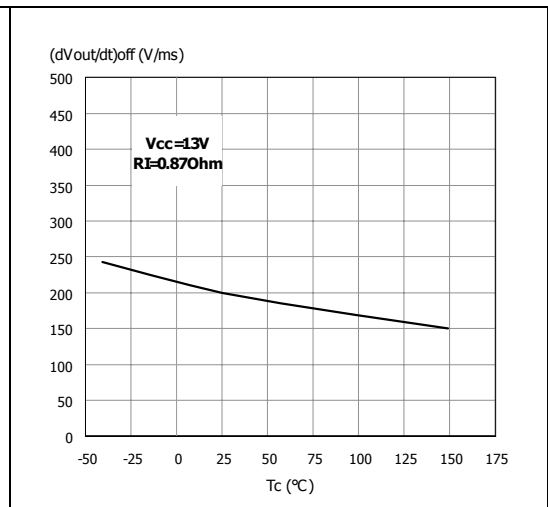


Figure 19. CS_DIS high level voltage

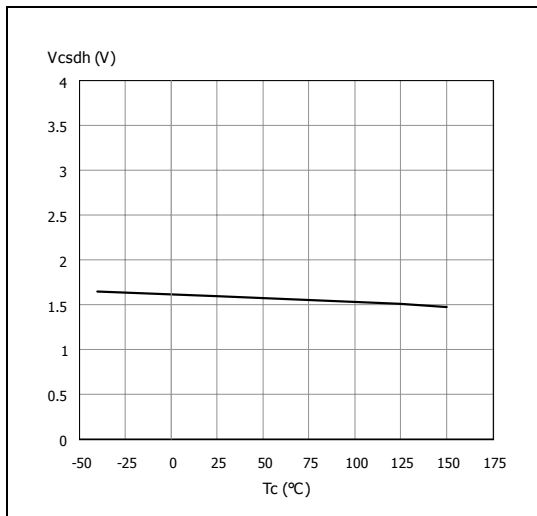


Figure 20. CS_DIS clamp voltage

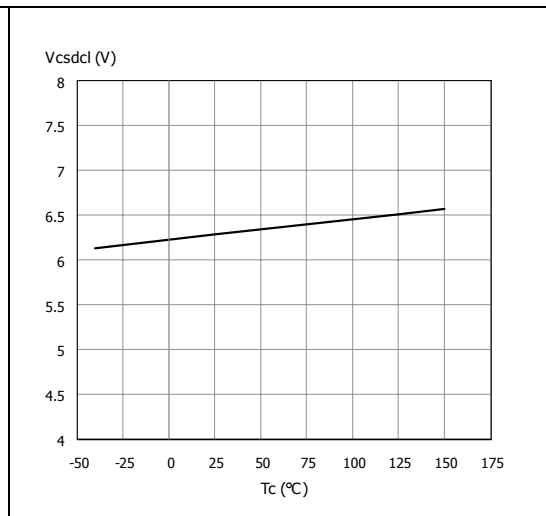
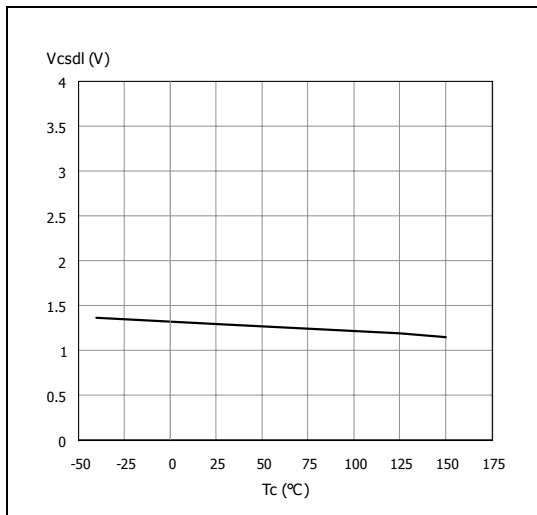
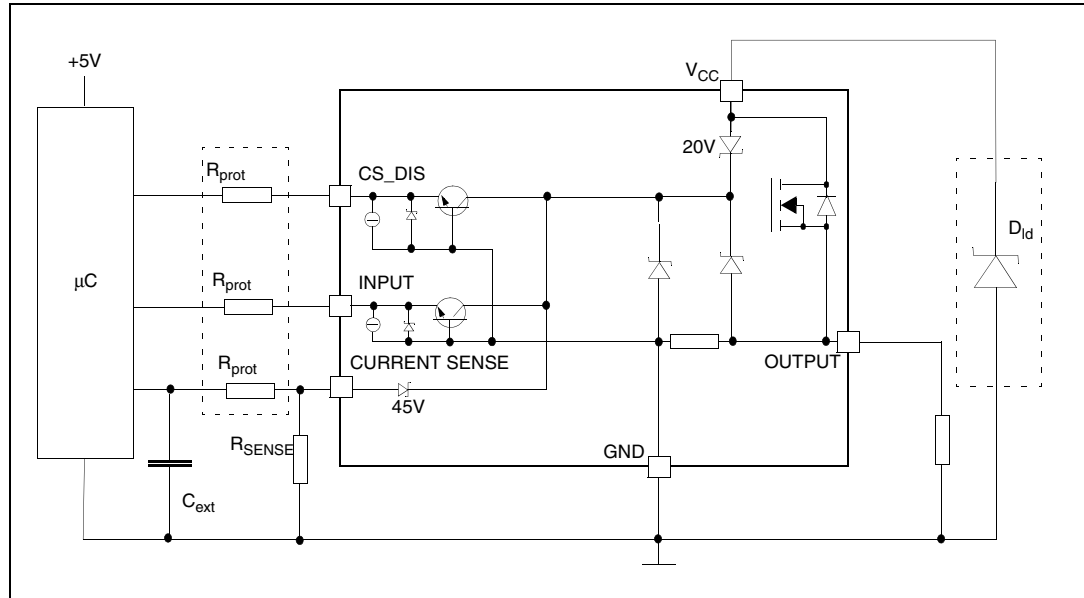


Figure 21. CS_DIS low level voltage



3 Application information

Figure 22. Application schematic



3.1 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins will be pulled negative to approximately -1.5V.

ST suggests the insertion of resistors (R_{prot}) in the lines to prevent the µC I/Os pins from latching up.

The values of these resistors provide a compromise between the leakage current of the µC, the current required by the HSD I/Os (input levels compatibility) and the latch-up limit of the µC I/Os.

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = -1.5V and I_{latchup} ≥ 20mA; V_{OHµC} ≥ 4.5V

$$75\Omega \leq R_{prot} \leq 240k\Omega$$

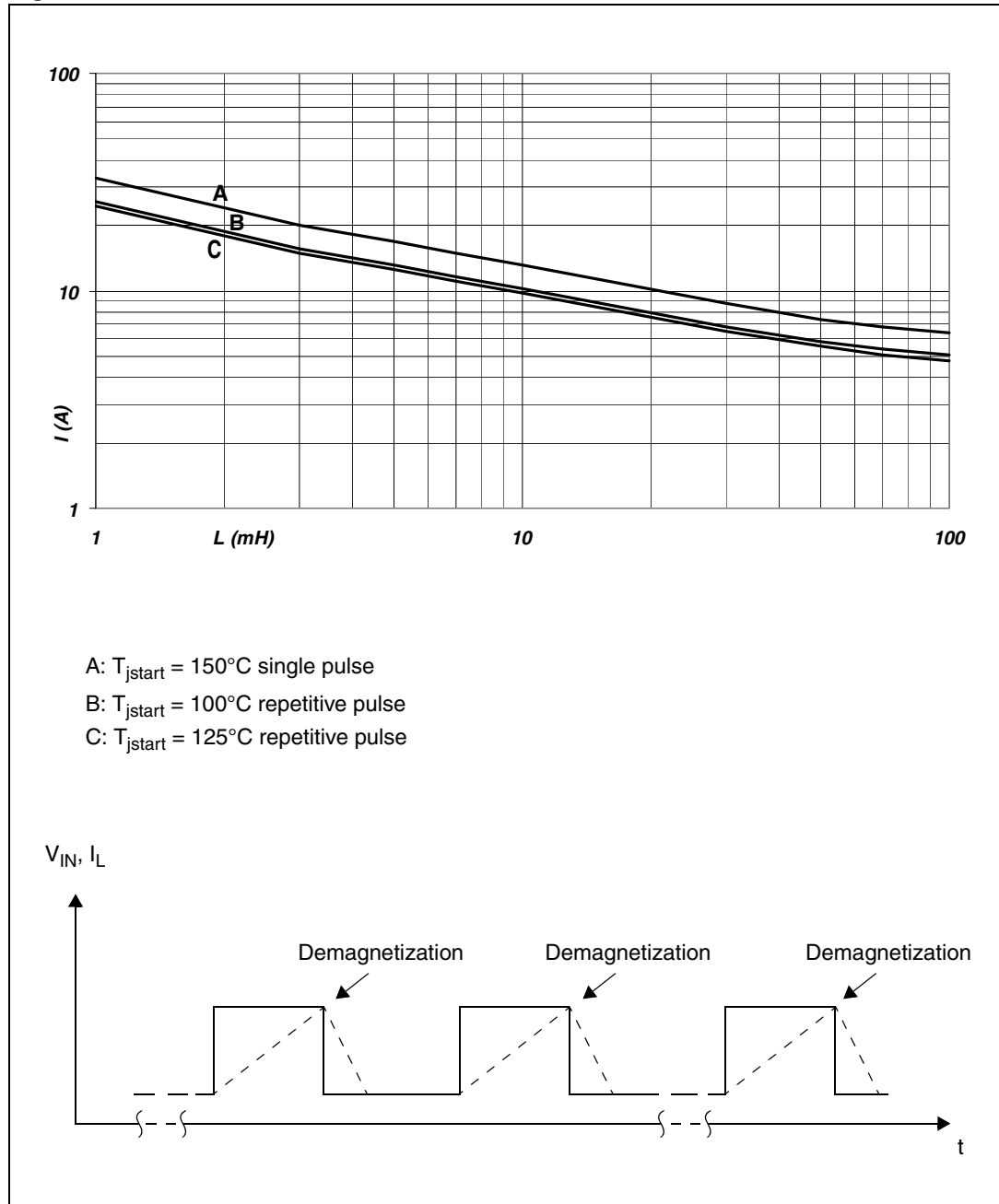
Recommended values: R_{prot} = 10kΩ, C_{EXT} = 10nF

3.2 Load dump protection

D_{id} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CCPK} max rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 Maximum demagnetization energy ($V_{CC} = 13.5V$)

Figure 23. Maximum turn off current versus inductance

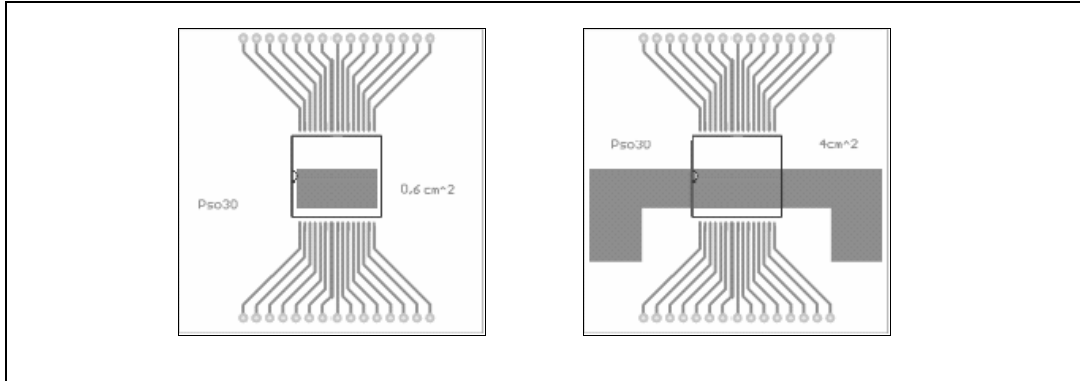


Note: Values are generated with $R_L = 0 \Omega$
 In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 MultiPowerSO-30 thermal data

Figure 24. MultiPowerSO-30 PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 58mm x 58mm, PCB thickness=2mm, Cu thickness=35 μ m (front and back side), Copper areas: from minimum pad lay-out to 16cm²).

Figure 25. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON)

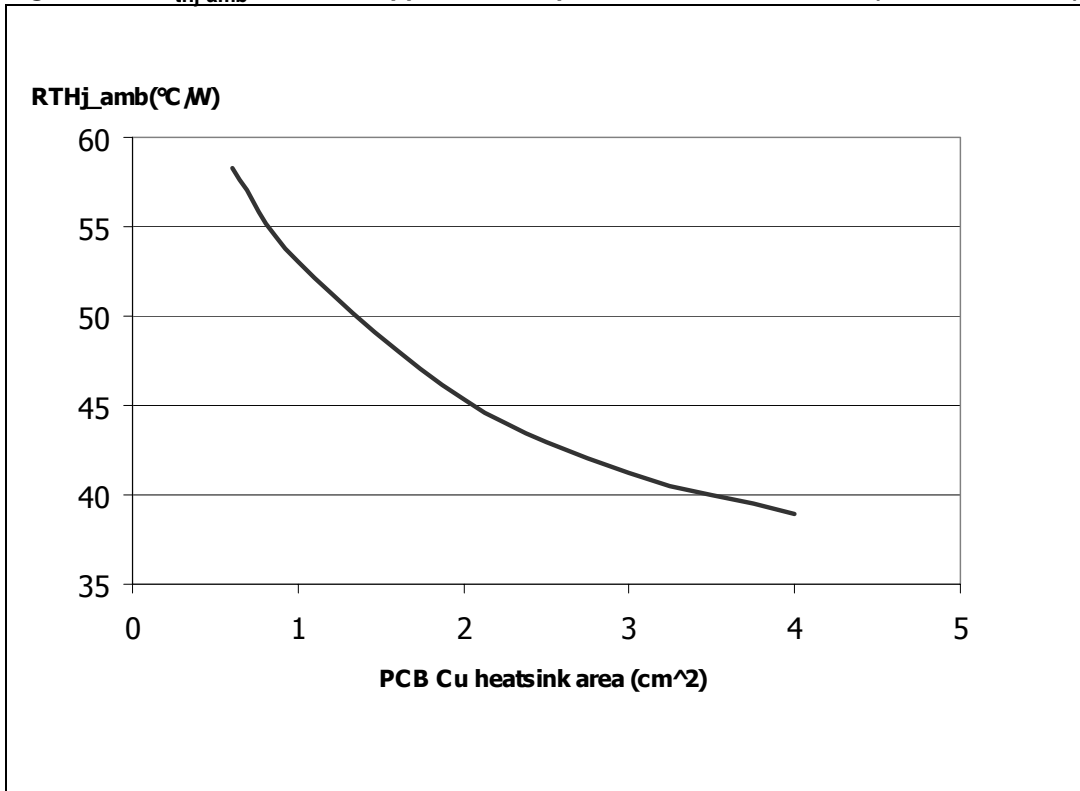


Figure 26. MultiPowerSO-30 thermal impedance junction ambient single pulse (one channel ON)

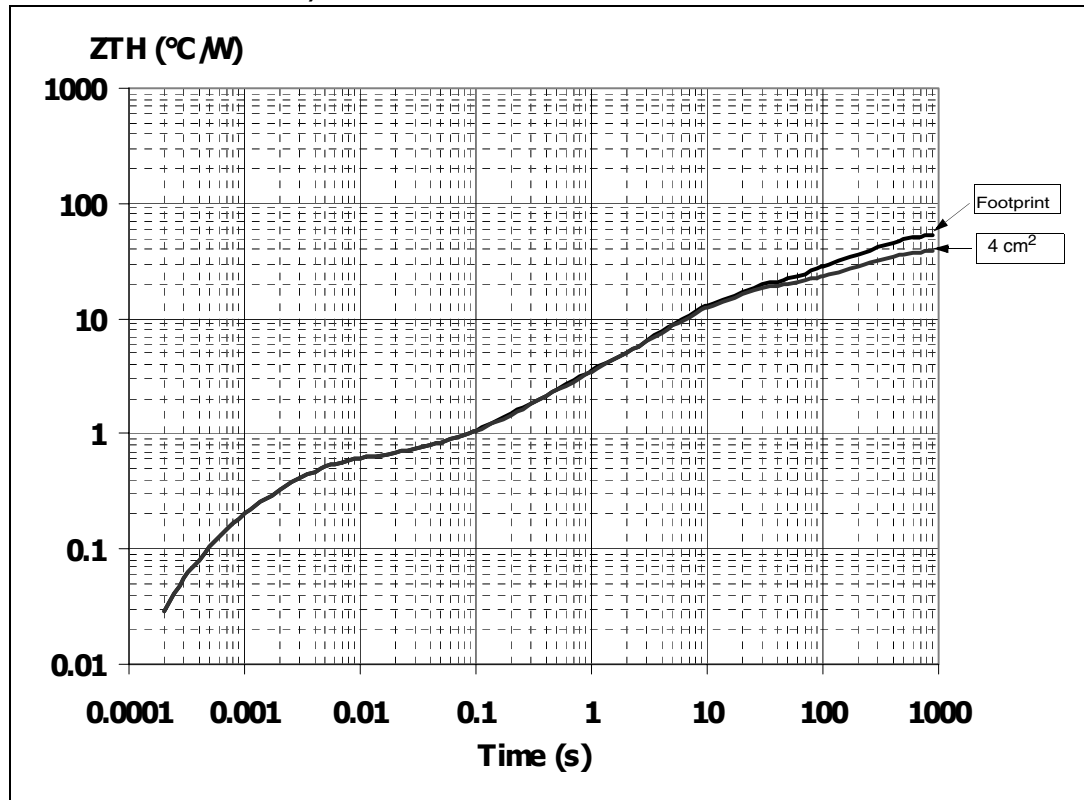
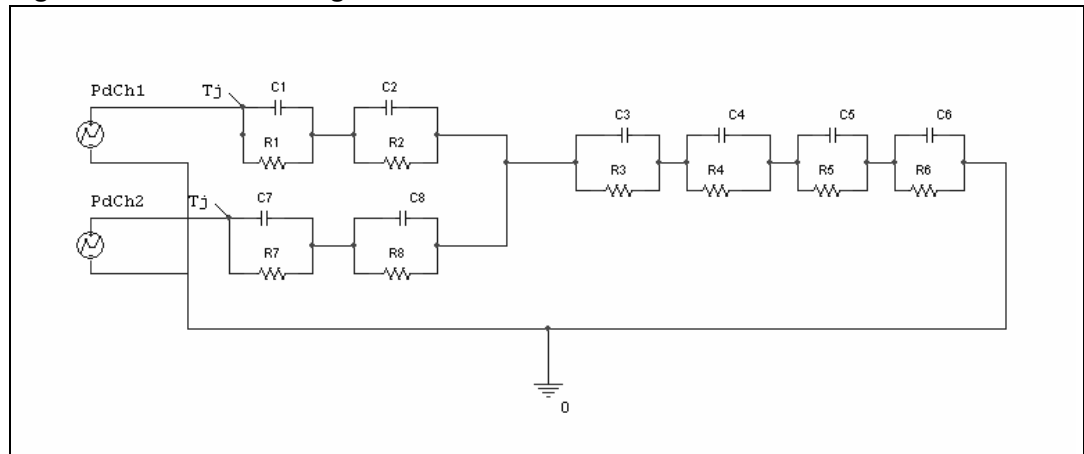


Figure 27. Thermal fitting model of a double channel HSD in MultiPowerSO-30 (a)



a. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 1: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

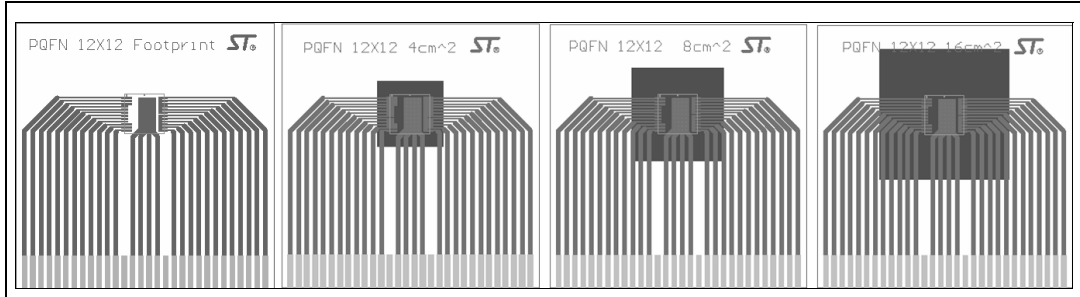
where $\delta = t_p / T$

Table 13. Thermal parameters for MultiPowerSO-30

| Area/island (cm ²) | Footprint | 4 |
|--------------------------------|-----------|------|
| R1 (°C/W) | 0.05 | |
| R2 (°C/W) | 0.3 | |
| R3 (°C/W) | 0.5 | |
| R4 (°C/W) | 1.3 | |
| R5 (°C/W) | 14 | |
| R6 (°C/W) | 44.7 | 23.7 |
| R7 (°C/W) | 0.05 | |
| R8 (°C/W) | 0.3 | |
| C1 (W.s/°C) | 0.005 | |
| C2 (W.s/°C) | 0.008 | |
| C3 (W.s/°C) | 0.01 | |
| C4 (W.s/°C) | 0.3 | |
| C5 (W.s/°C) | 0.6 | |
| C6 (W.s/°C) | 5 | 11 |
| C7 (W.s/°C) | 0.005 | |
| C8 (W.s/°C) | 0.008 | |

4.2 PQFN - 12x12 Power lead-less thermal data

Figure 28. 12x12 Power lead-less package PC board



Note: Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 78mm x 78mm, PCB thickness=2mm, Cu thickness=35 μ m (front and back side), Copper areas: minimum pad lay-out).

Figure 29. $R_{thj-amb}$ Vs. PCB copper area in open box free air condition (one channel ON)

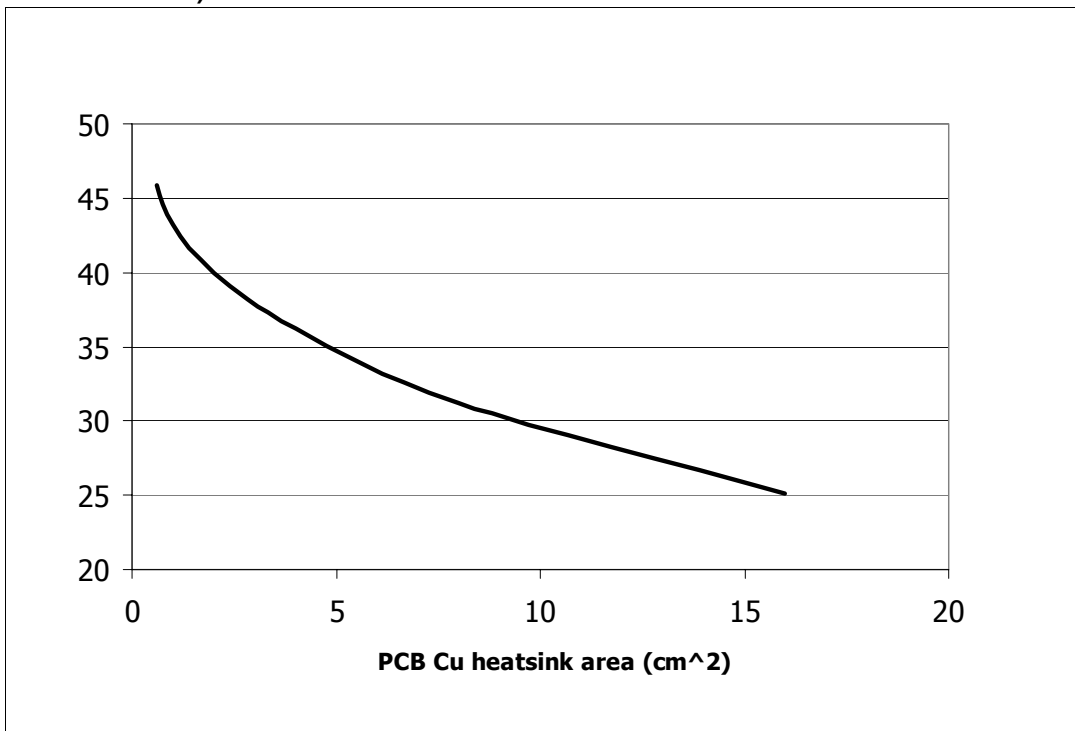


Figure 30. PQFN - 12x12 Power lead-less package thermal impedance junction ambient single pulse (one channel ON)

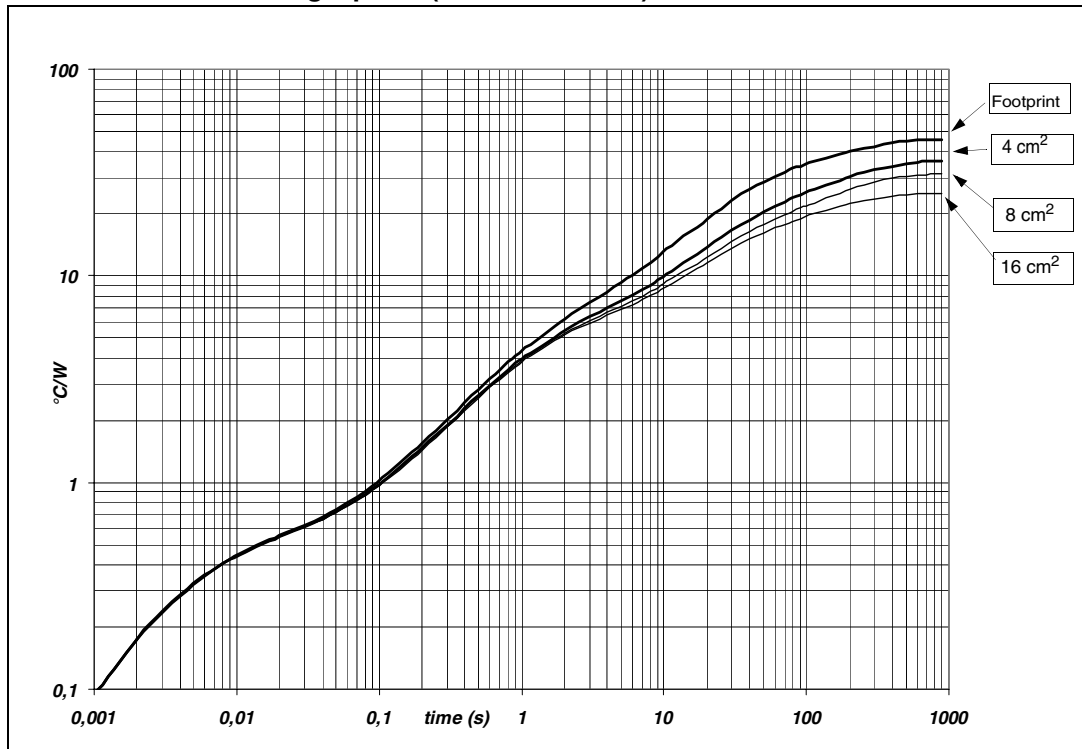
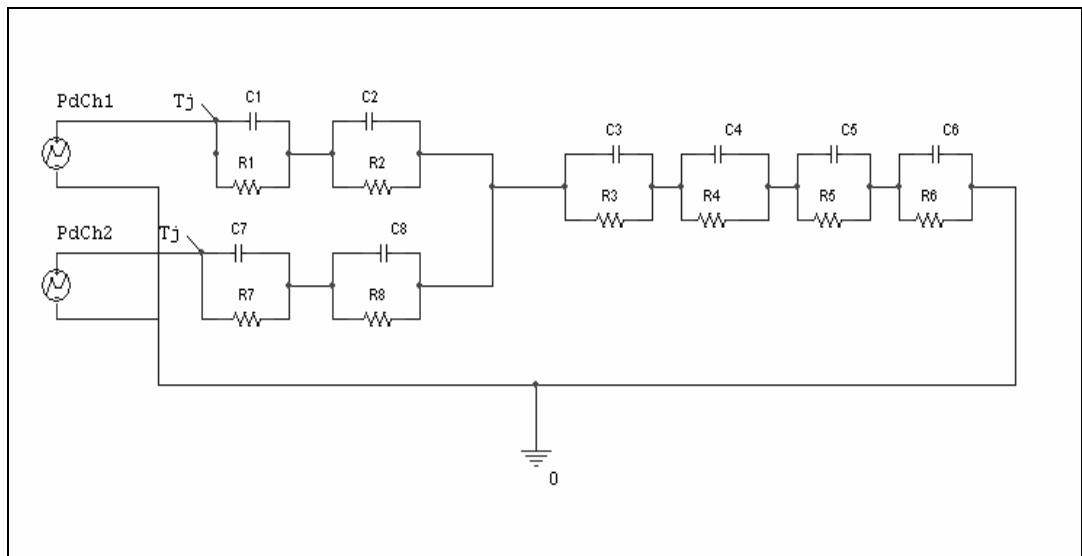


Figure 31. Thermal fitting model of a double channel HSD in PQFN - 12x12 Power lead-less^(b)



b. The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_p / T$

Table 14. Thermal parameters for PQFN - 12x12 Power lead-less

| Area/island (cm ²) | Footprint | 4 | 8 | 16 |
|--------------------------------|-----------|------|------|------|
| R1 (°C/W) | 0.3 | | | |
| R2 (°C/W) | 0.15 | | | |
| R3 (°C/W) | 4.2 | | | |
| R4 (°C/W) | 9.6 | 9.4 | 9.2 | 9 |
| R5 (°C/W) | 15.1 | 10.5 | 8.5 | 5.5 |
| R6 (°C/W) | 16.7 | 12 | 9 | 6 |
| R7 (°C/W) | 0.3 | | | |
| R8 (°C/W) | 0.15 | | | |
| C1 (W.s/°C) | 0.021 | | | |
| C2 (W.s/°C) | 0.015 | | | |
| C3 (W.s/°C) | 0.2 | | | |
| C4 (W.s/°C) | 1.9 | 2.2 | 2.32 | 2.45 |
| C5 (W.s/°C) | 2.45 | 7.3 | 13.7 | 20 |
| C6 (W.s/°C) | 11.85 | 22 | 25 | 30 |
| C7 (W.s/°C) | 0.021 | | | |
| C8 (W.s/°C) | 0.015 | | | |

5 Package and packing information

5.1 ECOPACK[®] packages

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. ECOPACK[®] packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

5.2 MultiPowerSO-30 mechanical data

Figure 32. MultiPowerSO-30 outline

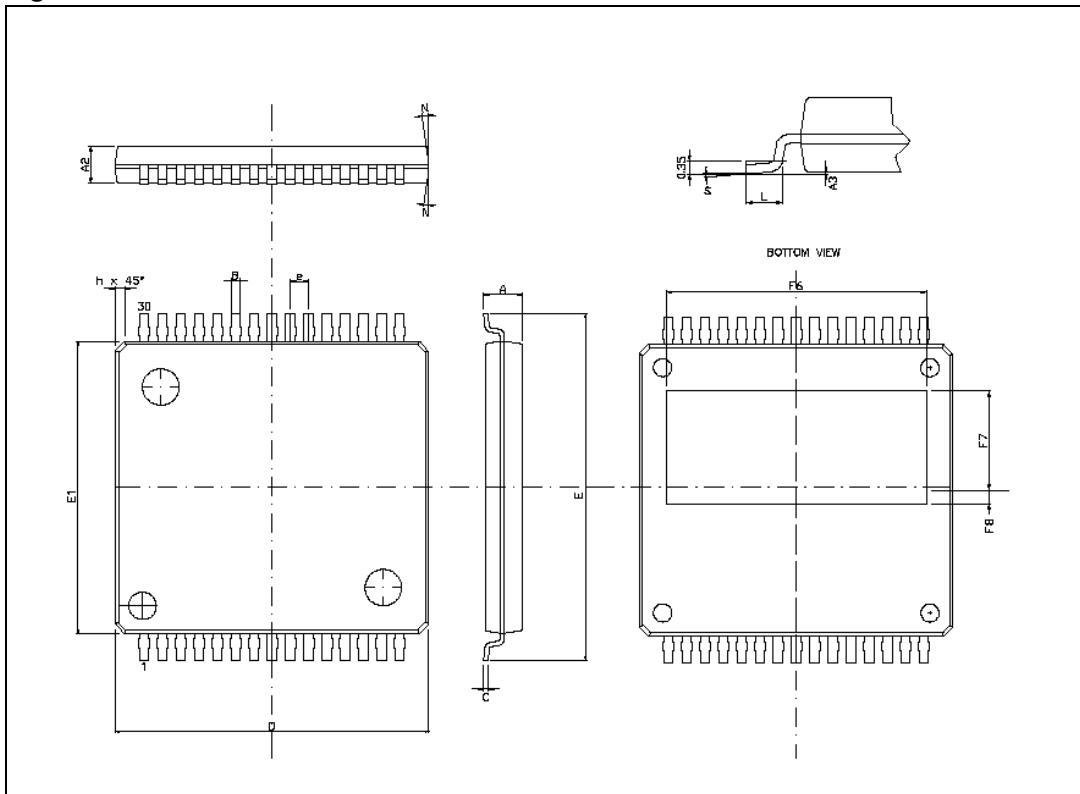


Table 15. MultiPowerSO-30 mechanical data

| Symbol | Millimeters | | |
|--------|-------------|------|--------|
| | Min. | Typ. | Max. |
| A | | | 2.35 |
| A2 | 1.85 | | 2.25 |
| A3 | 0 | | 0.1 |
| B | 0.42 | | 0.58 |
| C | 0.23 | | 0.32 |
| D | 17.1 | 17.2 | 17.3 |
| E | 18.85 | | 19.15 |
| E1 | 15.9 | 16 | 16.1 |
| "e" | 1 | | |
| F6 | | 14.3 | |
| F7 | | 5.45 | |
| F8 | | 0.73 | |
| L | 0.8 | | 1.15 |
| N | | | 10 Deg |
| S | 0 Deg | | 7 Deg |

5.3 PQFN - 12x12 Power lead-less mechanical data

Figure 33. PQFN - 12x12 Power lead-less outline

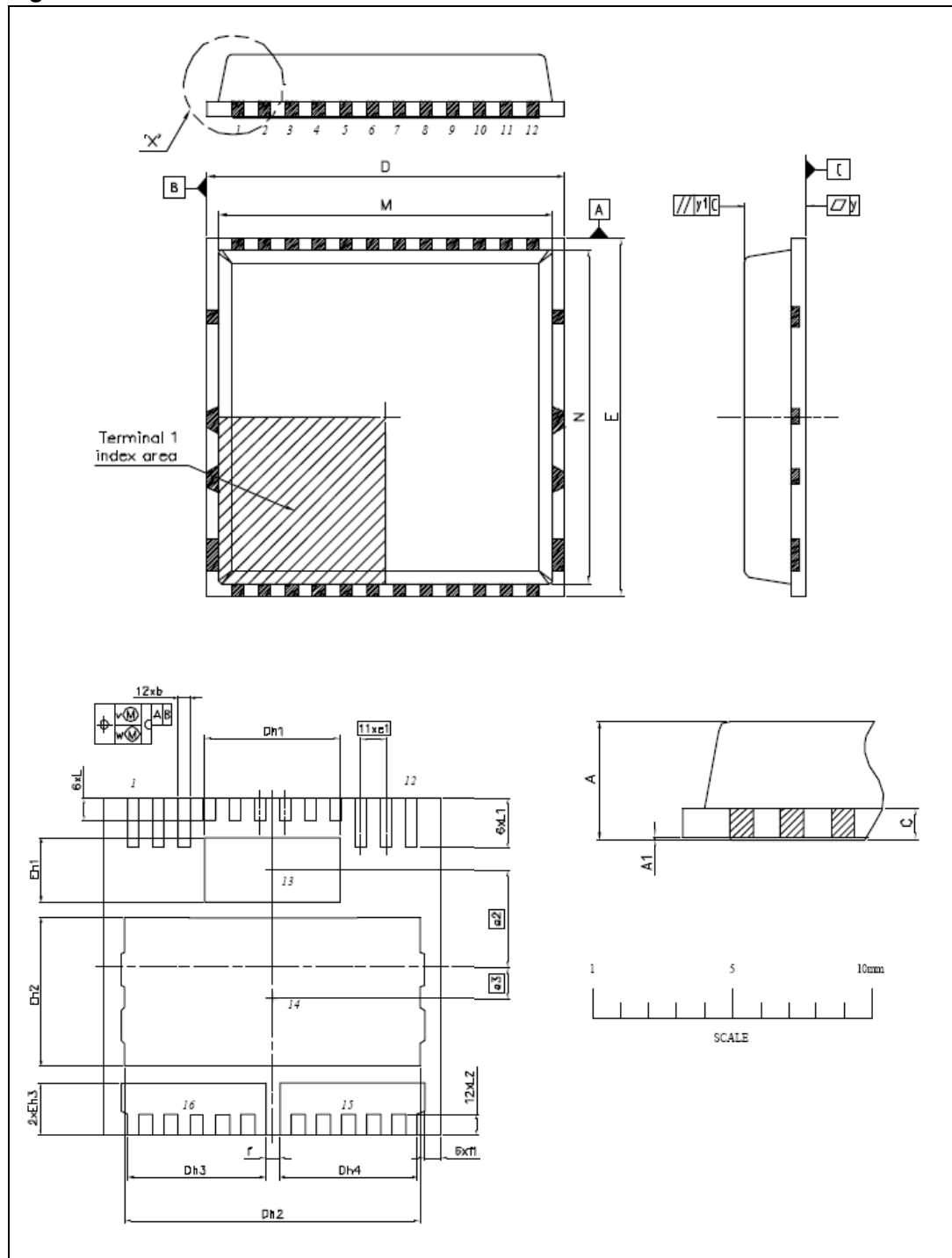


Table 16. PQFN - 12x12 Power lead-less mechanical data

| Symbol | Millimeters | | |
|--------|-------------|------|-------|
| | Min. | Typ. | Max. |
| A | 2 | | 2.2 |
| A1 | 0 | | 0.05 |
| b | 0.35 | | 0.47 |
| C | | 0.50 | |
| D | 11.90 | | 12.10 |
| Dh1 | 4.65 | | 4.95 |
| Dh2 | 10.45 | | 10.65 |
| Dh3 | 4.80 | | 5 |
| Dh4 | 4.80 | | 5 |
| E | 11.90 | | 12.10 |
| Eh1 | 2.15 | | 2.45 |
| Eh2 | 5.15 | | 5.45 |
| Eh3 | 1.70 | | 2 |
| e1 | | 0.90 | |
| e2 | | 3.45 | |
| e3 | | 1.10 | |
| f | | 0.50 | |
| f1 | | 0.60 | |
| L | 0.75 | | 0.95 |
| L1 | 1.65 | | 1.90 |
| L2 | 0.76 | | 0.78 |
| M | 11.10 | | 11.30 |
| N | 11.10 | | 11.30 |
| v | | 0.1 | |
| w | | 0.05 | |
| y | | 0.05 | |
| y1 | | 0.1 | |

5.4 MultiPowerSO-30 packing information

The devices can be packed in tube or tape and reel shipments (see the [Devices summary on page 1](#) for packaging quantities).

Figure 34. MultiPowerSO-30 tube shipment (no suffix)

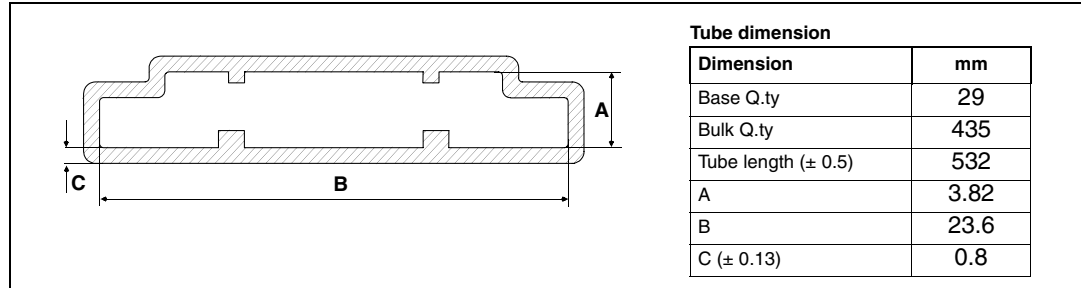
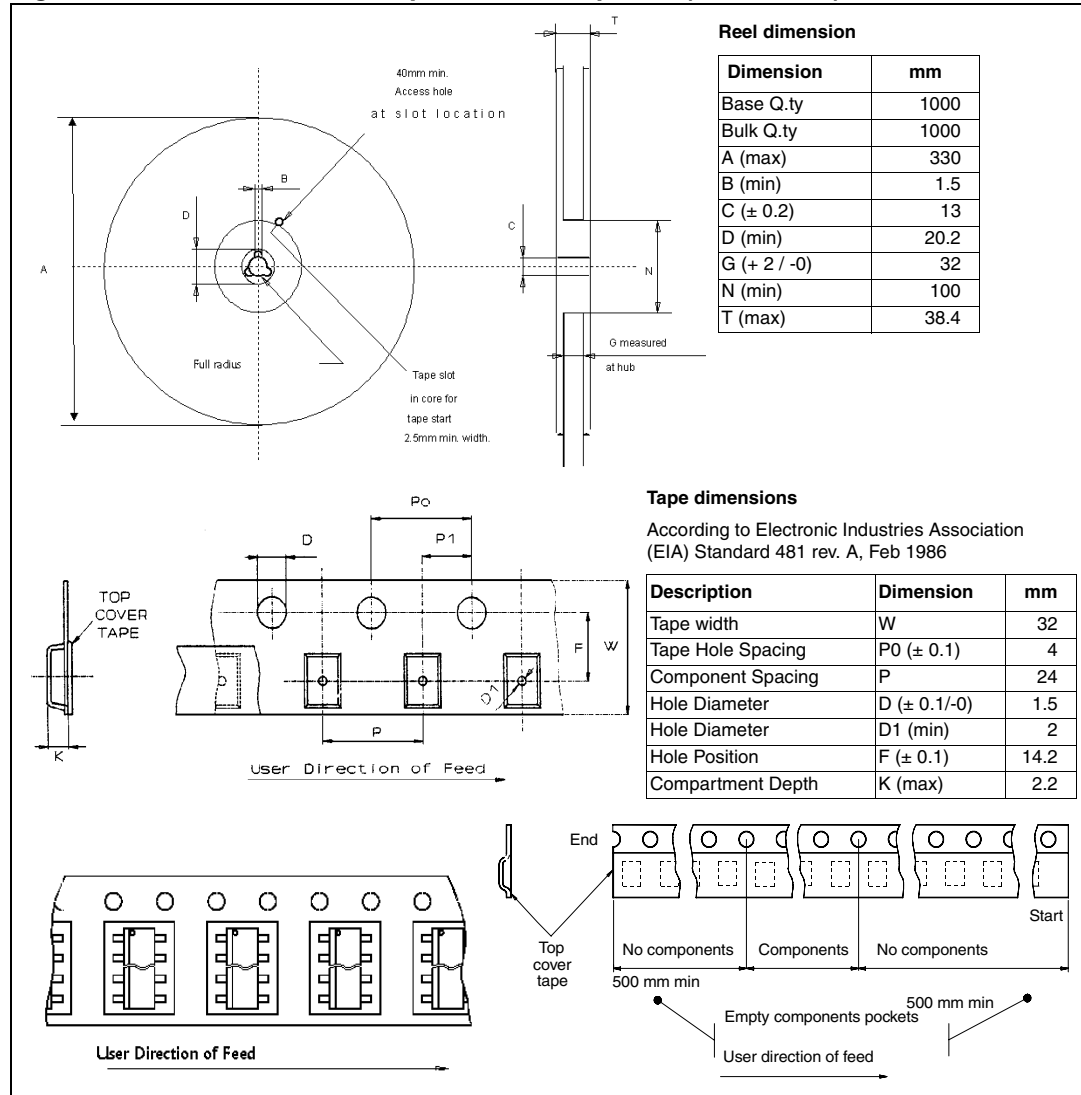


Figure 35. MultiPowerSO-30 tape and reel shipment (suffix “TR”)



5.5 PQFN - 12x12 Power lead-less packing information

The devices can be packed in tray or tape and reel shipments (see the [Devices summary on page 1](#) for packaging quantities).

Figure 36. PQFN - 12x12 Power lead-less tray shipment (no suffix)

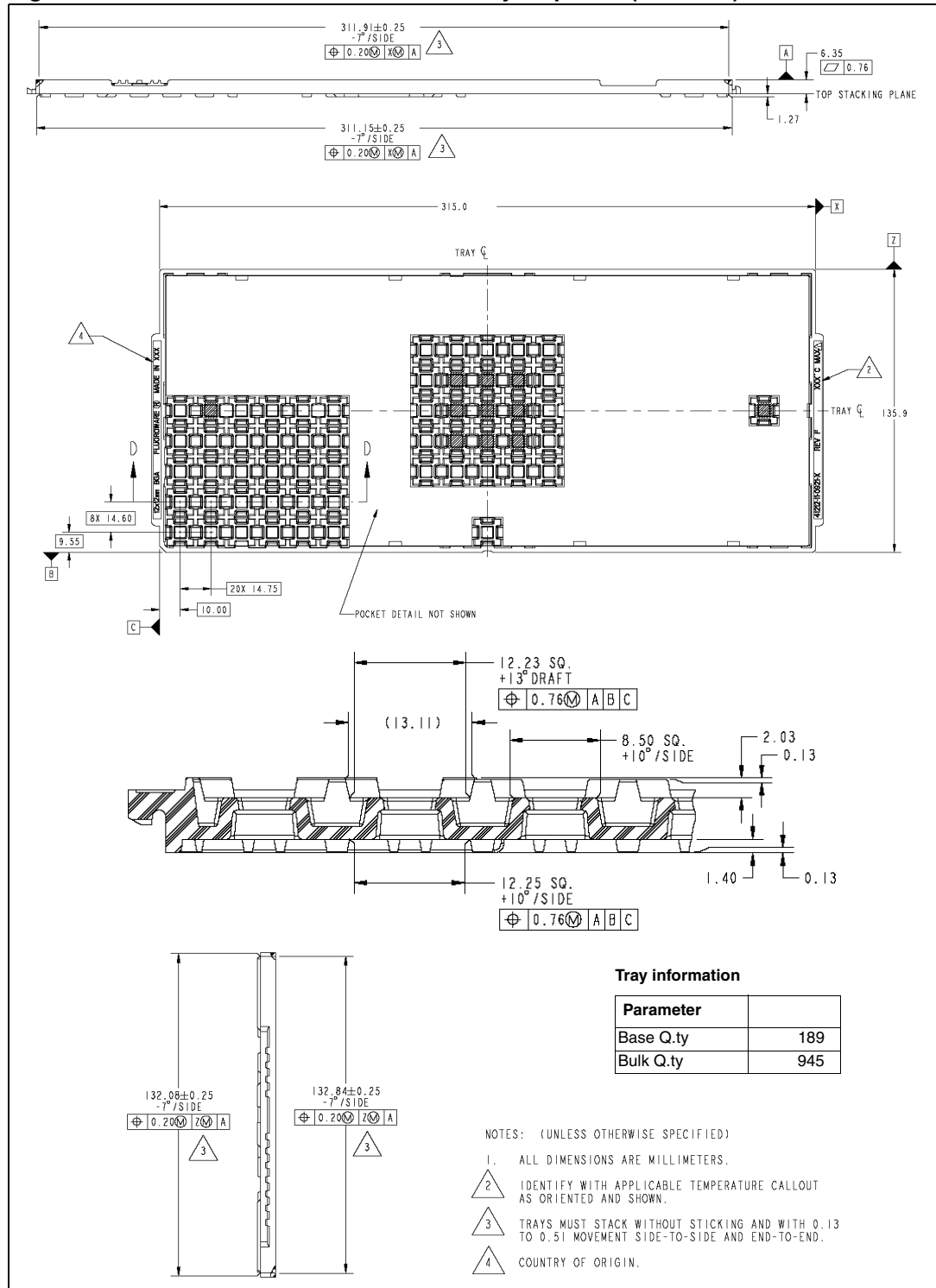
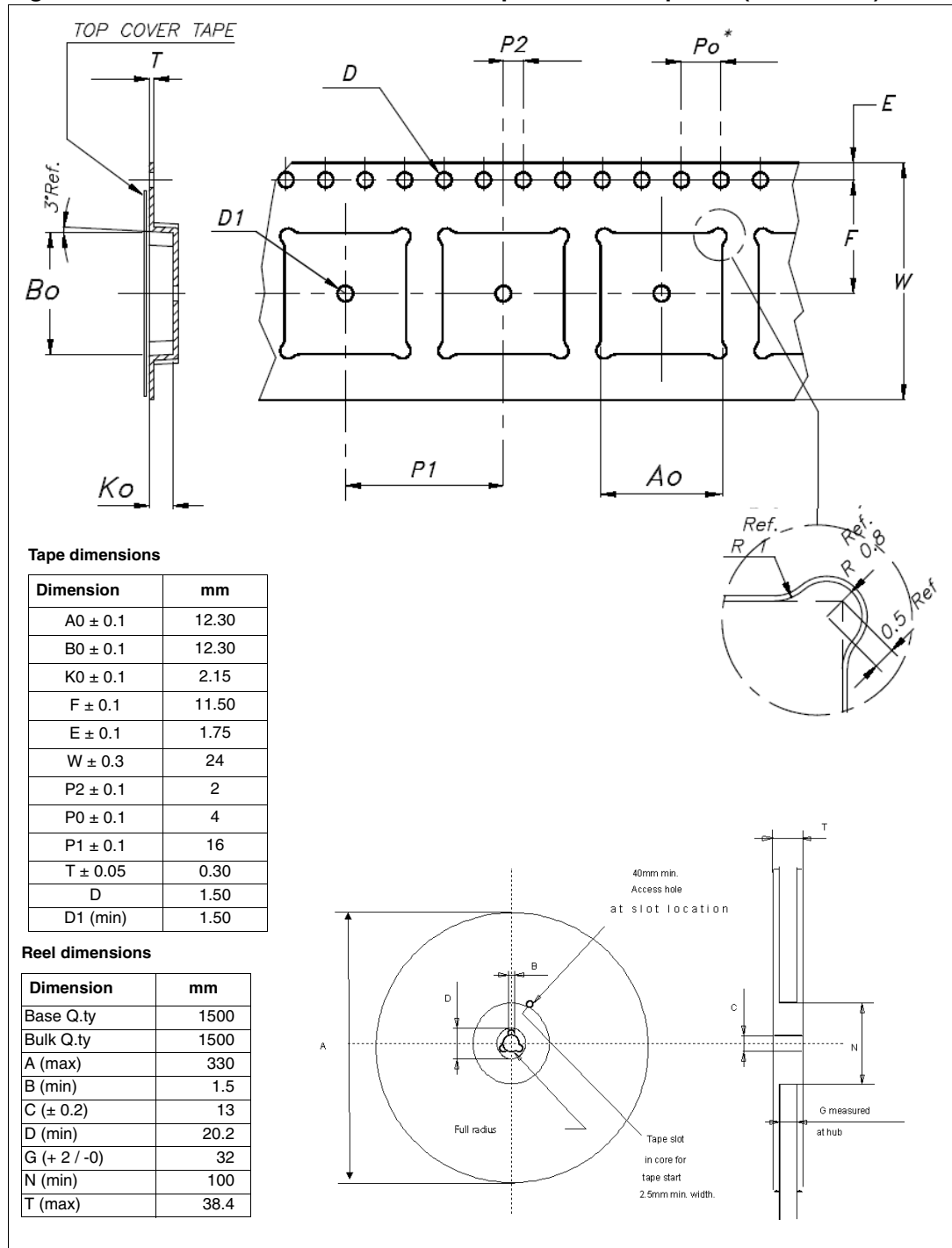


Figure 37. PQFN - 12x12 Power lead-less tape and reel shipment (suffix "TR")



6 Revision history

Table 17. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 15-Sep-2003 | 1 | Initial release. |
| 21-Jun-2004 | 2 | MultiPowerSO-30 package insertion. |
| 22-Mar-2006 | 3 | Major general update |
| 02-Jul-2007 | 4 | Document converted into new ST corporate template. Contents and lists of tables and figures added. <i>Section 3.3: Maximum demagnetization energy (VCC = 13.5V)</i> added. <i>Section 5: Package and packing information</i> updated |
| 10-Dec-2007 | 5 | <i>Table 12: Electrical transient requirements</i> - added note 3. |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2007 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com