



VNS3NV04D

“OMNIFET II”: FULLY AUTOPROTECTED POWER MOSFET

TYPE	$R_{DS(on)}$	I_{lim}	V_{clamp}
VNS3NV04D	120 m Ω (*)	3.5 A (*)	40 V (*)

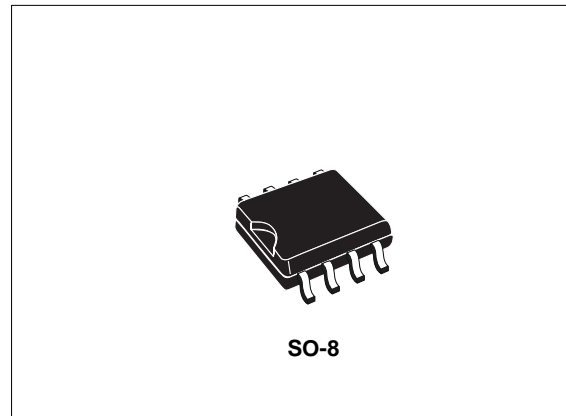
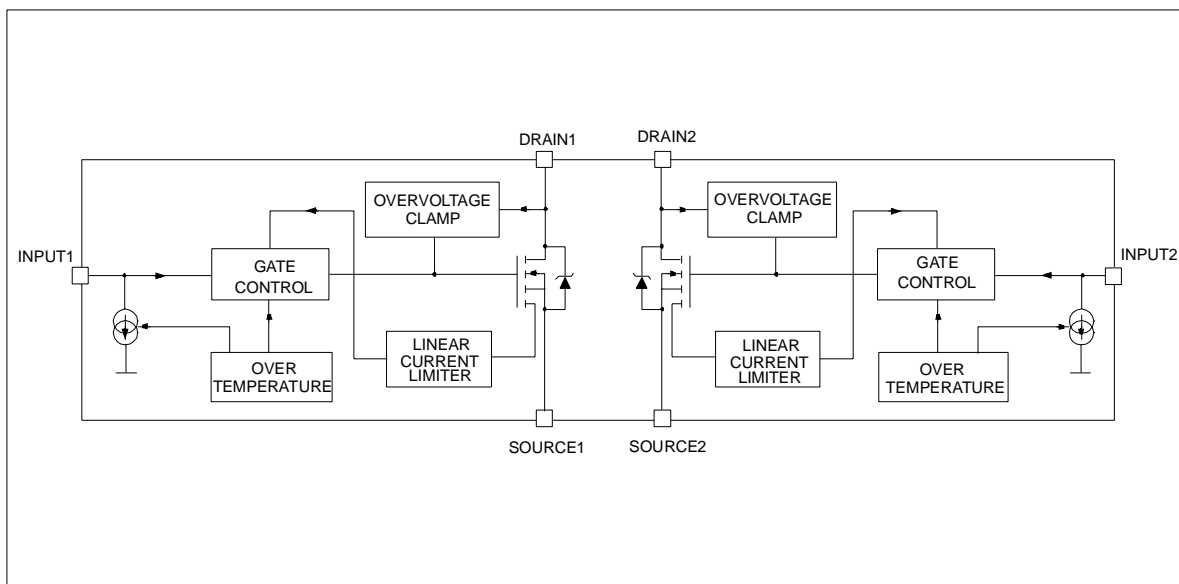
(*)Per each device

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

DESCRIPTION

The VNS3NV04D is a device formed by two monolithic OMNIFET II chips housed in a standard SO-8 package. The OMNIFET II are designed in STMicroelectronics VIPower M0-3 Technology: they are intended for replacement of standard Power MOSFETS from DC up to 50KHz

BLOCK DIAGRAM



applications. Built in thermal shutdown, linear current limitation and overvoltage clamp protects the chip in harsh environments.

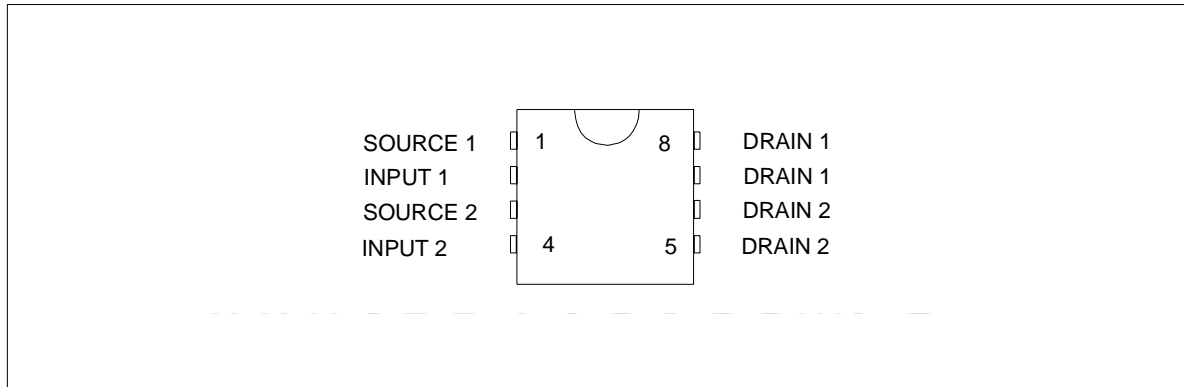
Fault feedback can be detected by monitoring the voltage at the input pin.

VNS3NV04D

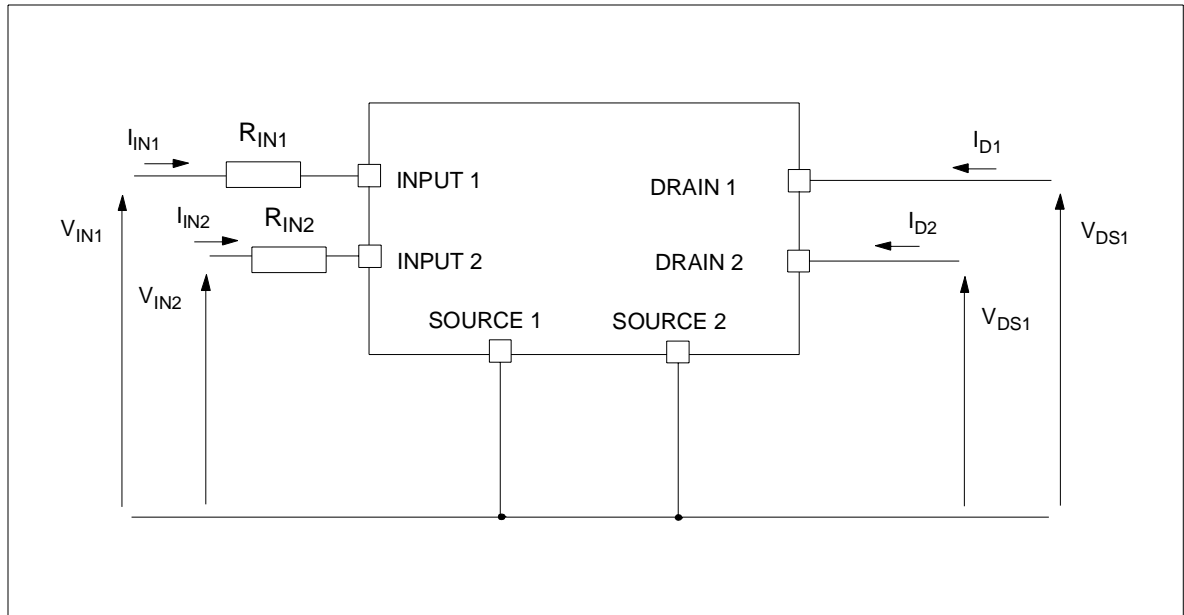
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DSn}	Drain-source Voltage ($V_{INn}=0V$)	Internally Clamped	V
V_{INn}	Input Voltage	Internally Clamped	V
I_{INn}	Input Current	+/-20	mA
$R_{IN MINn}$	Minimum Input Series Impedance	220	Ω
I_{Dn}	Drain Current	Internally Limited	A
I_{Rn}	Reverse DC Output Current	-5.5	A
V_{ESD1}	Electrostatic Discharge ($R=1.5K\Omega$, $C=100pF$)	4000	V
V_{ESD2}	Electrostatic Discharge on output pins only ($R=330\Omega$, $C=150pF$)	16500	V
P_{tot}	Total Dissipation at $T_c=25^\circ C$	4	W
T_j	Operating Junction Temperature	Internally limited	$^\circ C$
T_c	Case Operating Temperature	Internally limited	$^\circ C$
T_{stg}	Storage Temperature	-55 to 150	$^\circ C$

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th-lead}$	Thermal Resistance Junction-lead (per channel)	MAX	30
R_{th-amb}	Thermal Resistance Junction-ambient	MAX	80(*)

(*) When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 μm thick) connected to all DRAIN pins of the relative channel.

ELECTRICAL CHARACTERISTICS (-40°C < T_j < 150°C, unless otherwise specified)
(Per each device)

OFF

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V _{CLAMP}	Drain-source Clamp Voltage	V _{IN} =0V; I _D =1.5A	40	45	55	V
V _{CLTH}	Drain-source Clamp Threshold Voltage	V _{IN} =0V; I _D =2mA	36			V
V _{INTH}	Input Threshold Voltage	V _{DS} =V _{IN} ; I _D =1mA	0.5		2.5	V
I _{ISS}	Supply Current from Input Pin	V _{DS} =0V; V _{IN} =5V		100	150	μA
V _{INCL}	Input-Source Clamp Voltage	I _{IN} =1mA I _{IN} =-1mA	6 -1.0	6.8	8 -0.3	V
I _{DSS}	Zero Input Voltage Drain Current (V _{IN} =0V)	V _{DS} =13V; V _{IN} =0V; T _j =25°C V _{DS} =25V; V _{IN} =0V			30 75	μA

ON

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
R _{DS(on)}	Static Drain-source On Resistance	V _{IN} =5V; I _D =1.5A; T _j =25°C V _{IN} =5V; I _D =1.5A			120 240	mΩ

VNS3NV04D

ELECTRICAL CHARACTERISTICS (continued) ($T_j=25^\circ\text{C}$, unless otherwise specified)

DYNAMIC

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
g_{fs}^*	Forward Transconductance	$V_{DD}=13\text{V}; I_D=1.5\text{A}$		5.0		S
C_{OSS}	Output Capacitance	$V_{DS}=13\text{V}; f=1\text{MHz}; V_{IN}=0\text{V}$		150		pF

SWITCHING

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}; I_D=1.5\text{A}$		90	300	ns
t_r	Rise Time			250	750	ns
$t_{d(off)}$	Turn-off Delay Time	$V_{gen}=5\text{V}; R_{gen}=R_{IN\ MINn}=220\Omega$ (see figure 1)		450	1350	ns
t_f	Fall Time			250	750	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=15\text{V}; I_D=1.5\text{A}$		0.45	1.35	μs
t_r	Rise Time			2.5	7.5	μs
$t_{d(off)}$	Turn-off Delay Time	$V_{gen}=5\text{V}; R_{gen}=2.2\text{K}\Omega$ (see figure 1)		3.3	10.0	μs
t_f	Fall Time			2.0	6.0	μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD}=15\text{V}; I_D=1.5\text{A}$ $V_{gen}=5\text{V}; R_{gen}=R_{IN\ MINn}=220\Omega$		4.7		$\text{A}/\mu\text{s}$
Q_i	Total Input Charge	$V_{DD}=12\text{V}; I_D=1.5\text{A}; V_{IN}=5\text{V}$ $I_{gen}=2.13\text{mA}$ (see figure 5)		8.5		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{SD}^*	Forward On Voltage	$I_{SD}=1.5\text{A}; V_{IN}=0\text{V}$		0.8		V
t_{rr}	Reverse Recovery Time	$I_{SD}=1.5\text{A}; di/dt=12\text{A}/\mu\text{s}$		107		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD}=30\text{V}; L=200\mu\text{H}$		37		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, figure 2)		0.7		A

PROTECTIONS ($-40^\circ\text{C} < T_j < 150^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	Drain Current Limit	$V_{IN}=5\text{V}; V_{DS}=13\text{V}$	3.5	5	7	A
t_{dlim}	Step Response Current Limit	$V_{IN}=5\text{V}; V_{DS}=13\text{V}$		10		μs
T_{jsh}	Overtemperature Shutdown		150	175	200	$^\circ\text{C}$
T_{jrs}	Overtemperature Reset		135			$^\circ\text{C}$
I_{gf}	Fault Sink Current	$V_{IN}=5\text{V}; V_{DS}=13\text{V}; T_j=T_{jsh}$	10	15	20	mA
E_{as}	Single Pulse Avalanche Energy	starting $T_j=25^\circ\text{C}; V_{DD}=24\text{V}$ $V_{IN}=5\text{V}; R_{gen}=R_{IN\ MINn}=220\Omega; L=24\text{mH}$ (see figures 3 & 4)	100			mJ

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

PROTECTION FEATURES

During normal operation, the INPUT pin is electrically connected to the gate of the internal power MOSFET through a low impedance path.

The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50KHz. The only difference from the user's standpoint is that a small DC current I_{SS} (typ. 100 μ A) flows into the INPUT pin in order to supply the internal circuitry.

The device integrates:

- **OVERVOLTAGE CLAMP PROTECTION:** internally set at 45V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.

- **LINEAR CURRENT LIMITER CIRCUIT:** limits the drain current I_D to I_{lim} whatever the INPUT pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

- **OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:** these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190 °C, a typical value being 170 °C. The device is automatically restarted when the chip temperature falls of about 15°C below shut-down temperature.

- **STATUS FEEDBACK:** in the case of an overtemperature fault condition ($T_j > T_{jsh}$), the device tries to sink a diagnostic current I_{gf} through the INPUT pin in order to indicate fault condition. If driven from a low impedance source, this current may be used in order to warn the control circuit of a device shutdown. If the drive impedance is high enough so that the INPUT pin driver is not able to supply the current I_{gf} , the INPUT pin will fall to 0V. **This will not however affect the device operation: no requirement is put on the current capability of the INPUT pin driver except to be able to supply the normal operation drive current I_{SS} .**

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit.

Fig.1: Switching Time Test Circuit for Resistive Load

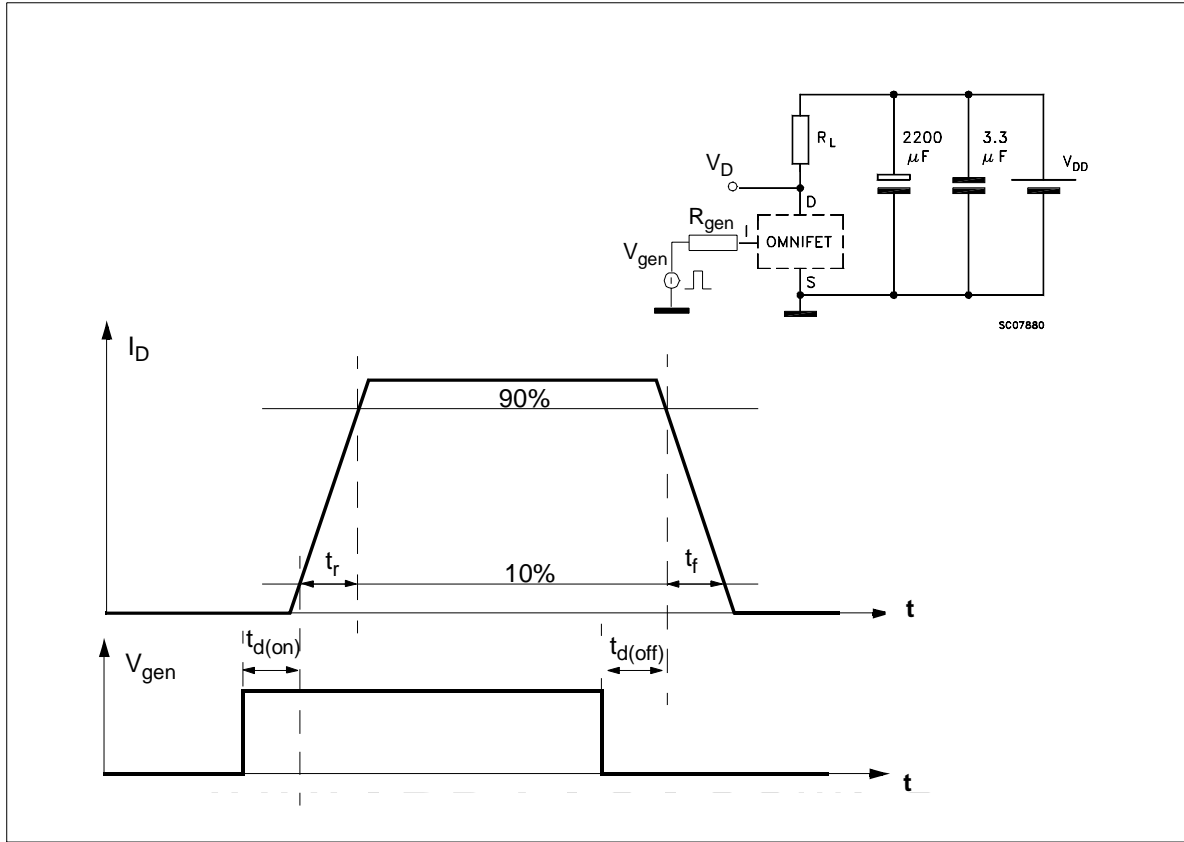


Fig.2: Test Circuit for Diode Recovery Times

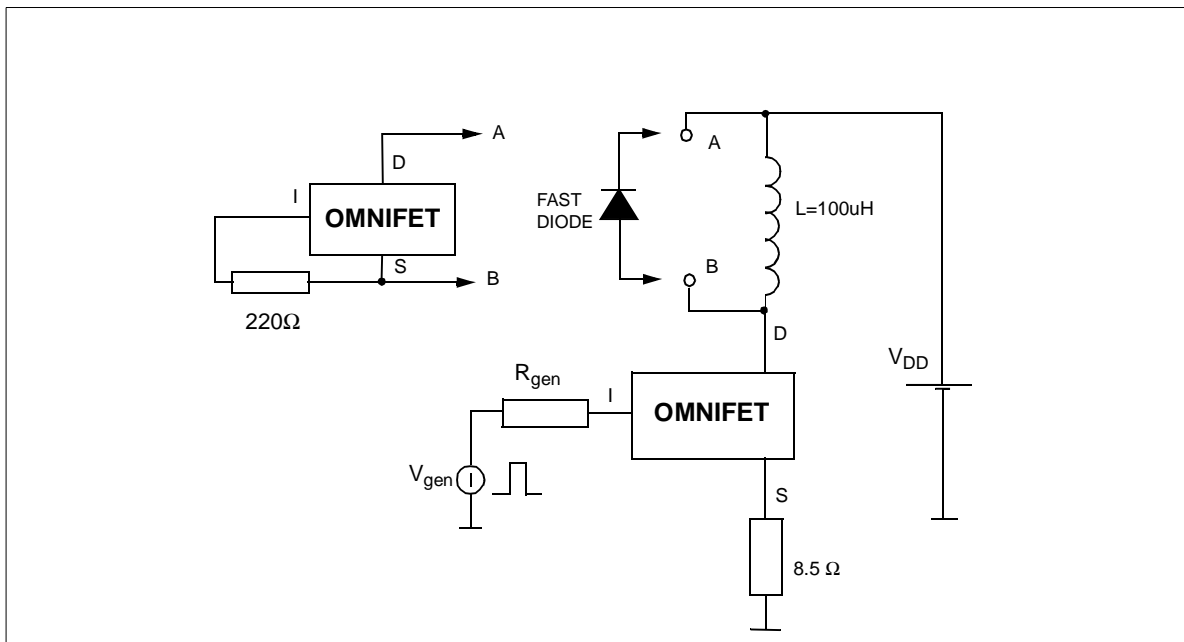


Fig. 3: Unclamped Inductive Load Test Circuits

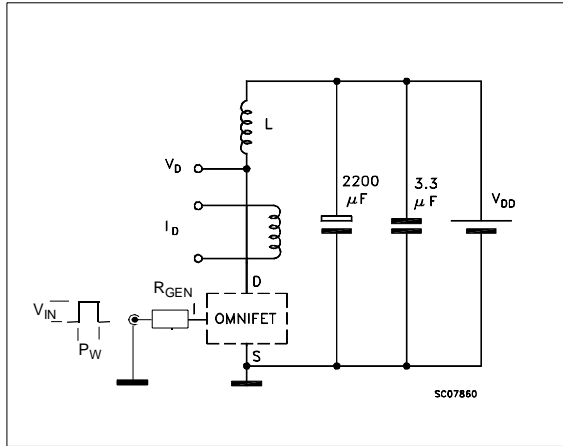


Fig. 4: Unclamped Inductive Waveforms

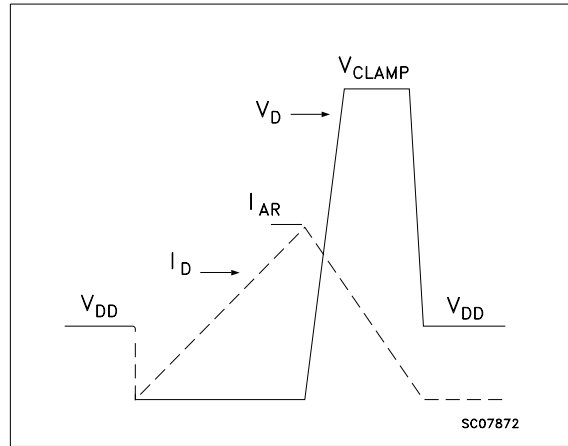
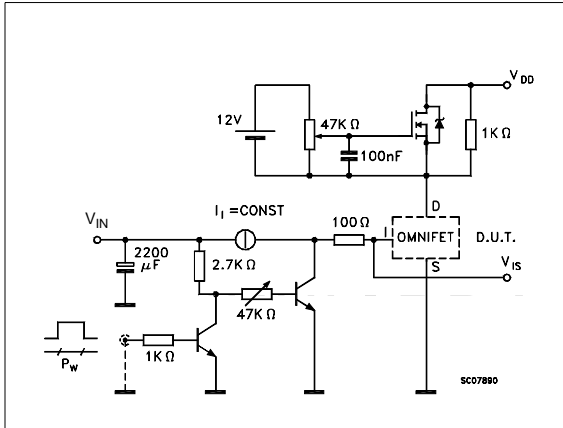
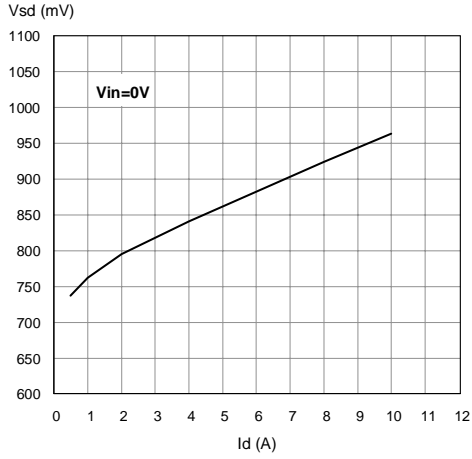


Fig. 5: Input Charge Test Circuit

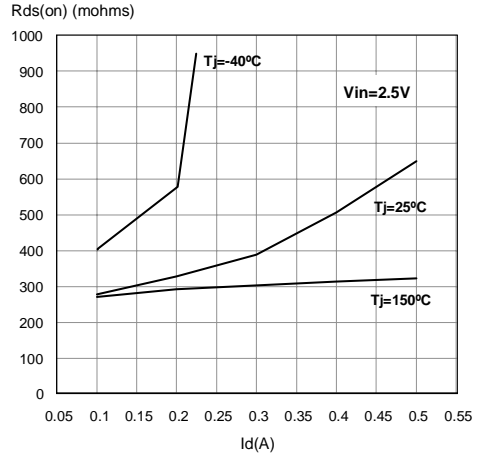


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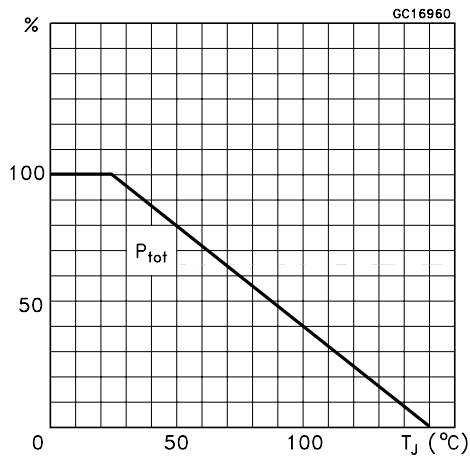
Source-Drain Diode Forward Characteristics



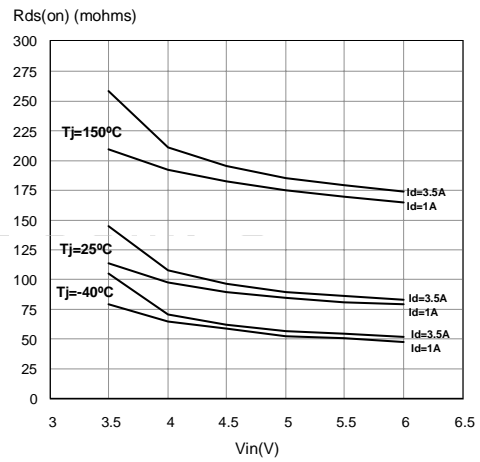
Static Drain Source On Resistance



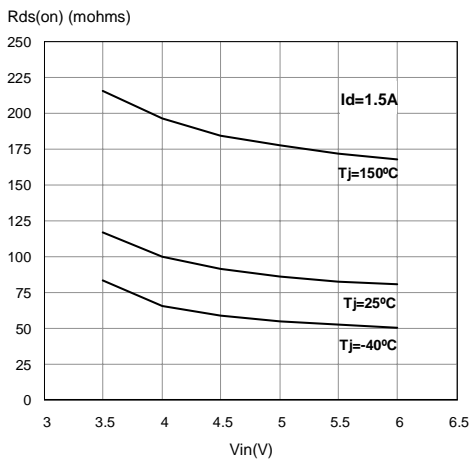
Derating Curve



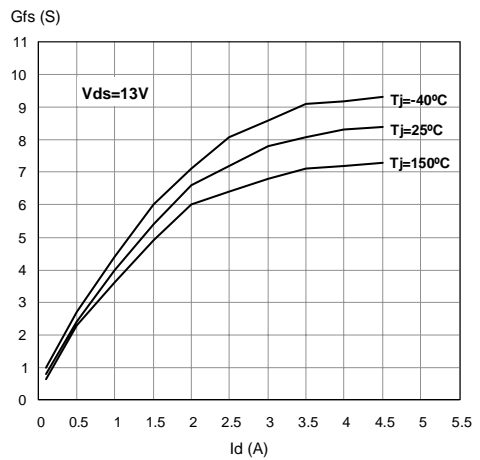
Static Drain-Source On resistance Vs. Input Voltage



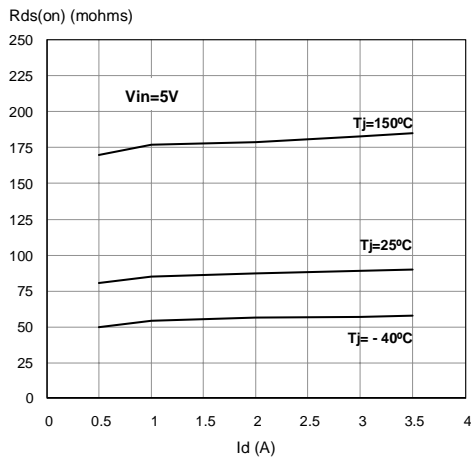
Static Drain-Source On resistance Vs. Input Voltage



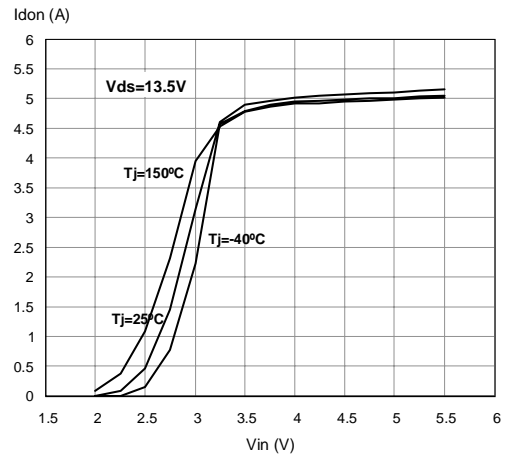
Transconductance



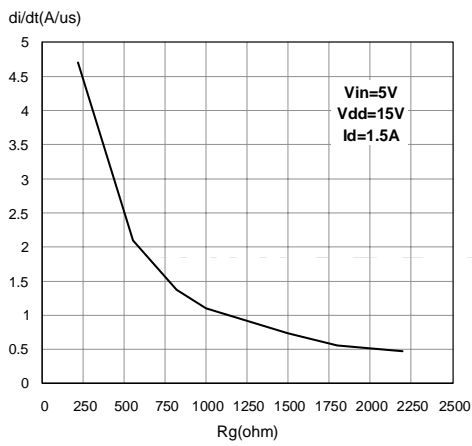
Static Drain-Source On Resistance Vs. Id



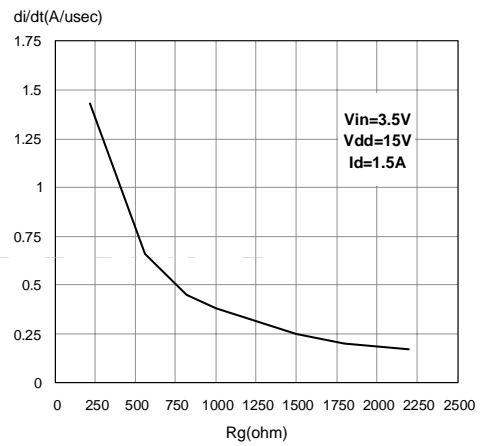
Transfer Characteristics



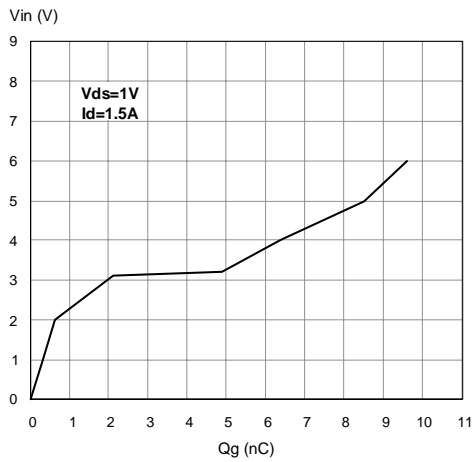
Turn On Current Slope



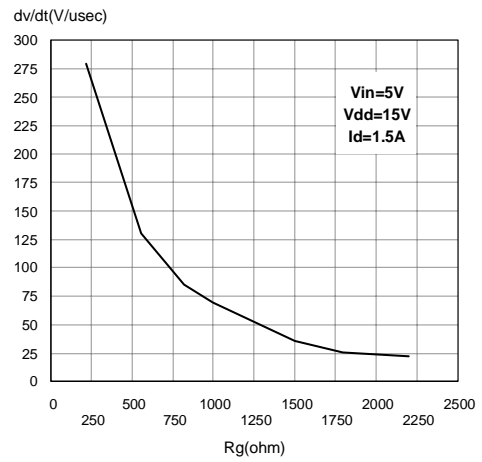
Turn On Current Slope



Input Voltage Vs. Input Charge

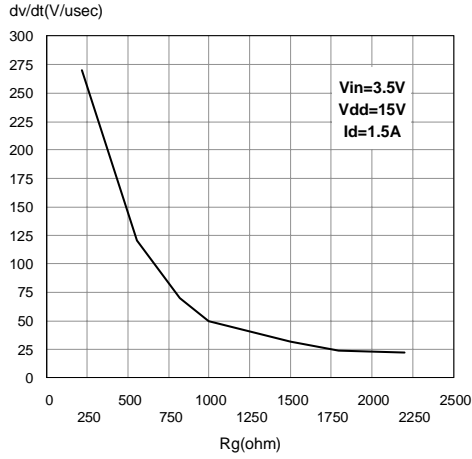


Turn off drain source voltage slope

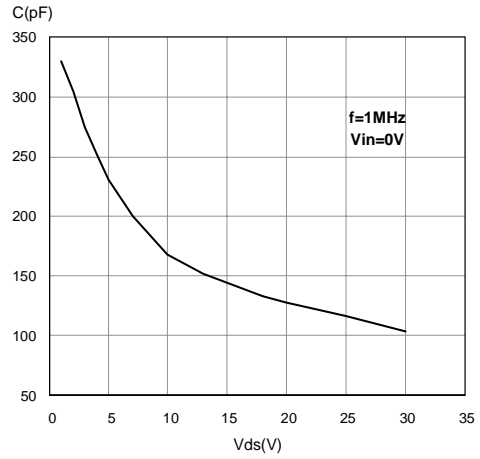


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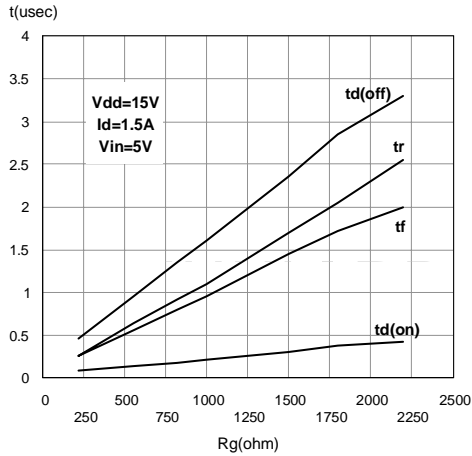
Turn Off Drain-Source Voltage Slope



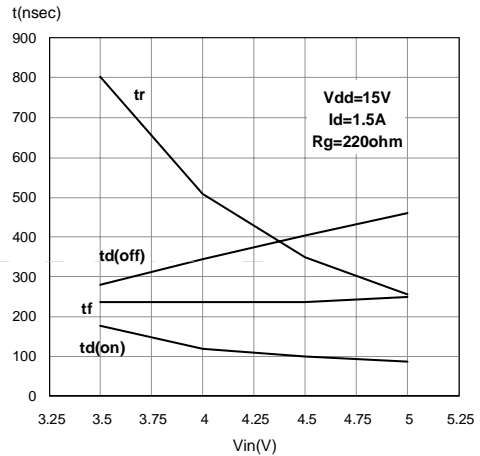
Capacitance Variations



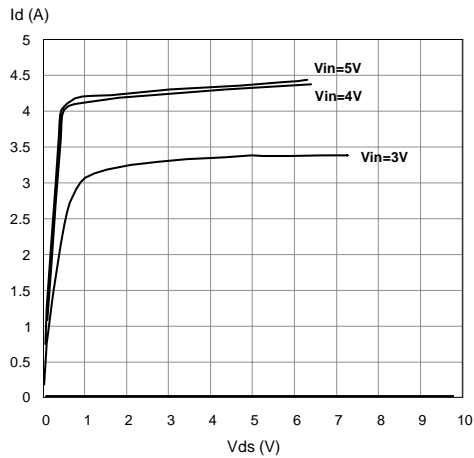
Switching Time Resistive Load



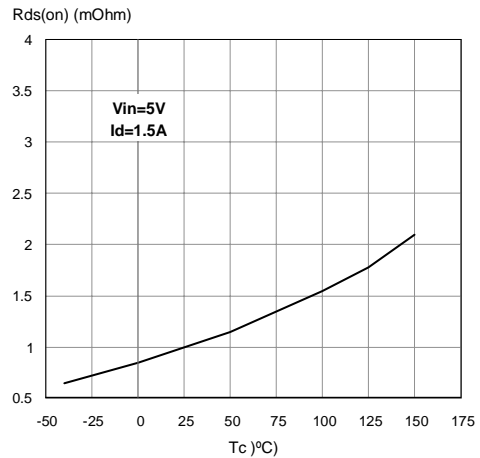
Switching Time Resistive Load



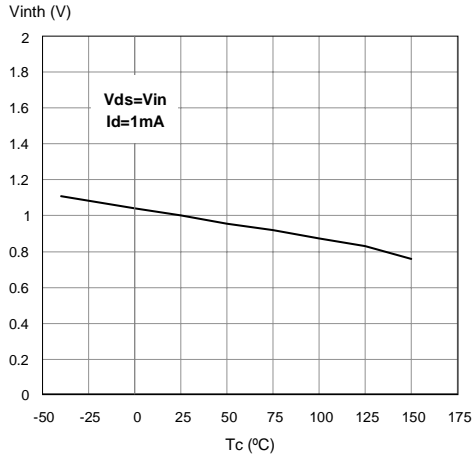
Output Characteristics



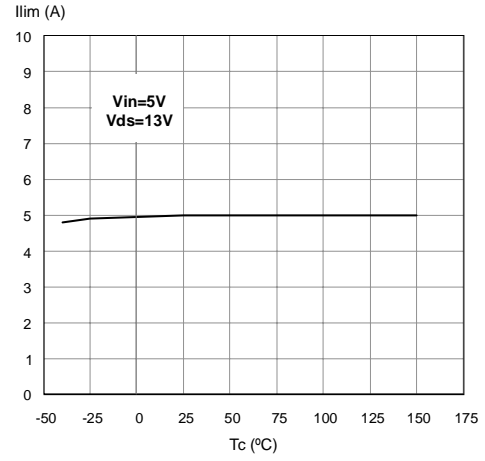
Normalized On Resistance Vs. Temperature



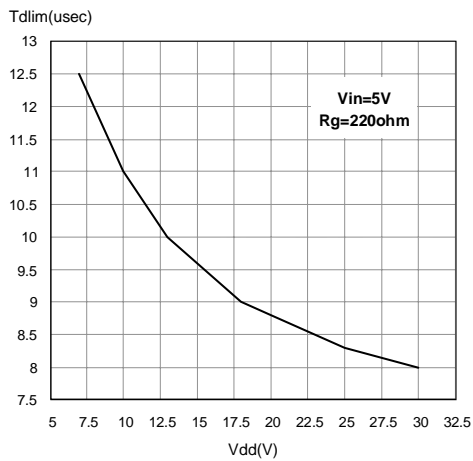
Normalized Input Threshold Voltage Vs. Junction Temperature



Normalized Current Limit Vs. Junction Temperature

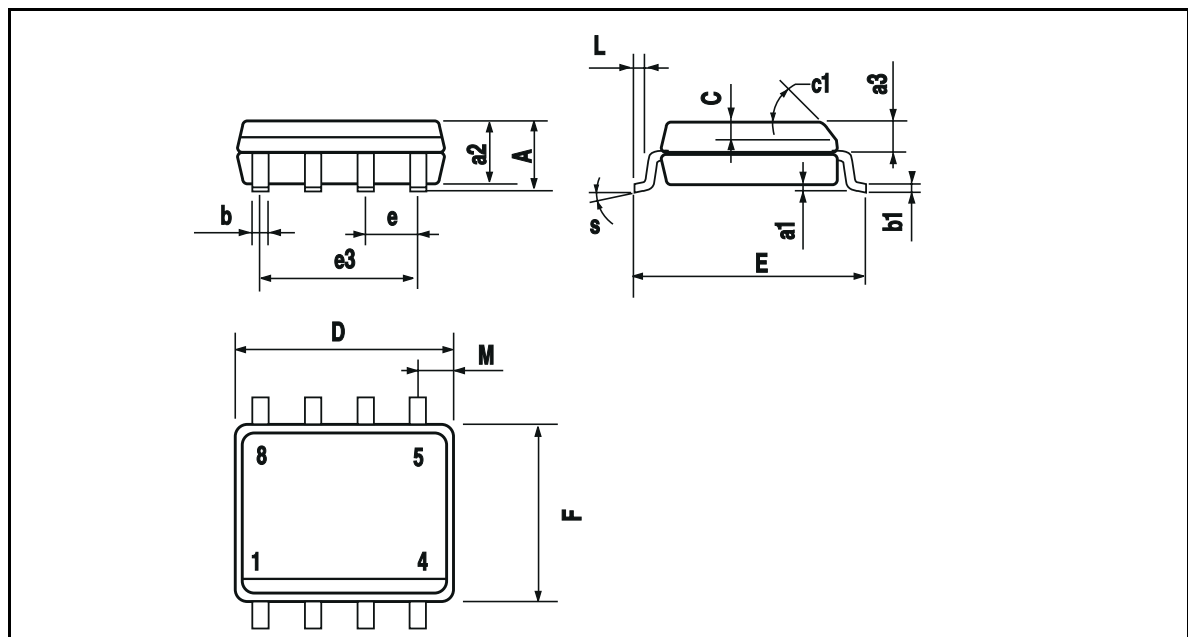


Step Response Current Limit

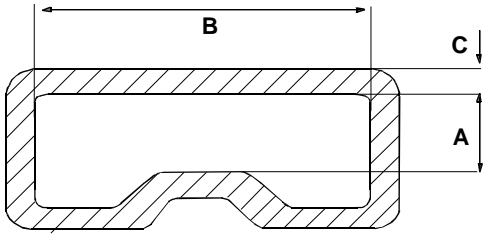


SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
F	8 (max.)					



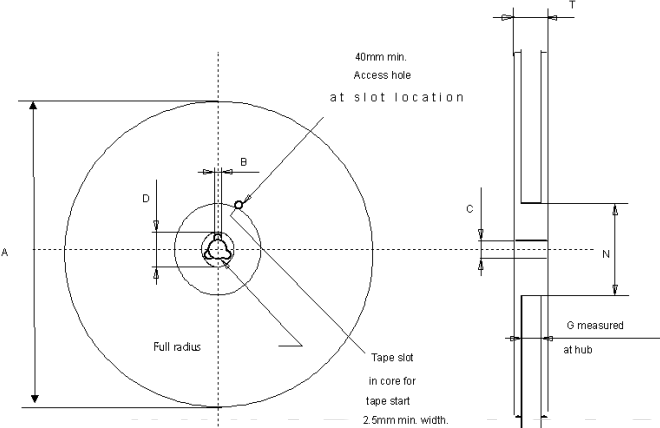
SO-8 TUBE SHIPMENT (no suffix)



Base Q.ty	100
Bulk Q.ty	2000
Tube length (± 0.5)	532
A	3.2
B	6
C (± 0.1)	0.6

All dimensions are in mm.

TAPE AND REEL SHIPMENT (suffix "13TR")



Base Q.ty	2500
Bulk Q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	12.4
N (min)	60
T (max)	18.4

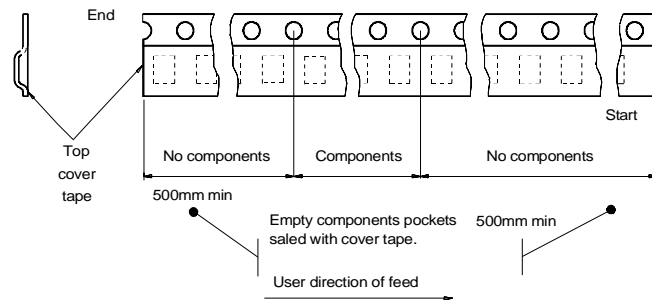
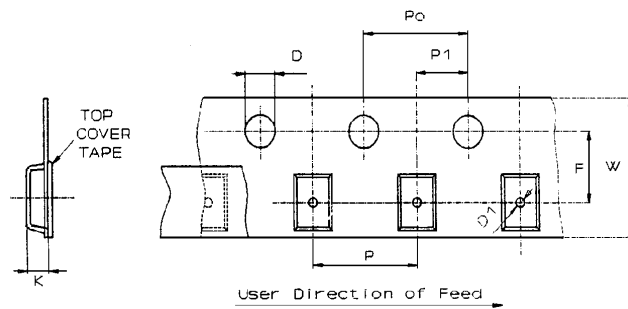
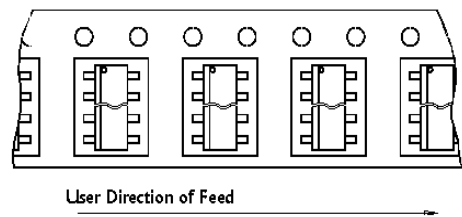
All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	12
Tape Hole Spacing	P0 (± 0.1)	4
Component Spacing	P	8
Hole Diameter	D (± 0.1/-0)	1.5
Hole Diameter	D1 (min)	1.5
Hole Position	F (± 0.05)	5.5
Compartment Depth	K (max)	4.5
Hole Spacing	P1 (± 0.1)	2

All dimensions are in mm.



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