# 具有双倍速率低压差分信号(DDR LVDS)和 CMOS 输出的14 位，65每秒百万次采样(MSPS)模数转换器(ADC)

查询样品: ADS6142-HT

## 特性

- 最大采样率
- 无丢码的**14**位分辨率
- 用于信噪比**(SNR)/**无杂散动态范围**(SFDR)**权衡的**3.5dB**粗调增益和最高**6dB**可编程微调增益
- 并行**CMOS**和双倍速率**(DDR) LVDS**输出选项
- 支持正弦，低压**COMS(LVCOMS)**，低电压正射极耦合逻辑**(LVPECL)**，**LVDS**时钟输入，和时钟振幅低至**400mV$_{PP}$**
- 时钟占空比稳定器
- 支持外部基准的内部基准
- 无需为基准提供外部退偶装置
- 可编程输出时钟位置和数据捕捉的驱动强度
- **3.3V**模拟和**1**数字电源

## 应用范围

- 潜孔钻孔
- 高温环境
- 无线通信基础设施
- 软件定义无线电
- 功率放大器线性化
- **802.16d/e**
- 测试和测量仪器
- 高清音频
- 医疗成像
- 雷达系统

## 支持极端温度环境下的应用

- 受控基线
- 一个组装**/**测试场所
- 一个制造场所
- 可在极端温度范围内**(–40°C/210°C)**工作(1)
- 延长的产品使用寿命周期
- 延长产品的变更通知周期
- 产品可追溯性
- 德州仪器高温产品利用高度优化的硅（芯片）解决方案，此解决方案对设计和制造工艺进行了提升以在拓展的温度范围内大大地提高性能。 所有器件可在最大额定温度下连续运行**1000**小时。

(1) 可定制温度范围

## 说明

ADS6142是一款高性能和低功率耗散14位模拟/数字(A/D)转换器，此转换器采样频率为65每秒百万次采样(MSPS)。 即使在高输入频率下，一个内部高带宽采样和保持以及一个低抖动时钟缓冲器可帮助实现高信噪比(SNR)和宽无杂散动态范围(SFDR)。

ADS6142特有粗调和微调增益选项，在较低全幅模拟输入范围内，可改进SFDR性能。

此数字输出是并行CMOS或者是DDR(双倍速率)LVDS。 有几个特性可以使数据捕捉更加容易 - 输出时钟位置的控制和输出缓冲器驱动能力，LVDS电流，和内部终止可编程性。

输出接口类型，增益，和其它功能可使用3线制串口进行编程。 或者，可使用专用并行引脚对一些功能进行配置，因此此器件驱动到所需状态。

ADS6142在包含内部基准的同时去除了传统的基准引脚和相关的外部退偶装置。 也支持外部基准模式。

ADS6142可在极端温度范围(–40°C至 210°C)内工作。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

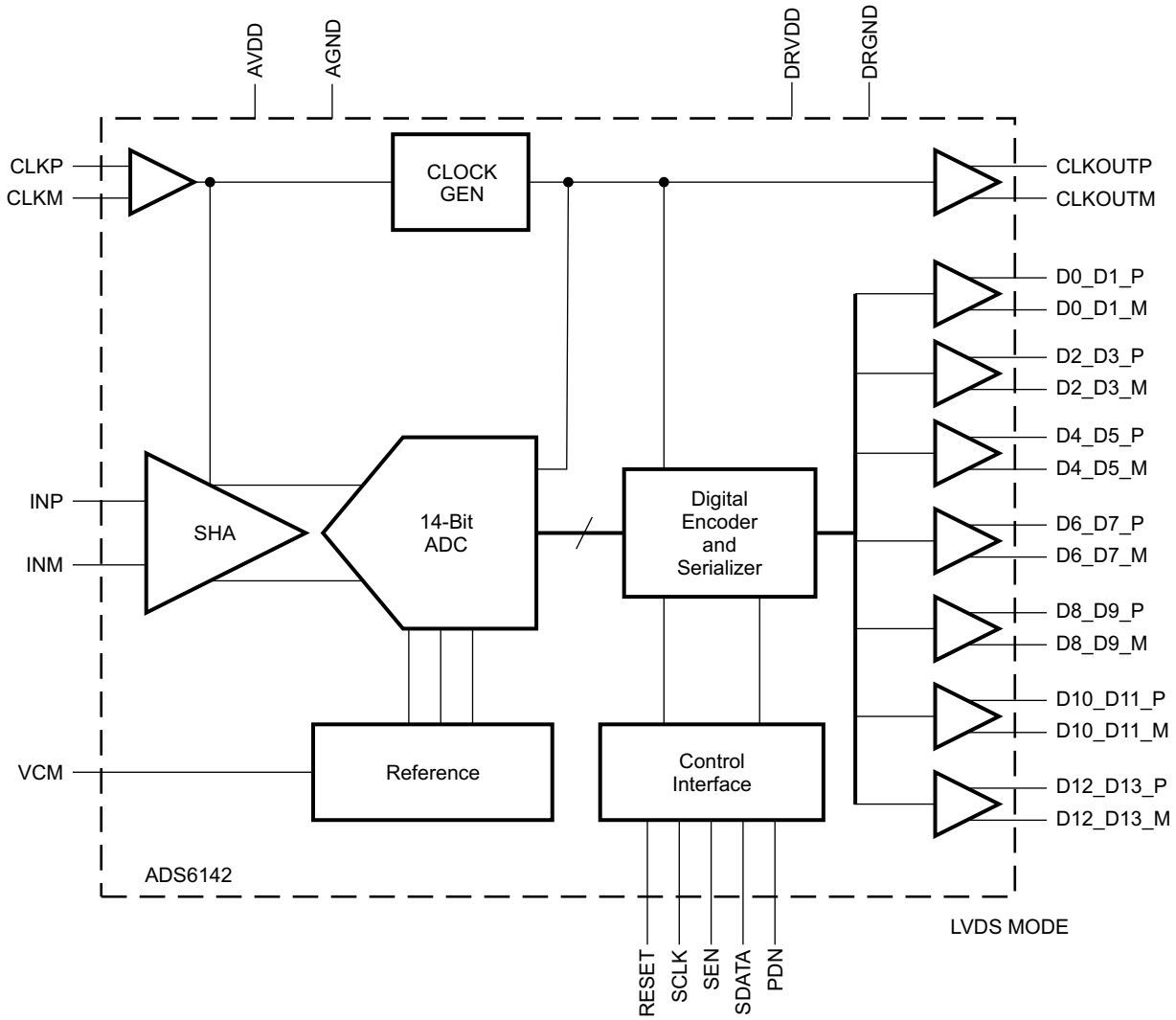



**Table 1. ORDERING INFORMATION(1)**

| TA | PACKAGE(2) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|
| –40°C to 210°C | KGD (bare die) | ADS6142SKGD1 | NA |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## BARE DIE INFORMATION

| DIE SIZE | DIE PAD SIZE | DIE PAD COORDINATES | DIE THICKNESS | BACKSIDE FINISH | BACKSIDE POTENTIAL | BOND PAD METALLIZATION COMPOSITION | BOND PAD THICKNESS |
|---|---|---|---|---|---|---|---|
| 2715 x 2460 µm<br>96.85 x 106.89 mils | 70 x 70 µm | See Table 2 | 11 mils | Silicon with backgrind | DRVSS | Ti/Al-Cu/TiN | 1100 nm |

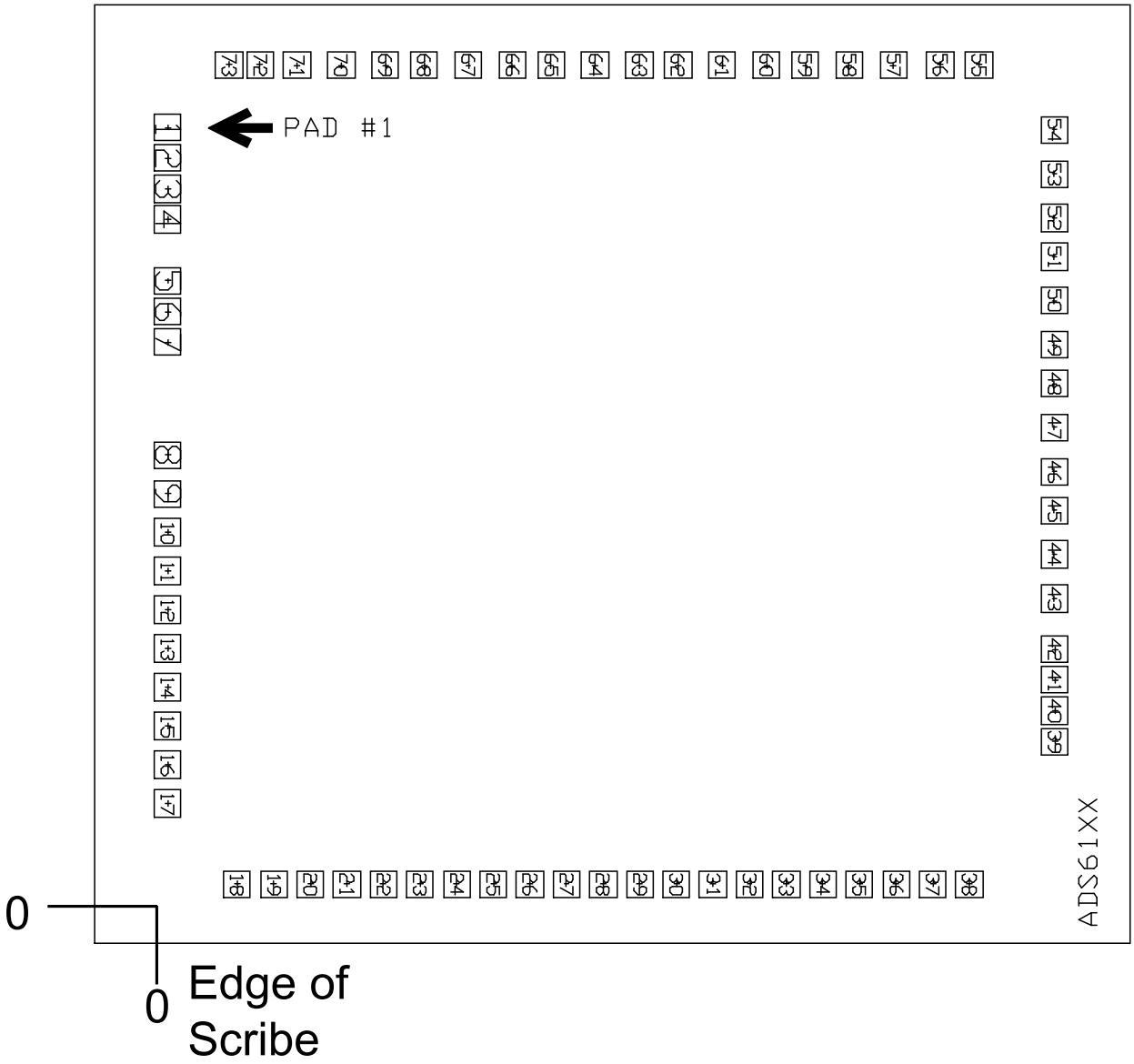


**Table 2. BOND PAD COORDINATES**

| DESCRIPTION | PAD NUMBER | X MIN | Y MIN | X MAX | Y MAX |
|---|---|---|---|---|---|
| DRVDD | 1 | 80.92 | 2065 | 150.92 | 2135 |
| N/C | 2 | 80.92 | 1984.5 | 150.92 | 2054.5 |
| N/C | 3 | 80.92 | 1904 | 150.92 | 1974 |
| RESET | 4 | 80.92 | 1823.5 | 150.92 | 1893.5 |
| SCLK | 5 | 80.92 | 1662.5 | 150.92 | 1732.5 |
| SDATA | 6 | 80.92 | 1582 | 150.92 | 1652 |
| SEN | 7 | 80.92 | 1501.5 | 150.92 | 1571.5 |
| N/C | 8 | 80.92 | 1206.1 | 150.92 | 1276.1 |
| N/C | 9 | 80.92 | 1104.6 | 150.92 | 1174.6 |
| AGND | 10 | 80.92 | 1003.1 | 150.92 | 1073.1 |
| AGND | 11 | 80.92 | 901.6 | 150.92 | 971.6 |
| AGND | 12 | 80.92 | 800.1 | 150.92 | 870.1 |
| CLKP | 13 | 80.92 | 698.6 | 150.92 | 768.6 |
| CLKP | 14 | 80.92 | 597.1 | 150.92 | 667.1 |
| CLKM | 15 | 80.92 | 495.6 | 150.92 | 565.6 |
| CLKM | 16 | 80.92 | 394.1 | 150.92 | 464.1 |
| N/C | 17 | 80.92 | 292.6 | 150.92 | 362.6 |
| N/C | 18 | 262.5 | 80.92 | 332.5 | 150.92 |
| AGND | 19 | 358.365 | 80.92 | 428.365 | 150.92 |
| AGND | 20 | 454.23 | 80.92 | 524.23 | 150.92 |
| N/C | 21 | 550.095 | 80.92 | 620.095 | 150.92 |
| INP | 22 | 645.96 | 80.92 | 715.96 | 150.92 |
| INP | 23 | 741.825 | 80.92 | 811.825 | 150.92 |
| INM | 24 | 837.69 | 80.92 | 907.69 | 150.92 |
| INM | 25 | 933.555 | 80.92 | 1003.555 | 150.92 |
| N/C | 26 | 1029.42 | 80.92 | 1099.42 | 150.92 |
| AGND | 27 | 1125.285 | 80.92 | 1195.285 | 150.92 |
| AGND | 28 | 1221.15 | 80.92 | 1291.15 | 150.92 |
| N/C | 29 | 1317.015 | 80.92 | 1387.015 | 150.92 |
| AVDD | 30 | 1412.88 | 80.92 | 1482.88 | 150.92 |
| AVDD | 31 | 1508.745 | 80.92 | 1578.745 | 150.92 |
| VCM | 32 | 1604.61 | 80.92 | 1674.61 | 150.92 |
| VCM | 33 | 1700.475 | 80.92 | 1770.475 | 150.92 |
| N/C | 34 | 1796.34 | 80.92 | 1866.34 | 150.92 |
| N/C | 35 | 1892.205 | 80.92 | 1962.205 | 150.92 |
| N/C | 36 | 1988.07 | 80.92 | 2058.07 | 150.92 |
| AVDD | 37 | 2083.935 | 80.92 | 2153.935 | 150.92 |
| PDN | 38 | 2179.8 | 80.92 | 2249.8 | 150.92 |
| N/C | 39 | 2404.08 | 455 | 2474.08 | 525 |
| N/C | 40 | 2404.08 | 535.5 | 2474.08 | 605.5 |
| N/C | 41 | 2404.08 | 616 | 2474.08 | 686 |
| N/C | 42 | 2404.08 | 696.5 | 2474.08 | 766.5 |
| D0 | 43 | 2402.925 | 829.71 | 2472.925 | 899.71 |
| N/C | 44 | 2402.925 | 945.28 | 2472.925 | 1015.28 |
| D1 | 45 | 2402.925 | 1060.85 | 2472.925 | 1130.85 |
| D2 | 46 | 2402.925 | 1162.21 | 2472.925 | 1232.21 |
| SUBST | 47 | 2402.925 | 1277.78 | 2472.925 | 1347.78 |

**Table 2. BOND PAD COORDINATES (continued)**

| DESCRIPTION | PAD NUMBER | X MIN | Y MIN | X MAX | Y MAX |
|---|---|---|---|---|---|
| D3 | 48 | 2402.925 | 1393.35 | 2472.925 | 1463.35 |
| D4 | 49 | 2402.925 | 1494.71 | 2472.925 | 1564.71 |
| SUBST | 50 | 2402.925 | 1610.28 | 2472.925 | 1680.28 |
| D5 | 51 | 2402.925 | 1725.85 | 2472.925 | 1795.85 |
| D6 | 52 | 2402.925 | 1827.21 | 2472.925 | 1897.21 |
| N/C | 53 | 2402.925 | 1942.78 | 2472.925 | 2012.78 |
| D7 | 54 | 2402.925 | 2058.35 | 2472.925 | 2128.35 |
| SUBST | 55 | 2205 | 2229.08 | 2275 | 2299.08 |
| SUBST | 56 | 2103.5 | 2229.08 | 2173.5 | 2299.08 |
| OVR | 57 | 1980.79 | 2227.925 | 2050.79 | 2297.925 |
| SUBST | 58 | 1865.22 | 2227.925 | 1935.22 | 2297.925 |
| CLKOUT | 59 | 1749.65 | 2227.925 | 1819.65 | 2297.925 |
| N/C | 60 | 1648.29 | 2227.925 | 1718.29 | 2297.925 |
| SUBST | 61 | 1532.72 | 2227.925 | 1602.72 | 2297.925 |
| N/C | 62 | 1417.15 | 2227.925 | 1487.15 | 2297.925 |
| D8 | 63 | 1315.79 | 2227.925 | 1385.79 | 2297.925 |
| SUBST | 64 | 1200.22 | 2227.925 | 1270.22 | 2297.925 |
| D9 | 65 | 1084.65 | 2227.925 | 1154.65 | 2297.925 |
| D10 | 66 | 983.29 | 2227.925 | 1053.29 | 2297.925 |
| SUBST | 67 | 867.72 | 2227.925 | 937.72 | 2297.925 |
| D11 | 68 | 752.15 | 2227.925 | 822.15 | 2297.925 |
| D12 | 69 | 650.79 | 2227.925 | 720.79 | 2297.925 |
| SUBST | 70 | 535.22 | 2227.925 | 605.22 | 2297.925 |
| D13 | 71 | 419.65 | 2227.925 | 489.65 | 2297.925 |
| SUBST | 72 | 322 | 2229.08 | 392 | 2299.08 |
| DRVDD | 73 | 241.5 | 2229.08 | 311.5 | 2299.08 |
| Substrate should be connected to DRVSS | | | | | |

## ABSOLUTE MAXIMUM RATINGS(1)

| | | VALUE | UNIT |
|---|---|---|---|
| $V_I$ | Supply voltage range, AVDD | –0.3 to 3.9 | V |
| | Supply voltage range, DRVDD | –0.3 to 3.9 | V |
| | Voltage between AGND and DRGND | –0.3 to 0.3 | V |
| | Voltage between AVDD to DRVDD | –0.3 to 3.3 | V |
| | Voltage applied to VCM pin (in external reference mode) | –0.3 to 2 | V |
| | Voltage applied to analog input pins, INP and INM | –0.3 to minimum ( 3.6, AVDD + 0.3) | V |
| | Voltage applied to analog input pins, CLKP and CLKM | –0.3 to (AVDD + 0.3) | V |
| $T_J$ | Operating junction temperature range | -40 to 210 | °C |
| $T_{stg}$ | Storage temperature range | –65 to 210 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | Tj = -40°C to 125°C | | | Tj = 210°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| **SUPPLIES** | | | | | | | | | |
| AVDD | Analog supply voltage | | 3 | 3.3 | 3.6 | 3 | 3.3 | 3.6 | V |
| DRVDD | Output buffer supply voltage | CMOS Interface | 1.65 | 1.8 to 3.3 | 3.6 | 1.65 | 1.8 to 3.3 | 3.6 | V |
| | | LVDS Interface | 3 | 3.3 | 3.6 | 3 | 3.3 | 3.6 | V |
| **ANALOG INPUTS** | | | | | | | | | |
| | Differential input voltage range | | | 2 | | | 2 | | $V_{pp}$ |
| $V_{IC}$ | Input common-mode voltage | | | 1.5 ± 0.1 | | | 1.5 ± 0.1 | | V |
| | Voltage applied on VCM in external reference mode | | 1.45 | 1.5 | 1.55 | 1.45 | 1.5 | 1.55 | V |
| **CLOCK INPUT** | | | | | | | | | |
| | Input clock sample rate, $F_S$ | | 1 | | 65 | 1 | | 65 | MSPS |
| | Input clock amplitude differential ($V_{CLKP} - V_{CLKM}$) | Sine wave, ac-coupled | 0.4 | 1.5 | | 0.4 | 1.5 | | $V_{pp}$ |
| | | LVPECL, ac-coupled | | ± 0.8 | | | ± 0.8 | | |
| | | LVDS, ac-coupled | | ± 0.35 | | | ± 0.35 | | |
| | | LVCMOS, ac-coupled | | 3.3 | | | 3.3 | | |
| | Input Clock duty cycle | | 35% | 50% | 65% | 35% | 50% | 65% | |
| **DIGITAL OUTPUTS** | | | | | | | | | |
| | Output buffer drive strength (1) | For $C_{LOAD}$ ≤ 5 pF and DRVDD ≥ 2.2 V | | DEFAULT strength | | | DEFAULT strength | | |
| | | For $C_{LOAD}$ > 5 pF and DRVDD ≥ 2.2 V | | MAXIMUM strength | | | MAXIMUM strength | | |
| | | For DRVDD < 2.2 V | | MAXIMUM strength | | | MAXIMUM strength | | |
| $C_{LOAD}$ | Maximum external load capacitance from each output pin to DRGND | CMOS Interface, maximum buffer strength | | 10 | | | 10 | | pF |
| | | LVDS Interface, without internal termination | | 5 | | | 5 | | |
| | | LVDS Interface, with internal termination | | 10 | | | 10 | | |
| $R_{LOAD}$ | Differential load resistance (external) between the LVDS output pairs | | | 100 | | | 100 | | Ω |
| $T_J$ | Operating junction temperature range | | -40 | | 125 | | | 210 | °C |

(1) See *Output Buffer Strength Programmability* in the application section.

## ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

| PARAMETER | | Tj = -40°C to 125°C | | | Tj = 210°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **RESOLUTION** | | | 14 | | | 14 | | Bits |
| **ANALOG INPUT** | | | | | | | | |
| | Differential input voltage range | | 2 | | | 2 | | $V_{PP}$ |
| | Differential input resistance (dc), see Figure 37 | | > 1 | | | > 1 | | MΩ |
| | Differential input capacitance, see Figure 38 | | 7 | | | 7 | | pF |
| | Analog input bandwidth | | 450 | | | 300 | | MHz |
| | Analog input common-mode current (per input pin of each ADC) | | 92 | | | 95 | | µA |
| **REFERENCE VOLTAGES** | | | | | | | | |
| VREFB | Internal reference bottom voltage | | 1 | | | 1 | | V |
| VREFT | Internal reference top voltage | | 2 | | | 2 | | V |
| $\Delta V_{REF}$ | Internal reference error (VREFT–VREFB) | -30 | ±5 | 30 | -55 | ±5 | 55 | mV |
| $V_{CM}$ | Common-mode output voltage | | 1.5 | | | 1.5 | | V |
| | $V_{CM}$ Output current capability | | 4 | | | 4 | | mA |
| **DC ACCURACY** | | | | | | | | |
| | No missing codes | | Specified | | | Specified | | |
| $E_O$ | Offset error | -11 | ±2 | 11 | -13 | ±10 | 13 | mV |
| | Offset error temperature coefficient | | 0.04 | | | 0.06 | | mV/°C |
| | There are two sources of gain error – internal reference inaccuracy and channel gain error | | | | | | | |
| $E_{GREF}$ | Gain error due to internal reference inaccuracy alone, ($\Delta V_{REF}$ /2) % | -1 | 0.6 | 1 | -1 | 0.65 | 1 | % FS |
| $E_{GCHAN}$ | Gain error of channel alone (1) | | ±0.3 | | | ±0.3 | | % FS |
| | Channel gain error temperature coefficient | | 0.005 | | | | | Δ%/°C |
| DNL | Differential nonlinearity | -0.95 | 0.5 | 2 | -0.99 | ±0.5 | 2.5 | LSB |
| INL | Integral nonlinearity | -10 | ±2 | 10 | -18 | ±6 | 18 | LSB |
| **POWER SUPPLY** | | | | | | | | |
| $I_{AVDD}$ | Analog supply current | | 0.75 | | | 0.76 | | mA |
| $I_{DRVDD}$ | Digital supply current, **CMOS** interface, DRVDD = 1.8 V, No load capacitance, $F_{in}$= 2 MHz (2) | | 4 | | | 4 | | mA |
| $I_{DRVDD}$ | Digital supply current, **LVDS** interface, DRVDD = 3.3 V, with 100-Ω external termination | | 21 | | | 48 | | mA |
| | Total power, **CMOS**, DRVDD = 3.3 V (3) | | 418 | 450 | | 422 | 500 | mW |
| | Global power down | | 30 | 60 | | 30 | 70 | mW |

(1) Specified by design and characterization; not tested in production.
(2) In CMOS mode, the DRVDD current scales with the sampling frequency and the load capacitance on the output pins (see **Figure 30**).
(3) The maximum DRVDD current depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance is 10 pF.

## ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | | Tj = -40°C to 125°C | | | Tj= 210°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DYNAMIC AC CHARACTERISTICS** | | | | | | | | | |
| SNR Signal-to-noise ratio, **CMOS** | $F_{in}$ = 10 MHz | | | 74.7 | | | | | dBFS |
| | $F_{in}$ = 50 MHz | | | 74.4 | | | | | |
| | $F_{in}$ = 70 MHz | | 61.5 | 74.4 | | 57.5 | 74 | | |
| | $F_{in}$ = 170 MHz | 0 dB Gain | | 72.7 | | | | | |
| | | 3.5 dB Coarse gain | | 71.8 | | | | | |
| | $F_{in}$ = 230 MHz | 0 dB Gain | | 71.7 | | | 65.5 | | |
| | | 3.5 dB Coarse gain | | 70.9 | | | 63 | | |
| SNR Signal-to-noise ratio, **LVDS** | $F_{in}$ = 10 MHz | | | 75 | | | | | dBFS |
| | $F_{in}$ = 50 MHz | | | 74.6 | | | | | |
| | $F_{in}$ = 70 MHz | | 68 | 74.6 | | 62 | 75 | | |
| | $F_{in}$ = 170 MHz | 0 dB Gain | | 72.9 | | | | | |
| | | 3.5 dB Coarse gain | | 72.1 | | | | | |
| | $F_{in}$ = 230 MHz | 0 dB Gain | | 72 | | | 60 | | |
| | | 3.5 dB Coarse gain | | 71.2 | | | | | |
| RMS output noise | Inputs tied to common-mode | | | 1.05 | | | | | LSB |
| SINAD Signal-to-noise and distortion ratio **CMOS** | $F_{in}$ = 10 MHz | | | 74.6 | | | | | dBFS |
| | $F_{in}$ = 50 MHz | | | 74.1 | | | | | |
| | $F_{in}$ = 70 MHz | | 60.5 | 74.0 | | 56.5 | 74 | | |
| | $F_{in}$ = 170 MHz | 0 dB Gain | | 72.2 | | | | | |
| | | 3.5 dB Coarse gain | | 71.5 | | | | | |
| | $F_{in}$ = 230 MHz | 0 dB Gain | | 70.6 | | | 56 | | |
| | | 3.5 dB Coarse gain | | 70.4 | | | 57 | | |
| SINAD Signal-to-noise and distortion ratio **LVDS** | $F_{in}$ = 10 MHz | | | 74.9 | | | | | dBFS |
| | $F_{in}$ = 50 MHz | | | 74.4 | | | | | |
| | $F_{in}$ = 70 MHz | | 67 | 74.4 | | 64 | 74 | | |
| | $F_{in}$ = 170 MHz | 0 dB Gain | | 72.4 | | | | | |
| | | 3.5 dB Coarse gain | | 71.9 | | | | | |
| | $F_{in}$ = 230 MHz | 0 dB Gain | | 70.5 | | | 56 | | |
| | | 3.5 dB Coarse gain | | 70.5 | | | | | |
| ENOB Effective number of bits | $F_{in}$ = 50 MHz | | | | | | | | Bits |
| | $F_{in}$ = 70 MHz | | 10.5 | 12 | | 9.4 | 12 | | |
| SFDR Spurious free dynamic range | $F_{in}$ = 10 MHz | | | 95 | | | | | dBc |
| | $F_{in}$ = 50 MHz | | | 89 | | | | | |
| | $F_{in}$ = 70 MHz | | 70 | 78 | | 66 | 77 | | |
| | $F_{in}$ = 170 MHz | 0 dB Gain | | 82 | | | | | |
| | | 3.5 dB Coarse gain | | 84 | | | | | |
| | $F_{in}$ = 230 MHz | 0 dB Gain | | 79 | | | 58 | | |
| | | 3.5 dB Coarse gain | | 82 | | | 60 | | |
| THD Total harmonic distortion | $F_{in}$ = 10 MHz | | | 93 | | | | | dBc |
| | $F_{in}$ = 50 MHz | | | 88 | | | | | |
| | $F_{in}$ = 70 MHz | | 72 | 85 | | 66 | 75 | | |
| | $F_{in}$ = 170 MHz | 0 dB Gain | | 80 | | | | | |
| | | 3.5 dB Coarse gain | | 82 | | | | | |
| | $F_{in}$ = 230 MHz | 0 dB Gain | | 76 | | | 56 | | |
| | | 3.5 dB Coarse gain | | 78.5 | | | 59 | | |

## ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | | Tj = -40°C to 125°C | | | Tj= 210°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| HD2 Second harmonic distortion | $F_{in}$ = 10 MHz | | | 98 | | | | | dBc |
| | $F_{in}$ = 50 MHz | | | 96 | | | | | |
| | $F_{in}$ = 70 MHz | | 73 | 93 | | 66 | 76 | | |
| | $F_{in}$ = 170 MHz | 0 dB Gain | | 86 | | | | | |
| | | 3.5 dB Coarse gain | | 87 | | | | | |
| | $F_{in}$ = 230 MHz | 0 dB Gain | | 79 | | | 58 | | |
| | | 3.5 dB Coarse gain | | 81 | | | 60 | | |
| HD3 Third harmonic distortion | $F_{in}$ = 10 MHz | | | 95 | | | | | dBc |
| | $F_{in}$ = 50 MHz | | | 89 | | | | | |
| | $F_{in}$ = 70 MHz | | 75 | 86 | | 70 | 84 | | |
| | $F_{in}$ = 170 MHz | 0 dB Gain | | 82 | | | | | |
| | | 3.5 dB Coarse gain | | 84 | | | | | |
| | $F_{in}$ = 230 MHz | 0 dB Gain | | 79 | | | 75 | | |
| | | 3.5 dB Coarse gain | | 82 | | | 74 | | |
| Worst spur (other than HD2, HD3) | $F_{in}$ = 10 MHz | | | 97 | | | | | dBc |
| | $F_{in}$ = 50 MHz | | | 96 | | | | | |
| | $F_{in}$ = 70 MHz | | | 95 | | | | | |
| | $F_{in}$ = 170 MHz | | | 91 | | | | | |
| | $F_{in}$ = 230 MHz | | | 90 | | | | | |
| IMD 2-Tone intermodulation distortion | F1 = 185 MHz, F2 = 190 MHz, Each tone at -7 dBFS | | | 91 | | | 90 | | dBFS |
| Input overload recovery | Recovery to within 3% (of final value) for 6-dB overload with sine wave input | | | 1 | | | 1 | | clock cycles |
| PSRR AC Power supply rejection ratio | For 100 mVpp signal on AVDD supply | | | 49 | | | 48 | | dBc |

## DIGITAL CHARACTERISTICS

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1, AVDD = 3.3 V

| PARAMETER | | TEST CONDITIONS | Tj = -40°C to 85°C | | | Tj = 210°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DIGITAL INPUTS PDN, SCLK, SDATA, and SEN** (1) | | | | | | | | | |
| | High-level input voltage | | 2.4 | | | 2.4 | | | V |
| | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| | High-level input current | | | 33 | | | 33 | | µA |
| | Low-level input current | | | –33 | | | –33 | | µA |
| | Input capacitance | | | 4 | | | 4 | | pF |
| **DIGITAL OUTPUTS CMOS INTERFACE, DRVDD = 1.8 to 3.3 V** | | | | | | | | | |
| | High-level output voltage | | | DRVDD | | | DRVDD | | V |
| | Low-level output voltage | | | 0 | | | 0 | | V |
| | Output capacitance | Output capacitance inside the device, from each output to ground | | 2 | | | 2 | | pF |
| **DIGITAL OUTPUTS LVDS INTERFACE, DRVDD = 3.3 V, $I_O$ = 3.5 mA, $R_L$ = 100 Ω** (2) | | | | | | | | | |
| | High-level output voltage | | | 1375 | | | 1375 | | mV |
| | Low-level output voltage | | | 1025 | | | 1025 | | mV |
| $\lvert V_{OD} \rvert$ | Output differential voltage | | 225 | 350 | | 225 | 350 | | mV |
| $V_{OS}$ | Output offset voltage, single-ended | Common-mode voltage of OUTP, OUTM | | 1200 | | | 1200 | | mV |
| | Output capacitance | Output capacitance inside the device, from either output to ground | | 2 | | | 2 | | pF |

(1) SCLK and SEN function as digital input pins when they are used for serial interface programming. When used as parallel control pins, analog voltage needs to be applied as per Table 3 & Table 4

(2) $I_O$ Refers to the LVDS buffer current setting, $R_L$ is the differential load resistance between the LVDS output pair.

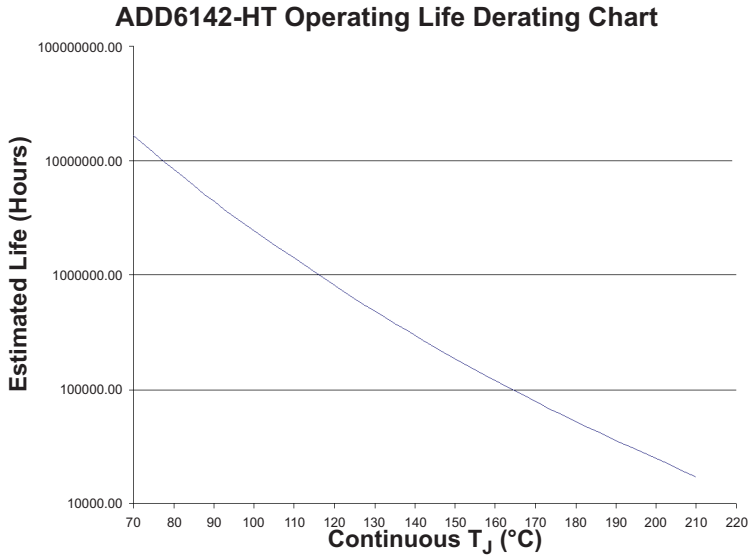
## TIMING CHARACTERISTICS – LVDS AND CMOS MODES(1)

Typical values are at 25°C, min and max values are across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 125°C or 210°C as indicated, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ clock amplitude, $C_L$ = 5 pF(2), $I_O$ = 3.5 mA, $R_L$ = 100 Ω (3), no internal termination, unless otherwise noted.

For timings at lower sampling frequencies, see section Output Timings in the APPLICATION INFORMATION of this data sheet.

| PARAMETER | | TEST CONDITIONS | | Tj = -55°C to 125°C | | | Tj = 210°C | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_a$ | Aperture delay | | | | 1.5 | | | | | ns |
| $t_j$ | Aperture jitter | | | | 150 | | | | | fs rms |
| | Wake-up time (to valid data) | From global power down | | | 15 | | | | | µs |
| | | From standby | | | 15 | | | | | µs |
| | | From output buffer disable | CMOS | | 100 | | | | | ns |
| | | | LVDS | | 200 | | | | | ns |
| | Latency | | | | 9 | | | | | clock cycles |
| **DDR LVDS MODE(4), DRVDD = 3.3 V** | | | | | | | | | | |
| $t_{su}$ | Data setup time(5) | Data valid (6) to zero-cross of CLKOUTP | | | 5.8 | | | 5.6 | | ns |
| $t_h$ | Data hold time(5) | Zero-cross of CLKOUTP to data becoming invalid(6) | | | 1.3 | | | 1.5 | | ns |
| $t_{PDI}$ | Clock propagation delay | Input clock rising edge zero-cross to output clock rising edge zero-cross | | | 6.2 | | | 7.2 | | ns |
| | LVDS bit clock duty cycle | Duty cycle of differential clock, (CLKOUTP-CLKOUTM), 10 ≤ $F_S$ ≤ 125 MSPS | | | 46% | | | 46% | | |
| $t_r$ $t_f$ | Data rise time, Data fall time | Rise time measured from –50 mV to 50 mV, Fall time measured from 50 mV to –50 mV, 1 ≤ $F_S$ ≤ 125 MSPS | | | 112 | | | 116 | | ps |
| $t_{CLKRISE}$ $t_{CLKFALL}$ | Output clock rise time, Output clock fall time | Rise time measured from –50 mV to 50 mV, Fall time measured from 50 mV to –50 mV, 1 ≤ $F_S$ ≤ 125 MSPS | | | 112 | | | 116 | | ps |
| **PARALLEL CMOS MODE, DRVDD = 2.5 V to 3.3 V, default output buffer drive strength (7)** | | | | | | | | | | |
| $t_{su}$ | Data setup time(5) | Data valid(8) to 50% of CLKOUT rising edge | | | 8 | | | 9 | | ns |
| $t_h$ | Data hold time(5) | 50% of CLKOUT rising edge to data becoming invalid(8) | | | 6.5 | | | 6.8 | | ns |
| $t_{PDI}$ | Clock propagation delay | Input clock rising edge zero-cross to 50% of CLKOUT rising edge | | | 7.3 | | | 8.3 | | ns |
| | Output clock duty cycle | Duty cycle of output clock (CLKOUT), 10 ≤ $F_S$ ≤ 125 MSPS | | | 42% | | | 42% | | |
| $t_r$ $t_f$ | Data rise time, Data fall time | Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, 1 ≤ $F_S$ ≤ 125 MSPS | | | 1.9 | | | 2.1 | | ns |
| $t_{CLKRISE}$ $t_{CLKFALL}$ | Output clock rise time, Output clock fall time | Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, 1 ≤ $F_S$ ≤ 125 MSPS | | | 1.9 | | | 2.1 | | ns |

(1) Timing parameters are specified by design and not tested in production.
(2) $C_L$ is the Effective external single-ended load capacitance between each output pin and ground.
(3) $I_O$ Refers to the LVDS buffer current setting; $R_L$ is the differential load resistance between the LVDS output pair.
(4) Measurements are done with a transmission line of 100 Ω characteristic impedance between the device and the load.
(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(6) Data valid refers to a logic high of +100 mV and logic low of –100 mV.
(7) For DRVDD < 2.2 V, it is recommended to use an external clock for data capture and NOT the device output clock signal (CLKOUT). See *Parallel CMOS interface* in the application section.
(8) Data valid refers to a logic high of 2 V (1.7 V) and logic low of 0.8 V (0.7 V) for DRVDD = 3.3 V (2.5 V).




(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

**Figure 1. ADS6142-HT Operating Life Derating Chart**

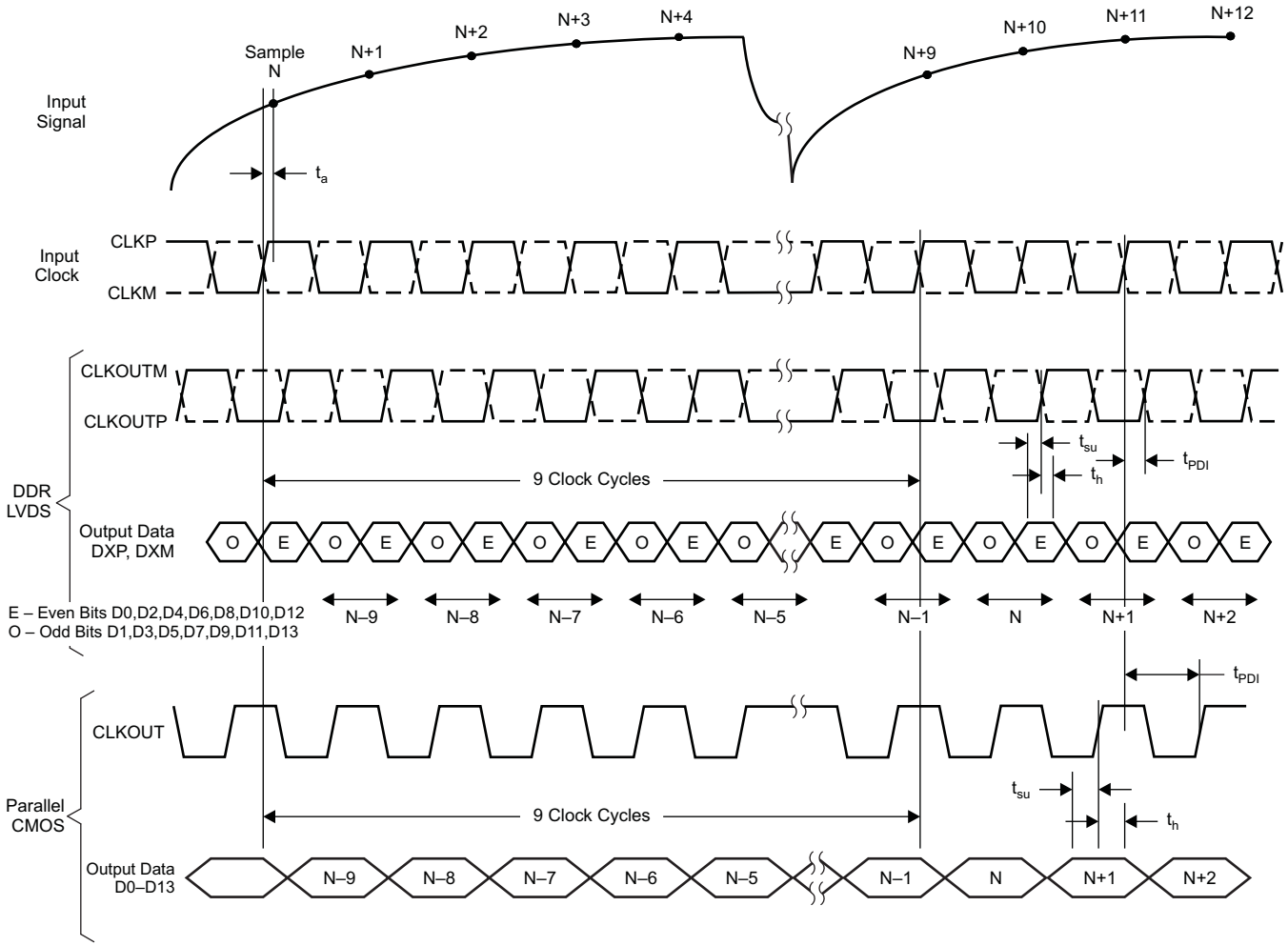
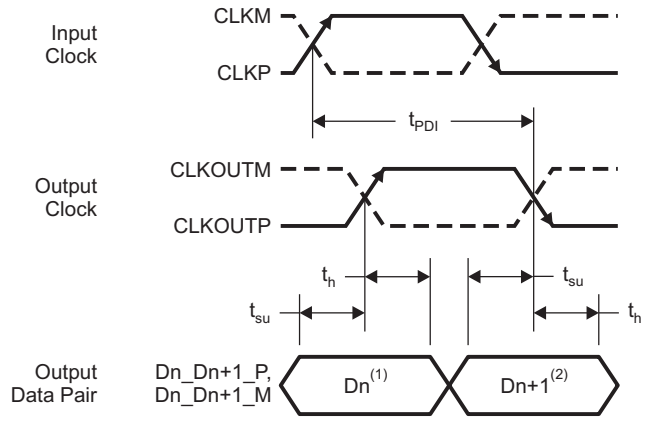
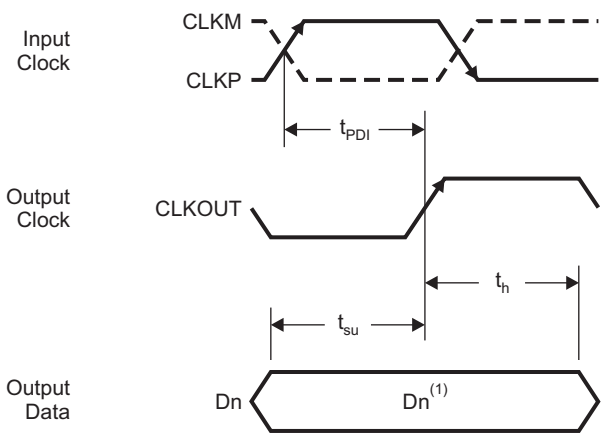



**Figure 2. Latency**




(1)Dn – Bits D0, D2, D4, D6, D8, D10, D12
(2)Dn+1 – Bits D1, D3, D5, D7, D9, D11, D13

**Figure 3. LVDS Mode Timing**




(1)Dn – Bits D0–D13

**Figure 4. CMOS Mode Timing**

## DEVICE PROGRAMMING MODES

The ADS6142 has several features that can be easily configured using either parallel interface control or serial interface programming.

### USING SERIAL INTERFACE PROGRAMMING ONLY

To program using the serial interface, the internal registers must first be reset to their default values, and the RESET pin must be kept ***low***. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of the ADC. The registers are reset either by applying a pulse on the RESET pin or by a ***high*** setting on the <RST> bit (D4 in register 0x00). The Serial Interface section describes register programming and register reset in more detail.

### USING PARALLEL INTERFACE CONTROL ONLY

To control the device using the parallel interface, keep RESET tied ***high*** (AVDD). Now SEN, SCLK, SDATA, and PDN function as parallel interface control pins. These pins can be used to directly control certain modes of the ADC by connecting them to the correct voltage levels (as described in Table 3 to Table 5). There is no need to apply a reset pulse.

Frequently used functions are controlled in this mode — standby, selection between LVDS/CMOS output format, internal/external reference, and 2s complement/straight binary output format.

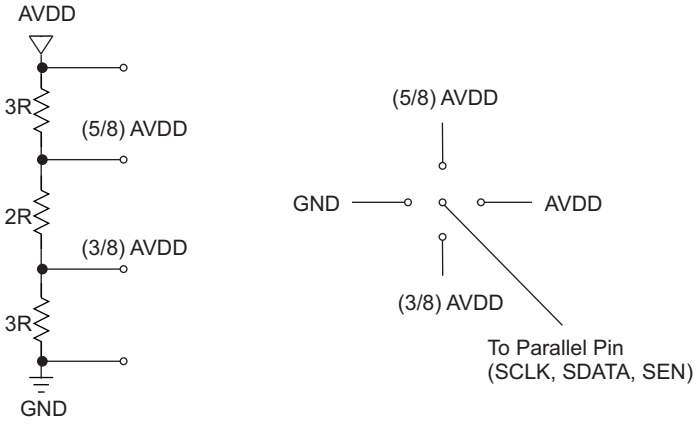



**Figure 5. Simple Scheme to Configure Parallel Pins**

#### *DESCRIPTION OF PARALLEL PINS*

**Table 3. SCLK (Analog Control Pin)**

| SCLK | DESCRIPTION |
|---|---|
| 0 | Internal reference and 0 dB gain (full-scale = 2 $V_{PP}$) |
| (3/8) AVDD | External reference and 0 dB gain (full-scale = 2 $V_{PP}$) |
| (5/8) AVDD | External reference and 3.5 dB coarse gain (full-scale = 1.34 $V_{PP}$) |
| AVDD | Internal reference and 3.5 dB coarse gain (full-scale = 1.34 $V_{PP}$) |

**Table 4. SEN (Analog Control Pin)**

| SEN | DESCRIPTION |
|---|---|
| 0 | 2s Complement format and DDR LVDS interface |
| (3/8) AVDD | Straight binary format and DDR LVDS interface |
| (5/8) AVDD | Straight binary and parallel CMOS interface |
| AVDD | 2s Complement format and parallel CMOS interface |

**Table 5. SDATA, PDN (Digital Control Pins)**

| SDATA | PDN | DESCRIPTION |
|---|---|---|
| Low | Low | Normal operation |
| Low | High (AVDD) | Standby - only the ADC is powered down |
| High (AVDD) | Low | Output buffers are powered down, fast wake-up time |
| High (AVDD) | High (AVDD) | Global power down. ADC, internal reference, and output buffers are powered down, slow wake-up time |

## SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed through the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock), SDATA (Serial Interface Data) and RESET. After device power-up, the internal registers must be reset to their default values by applying a high-going pulse on RESET (of width greater than 10 ns).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data is loaded in multiples of 16-bit words within a single active SEN pulse.

The first 5 bits form the register address and the remaining 11 bits form the register data.

The interface can work with a SCLK frequency from 20 MHz down to very low speeds (a few hertz) and also with a non-50% SCLK duty cycle.

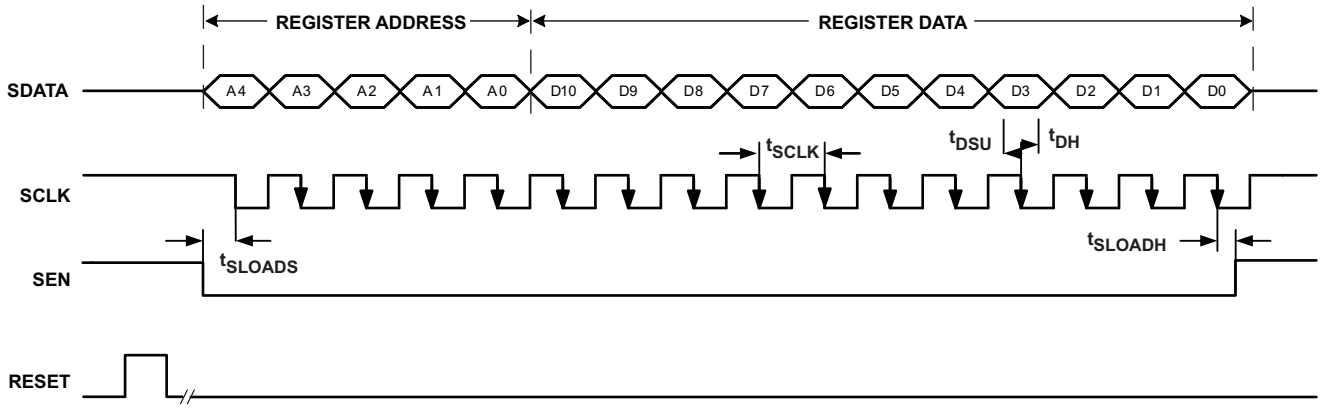



**Figure 6. Serial Interface Timing Diagram**

### REGISTER INITIALIZATION

After power-up, the internal registers *must* be reset to their default values. This is done in one of two ways:

1. Either through a hardware reset by applying a high-going pulse on the RESET pin (width greater than 10 ns) as shown in Figure 6.

   OR

2. By applying a software reset. Using the serial interface, set the <RST> bit (D4 in register 0x00) to ***high***. This initializes the internal registers to their default values and then self-resets the <RST> bit to ***low***. In this case the RESET pin is kept ***low***.

## SERIAL INTERFACE TIMING

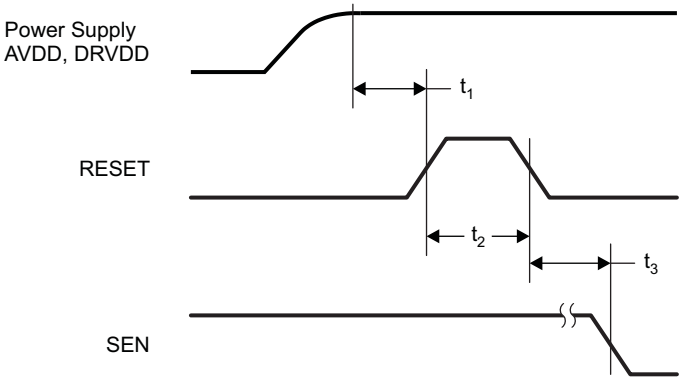
Typical values at 25°C, min and max values across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 210°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{SCLK}$ | SCLK Frequency = $1/t_{SCLK}$ | > DC | | 20 | MHz |
| $t_{SLOADS}$ | SEN to SCLK Setup time | 25 | | | ns |
| $t_{SLOADH}$ | SCLK to SEN Hold time | 25 | | | ns |
| $t_{DSU}$ | SDATA Setup time | 25 | | | ns |
| $t_{DH}$ | SDATA Hold time | 25 | | | ns |

## RESET TIMING

Typical values at 25°C, min and max values across the full temperature range $T_{MIN}$ = –40°C to $T_{MAX}$ = 85°C, AVDD = DRVDD = 3.3 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_1$ | Power-on delay | Delay from power-up of AVDD and DRVDD to RESET pulse active | 5 | | | ms |
| $t_2$ | Reset pulse width | Pulse width of active RESET signal | 10 | | | ns |
| $t_3$ | Register write delay | Delay from RESET disable to SEN active | 25 | | | ns |
| $t_{PO}$ | Power-up time | Delay from power-up of AVDD and DRVDD to output stable | | 6.5 | | ms |




NOTE: A high-going pulse on the RESET pin is required in serial interface mode in the case of initialization through a hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

**Figure 7. Reset Timing Diagram**

## SERIAL REGISTER MAP

Table 6 gives a summary of all the modes that can be programmed through the serial interface.

**Table 6. Summary of Functions Supported by Serial Interface(1) (2)**

| REGISTER ADDRESS IN HEX | REGISTER FUNCTIONS | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A4 - A0** | **D10** | **D9** | **D8** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| 00 | **<PDN OBUF>** Output buffers powered down | **<COARSE GAIN>** Coarse gain | **<LVDS CMOS>** LVDS or CMOS Output interface | 0 | 0 | **<REF>** Internal or external Reference | **<RST>** Software reset | 0 | **<PDN CLKOUT>** Output clock buffer powered down | 0 | **<STBY>** ADC Power down |
| 04 | **<DATAOUT POSN>** Output data position control | **<CLKOUT EDGE>** Output clock edge control | **<CLKOUT POSN>** Output clock position control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09 | Bit-wise or Byte-wise control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0A | **<DATA FORMAT>** 2s Complement or straight binary | 0 | 0 | **<TEST PATTERNS>** | | | 0 | 0 | 0 | 0 | 0 |
| 0B | **<CUSTOM LOW>** Custom pattern lower 9 bits | | | | | | | | | 0 | 0 |
| 0C | **<FINE GAIN>** Fine gain 0 to 6dB | | | 0 | 0 | 0 | **<CUSTOM HIGH>** Custom pattern upper 5 bits | | | | |
| 0E | 0 | LVDS Termination LVDS Internal termination control for output data and clock | | | | | | **<LVDS CURRENT>** LVDS Current control | | **<CURRENT DOUBLE>** LVDS current double | |
| 0F | 0 | 0 | 0 | **<DRIVE STRENGTH>** CMOS output buffer drive strength control | | | | 0 | 0 | 0 | 0 |

(1) The unused bits in each register (shown by blank cells in above table) must be programmed as '0'.
(2) Multiple functions in a register can be programmed in a single write operation.

## DESCRIPTION OF SERIAL REGISTERS

Each register function is explained in detail.

**Table 7.**

| A4–A0 (hex) | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | <PDN OBUF> Output buffers powered down | <COARSE GAIN> Coarse gain | <LVDS CMOS> LVDS or CMOS Output interface | 0 | 0 | <REF> Internal or external reference | <RST> Software reset | 0 | <PDN CLKOUT> Output clock buffer powered down | 0 | <STBY> ADC Power down |

| | |
|---|---|
| **D0** | **<STBY>** Power down modes |
| 0 | Normal operation |
| 1 | Device enters standby mode where only ADC is powered down. |
| **D2** | **<PDN CLKOUT>** Power down modes |
| 0 | Output clock is active (on CLKOUT pin) |
| 1 | Output clock buffer is powered down and becomes three-stated. Data outputs are unaffected. |
| **D4** | **<RST>** |
| 1 | Software reset applied - resets all internal registers and the bit self-clears to 0. |
| **D5** | **<REF>** Reference selection |
| 0 | Internal reference enabled |
| 1 | External reference enabled |
| **D8** | **<LVDS CMOS>** Output Interface selection |
| 0 | Parallel CMOS interface |
| 1 | DDR LVDS Interface |
| **D9** | **<COARSE GAIN>** Gain programming |
| 0 | 0 dB Coarse gain |
| 1 | 3.5 dB Coarse gain |
| **D10** | **<PDN OBUF>** Power down modes |
| 0 | Output data and clock buffers enabled |
| 1 | Output data and clock buffers disabled |

**Table 8.**

| A4–A0 (hex) | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 04 | <DATAOUT POSN> Output data position control | <CLKOUT EDGE> Output Clock edge control | <CLKOUT POSN> Output clock position control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D8 | <CLKOUT POSN> Output clock position control |
|---|---|
| 0 | Default output clock position after reset. The setup/hold timings for this clock position are specified in the timing specifications table. |
| 1 | Output clock shifted (delayed) by 400 ps |

| D9 | <CLKOUT EDGE> |
|---|---|
| 0 | Use rising edge to capture data |
| 1 | Use falling edge to capture data |

| D10 | <DATAOUT_POSN> |
|---|---|
| 0 | Default position (after reset) |
| 1 | Data transition delayed by half clock cycle with respect to default position |

**Table 9.**

| A4–A0 (hex) | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 09 | Bit-wise or Byte-wise control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| D10 | Bit-wise or byte-wise selection (DDR LVDS mode only) |
|---|---|
| 0 | Bit-wise sequence - Even data bits (D0, D2, D4,..D12) are output at the rising edge of CLKOUTP and odd data bits (D1, D3, D5,..D13) at the falling edge of CLKOUTP |
| 1 | Byte-wise sequence - Lower 7 data bits (D0-D7) are output at the rising edge of CLKOUTP and upper 7 data bits (D8-D13) at the falling edge of CLKOUTP |

**Table 10.**

| A4–A0 (hex) | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0A | <DF> 2s Complement or straight binary | 0 | 0 | <TEST PATTERNS> | | | 0 | 0 | 0 | 0 | 0 |

| D7-D5 | Test patterns |
|---|---|
| 000 | Normal operation - <D13:D0> = ADC output |
| 001 | All zeros - <D13:D0> = 0x0000 |
| 010 | All ones - <D13:D0> = 0x3FFF |
| 011 | Toggle pattern - <D13:D0> toggles between 0x2AAA and 0x1555 |
| 100 | Digital ramp - <D13:D0> increments from 0x0000 to 0x3FFF by one code every cycle |
| 101 | Custom pattern - <D13:D0> = contents of CUSTOM PATTERN registers |
| 110 | Unused |
| 111 | Unused |

| D10 | <DATA FORMAT> |
|---|---|
| 0 | 2s Complement |
| 1 | Straight binary |

**Table 11.**

| A4–A0 (hex) | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0B | <CUSTOM LOW> Lower 9 bits of custom pattern | | | | | | | | | 0 | 0 |

**Table 12.**

| A4–A0 (hex) | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0C | <FINE GAIN> Fine gain 0 to 6dB | | | 0 | 0 | 0 | <CUSTOM HIGH> Upper 5 bits of custom pattern | | | | |

Reg 0B D10-D2 **<CUSTOM LOW>** - Specifies lower 9 bits of custom pattern

Reg 0C D4-D0 **<CUSTOM HIGH>** - Specifies upper 5 bits of custom pattern

| D10-D8 | <FINE GAIN> Gain programming |
|---|---|
| 000 | 0 dB Gain |
| 001 | 1 dB Gain |
| 010 | 2 dB Gain |
| 011 | 3 dB Gain |
| 100 | 4 dB Gain |
| 101 | 5 dB Gain |
| 110 | 6 dB Gain |
| 111 | Unused |

**Table 13.**

| A4–A0 (hex) | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0E | 0 | <LVDS TERMINATION> LVDS Internal termination control for output data and clock | | | | | | <LVDS CURRENT> LVDS Current control | | <CURRENT DOUBLE> LVDS Current double | |

| | |
|---|---|
| **D1-D0** | **<CURRENT DOUBLE>** LVDS current programming |
| **D0** | **LVDS Data buffer current control** |
| 0 | Default current, set by <LVDS_CURR> |
| 1 | 2x LVDS Current set by <LVDS_CURR> |
| **D1** | **LVDS Clock buffer current control** |
| 0 | Default current, set by <LVDS_CURR> |
| 1 | 2x LVDS Current set by <LVDS_CURR> |
| **D3-D2** | **<LVDS CURRENT>** LVDS current programming |
| 00 | 3.5 mA |
| 01 | 2.5 mA |
| 10 | 4.5 mA |
| 11 | 1.75 mA |
| **D9-D4** | LVDS internal termination |
| **D9-D7** | **<DATA TERM>** Internal termination for LVDS output data bits |
| 000 | No internal termination |
| 001 | 300 Ω |
| 010 | 185 Ω |
| 011 | 115 Ω |
| 100 | 150 Ω |
| 101 | 100 Ω |
| 110 | 80 Ω |
| 111 | 65 Ω |
| **D6-D4** | **<CLKOUT TERM>** Internal termination for LVDS output clock |
| 000 | No internal termination |
| 001 | 300 Ω |
| 010 | 185 Ω |
| 011 | 115 Ω |
| 100 | 150 Ω |
| 101 | 100 Ω |
| 110 | 80 Ω |
| 111 | 65 Ω |

**Table 14.**

| A4–A0 (hex) | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0F | 0 | 0 | 0 | <DRIVE STRENGTH> CMOS Output buffer drive strength control | | | | 0 | 0 | 0 | 0 |

| D7-D4 | <DRIVE STRENGTH> Output buffer drive strength controls |
|---|---|
| 0101 | WEAKER than default drive |
| 0000 | DEFAULT drive strength |
| 1111 | STRONGER than default drive strength (recommended for load capacitances > 5 pF) |
| 1010 | MAXIMUM drive strength (recommended for load capacitances > 5 pF) |
| Other combinations | Do not use |

## TYPICAL CHARACTERISTICS

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

**FFT for 230 MHz INPUT SIGNAL**

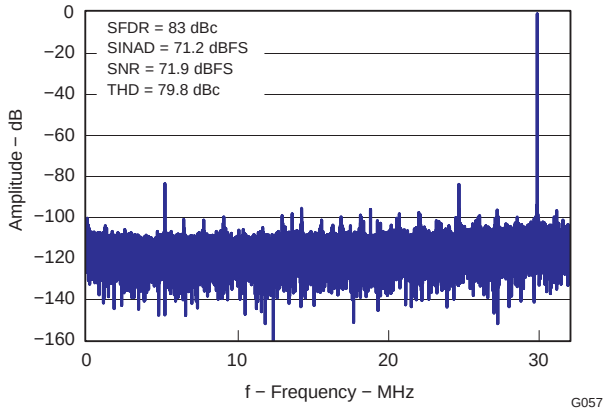



**Figure 8.**

**INTERMODULATION DISTORTION (IMD) vs FREQUENCY**

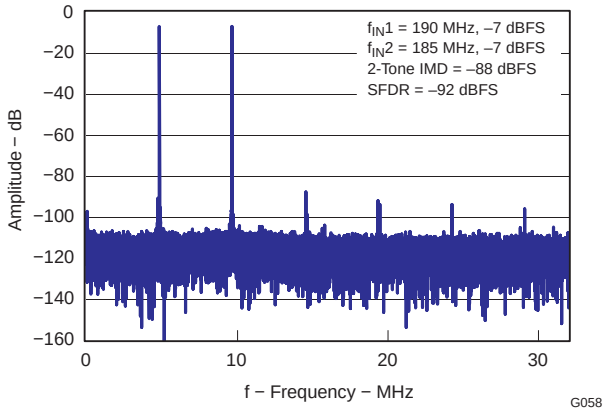



**Figure 9.**

**SFDR vs INPUT FREQUENCY**

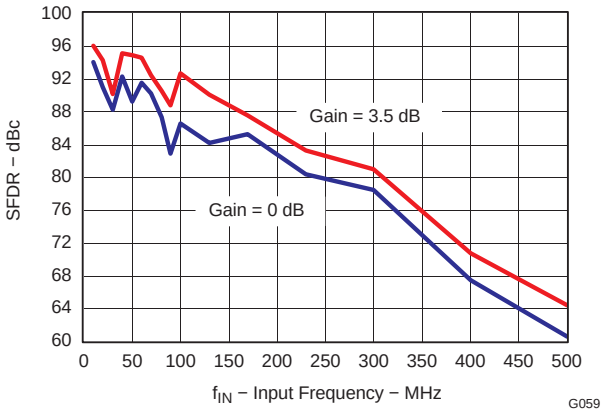



**Figure 10.**

**SNR vs INPUT FREQUENCY**

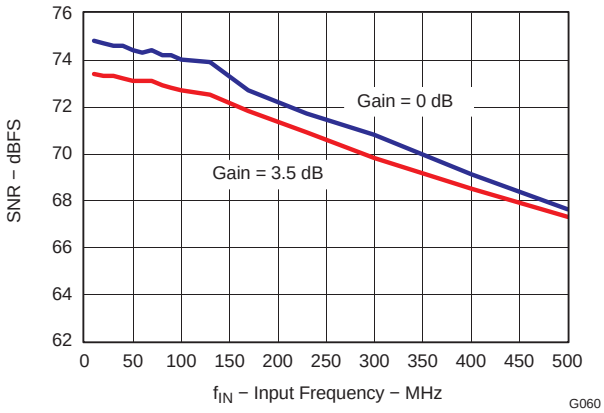



**Figure 11.**

**SFDR vs INPUT FREQUENCY (LVDS interface)**

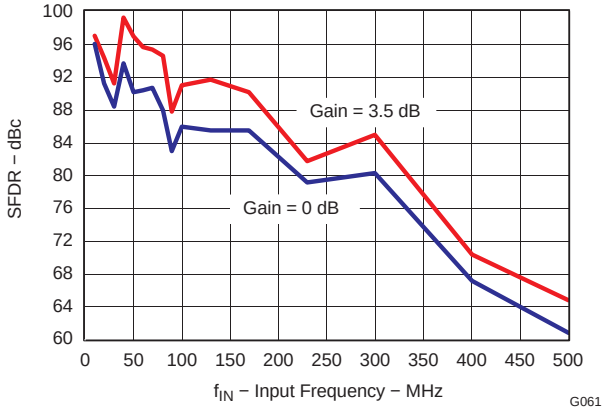



**Figure 12.**

**SNR vs INPUT FREQUENCY (LVDS interface)**

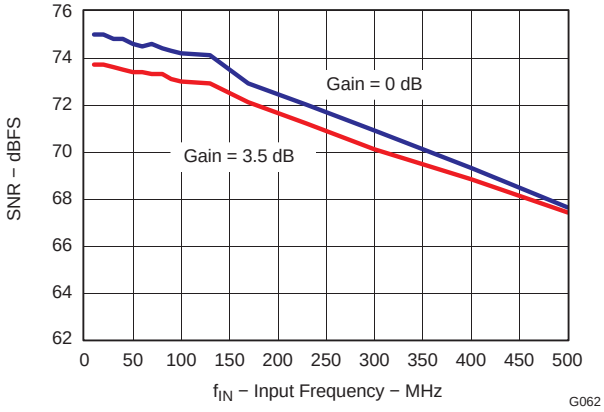



**Figure 13.**

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

**SFDR vs INPUT FREQUENCY ACROSS GAINS**

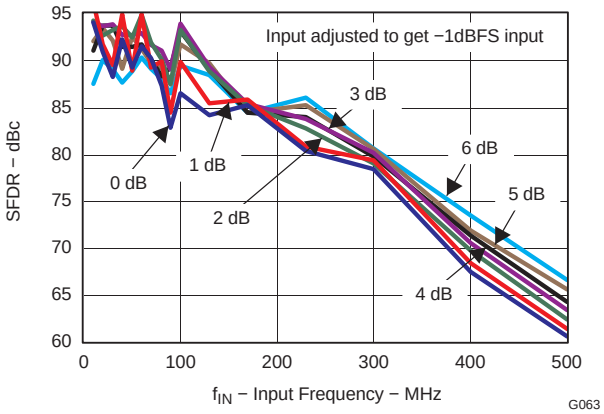



**Figure 14.**

**SINAD vs INPUT FREQUENCY ACROSS GAINS**

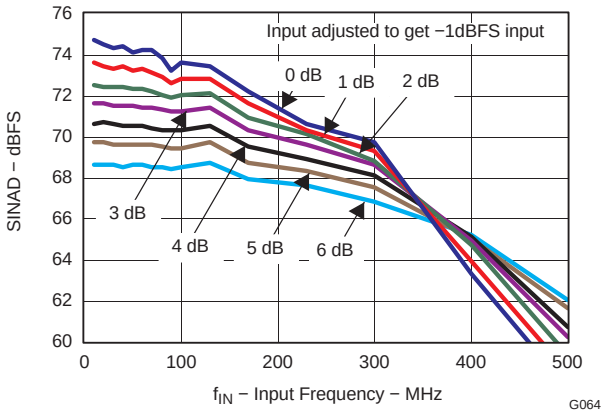



**Figure 15.**

**PERFORMANCE vs AVDD**

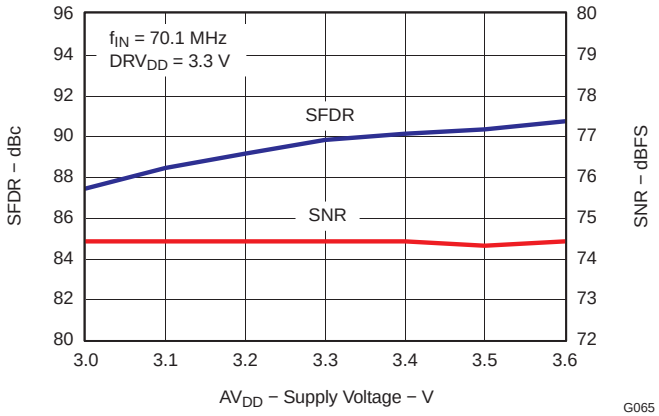



**Figure 16.**

**PERFORMANCE vs DRVDD**

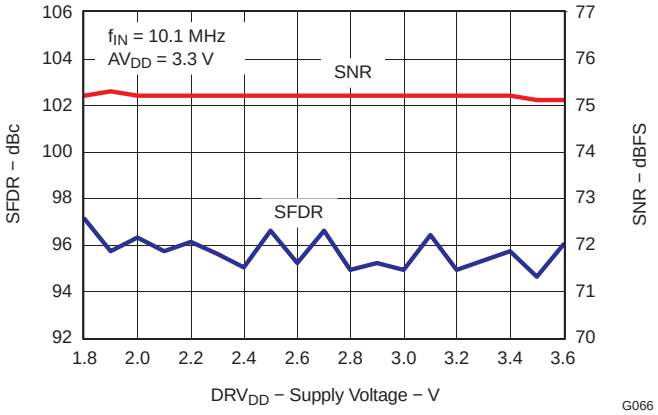



**Figure 17.**

**PERFORMANCE vs TEMPERATURE**

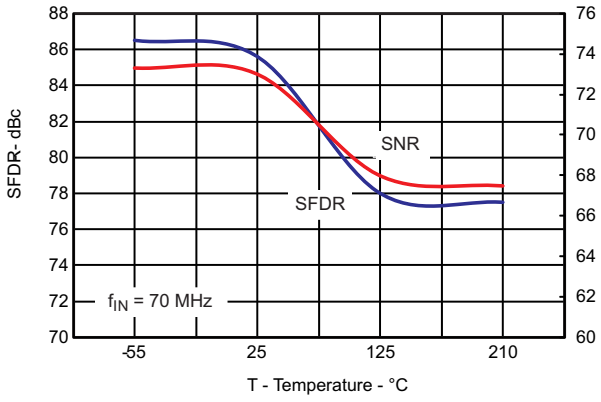



**Figure 18.**

**PERFORMANCE vs INPUT AMPLITUDE**

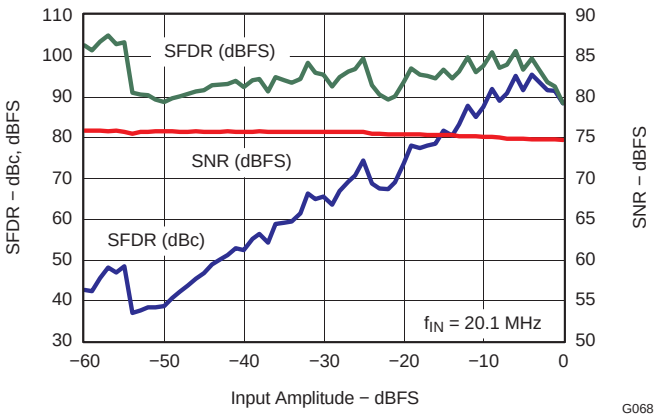



**Figure 19.**

## TYPICAL CHARACTERISTICS (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

**PERFORMANCE vs CLOCK AMPLITUDE**

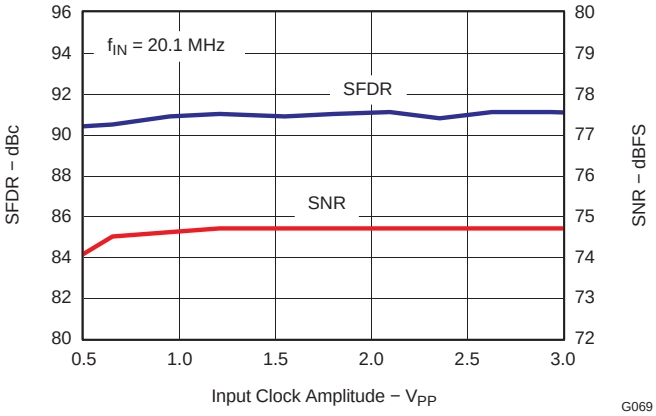



**Figure 20.**

**PERFORMANCE vs INPUT CLOCK DUTY CYCLE**

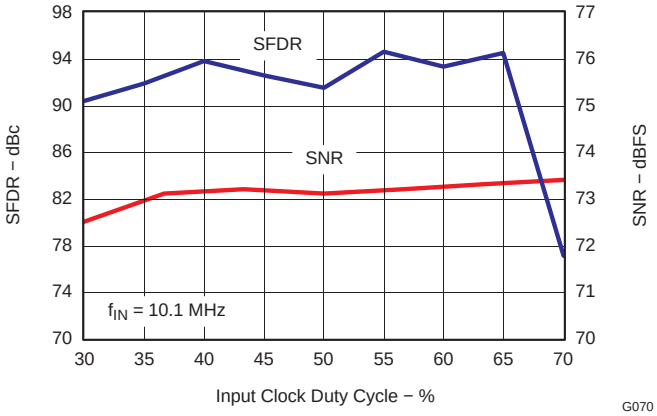



**Figure 21.**

**OUTPUT NOISE HISTOGRAM WITH INPUTS TIED TO COMMON-MODE**

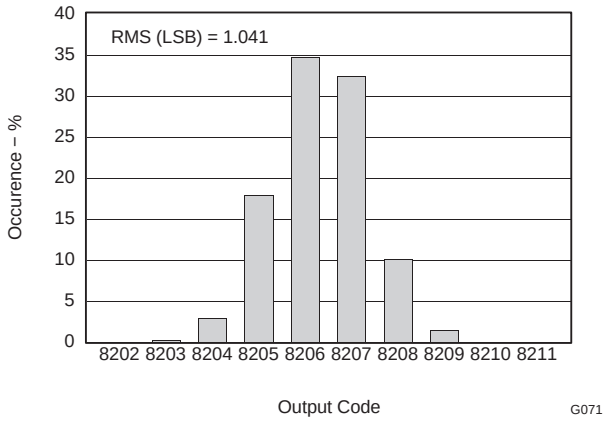



**Figure 22.**

**PERFORMANCE IN EXTERNAL REFERENCE MODE**

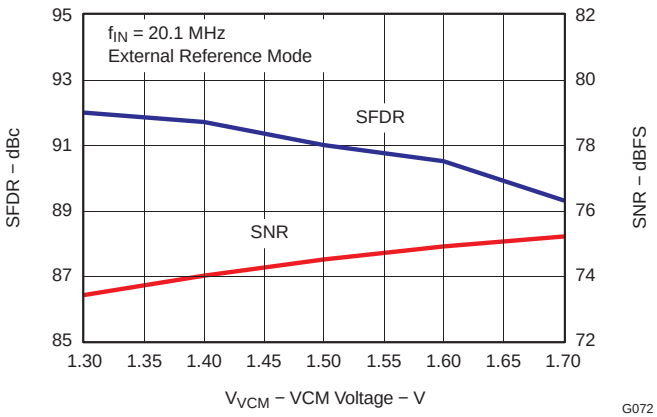



**Figure 23.**

## TYPICAL CHARACTERISTICS - LOW SAMPLING FREQUENCIES

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

### $F_S$ = 40 MSPS

**SFDR vs INPUT FREQUENCY**

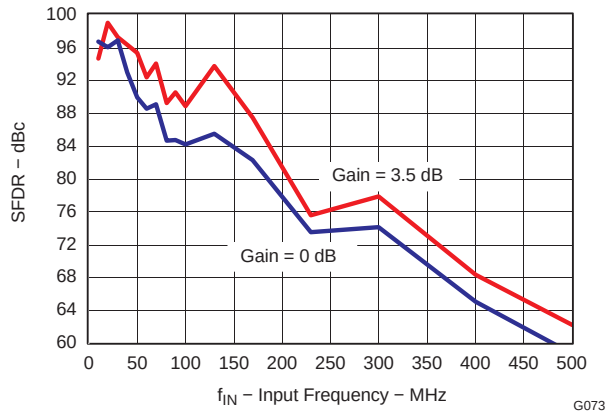



**Figure 24.**

**SNR vs INPUT FREQUENCY**

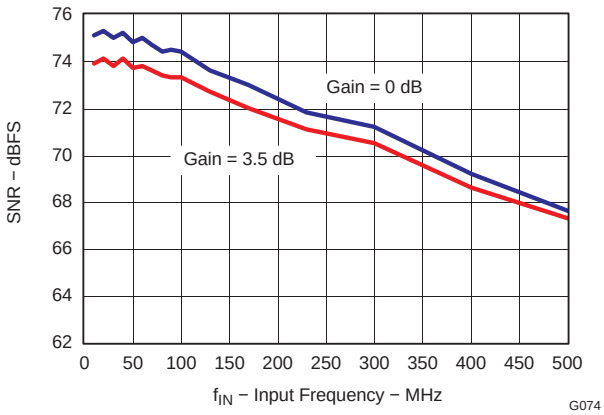



**Figure 25.**

### $F_S$ = 25 MSPS

**SFDR vs INPUT FREQUENCY**

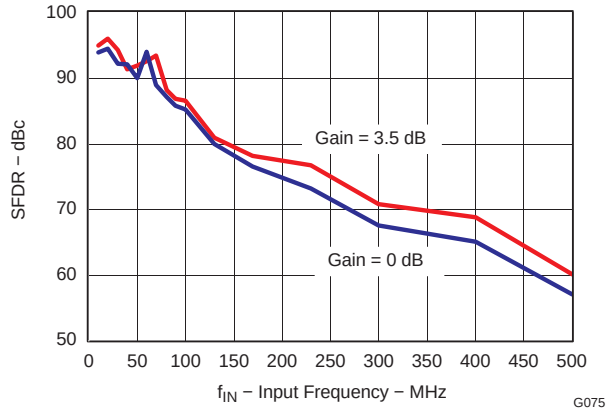



**Figure 26.**

**SNR vs INPUT FREQUENCY**

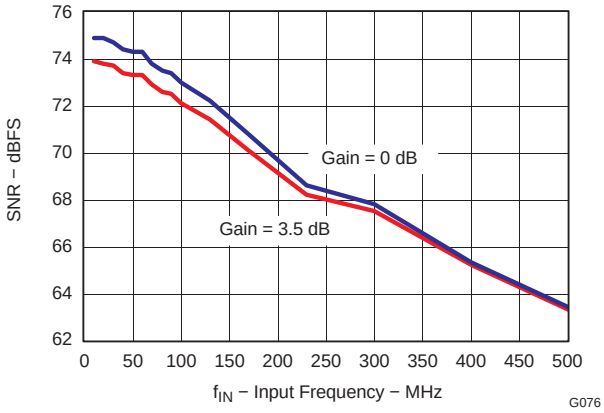



**Figure 27.**

## COMMON PLOTS

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 $V_{PP}$ differential clock amplitude, 50% clock duty cycle, –1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

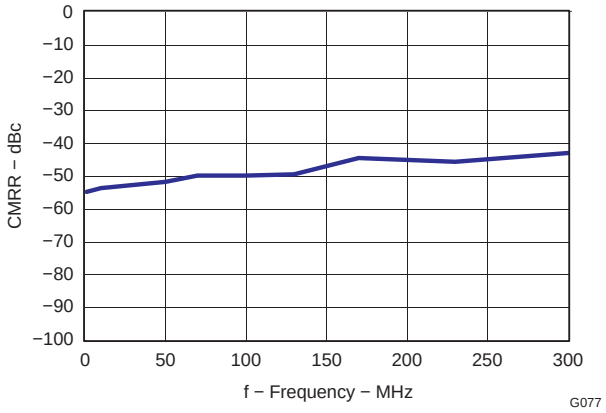



**Figure 28.**

**POWER DISSIPATION vs SAMPLING FREQUENCY (DDR LVDS and CMOS)**

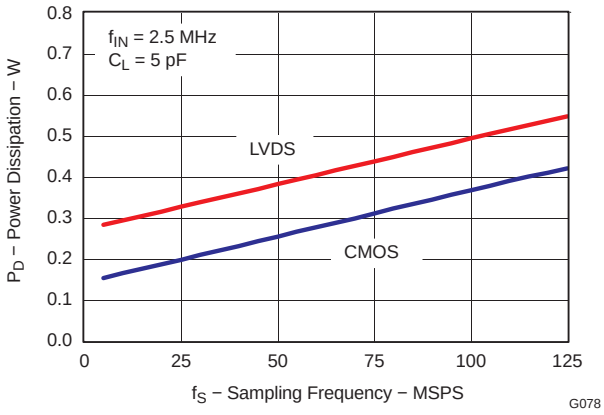



**Figure 29.**

**DRVDD current vs SAMPLING FREQUENCY ACROSS LOAD CAPACITANCE (CMOS)**

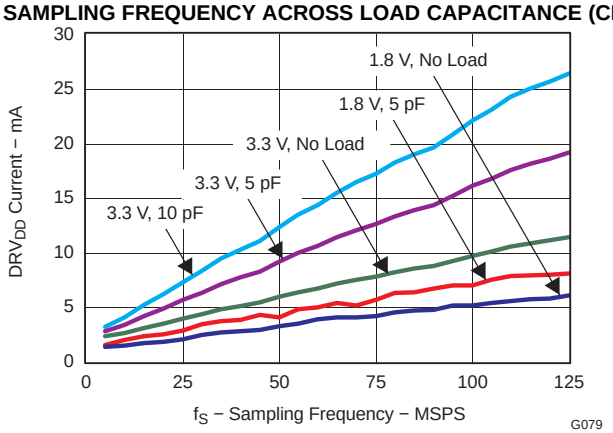



**Figure 30.**

## Contour Plots Across Input and Sampling Frequencies

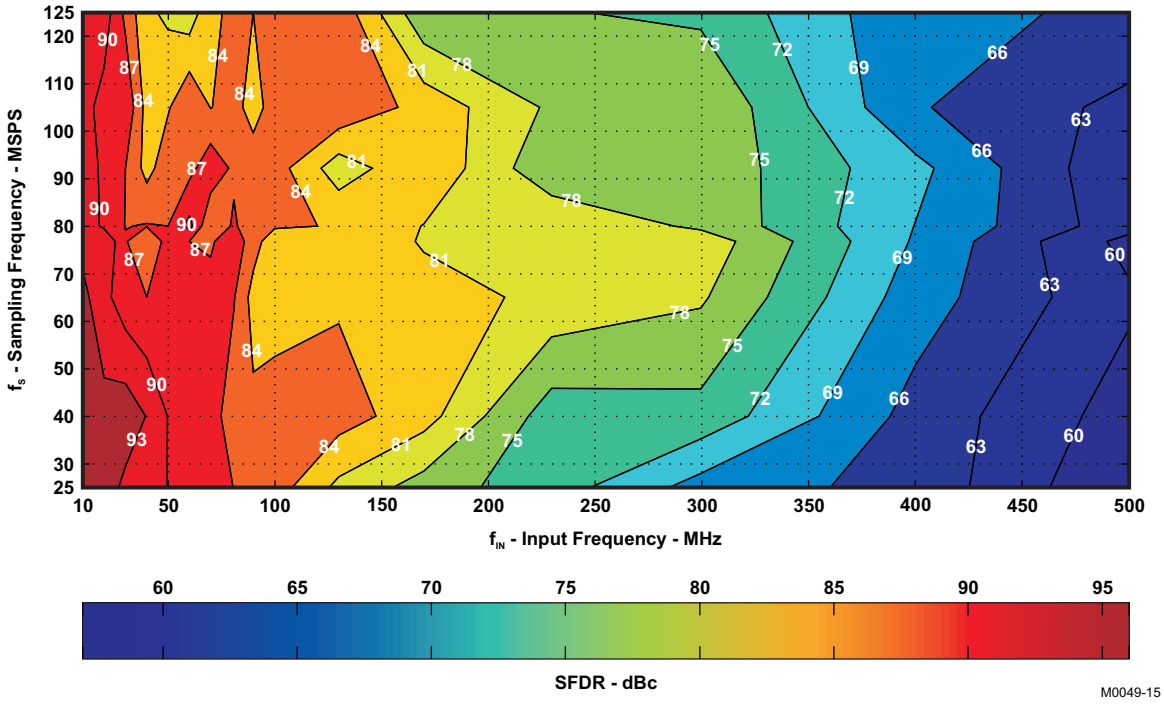



Figure 31. SFDR Contour (no gain, $F_S$ = 2 $V_{PP}$)

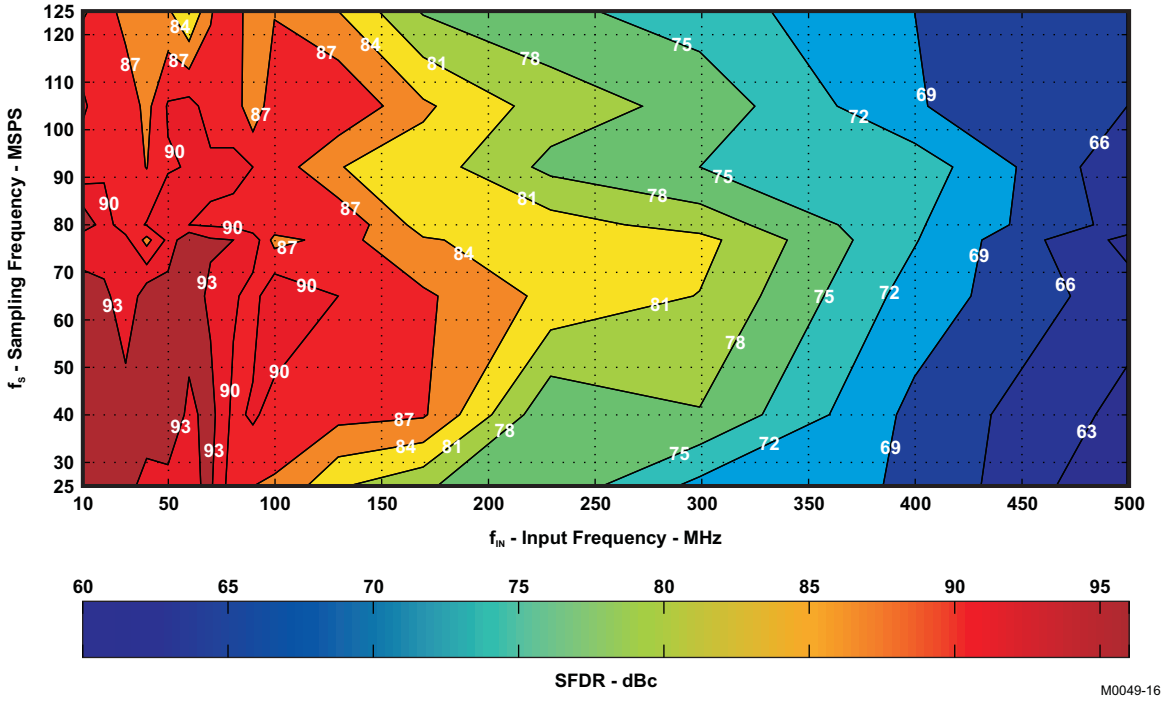



Figure 32. SFDR Contour (with 3.5 dB coarse gain, $F_S$ = 1.34 $V_{PP}$)

## Contour Plots Across Input and Sampling Frequencies (continued)

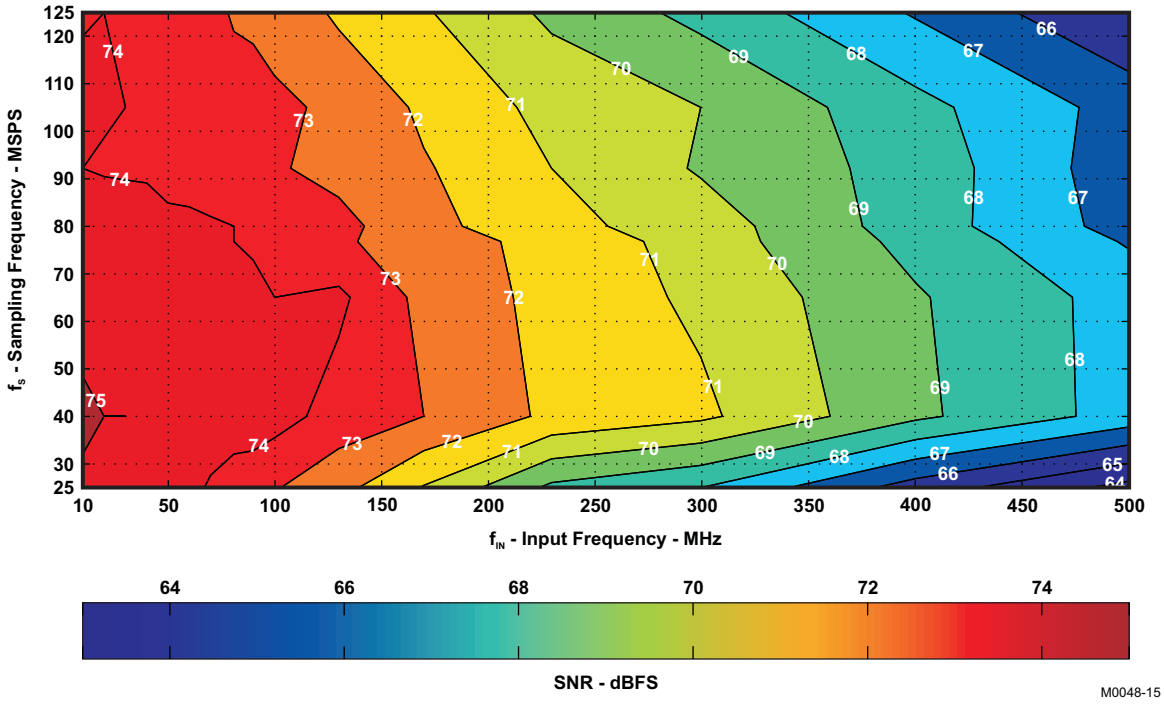



Figure 33. SNR Contour (no gain, $F_S$ = 2 $V_{PP}$)

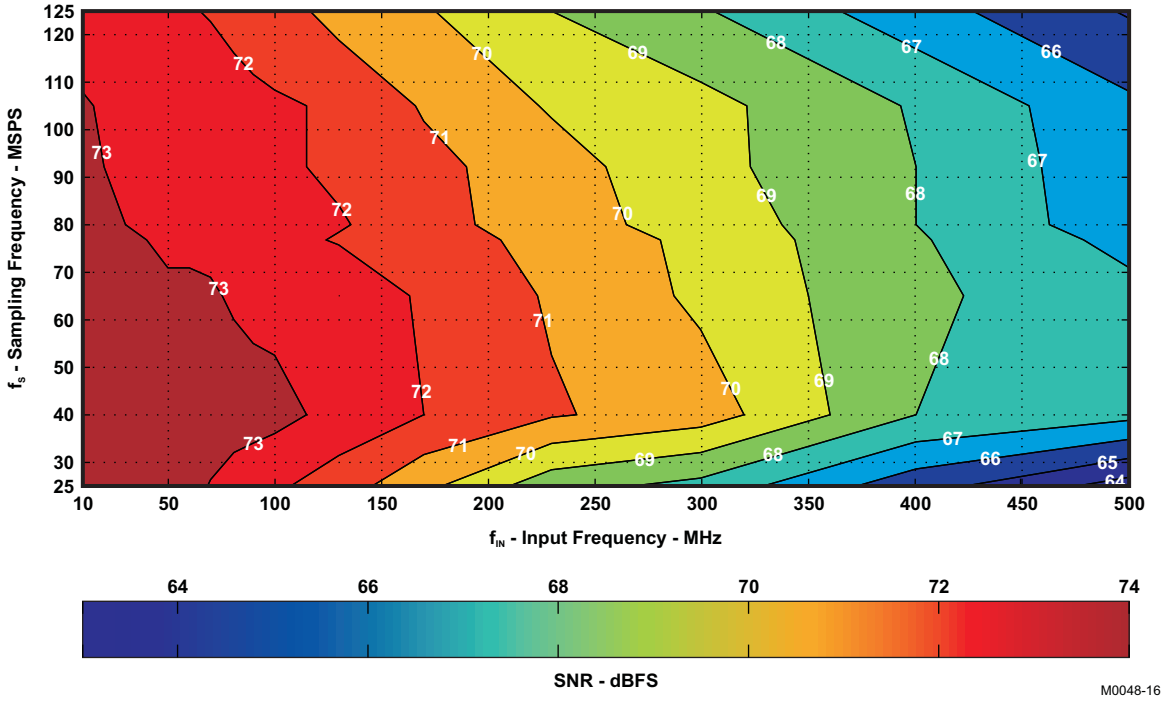



Figure 34. SNR Contour (with 3.5 dB coarse gain, $F_S$ = 1.34 $V_{PP}$)

# APPLICATION INFORMATION

## THEORY OF OPERATION

The ADS6142 is a low power, 14-bit pipeline ADC in a CMOS process with a 65 MSPS sampling frequency. This device is based on switched capacitor technology and run off a single 3.3-V supply. The conversion process is initiated by the rising edge of the external input clock. Once the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline resulting in a data latency of 9 clock cycles. The output is available as 14-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2s complement format.

## ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 35.

This differential topology results in good ac-performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V available on the VCM pin. For a full-scale differential input, each input pin (INP, INM) has to swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a $2V_{PP}$ differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.5 V nominal) and REFM (0.5 V, nominal).

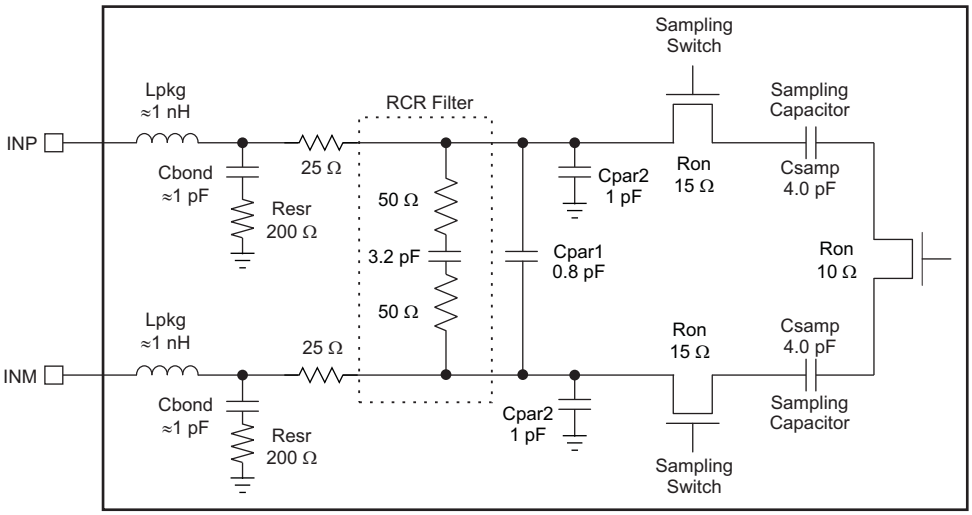



**Figure 35. Input Stage**

The input sampling circuit has a high 3dB bandwidth that extends up to 300 MHz (measured from the input pins to the voltage across the sampling capacitors).

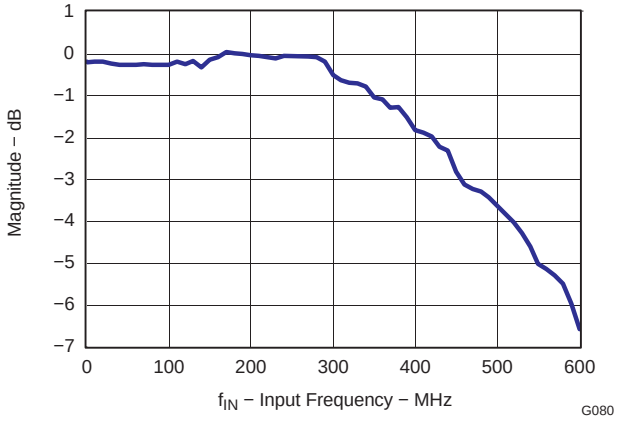



**Figure 36. ADC Analog Input Bandwidth**

### Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even-order harmonic rejection.

A 5-Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics. It is also necessary to present low impedance (< 50 Ω) for the common-mode switching currents. For example, this is achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance (Zin) must be considered. Over a wide frequency range, the input impedance can be approximated by a parallel combination of Rin and Cin (Zin = Rin||Cin).

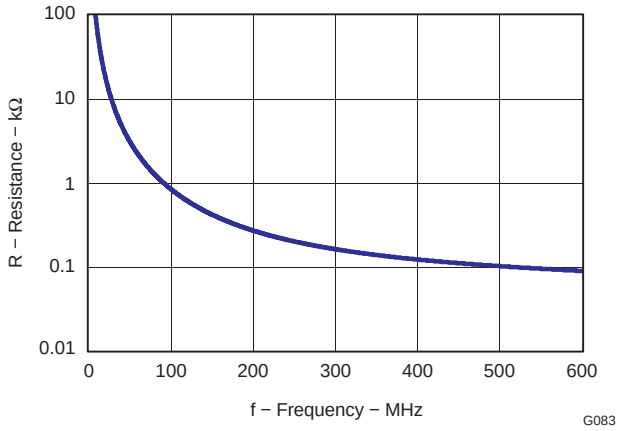



**Figure 37. ADC Input Resistance, Rin**

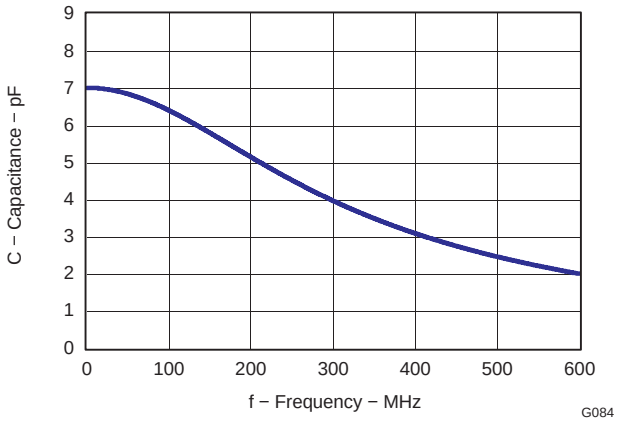



**Figure 38. ADC Input Capacitance, Cin**

### Using RF-Transformer Based Drive Circuits

Figure 39 shows a configuration using a single 1:1 turn ratio transformer (for example, Coilcraft WBC1-1) that can be used for low input frequencies (about 100 MHz).

The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the sampling circuit from the RF transformer's leakage inductances. The termination is accomplished by two resistors connected in series, with the center point connected to the 1.5 V common mode (VCM pin). The value of the termination resistors (connected to common mode) has to be low (< 100 Ω) to provide a low-impedance path for the ADC common-mode switching current.

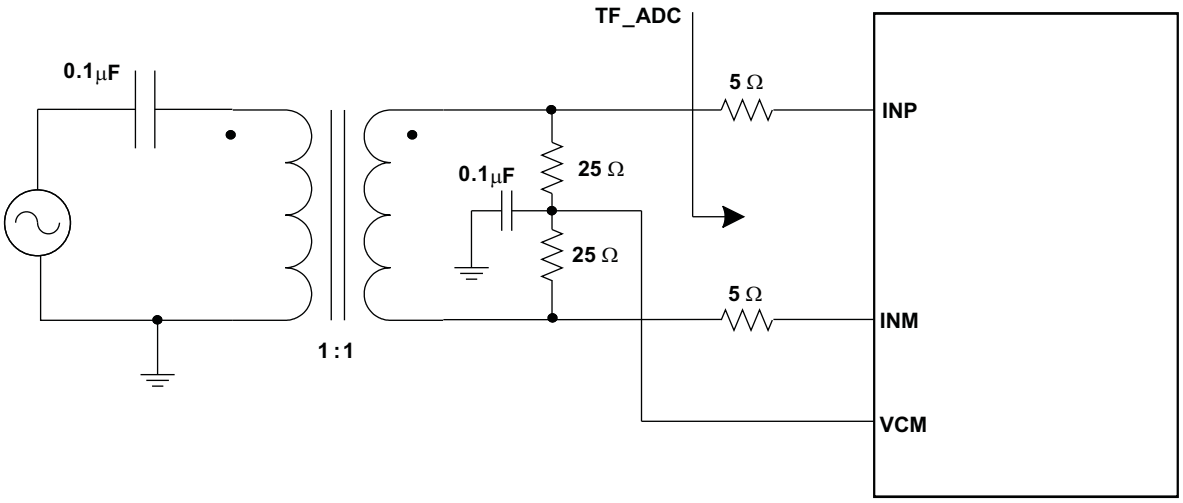



**Figure 39. Single Transformer Drive Circuit**

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch, and good performance is obtained for high frequency input signals. Figure 40 shows an example using two transformers (Coilcraft WBC1-1). An additional termination resistor pair (enclosed within the dotted box in Figure 40) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground.

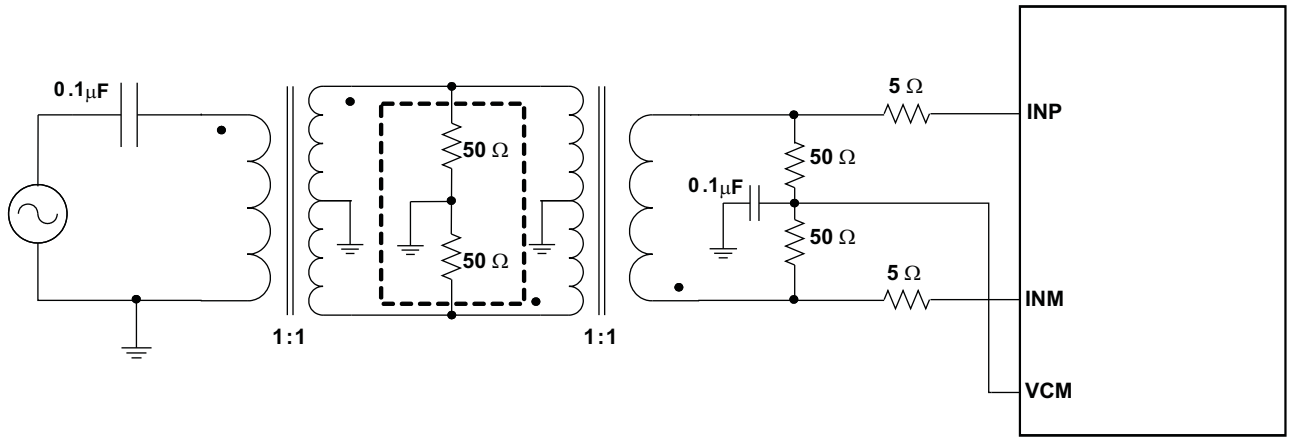



**Figure 40. Two Transformer Drive Circuit**

## REFERENCE

The ADS6142 has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the integration of the requisite reference capacitors on-chip eliminates the need for external decoupling. The full-scale input range of the converter is controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the serial interface register bit **<REF>** (Table 7).

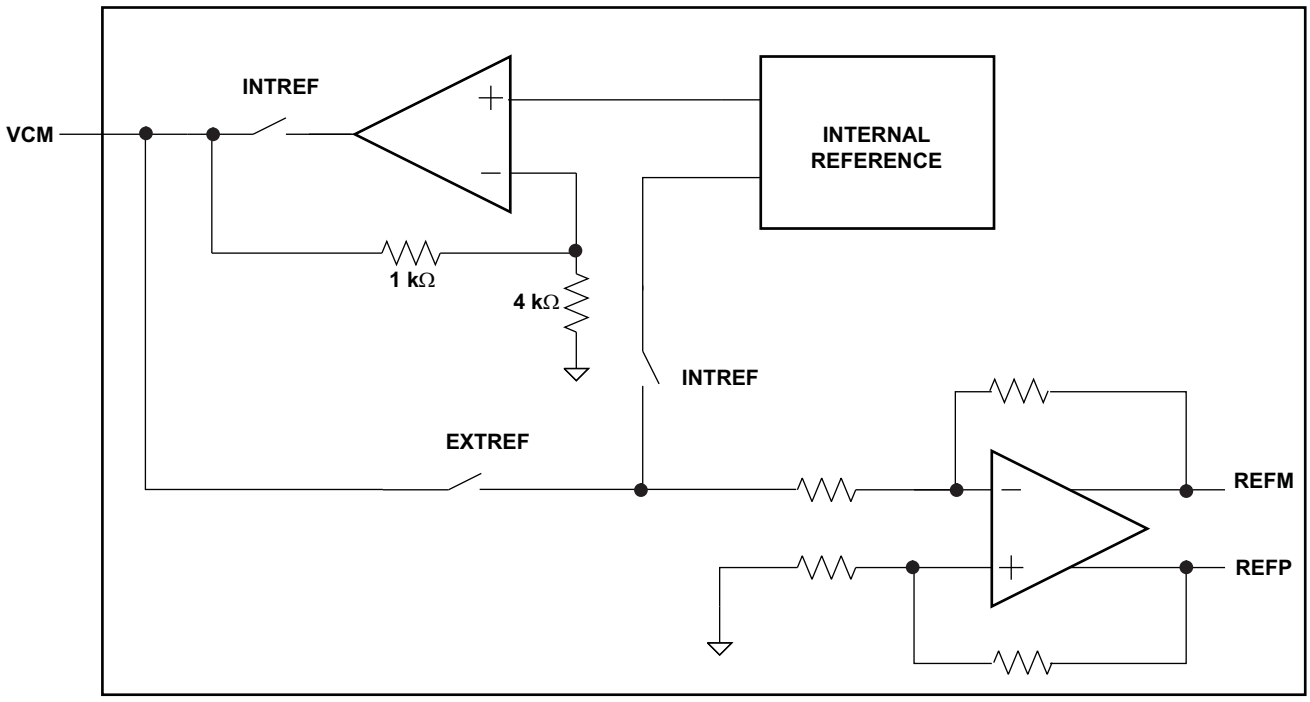



**Figure 41. Reference Section**

### Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on the VCM pin, which can be used to externally bias the analog input pins.

### External Reference

When the device is in external reference mode, VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 1.

$$\text{Full−scale differential input pp} = (\text{Voltage forced on VCM}) \times 1.33 \quad (1)$$

In this mode, the 1.5-V common-mode voltage to bias the input pins has to be generated externally. There is no change in performance compared to internal reference mode.

## COARSE GAIN AND PROGRAMMABLE FINE GAIN

The ADS6142 includes gain settings that can be used to improve SFDR performance (compared to 0 dB gain mode). The gain settings are 3.5 dB coarse gain and 0 dB to 6 dB programmable fine gain. For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 15.

The coarse gain is a fixed setting of 3.5 dB and is designed to improve SFDR with little degradation in SNR. The fine gain is programmable in 1 dB steps from 0 dB to 6 dB. With fine gain, SFDR improvement is also achieved, but at the expense of SNR (there is about 1 dB SNR degradation for every 1 dB of fine gain).

So, the fine gain can be used to trade-off between SFDR and SNR. The coarse gain makes it possible to get the best SFDR but without losing SNR significantly. At high input frequencies, the gains are especially useful as the SFDR improvement is significant with marginal degradation in SINAD. The gains can be programmed using the register bits **<COARSE GAIN>** (see Table 7) and **<FINE GAIN>** (see Table 12). Note that the default gain after reset is 0 dB.

**Table 15. Full-Scale Range Across Gains**

| GAIN, dB | TYPE | FULL-SCALE RANGE, $V_{PP}$ |
|---|---|---|
| 0 | Default after reset | 2.00 |
| 3.5 | Coarse setting (fixed) | 1.34 |
| 1 | Fine gain (programmable) | 1.78 |
| 2 | | 1.59 |
| 3 | | 1.42 |
| 4 | | 1.26 |
| 5 | | 1.12 |
| 6 | | 1.00 |

## CLOCK INPUT

The clock inputs of the ADS6142 can be driven differentially (SINE, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between configurations. The common-mode voltage of the clock inputs is set to VCM using internal 5-kΩ resistors as shown in Figure 42. This allows the use of transformer-coupled drive circuits for the sine wave clock, or ac-coupling for the LVPECL, LVDS clock sources (see Figure 44 and Figure 45).

For best performance, it is recommended to drive the clock inputs differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.1-µF capacitors, as shown in Figure 44. A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 45.

For high input frequency sampling, a clock source with very low jitter is recommended. Band-pass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

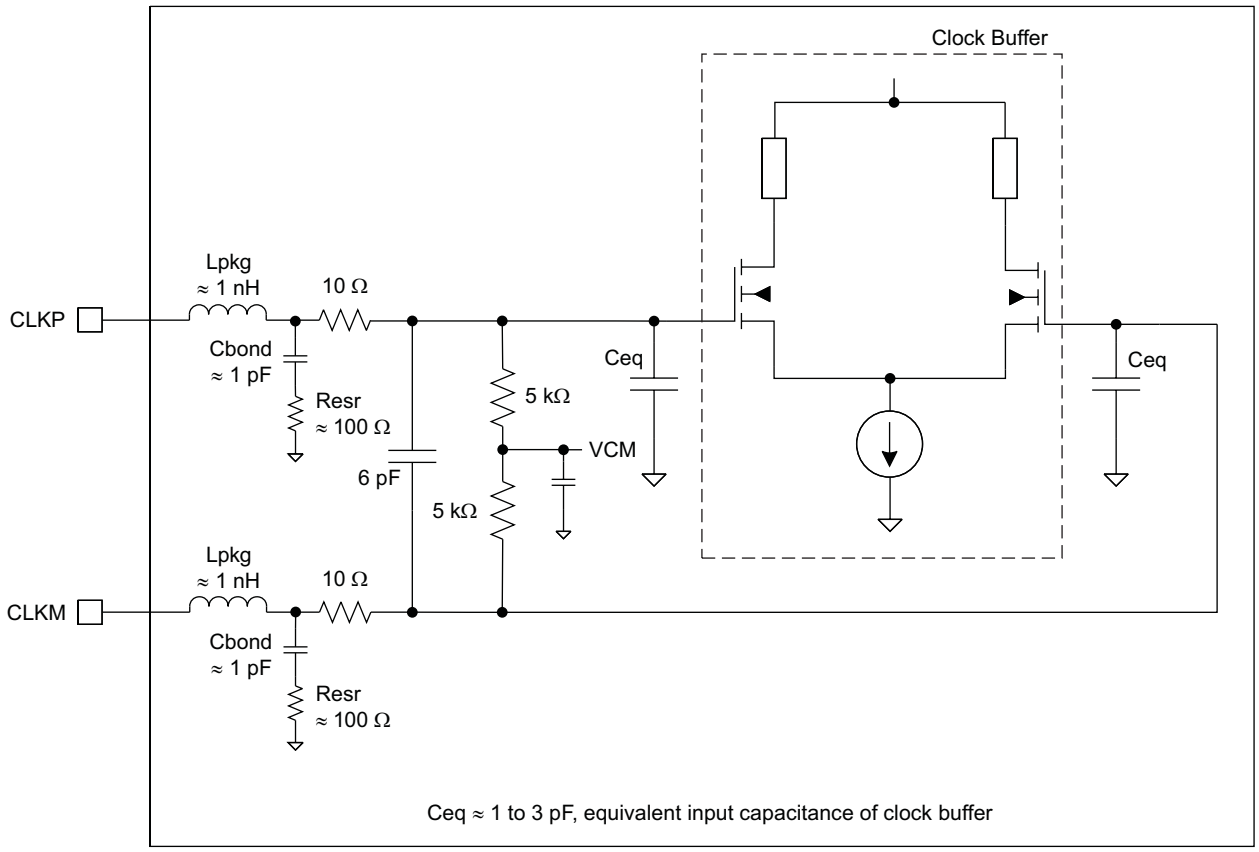



**Figure 42. Internal Clock Buffer**

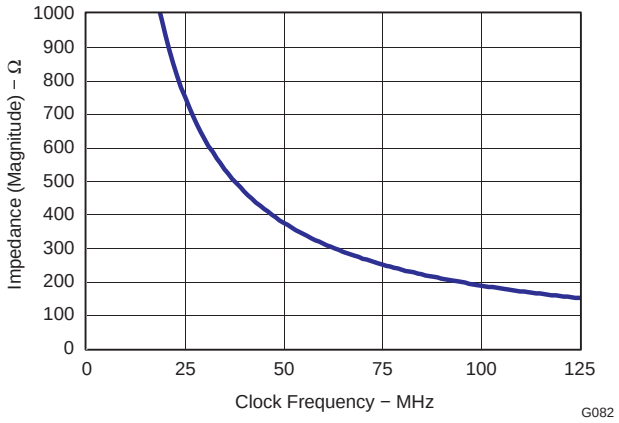



**Figure 43. Clock Buffer Input Impedance**

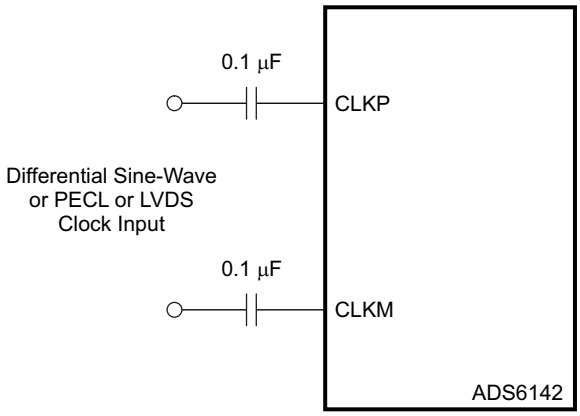



**Figure 44. Differential Clock Driving Circuit**

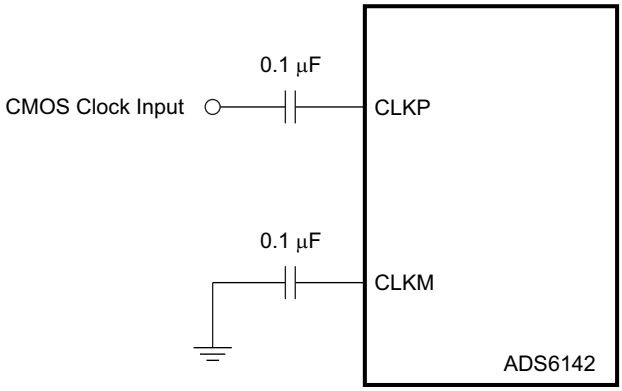



**Figure 45. Single-Ended Clock Driving Circuit**

## POWER-DOWN MODES

The ADS6142 has four power-down modes – global power down, standby, output buffer disable, and input clock stopped. These modes can be set using the serial interface or using the parallel interface (pins SDATA and PDN).

**Table 16. Power-Down Modes**

| POWER-DOWN MODES | PARALLEL INTERFACE | | SERIAL INTERFACE REGISTER BIT (Table 7) | TOTAL POWER, mW | WAKE-UP TIME (to valid data) |
|---|---|---|---|---|---|
| | SDATA | PDN | | | |
| **Normal operation** | Low | Low | <**PDN OBUF**>=0 and <**STBY**>=0 | 417 | - |
| **Standby** | Low | High | <**PDN OBUF**>=0 and <**STBY**>=1 | 72 | Slow (15 µs) |
| **Output buffer disable** | High | Low | <**PDN OBUF**>=1 and <**STBY**>=0 | 408 | Fast (200 ns) |
| **Global power down** | High | High | <**PDN OBUF**>=1 and <**STBY**>=1 | 30 | Slow (15 µs) |

### Global Power Down

In this mode, the A/D converter, internal references, and the output buffers are powered down and the total power dissipation reduces to about 30 mW. The output buffers are in a high-impedance state. The wake-up time from the global power down to output data becoming valid in normal mode is a maximum of 50 µs. Note that after coming out of global power down, optimum performance is achieved after the internal reference voltages have stabilized (about 1 ms).

### Standby

Only the A/D converter is powered down and total power dissipation is approximately 72 mW. The wake-up time from standby to output data becoming valid is a maximum of 50 µs.

### Output Buffer Disable

The data output buffers can be disabled, reducing total power to about 408 mW. With the buffers disabled, the outputs are in a high-impedance state. The wake-up time from this mode to data becoming valid in normal mode is a maximum of 500 ns in LVDS mode and 200 ns in CMOS mode.

### Input Clock Stop

The converter enters this mode when the input clock frequency falls below 1 MSPS. Power dissipation is approximately 120 mW, and the wake-up time from this mode to data becoming valid in normal mode is a maximum of 50 µs.

### Power Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

## DIGITAL OUTPUT INTERFACE

The ADS6142 outputs 14 data bits together with an output clock. The output interface is either parallel CMOS or DDR LVDS voltage levels and can be selected using the serial register bit **<LVDS CMOS>** or parallel pin SEN.

### Parallel CMOS Interface

In CMOS mode, the output buffer supply (DRVDD) can be operated over a wide range from 1.8 V to 3.3 V (typical). Each data bit is output on a separate pin as a CMOS voltage level, every clock cycle.

For DRVDD ≥ 2.2 V, it is recommended to use the CMOS output clock (CLKOUT) to latch data in the receiving chip. The rising edge of CLKOUT can be used to latch data in the receiver, even at the highest sampling speed (125 MSPS). It is recommended to minimize the load capacitance seen by the data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

For DRVDD < 2.2 V, it is recommended to use an external clock (for example, input clock delayed to get desired setup/hold times).

#### *Output Clock Position Programmability*

There is an option to shift (delay) the output clock position so that the setup time increases by 400 ps (typical, with respect to the default timings specified). This may be useful if the receiver needs more setup time, especially at high sampling frequencies. This can be programmed using the serial interface register bit **<CLKOUT_POSN>** (Table 8).

#### *Output Buffer Strength Programmability*

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, the ADS6142 CMOS output buffers are designed with a controlled drive strength for the best SNR. The default drive strength also ensures a wide data stable window for load capacitances up to 5 pF and a DRVDD supply voltage ≥ 2.2 V.

To ensure a wide data stable window for load capacitances > 5 pF, there is an option to increase the drive strength using the serial interface (**<DRIVE STRENGTH>**, see Table 14). Note that for a DRVDD supply voltage < 2.2 V, it is recommended to use the maximum drive strength (for any value of load capacitance).

#### *CMOS Mode Power Dissipation*

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

$$\text{Digital current due to CMOS output switching} = C_L \times \text{DRVDD} \times (N \times F_{AVG}) \quad (2)$$

where $C_L$ = load capacitance, $N \times F_{AVG}$ = average number of output bits switching

Figure 30 shows the current with various load capacitances across sampling frequencies with a 2-MHz analog input frequency.

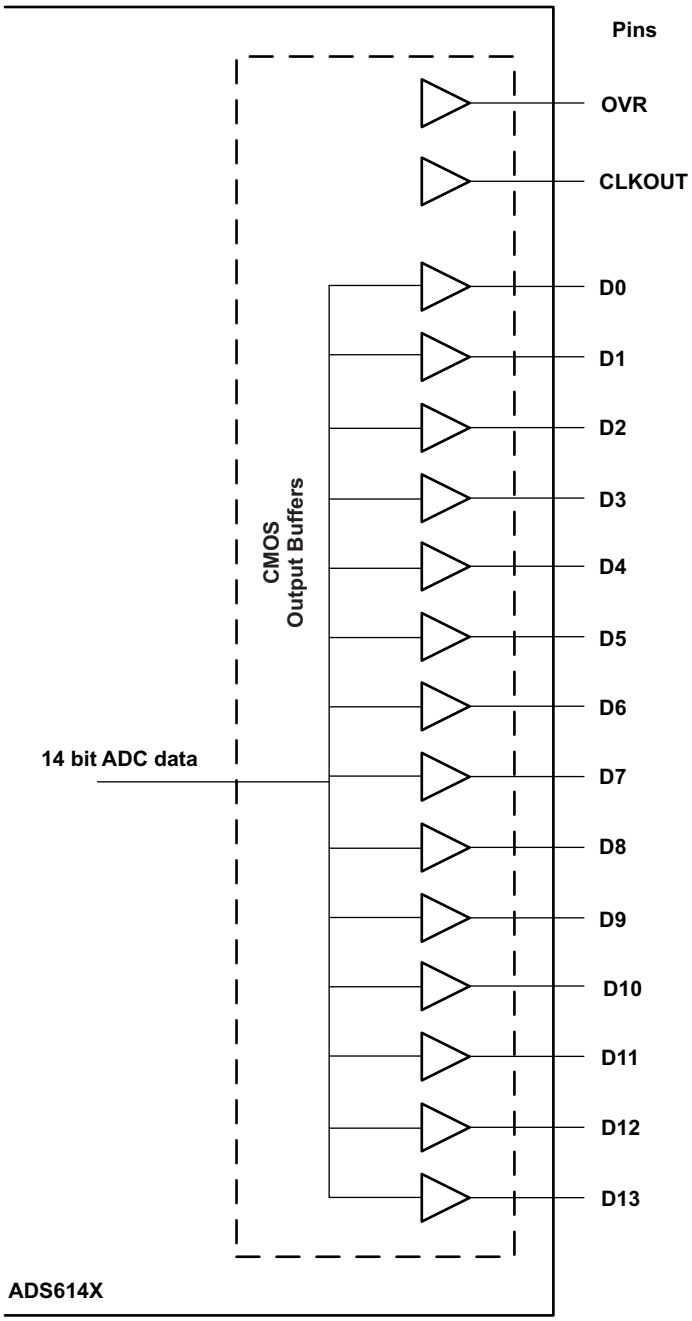



**Figure 46. CMOS Output Buffers**

### DDR LVDS Interface

The LVDS interface works only with a 3.3-V DRVDD supply. In this mode, the 14 data bits and the output clock are available as LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair every clock cycle (DDR - Double Data Rate, see Figure 47 ). So, there are 7 LVDS output pairs for the 14 data bits and 1 LVDS output pair for the output clock.

#### *LVDS Buffer Current Programmability*

The default LVDS buffer output current is 3.5 mA. When terminated by 100 Ω, this results in a 350-mV single-ended voltage swing (700-$mV_{PP}$ differential swing). The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.75 mA (register bits **<LVDS CURRENT>**, see Table 13). In addition, there is a current double mode, where this current is doubled for the data and output clock buffers (register bits **<CURRENT DOUBLE>**, see Table 13).

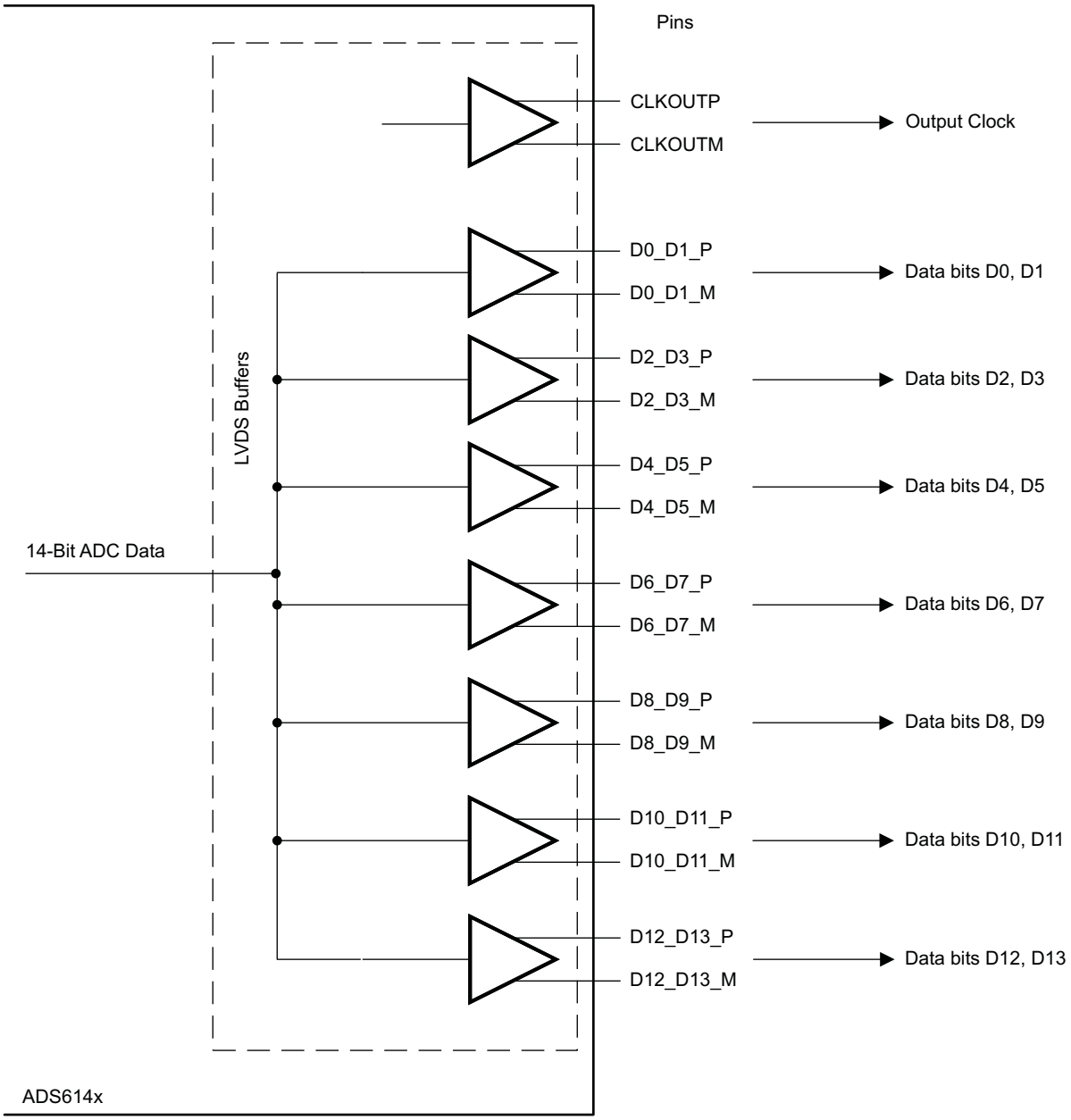



**Figure 47. DDR LVDS Outputs**

Even data bits D0, D2, D4, D6, D8, D10, and D12 are output at the rising edge of CLKOUTP and the odd data bits D1, D3, D5, D7, D9, D11, and D13 are output at the falling edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all 14 data bits (see Figure 48).

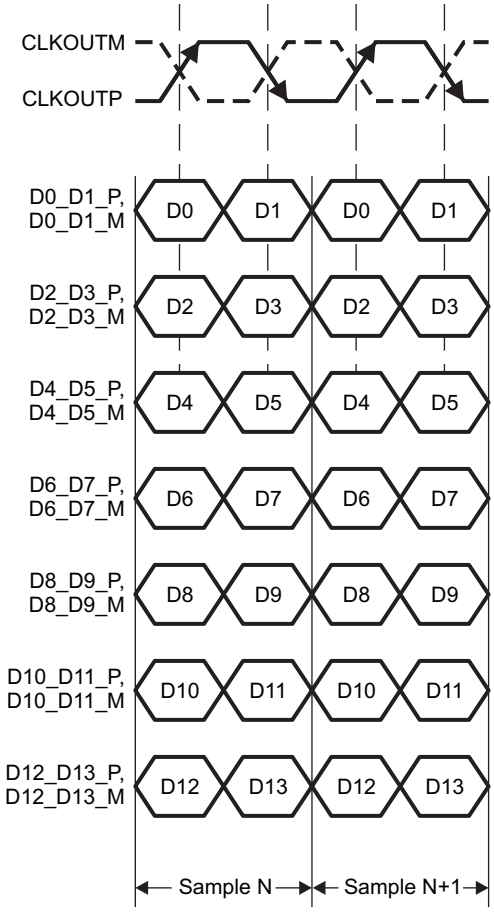



**Figure 48. DDR LVDS Interface**

### *LVDS Buffer Internal Termination*

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. The termination resistances available are – 300 Ω, 185 Ω, and 150 Ω (nominal with ±20% variation). Any combination of these three terminations can be programmed; the effective termination is the parallel combination of the selected resistances. This results in eight effective terminations from open (no termination) to 65 Ω.

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100-Ω internal and 100-Ω external termination, the voltage swing at the receiver end is halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode. Figure 49 and Figure 50 compare the LVDS eye diagrams without and with internal termination (100 Ω). With internal termination, the eye looks clean even with 10-pF load capacitance (from each output pin to ground). The termination is programmed using register bits <**DATA TERM**> and <**CLKOUT TERM**> (see Table 13).

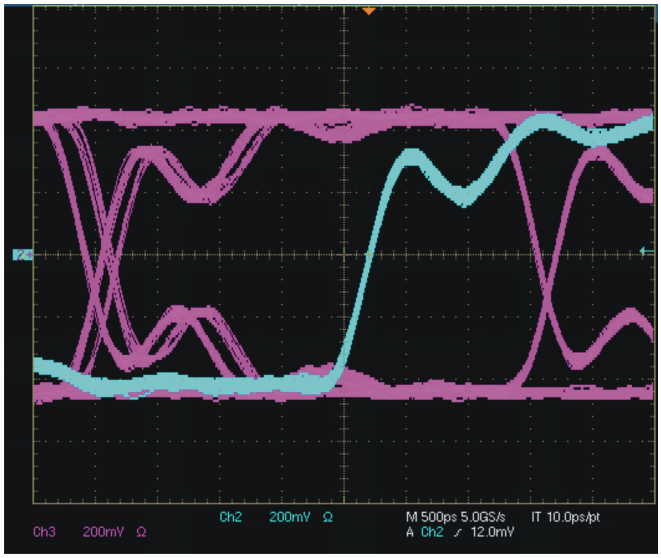



**Figure 49. LVDS Eye Diagram - No Internal Termination**
**5-pF Load Capacitance**
**Blue Trace - Output Clock (CLKOUT)**
**Pink Trace - Output Data**

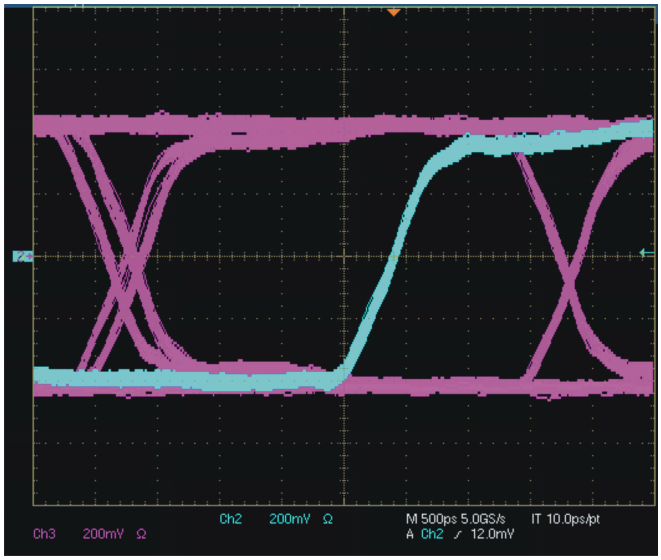



**Figure 50. LVDS Eye Diagram with 100-Ω Internal Termination**
**10-pF Load Capacitance**
**Blue Trace - Output Clock (CLKOUT)**
**Pink Trace - Output Data**

### Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the parallel control pin SEN or the serial interface register bit **<DATA FORMAT>** (see Table 10).

### Output Timings

The tables below show the timings at lower sampling frequencies.

**Table 17. Timing Characteristics at Lower Sampling Frequencies (1) (2)**

| $F_S$, MSPS | $t_{su}$ DATA SETUP TIME, ns | | | $t_h$ DATA HOLD TIME, ns | | | $t_{PDI}$ CLOCK PROPAGATION DELAY, ns | | |
|---|---|---|---|---|---|---|---|---|---|
| | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX |
| **CMOS INTERFACE, DRVDD = 2.5 V to 3.3 V** | | | | | | | | | |
| 40 | | 12.8 | | | 11.2 | | | 6.5 | |
| 20 | | 25 | | | 23 | | | | |
| 10 | | 50 | | | 48 | | | | |
| **DDR LVDS INTERFACE, DRVDD = 3.3 V** | | | | | | | | | |
| 40 | | 10.8 | | | 1.7 | | | 5.8 | |
| 20 | | 23 | | | 1.7 | | | 6.5 | |
| 10 | | 48 | | | 1.7 | | | 6.5 | |

(1) Timing parameters are specified by design and not tested in production.
(2) Timings are specified with default output buffer drive strength and $C_L$= 5 pF.

## BOARD DESIGN CONSIDERATIONS

### Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide (SLWU028) for details on layout and grounding.

### Supply Decoupling

As the ADS6142 already includes internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

It is recommended to use separate supplies for the analog and digital supply pins to isolate digital switching noise from sensitive analog circuitry. In case only a single 3.3-V supply is available, it should be routed first to AVDD. It can then be tapped and isolated with a ferrite bead (or inductor) with decoupling capacitor, before being routed to DRVDD.

### Exposed Thermal Pad

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes ***QFN Layout Guidelines*** (SLOA122) and ***QFN/SON PCB Attachment*** (SLUA271).

## DEFINITION OF SPECIFICATIONS

### Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

### Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

### Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

### Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

### Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

### Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

### Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

### Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

### Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

### Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

### Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from $T_{MIN}$ to $T_{MAX}$. It is calculated by dividing the maximum deviation of the parameter across the $T_{MIN}$ to $T_{MAX}$ range by the difference $T_{MAX}–T_{MIN}$.

### Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental ($P_S$) to the noise floor power ($P_N$), excluding the power at dc and the first nine harmonics.

$$SNR = 10Log^{10}\frac{P_S}{P_N} \quad (3)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

### Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental ($P_S$) to the power of all the other spectral components including noise ($P_N$) and distortion ($P_D$), but excluding dc.

$$SINAD = 10Log^{10}\frac{P_S}{P_N + P_D} \quad (4)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

### Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (5)$$

### Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental ($P_S$) to the power of the first nine harmonics ($P_D$).

$$THD = 10Log^{10}\frac{P_S}{P_N} \quad (6)$$

THD is typically given in units of dBc (dB to carrier).

### Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

### Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies f1 and f2) to the power of the worst spectral component at either frequency 2f1–f2 or 2f2–f1. IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

### DC Power Supply Rejection Ratio (DC PSRR)

The DC PSSR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

### AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR is the measure of rejection of variations in the supply voltage of the ADC. If $\Delta V_{SUP}$ is the change in the supply voltage and $\Delta V_{OUT}$ is the resultant change in the ADC output code (referred to the input), then

$$PSRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \text{ (Expressed in dBc)} \quad (7)$$

### Common-Mode Rejection Ratio (CMRR)

CMRR is the measure of rejection of variations in the input common-mode voltage of the ADC. If ΔVcm is the change in the input common-mode voltage and $\Delta V_{OUT}$ is the resultant change in the ADC output code (referred to the input), then

$$CMRR = 20Log^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \text{ (Expressed in dBc)} \quad (8)$$

### Voltage Overload Recovery

The number of clock cycles taken to recover to less than 1% error for a 6-dB overload on the analog inputs. A 6-dBFS sine wave at Nyquist frequency is used as the test stimulus.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| ADS6142SKGD1 | ACTIVE | XCEPT | KGD | 0 | 80 | TBD | Call TI | N / A for Pkg Type | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



**OTHER QUALIFIED VERSIONS OF ADS6142-HT :**

- Catalog: ADS6142

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

# 重要声明

德州仪器(TI) 及其下属子公司有权在不事先通知的情况下, 随时对所提供的产品和服务进行更正、修改、增强、改进或其它更改，并有权随时中止提供任何产品和服务。客户在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的硬件产品的性能符合TI 标准保修的适用规范。仅在TI 保证的范围内，且TI 认为有必要时才会使用测试或其它质量控制技术。除非政府做出了硬性规定，否则没有必要对每种产品的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何TI 专利权、版权、屏蔽作品权或其它与使用了TI 产品或服务的组合设备、机器、流程相关的TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是TI 的专利权或其它知识产权方面的许可。

对于TI 的产品手册或数据表，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。在复制信息的过程中对内容的篡改属于非法的、欺诈性商业行为。TI 对此类篡改过的文件不承担任何责任。

在转售TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关TI 产品或服务的明示或暗示授权，且这是非法的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

TI 产品未获得用于关键的安全应用中的授权，例如生命支持应用（在该类应用中一旦TI 产品故障将预计造成重大的人员伤亡），除非各方官员已经达成了专门管控此类使用的协议。购买者的购买行为即表示，他们具备有关其应用安全以及规章衍生所需的所有专业技术和知识，并且认可和同意，尽管任何应用相关信息或支持仍可能由TI 提供，但他们将独力负责满足在关键安全应用中使用其产 品及TI 产品所需的所有法律、法规和安全相关要求。此外，购买者必须全额赔偿因在此类关键安全应用中使用TI 产品而对TI 及其 代表造成的损失。

TI 产品并非设计或专门用于军事/航空应用，以及环境方面的产品，除非TI 特别注明该产品属于“军用”或“增强型塑料”产品。只 有TI 指定的军用产品才满足军用规格。购买者认可并同意，对TI 未指定军用的产品进行军事方面的应用，风险由购买者单独承担，并且独力负责在此类相关使用中满足所有法律和法规要求。

TI 产品并非设计或专门用于汽车应用以及环境方面的产品，除非TI 特别注明该产品符合ISO/TS 16949 要求。购买者认可并同意，如果他们在汽车应用中使用任何未被指定的产品，TI 对未能满足应用所需要求不承担任何责任。

可访问以下URL 地址以获取有关其它TI 产品和应用解决方案的信息：

| | 产品 | | 应用 |
|---|---|---|---|
| 数字音频 | www.ti.com.cn/audio | 通信与电信 | www.ti.com.cn/telecom |
| 放大器和线性器件 | www.ti.com.cn/amplifiers | 计算机及周边 | www.ti.com.cn/computer |
| 数据转换器 | www.ti.com.cn/dataconverters | 消费电子 | www.ti.com/consumer-apps |
| DLP® 产品 | www.dlp.com | 能源 | www.ti.com/energy |
| DSP - 数字信号处理器 | www.ti.com.cn/dsp | 工业应用 | www.ti.com.cn/industrial |
| 时钟和计时器 | www.ti.com.cn/clockandtimers | 医疗电子 | www.ti.com.cn/medical |
| 接口 | www.ti.com.cn/interface | 安防应用 | www.ti.com.cn/security |
| 逻辑 | www.ti.com.cn/logic | 汽车电子 | www.ti.com.cn/automotive |
| 电源管理 | www.ti.com.cn/power | 视频和影像 | www.ti.com.cn/video |
| 微控制器 (MCU) | www.ti.com.cn/microcontrollers | | |
| RFID 系统 | www.ti.com.cn/rfidsys | | |
| OMAP 机动性处理器 | www.ti.com/omap | | |
| 无线连通性 | www.ti.com.cn/wirelessconnectivity | | |
| | 德州仪器在线技术支持社区 | www.deyisupport.com | |

邮寄地址： 上海市浦东新区世纪大道 1568 号，中建大厦 32 楼 邮政编码： 200122