10 位、1.25-MSPS 微功耗小型化 SAR 模数转换器

查询样品: **ADS7887M**

特性

- **1.25-MHz** 采样速率串行器件
- **10** 位分辨率
- 零延迟
- **25-MHz** 串行接口
- 电源范围：**2.35 V** 至 **5.25 V**
- 在 **1.25 MSPS** 采样速率下的典型功耗：
  - **3.8 mW**，在 **3-V** V_{DD}
  - **8 mW**，在 **5-V** V_{DD}
- **±0.35 LSB INL**、**DNL**
- **61-dB SINAD**、**–84-dB THD**
- 单极输入范围： **0 V** 至 V_{DD}
- 断电电流：**10 μA**（最大值）
- 宽输入带宽：**15 MHz**（在 **3 dB** 时）
- **6** 引脚**SOT23** 封装

应用

- 射频通信中的基带转换器
- 数字驱动器中的电机电流**/**总线电压传感器
- 光网络（基于 **DWDM**、**MEMS** 的开关）
- 光传感器
- 电池供电型系统
- 医疗仪表
- 高速数据采集系统
- 高速闭环系统

说明

ADS7887 是一款 10 位、1.25-MSPS 模数转换器 (ADC)。 该器件包括一个基于电容器的 SAR A/D 转换器及固有的采样及保持功能。 串行接口受控于$\overline{\text{CS}}$ 和 SCLK 信号，以实现与微处理器及 DSP 的无缝连接。 输入信号利用 CS 的下降沿进行采样 $\overline{\text{CS}}$，而 SCLK 则用于转换及串行数据输出。

该器件可在 2.35 V 至 5.25 V 的宽电源范围内工作。这款器件的低功耗特性使其成为电池供电型应用的合适之选。另外，该器件还具有一种节能的断电功能，可在器件工作于较低转换速度时使用。

器件数字输入的高电平未被限制在器件的 V_{DD}时，器件会自动进入旁路模式。 这意味着，当器件电源为 2.35V 时，数字输入可变至高达 5.25V。当数字信号来自具有不同电源电平的其他电路时，这种特性很有用处。 而且，这还放宽了对上电排序的限制。

ADS7887 采用 6 引脚 SOT23 封装，并具有 –55°C 至 125°C 的工作温度范围。

English Data Sheet: SLAS750A

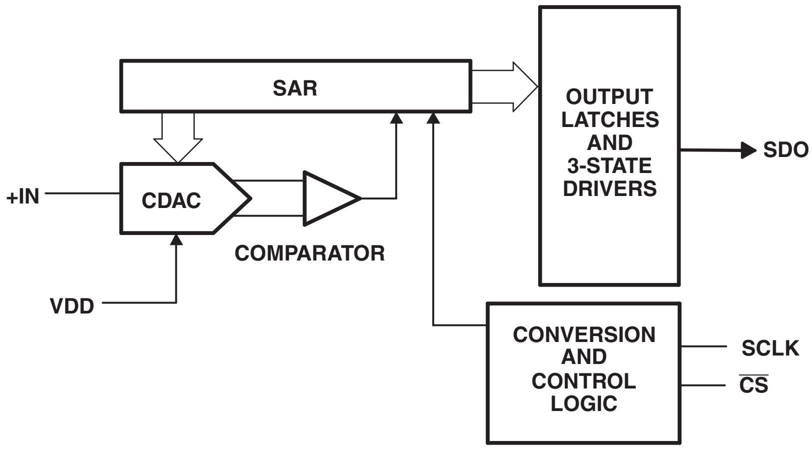
这些装置包含有限的内置 ESD 保护。

存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOT-23 – DBV	Reel of 250	ADS7887MDBVT	BCNM

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



ABSOLUTE MAXIMUM RATINGS(1)

+IN to AGND		–0.3 V to $+V_{DD}$ +0.3 V
$+V_{DD}$ to AGND		–0.3 V to 7.0 V
Digital input voltage to GND		–0.3V to (7.0 V)
Digital output to GND		–0.3 V to ($+V_{DD}$ + 0.3 V)
Operating temperature range		–55°C to 125°C
Storage temperature range		–65°C to 150°C
Junction temperature (T_J Max)		150°C
Power dissipation		(T_J Max–T_A)/θ_{JA}
θ_{JA} Thermal impedance(2)		295.2°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
(2) The package thermal impedance is calculated in accordance with JESD 51-7, except for through-hole packages, which use a trace length of zero.

ELECTRICAL SPECIFICATIONS

$+V_{DD}$ = 2.35 V to 5.25 V, T_A = –55°C to 125°C, f_{sample} = 1.25 MHz

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
	Full-scale input voltage span[1]		0		V_{DD}	V
	Absolute input voltage range	+IN	–0.20		V_{DD}+0.20	V
C_i	Input capacitance[2]			21		pF
I_{lkg}	Input leakage current	T_A = 125°C		40		nA
SYSTEM PERFORMANCE						
	Resolution			10		Bits
	No missing codes		10			Bits
INL	Integral nonlinearity		–1.2	±0.35	1.2	LSB[3]
DNL	Differential nonlinearity		–1[4]	±0.35	1.35	LSB
E_O	Offset error[5] [6] [7]		–2.5	±0.5	2.5	LSB
E_G	Gain error[6]		–2	±0.5	2	LSB
SAMPLING DYNAMICS						
	Conversion time	25-MHz SCLK	530	560		ns
	Acquisition time		260			ns
	Maximum throughput rate	25-MHz SCLK			1.25	MHz
	Aperture delay			5		ns
	Step response			160		ns
	Overvoltage recovery			160		ns
DYNAMIC CHARACTERISTICS						
THD	Total harmonic distortion[8]	100 kHz		–84	–67	dB
SINAD	Signal-to-noise and distortion	100 kHz	59	61		dB
SFDR	Spurious free dynamic range	100 kHz	70	81		dB
	Full power bandwidth	At –3 dB		15		MHz
DIGITAL INPUT/OUTPUT						
Logic family — CMOS						
V_{IH}	High-level input voltage	VDD = 2.35 V to 5.25 V	V_{DD} – 0.4		5.25	V
V_{IL}	Low-level input voltage	V_{DD} = 5 V			0.8	V
		V_{DD} = 3 V			0.4	
V_{OH}	High-level output voltage	At I_{source} = 200 µA	V_{DD}–0.2			V
V_{OL}	Low-level output voltage	At I_{sink} = 200 µA			0.4	
POWER SUPPLY REQUIREMENTS						
$+V_{DD}$	Supply voltage		2.35	3.3	5.25	V
	Supply current (normal mode)	At V_{DD} = 2.35 V to 5.25 V, 1.25-MHz throughput			2	mA
		At V_{DD} = 2.35 V to 5.25 V, static state			1.5	
	Power-down state supply current	SCLK off			10	µA
		SCLK on (25 MHz)			200	
	Power dissipation at 1.25 MHz throughput	V_{DD} = 5 V		8	10	mW
		V_{DD} = 3 V		3.8	6	

(1) Ideal input span; does not include gain or offset error.
(2) Refer 图 21 for details on sampling circuit
(3) LSB means least significant bit
(4) Exclusive
(5) Measured relative to an ideal full-scale input
(6) Offset error and gain error ensured by characterization.
(7) First transition of 000H to 001H at 0.5 × ($V_{ref}/2^{10}$)
(8) Calculated on the first nine harmonics of the input frequency

ELECTRICAL SPECIFICATIONS (接下页)

$+V_{DD}$ = 2.35 V to 5.25 V, T_A = –55°C to 125°C, f_{sample} = 1.25 MHz

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power dissipation in static state	V_{DD} = 5 V		5.5	7.5	mW
	V_{DD} = 3 V		3	4.5	
Power down time				0.1	µs
Power up time				0.8	µs
Invalid conversions after power up				1	
TEMPERATURE RANGE					
Specified performance		–55		125	°C

TIMING REQUIREMENTS (see 图 1)

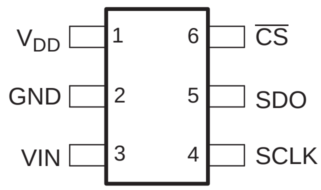
All specifications typical at T_A = –55°C to 125°C, V_{DD} = 2.35 V to 5.25 V, unless otherwise specified.

	PARAMETER	TEST CONDITIONS[(1)]	MIN	TYP	MAX	UNIT
t_{conv}	Conversion time	V_{DD} = 3 V			14 × t_{SCLK}	ns
		V_{DD} = 5 V			14 × t_{SCLK}	
t_q	Minimum quiet time needed from bus 3-state to start of next conversion	V_{DD} = 3 V	40			ns
		V_{DD} = 5 V	40			
t_{d1}	Delay time, $\overline{CS}$ low to first data (0) out	V_{DD} = 3 V		15	25	ns
		V_{DD} = 5 V		13	25	
t_{su1}	Setup time, $\overline{CS}$ low to SCLK low	V_{DD} = 3 V	10			ns
		V_{DD} = 5 V	10			
t_{d2}	Delay time, SCLK falling to SDO	V_{DD} = 3 V		15	25	ns
		V_{DD} = 5 V		13	25	
t_{h1}	Hold time, SCLK falling to data valid[(2)]	V_{DD} < 3 V	7			ns
		V_{DD} > 5 V	5.5			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state	V_{DD} = 3 V		10	25	ns
		V_{DD} = 5 V		8	20	
t_{w1}	Pulse duration, $\overline{CS}$	V_{DD} = 3 V	25	40		ns
		V_{DD} = 5 V	25	40		
t_{d4}	Delay time, $\overline{CS}$ high to SDO 3-state	V_{DD} = 3 V		17	30	ns
		V_{DD} = 5 V		15	25	
t_{wH}	Pulse duration, SCLK high	V_{DD} = 3 V	0.4 × t_{SCLK}			ns
		V_{DD} = 5 V	0.4 × t_{SCLK}			
t_{wL}	Pulse duration, SCLK low	V_{DD} = 3 V	0.4 × t_{SCLK}			ns
		V_{DD} = 5 V	0.4 × t_{SCLK}			
	Frequency, SCLK	V_{DD} = 3 V			25	MHz
		V_{DD} = 5 V			25	
t_{d5}	Delay time, second falling edge of clock and $\overline{CS}$ to enter in powerdown (use minimum specification to avoid accidently entering powerdown) 图 2	V_{DD} = 3 V	-2		5	ns
		V_{DD} = 5 V	-2		5	
t_{d6}	Delay time, $\overline{CS}$ and 10th falling edge of clock to enter in powerdown (use maximum specification to avoid accidently entering powerdown) 图 2	V_{DD} = 3 V	2		-5	ns
		V_{DD} = 5 V	2		-5	

(1) 3-V Specifications apply from 2.35 V to 3.6 V, and 5-V specifications apply from 4.75 V to 5.25 V.
(2) With 50-pf load.

DEVICE INFORMATION

SOT23 PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	–	Power supply input also acts like a reference voltage to ADC.
GND	2	–	Ground for power supply, all analog and digital signals are referred with respect to this pin.
VIN	3	I	Analog signal input
SCLK	4	I	Serial clock
SDO	5	O	Serial data out
$\overline{CS}$	6	I	Chip select signal, active low

NORMAL OPERATION

The cycle begins with the falling edge of $\overline{CS}$. This point is indicated as **a** in 图 1. With the falling edge of $\overline{CS}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains 4 leading zeros, followed by 10-bit data in MSB first format and padded by 2 lagging zeros.

The falling edge of $\overline{CS}$ clocks out the first zero, and a zero is clocked out on every falling edge of the clock until the third edge. Data is in MSB first format with the MSB being clocked out on the 4th falling edge. Data is padded with two lagging zeros as shown in 图 1. On the 16th falling edge of SCLK, SDO goes to the 3-state condition. The conversion ends on the 14th falling edge of SCLK. The device enters the acquisition phase on the first rising edge of SCLK after the 13th falling edge. This point is indicated by **b** in 图 1.

$\overline{CS}$ can be asserted (pulled high) after 16 clocks have elapsed. Do not start the next conversion by pulling $\overline{CS}$ low until the end of the quiet time (t_q) after SDO goes to 3-state. To continue normal operation, do not pull $\overline{CS}$ high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to power down mode for more details.) $\overline{CS}$ going high any time after the conversion start aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.25 V when the device supply is 2.35 V. This feature is useful when digital signals are coming from another circuit with different supply levels. Also, this relaxes the restriction on power up sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in the SPECIFICATIONS table.

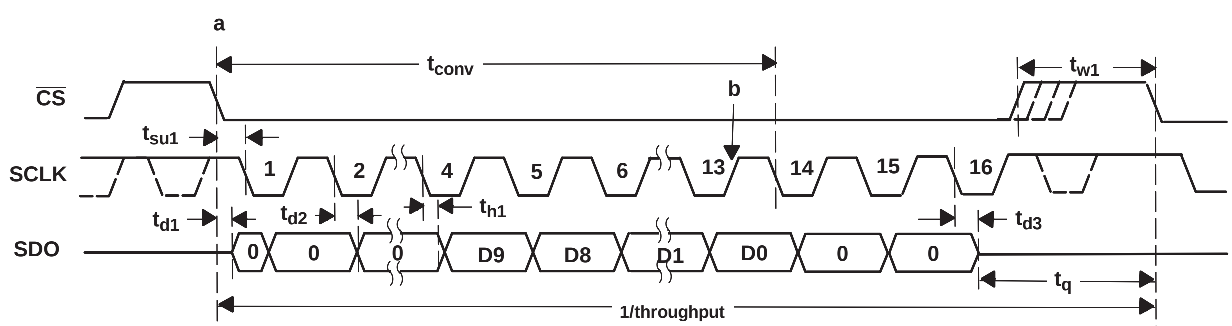


图 1. Interface Timing Diagram

POWER-DOWN MODE

The device enters power down mode if $\overline{CS}$ goes high anytime after the second SCLK falling edge to before the tenth SCLK falling edge. Ongoing conversion stops and SDO goes to 3-state under this power-down condition as shown in 图 2.

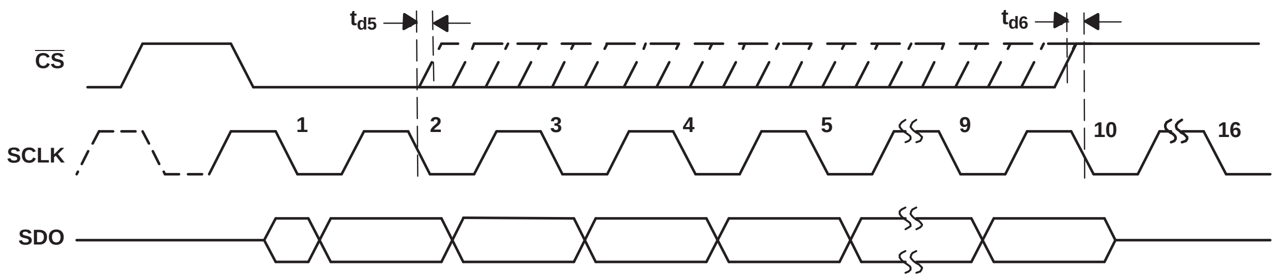


图 2. Entering Power Down Mode

A dummy cycle with $\overline{CS}$ low for more than ten SCLK falling edges brings the device out of power-down mode. For the device to come to the fully powered up condition it takes 0.8 µs. $\overline{CS}$ can be pulled high any time after the 10th falling edge as shown in 图 3. It is not necessary to continue until the 16th clock if the next conversion starts 0.8 µs after $\overline{CS}$ going low of the dummy cycle and the quiet time (t_q) condition is met.

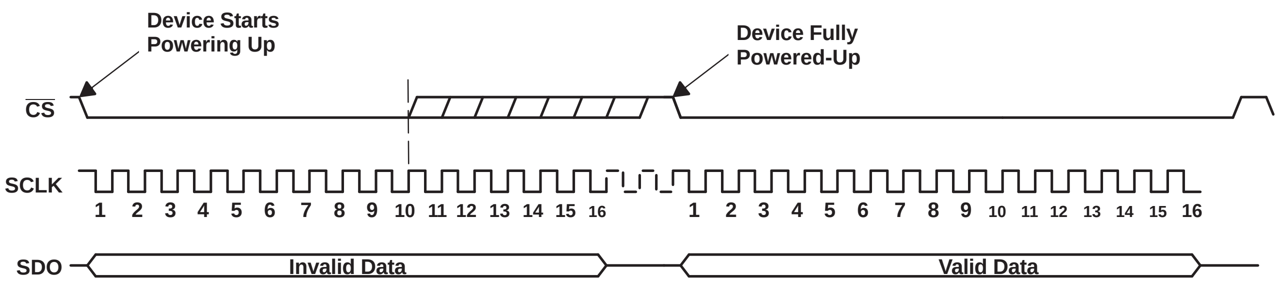


图 3. Exiting Power Down Mode

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

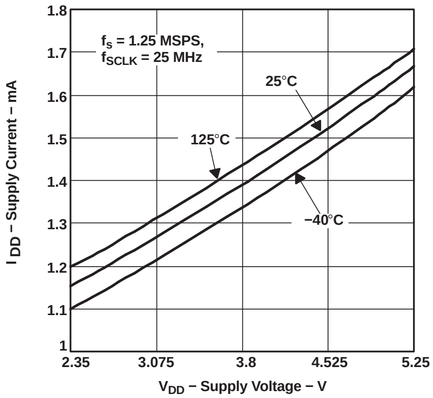


图 4.

SUPPLY CURRENT vs SCLK FREQUENCY

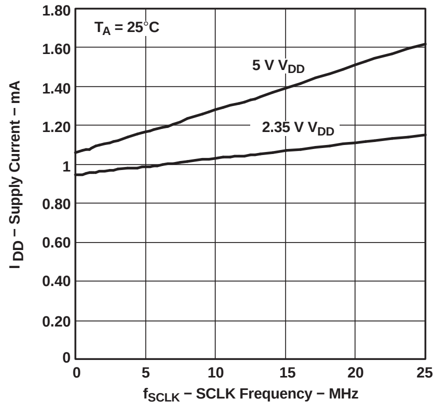


图 5.

SUPPLY CURRENT vs SAMPLE RATE

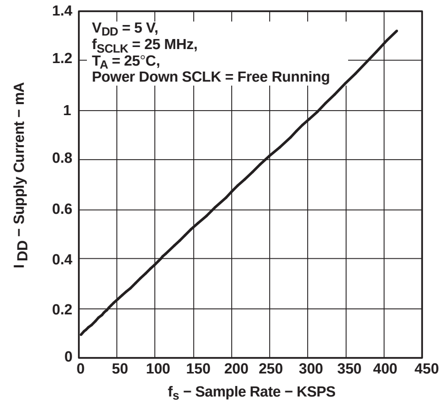


图 6.

ANALOG INPUT LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

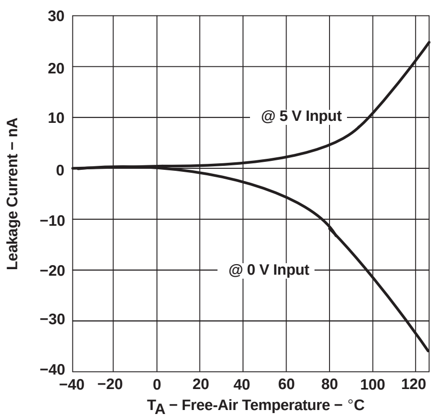


图 7.

SIGNAL-TO-NOISE AND DISTORTION vs INPUT FREQUENCY

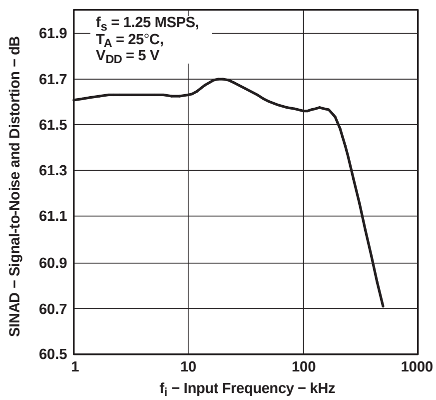


图 8.

SIGNAL-TO-NOISE AND DISTORTION vs SUPPLY VOLTAGE

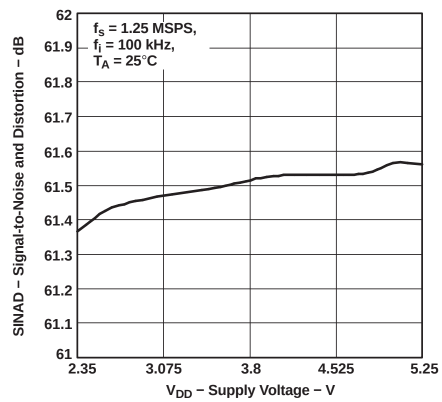


图 9.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

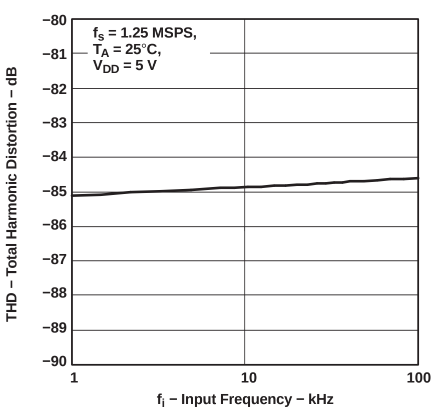


图 10.

TOTAL HARMONIC DISTORTION vs SUPPLY VOLTAGE

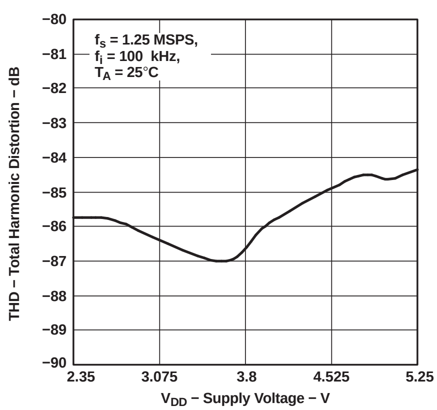


图 11.

SPURIOUS FREE DYNAMIC RANGE vs INPUT FREQUENCY

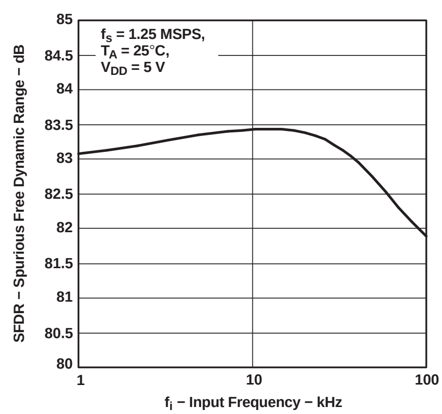


图 12.

TYPICAL CHARACTERISTICS (接下页)

SPURIOUS FREE DYNAMIC RANGE
vs
SUPPLY VOLTAGE

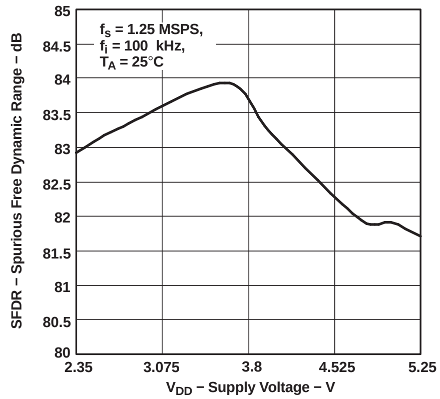


图 13.

OFFSET ERROR
vs
SUPPLY VOLTAGE

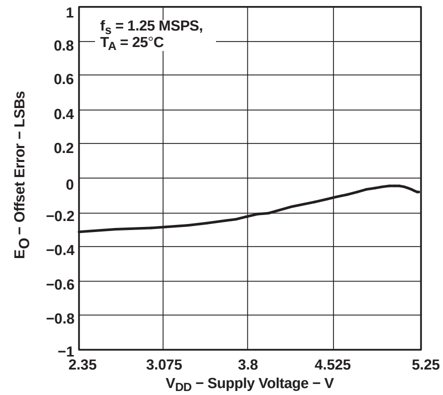


图 14.

OFFSET ERROR
vs
FREE-AIR TEMPERATURE

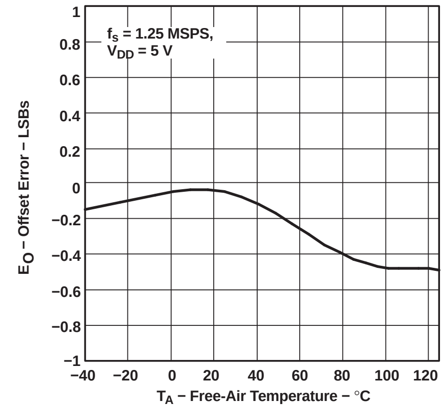


图 15.

GAIN ERROR
vs
SUPPLY VOLTAGE

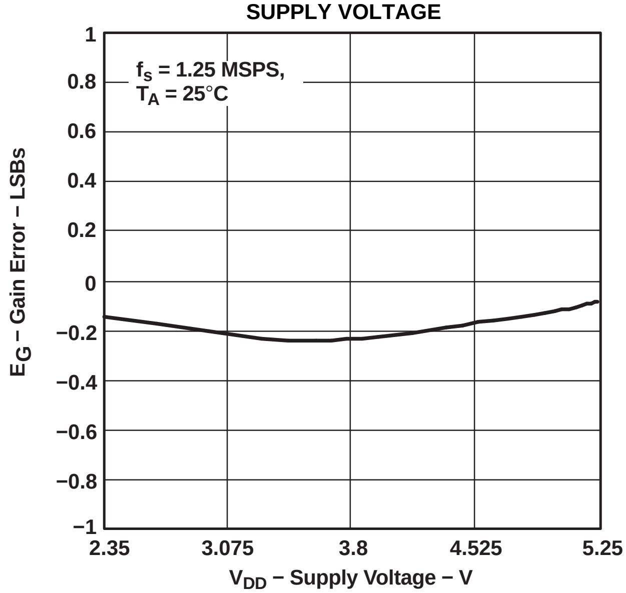


图 16.

GAIN ERROR
vs
FREE-AIR TEMPERATURE

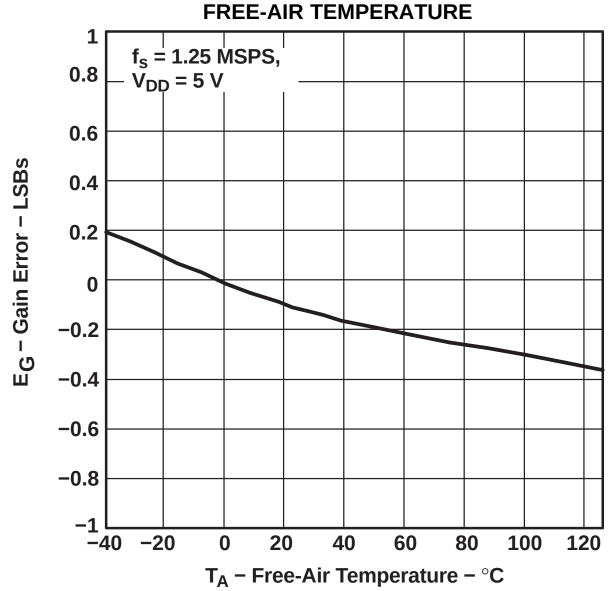


图 17.

TYPICAL CHARACTERISTICS (接下页)

DNL

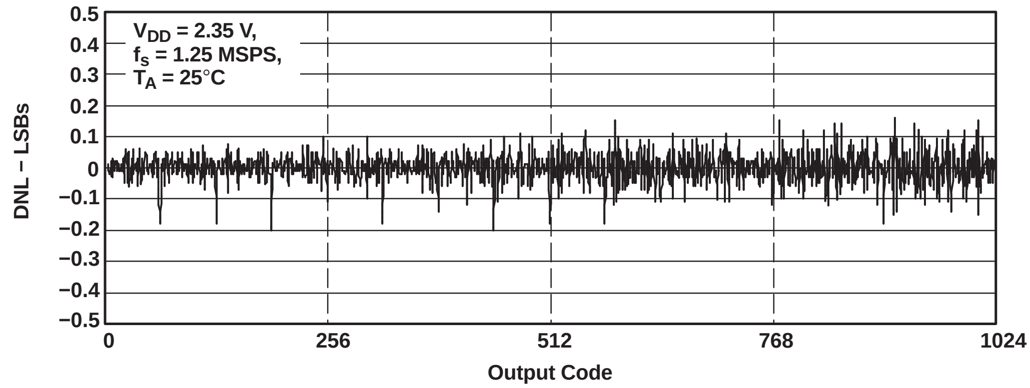


图 18.

INL

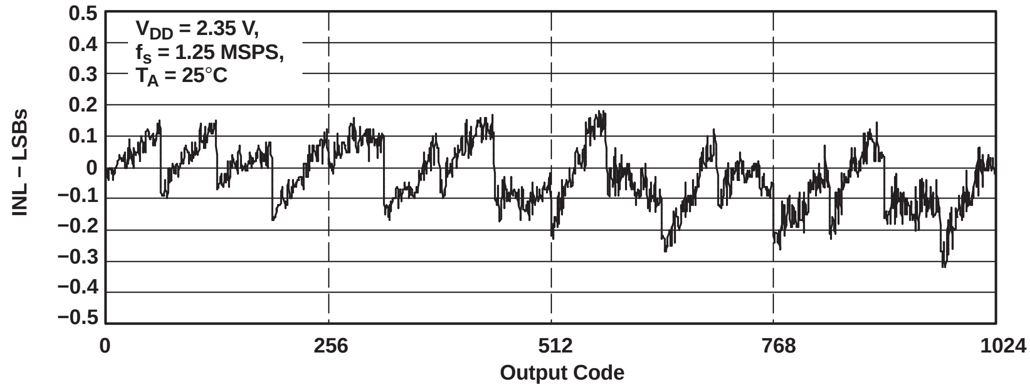


图 19.

FFT

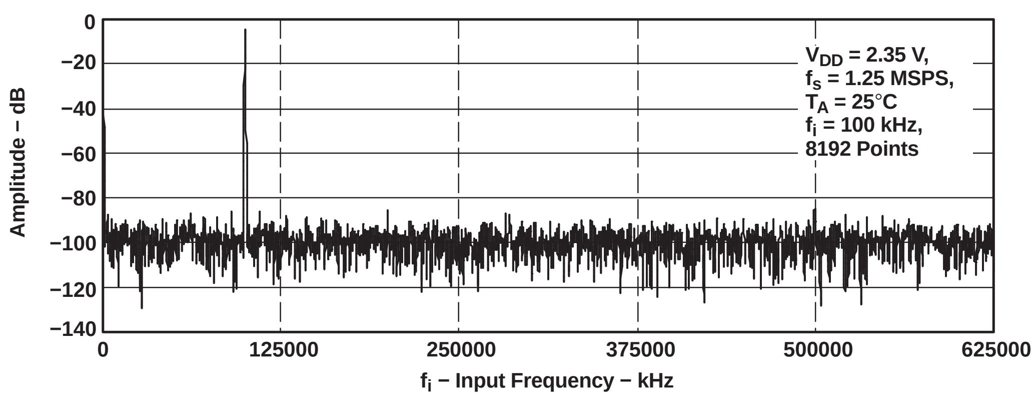


图 20.

APPLICATION INFORMATION

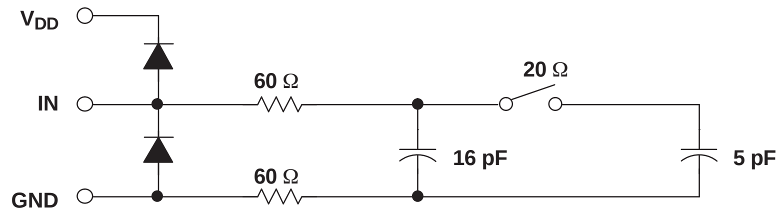


图 21. Typical Equivalent Sampling Circuit

Driving the VIN and V_{DD} Pins

The VIN input to the ADS7887 should be driven with a low-impedance source. In most cases, additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer helps achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the ADS7887 A/D converter is derived internally from the supply voltage. The device offer limited low-pass filtering functionality on-chip. The supply to the converter should be driven with a low-impedance source and should be decoupled to ground. A 1-μF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide low-impedance traces should be used to connect the capacitor to the pins of the device. The ADS7887 draws very little current from the supply lines. The supply line can be driven:

- Directly from the system supply.
- From a reference output from a low-drift and low-dropout reference voltage generator like REF3030 or REF3130. The ADS7887 can operate off a wide range of supply voltages. The actual choice of the reference voltage generator depends upon the system. 图 23 shows one possible application circuit.
- A low-pass filtered version of the system supply followed by a buffer such as the zero-drift OPA735 can also be used in cases where the system power supply is noisy. Care should be taken to ensure that the voltage at the V_{DD} input does not exceed 7 V (especially during power up) to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. 图 24 shows one possible application circuit.

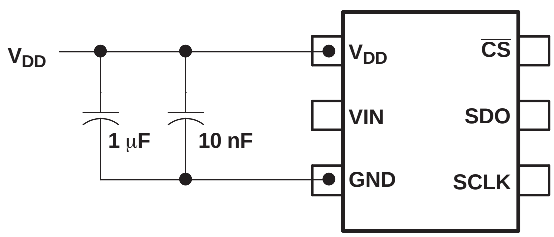


图 22. Supply/Reference Decoupling Capacitors

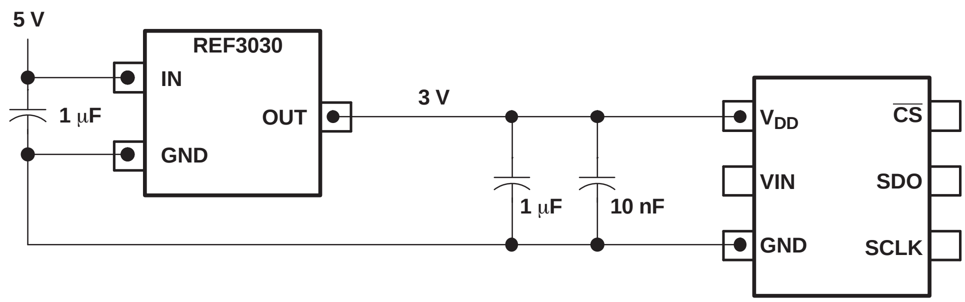


图 23. Using the REF3030 Reference

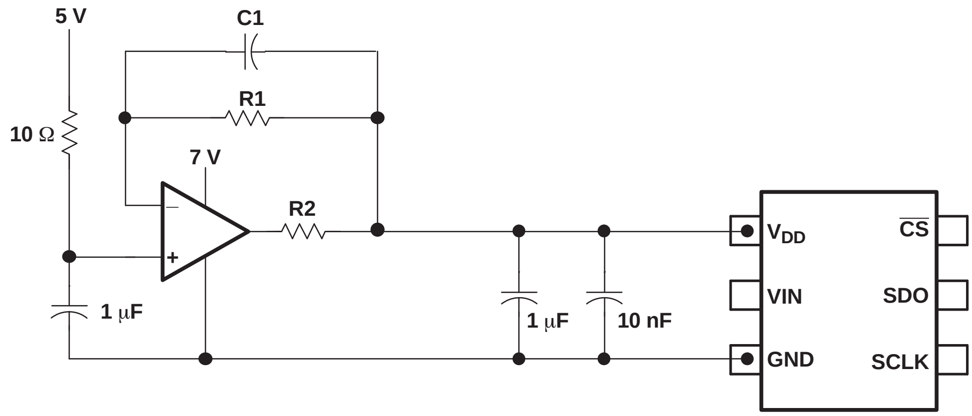


图 24. Buffering with the OPA735

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS7887MDBVT	ACTIVE	SOT-23	DBV	6	250	Pb-Free (RoHS Exempt)	CU SN	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF ADS7887M :

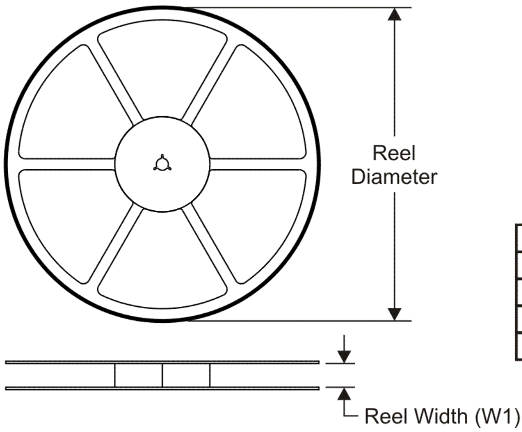
- Catalog: ADS7887

NOTE: Qualified Version Definitions:

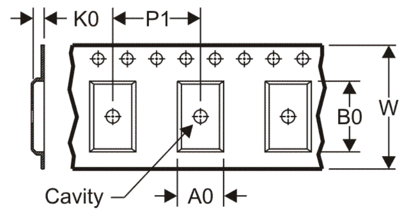
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

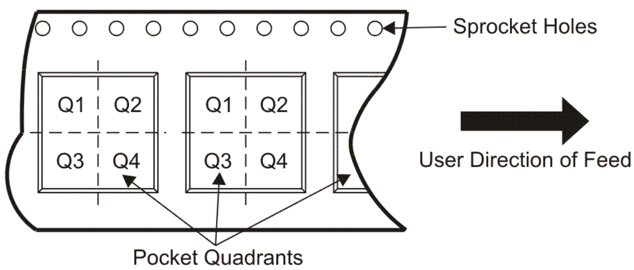


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

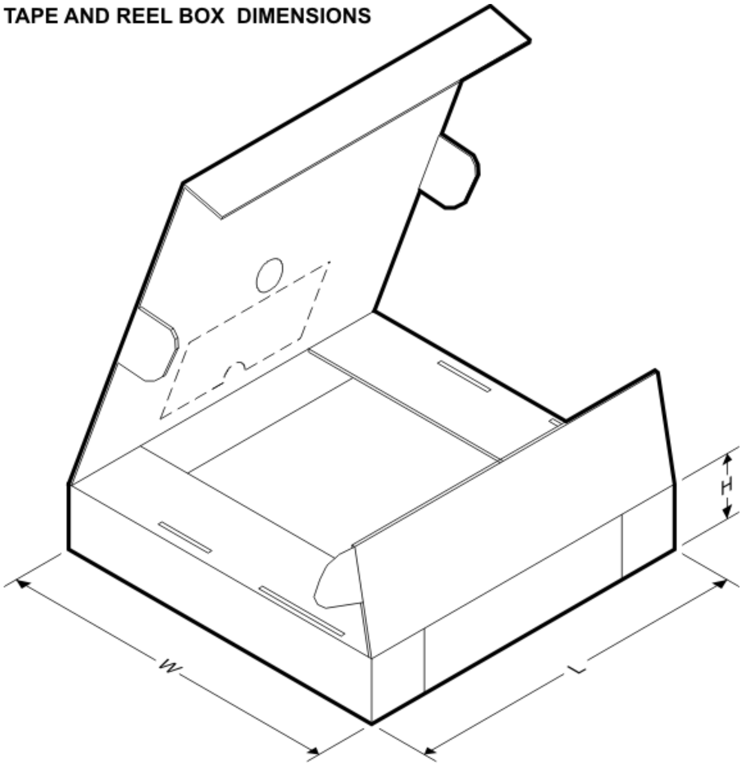
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7887MDBVT	SOT-23	DBV	6	250	177.8	9.7	3.2	3.1	1.39	4.0	8.0	Q3

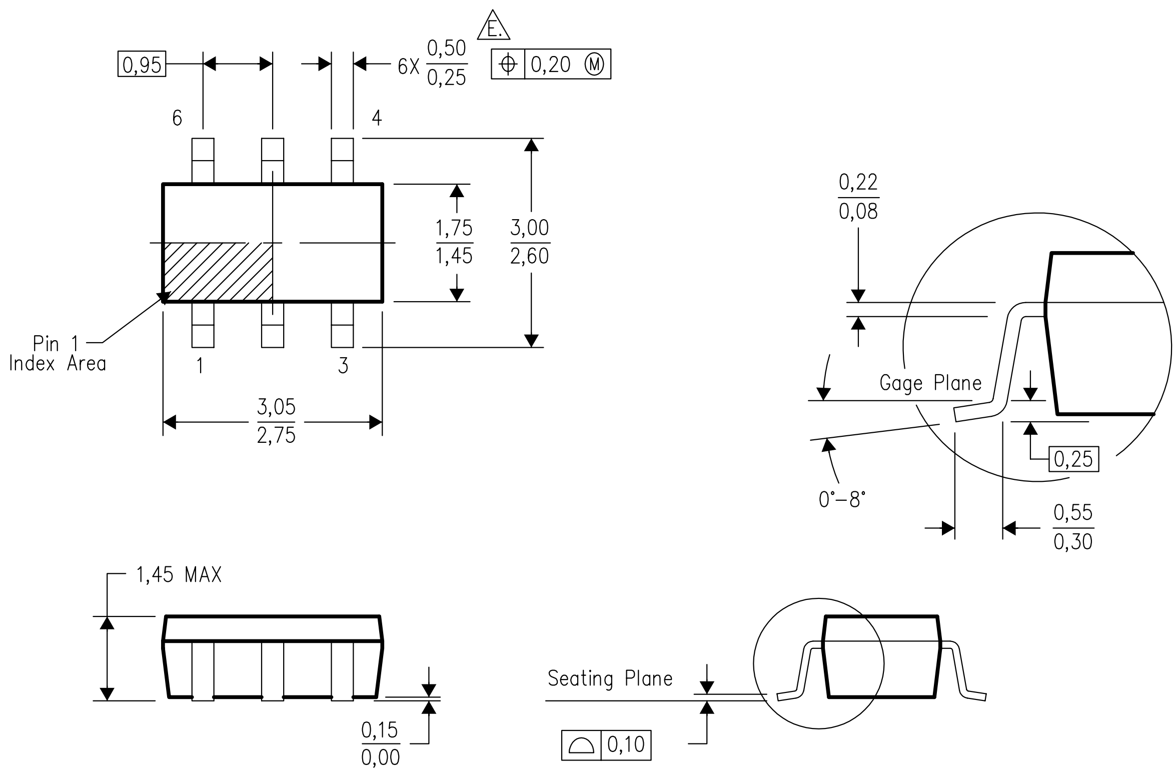
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7887MDBVT	SOT-23	DBV	6	250	184.0	184.0	50.0

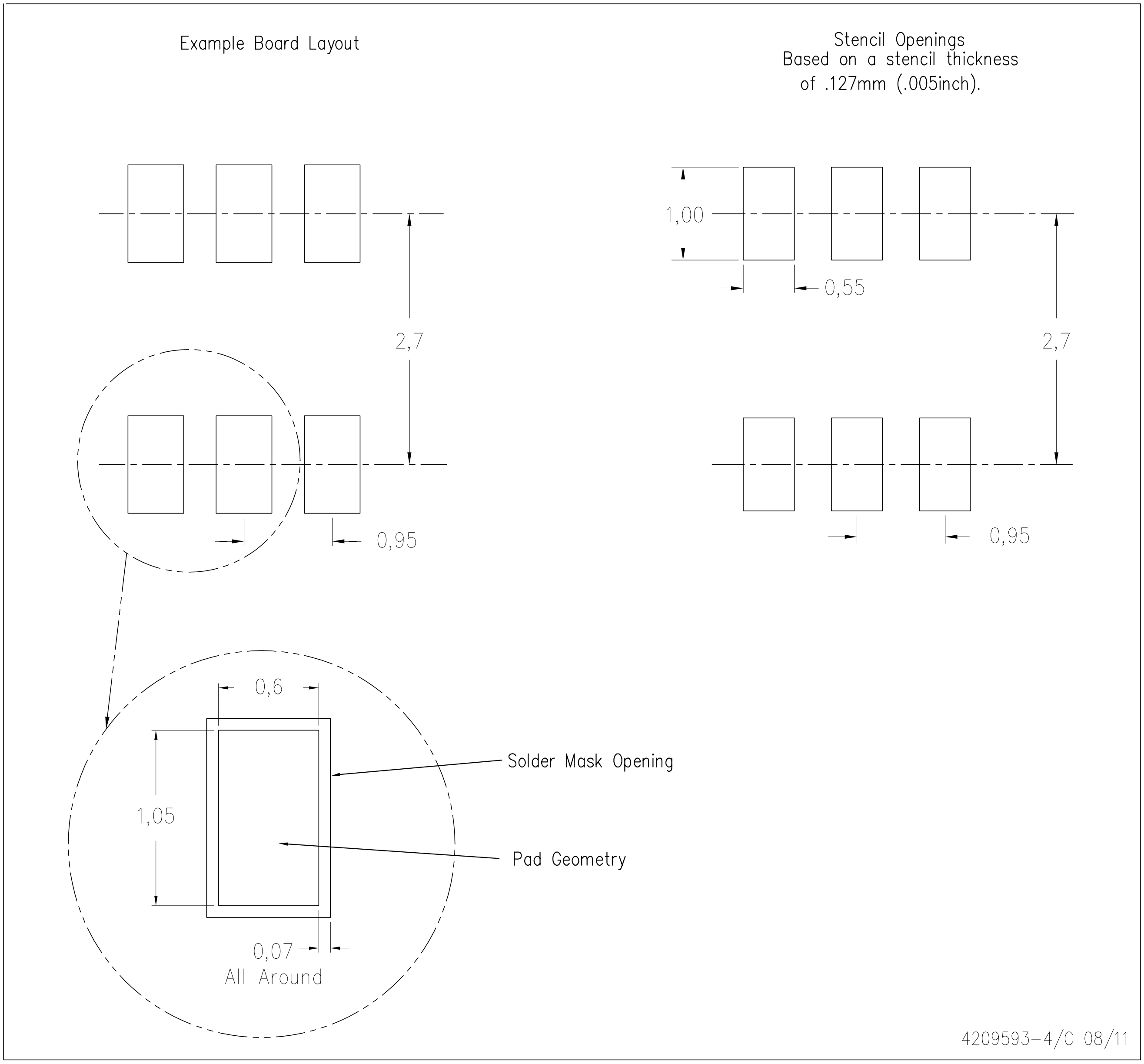
DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



4073253-5/K 03/2006

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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