Powerline Communications Analog Front-End

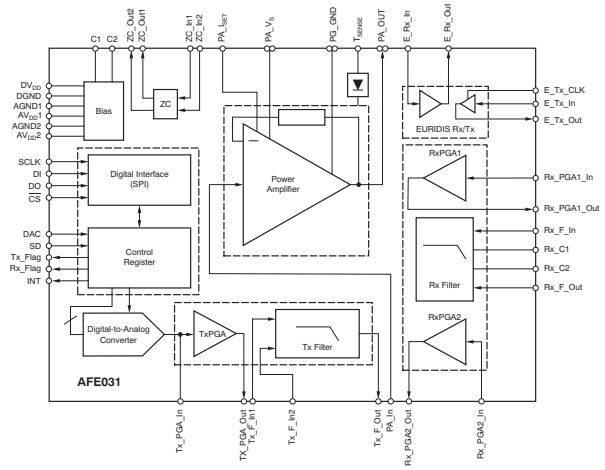
Check for Samples: AFE031

FEATURES

- **Integrated Powerline Driver with Thermal and Overcurrent Warnings**
- **Large Output Swing: $13V_{PP}$ at 1.5A (15V supply)**
- **Low Power Consumption 15mW (Receive Mode)**
- **Shutdown Override**
- **Receive Sensitivity $15\mu V_{RMS}$, Typ**
- **Supply Voltage: 7V to 24V**
- **Supports EN50065 Cenelec Bands A, B, C, D**
- **Supports FSK and OFDM**
- **Programmable Gain Control**
- **Four-Wire Serial Interface**
- **Two Integrated Zero Crossing Detectors**
- **Euridis 1 & 2 Transceiver Buffer**
- **48-Pin QFN PowerPAD™ Package**
- **Extended Temperature Range: –40°C to +125°C**

APPLICATIONS

- **eMetering**
- **Lighting**
- **Solar**



DESCRIPTION

The AFE031 is a low-cost, integrated powerline communications analog front-end (AFE) device that is capable of a transformer-coupled connection to the powerline while under the control of a DSP or microcontroller. It is ideal for driving high-current, low-impedance lines that drive up to 1.5A into reactive loads. The integrated receiver is able to detect signals down to $15\mu V_{RMS}$ and is capable of a wide range of gain options to adapt to varying input signal conditions. This monolithic integrated circuit provides high reliability in demanding powerline communications applications.

The AFE031 transmit power amplifier operates from a single supply in the range of 7V to 26V. At maximum output current, a wide output swing provides a $13V_{PP}$ (I_{OUT} = 1.5A) capability with a nominal 15V supply.

The AFE031 is internally protected against overtemperature conditions. It is also provides an accurate, user-selected, current limit. An interrupt output is provided that indicates current limit, thermal limit, and power lost. It also has a Shutdown pin that can be used to quickly put the device into its lowest power state. Through the four-wire SPI™, the user can enable or disable each functional block to optimize power dissipation.

The AFE031 is housed in a thermally-enhanced, surface-mount PowerPAD package (QFN-48). Operation is specified over the extended industrial temperature range, –40°C to +125°C.

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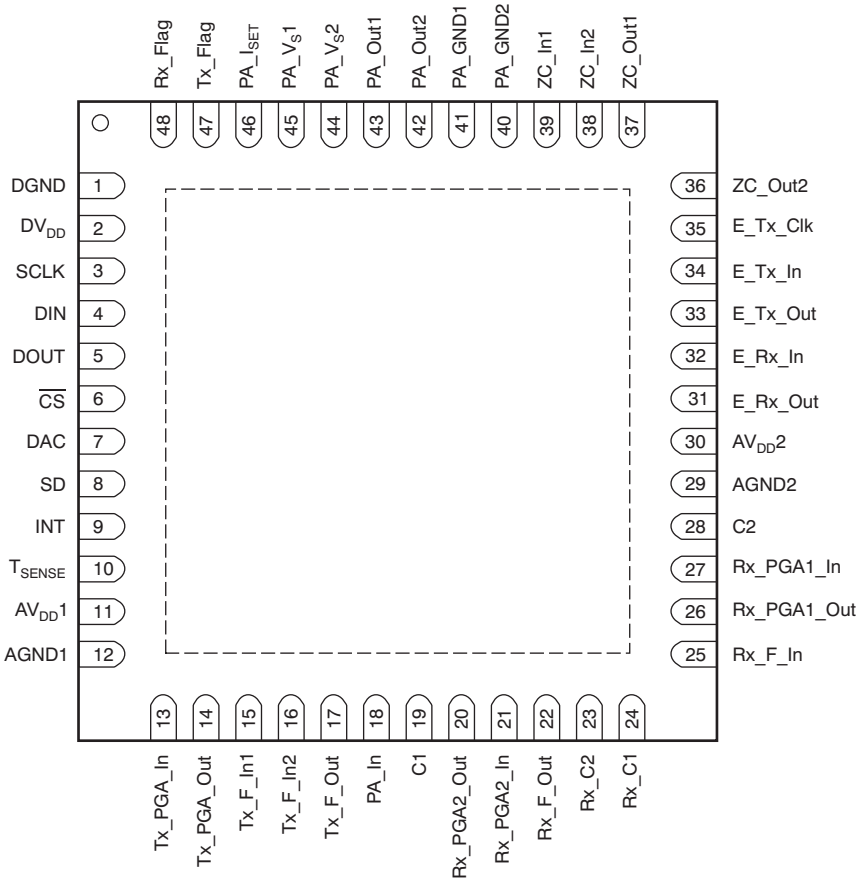
ADVANCE INFORMATION

PIN ASSIGNMENTS

RGZ PACKAGE
QFN-48
(TOP VIEW)



Note: Exposed thermal pad is connected to ground.

PIN DESCRIPTIONS

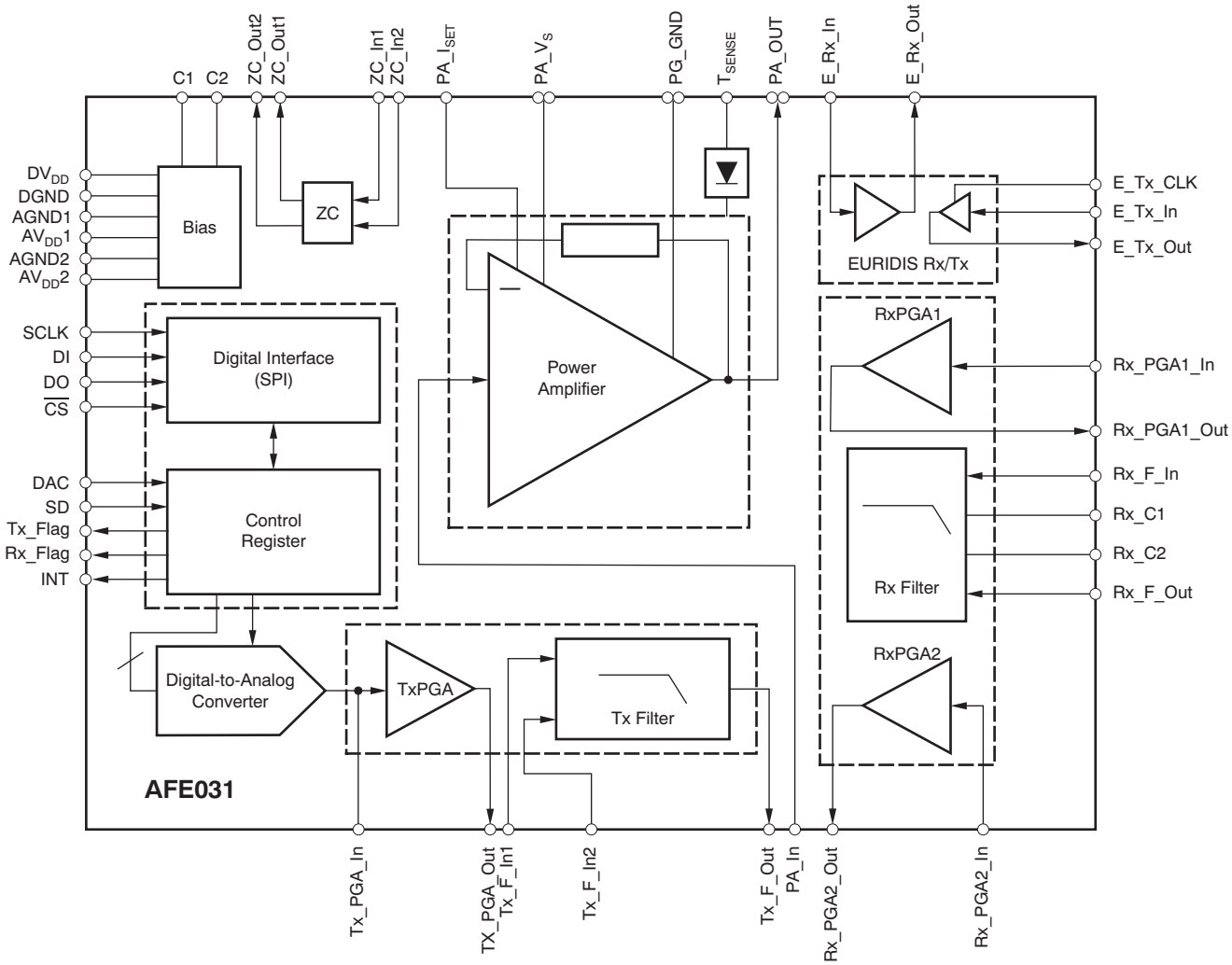
AFE031		DESCRIPTION
PIN NO.	NAME	
1	DGND	Digital Ground
2	DV_{DD}	Digital Supply
3	SCLK	SPI Serial Clock
4	DIN	SPI Digital Input
5	DOUT	SPI Digital Output
6	$\overline{CS}$	SPI Digital Chip Select
7	DAC	DAC Mode Select
8	SD	System Shutdown
9	INT	Interrupt on Overcurrent, Thermal, and Power Lost
10	T_{SENSE}	Temp Sensing Diode (Anode)
11	$AV_{DD}1$	Analog Supply Pin (tied internally to $AV_{DD}2$)
12	AGND1	Analog Ground (tied internally to AGND2)
13	Tx_PGA_In	Transmit PGA Input
14	Tx_PGA_Out	Transmit PGA Output
15	Tx_F_In1	Transmit Filter Input 1

PIN DESCRIPTIONS (continued)

AFE031		DESCRIPTION
PIN NO.	NAME	
16	Tx_F_In2	Transmit Filter Input 2
17	Tx_F_Out	Transmit Filter Output
18	PA_In	Power Amplifier Input
19	C1	Power Amplifier Noise Reducing Capacitor
20	Rx_PGA2_Out	Receiver PGA(2) Output
21	Rx_PGA2_In	Receiver PGA(2) Input
22	Rx_F_Out	Receiver Filter Output
23	Rx_C2	Receiver External Frequency Adjust
24	Rx_C1	Receiver External Frequency Adjust
25	Rx_F_In	Receiver Filter Input
26	Rx_PGA1_Out	Receiver PGA(1) Output
27	Rx_PGA1_In	Receiver PGA(1) Input
28	C2	Receiver Noise Reducing Capacitor
29	AGND2	Analog Ground(tied internally to AGND1)
30	$AV_{DD}2$	Analog Supply (tied internally to $AV_{DD}1$)
31	E_Rx_Out	Euridis Receiver Output
32	E_Rx_In	Euridis Receiver Input
33	E_Tx_Out	Euridis Transmitter Output
34	E_Tx_In	Euridis Transmitter Input
35	E_Tx_Clk	Euridis Transmitter Clock Input
36	ZC_Out2	Zero Crossover Detector Output
37	ZC_Out1	Zero Crossover Detector Output
38	ZC_In2	Zero Crossover Detector Input
39	ZC_In1	Zero Crossover Detector Input
40	PA_GND2	Power Amplifier Ground
41	PA_GND1	Power Amplifier Ground
42	PA_Out2	Power Amplifier Output
43	PA_Out1	Power Amplifier Output
44	PA_V_S2	Power Amplifier Supply
45	PA_V_S1	Power Amplifier Supply
46	PA_I_{SET}	Power Amplifier Current Limit Set
47	Tx_Flag	Transmitter Ready Flag
48	Rx_Flag	Receiver Ready Flag

ADVANCE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



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