

#### AM26C32-EP QUADRUPLE DIFFERENTIAL LINE RECEIVER

±7 V Common-Mode Range With ±200 mV

Low Power,  $I_{CC} = 10 \text{ mA Typ}$ 

Input Hysteresis . . . 60 mV Typ

1B

1A 🛛 2

1Y 🛛

GII 4

2Y || 5

2A 🛛 6

2B 🛛 7

GND 8

3

**Operates From a Single 5 V Supply** 

Improved Replacements for AM26LS32

AM26C32... D PACKAGE

(TOP VIEW)

16 🛛 V<sub>CC</sub>

15

14

11 II 3Y

10 🛛 3A

9 🛛 3B

[] 4B

[] 4A

13 🛛 4Y

12 🛛 🖸

Sensitivity

•

t<sub>pd</sub> = 17 ns Typ

**3-State Outputs** 

Input Fail-Safe Circuitry

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#### **FEATURES**

- Controlled Baseline
  - One Assembly
  - One Test Site
  - One Fabrication Site
- Extended Temperature Performance of -55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree (1)
- Meets or Exceeds the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendation V.10 and V.11
- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

### DESCRIPTION/ORDERING INFORMATION

The AM26C32 is a quadruple differential line receiver for balanced or unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design specifies that if the inputs are open, the outputs always are high.

The AM26C32 devices are manufactured using a BiCMOS process, which is a combination of bipolar and CMOS transistors. This process provides the high voltage and current of bipolar with the low power of CMOS to reduce the power consumption to about one-fifth that of the standard AM26LS32, while maintaining ac and dc performance.

The AM26C32 is characterized for operation over the extended temperature range of -55°C to 125°C.

#### ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–55°C to 125°C	SOIC – D	Reel of 2500	AM26C32MDREP	26C32EP	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



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# AM26C32-EP QUADRUPLE DIFFERENTIAL LINE RECEIVER



TEXAS

INSTRUMENTS www.ti.com

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# FUNCTION TABLE (each receiver)

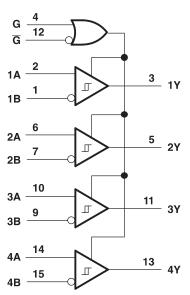
DIFFERENTIAL	ENA	BLES	OUTPUT
INPUT	G	G	Y
V SV	Н	Х	Н
$V_{ID} \ge V_{IT+}$	Х	L	Н
	Н	Х	?
$V_{\rm IT-} < V_{\rm ID} < V_{\rm IT+}$	Х	L	?
	Н	Х	L
$V_{ID} \leq V_{IT-}$	Х	L	L
Х	L	Н	Z

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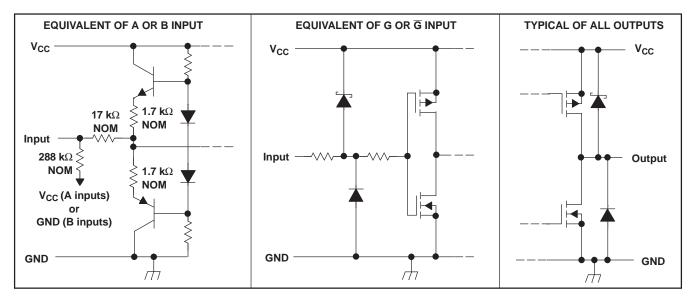


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#### LOGIC DIAGRAM (POSITIVE LOGIC)



#### **SCHEMATICS**



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## AM26C32-EP QUADRUPLE DIFFERENTIAL LINE RECEIVER



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#### **ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT	
$V_{CC}$	Supply voltage <sup>(2)</sup>			7	V	
V	Input voltage range	A or B inputs	-11	14	V	
VI		G or $\overline{G}$ inputs	-0.5	V <sub>CC</sub> + 0.5	V	
$V_{\text{ID}}$	Differential input voltage range		-14	14	V	
Vo	Output voltage range	-0.5	V <sub>CC</sub> + 0.5	V		
I <sub>O</sub>	Output current			±25	mA	
0	Package thermal impedance <sup>(3)(4)</sup>	D package		73	°C/W	
$\theta_{JA}$	Package merman impedance PW package			108	C/W	
TJ	Operating virtual junction temperature		150	°C		
	Lead temperature 1,6 mm (1/16 inch) from a	case for 10 seconds		260	°C	
T <sub>stg</sub>	Storage temperature range		-65	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values, except differential output voltage, V<sub>OD</sub>, are with respect to network GND. Currents into the device are positive and currents out of the device are negative.

(3) Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

#### **RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5	5.5	V
$V_{\text{IH}}$	High-level input voltage	2			V
$V_{\text{IL}}$	Low-level input voltage			0.8	V
V <sub>IC</sub>	Common-mode input voltage			±7	V
I <sub>OH</sub>	High-level output current			-6	mA
I <sub>OL</sub>	Low-level output current			6	mA
T <sub>A</sub>	Operating free-air temperature	-55		125	°C

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#### **ELECTRICAL CHARACTERISTICS**

over recommended ranges of V<sub>CC</sub>, V<sub>IC</sub>, and operating free-air temperature (unless otherwise noted)

	PARAMETER	TEST C	TEST CONDITIONS			MAX	UNIT
V	Differential input high threshold valtage	$V_{O} = V_{OH}$ (min),	$V_{IC} = -7 V \text{ to } 7 V$			0.2	V
V <sub>IT+</sub>	Differential input high-threshold voltage	I <sub>OH</sub> = -440 μA	$V_{IC} = 0$ to 5.5 V			0.1	
V	Differential input low threshold values	V <sub>O</sub> = 0.45 V,	$V_{IC} = -7 V \text{ to } 7 V$	-0.2 <sup>(2)</sup>			V
V <sub>IT-</sub> [	Differential input low-threshold voltage	I <sub>OL</sub> = 8 mA	$V_{IC} = 0$ to 5.5 V	-0.1 <sup>(2)</sup>			v
$V_{\text{hys}}$	Hysteresis voltage (V <sub>IT+</sub> – V <sub>IT-</sub> )				60		mV
V <sub>IK</sub>	Enable input clamp voltage	$V_{CC} = 4.5 V,$	I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>	High-level output voltage	V <sub>ID</sub> = 200 mV,	I <sub>OH</sub> = -6 mA	3.8			V
V <sub>OL</sub>	Low-level output voltage	$V_{ID} = -200 \text{ mV},$	$I_{OL} = 6 \text{ mA}$		0.2	0.3	V
I <sub>OZ</sub>	Off-state (high-impedance state) output current	$V_{O} = V_{CC}$ or GND			±0.5	±5	μΑ
		V <sub>I</sub> = 10 V,	Other input at 0 V			1.5	
I <sub>I</sub>	Line input current	$V_{I} = -10 V,$	Other input at 0 V			-2.5	mA
I <sub>IH</sub>	High-level enable current	V <sub>I</sub> = 2.7 V				20	μA
$I_{IL}$	Low-level enable current	V <sub>1</sub> = 0.4 V				-100	μA
r <sub>l</sub>	Input resistance	One input to ground		12	17		kΩ
I <sub>CC</sub>	Supply current	$V_{CC} = 5.5 V$			10	15	mA

(1) All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $V_{IC} = 0$ , and  $T_A = 25^{\circ}\text{C}$ . (2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage.

#### SWITCHING CHARACTERISTICS

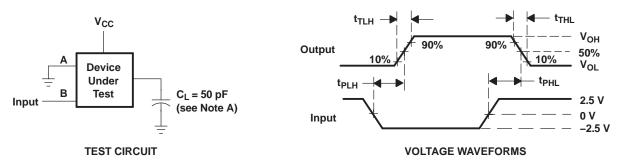
over recommended ranges of operation conditions,  $C_L = 50 \text{ pF}$  (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	See Figure 1	9	17	27	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	See Figure 1	9	17	27	ns
t <sub>TLH</sub>	Output transition time, low- to high-level output	See Figure 1		4	10	ns
t <sub>THL</sub>	Output transition time, high- to low-level output	See Figure 1		4	9	ns
t <sub>PZH</sub>	Output enable time to high level			13	22	ns
t <sub>PZL</sub>	Output enable time to low level	See Figure 2		13	22	ns
t <sub>PHZ</sub>	Output disable time from high level			13	26	ns
t <sub>PLZ</sub>	Output disable time from low level	See Figure 2		13	25	ns

(1) All typical values are at V<sub>CC</sub> = 5 V,  $T_A = 25^{\circ}C$ .

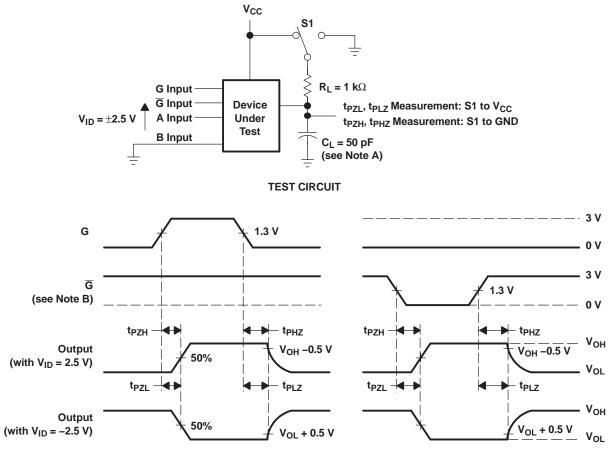


#### PARAMETER MEASUREMENT INFORMATION



A. C<sub>L</sub> includes probe and jig capacitance.





**VOLTAGE WAVEFORMS** 

A.  $C_L$  includes probe and jig capacitance.

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B. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle  $\leq$  50%, t<sub>r</sub> = t<sub>f</sub> = 6 ns.

Figure 2. Enable/Disable Time Test Circuit and Output Voltage Waveforms

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#### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
AM26C32MDREP	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/07648-01XE	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Addendum-Page 1

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OTHER QUALIFIED VERSIONS OF AM26C32-EP :

Catalog: AM26C32

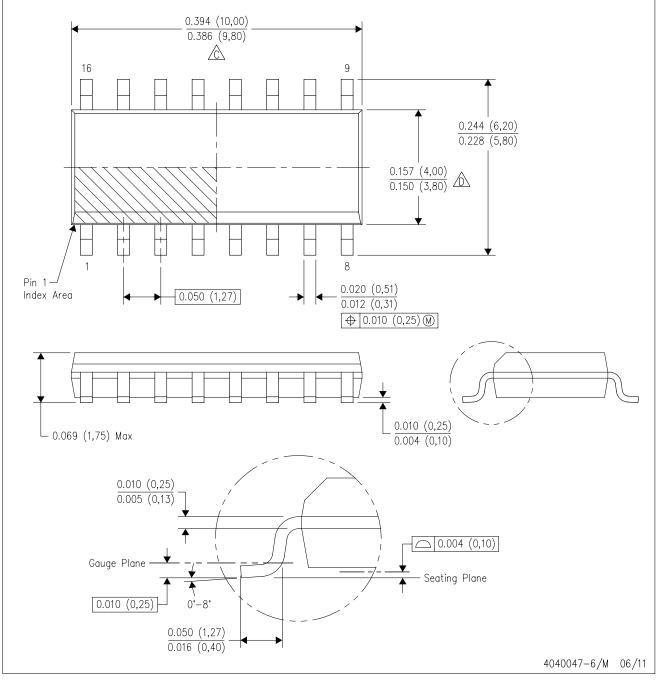
• Military: AM26C32M

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AC.



4211283-4/C 02/11

# D (R-PDSO-G16) PLASTIC SMALL OUTLINE Stencil Openings (Note D) Example Board Layout (Note C) -16x0,55 - 14x1,27 -14x1,27 16x1,95 4,80 4,80 Example Non Soldermask Defined Pad Example Pad Geometry (See Note C) 0,60

Example

Solder Mask Opening (See Note E)

NOTES: A. All linear dimensions are in millimeters.

2,00

B. This drawing is subject to change without notice.

← 0,07 All Around

- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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