高性能低功率射频收发器

特性

- 电源
  - 宽电源电压范围 **(2 V – 3.8 V)**
  - 低电流消耗：
    - **RX**：**21 mA**
    - **RX**：**3 mA**（采用 **RX** 嗅探模式）
    - **TX**：**45 mA +14 dBm**，**868 MHz**
  - 断电：**< 1 μA**
  - 高性能单片收发器
    - 绝佳的接收器灵敏度：
      - **1.2 kbps** 时为 **120 dBm**
      - **50 kbps** 时为 **108 dBm**
      - 使用 **DSSS** 模式 **122 dBm**
    - 阻断性能：**10 MHz** 时为 **86 dB**
    - 邻信道选择性：**61 dB**
    - 低相位噪声：**10 kHz** 偏移时为 **-115 dBc/Hz**
  - 步长为 **0.5 dB**、最高 **15 dBm**（**3.6V** 时为 **16 dBm**）的可编程输出功率
  - 自动输出功率递增
  - 可配置数据速率：**1.2** 至 **200 kbps**
  - 支持的调制格式：**2-FSK**、**2-GFSK**、**4-FSK**、**4-GFSK**、**MSK**、**ASK**、**OOK**、模拟 **FM**
  - 符合 **RoHS** 的 **5 x 5 mm QFN 32** 封装

应用

- 超低功耗无线系统（通道间距低至 **50 kHz**）
- **170 / 433 / 868 / 915 / 950 MHz ISM/SRD** 频带系统
- 无线计量和无线智能电网（**AMR** 和 **AMI**）
- **IEEE 802.15.4g** 系统
- 家庭和楼宇自动化
- 无线警报和安全系统
- 工业监控和控制
- 无线医疗应用
- 无线传感器网络和有源 **RFID**

符合规范

- 欧洲 **- ETSI EN 300 220**、**ETSI EN 54-25**
- 美国 **- FCC CRF47** 第 **15** 部分、**FCC CRF47** 第 **90** 部分
- 日本 **- ARIB STD-T96**

外设和支持功能

- 增强型无线电唤醒功能，用于自动低功耗 **Eeceive** 轮询
- 独立 **128** 字节 **RX** 和 **TX FIFO**
- 支持天线多样性
- 支持再传输
- 支持自动应答接收包
- **TCXO** 支持和控制（也采用功率模式）
- 说前先听 **(LBT)** 系统的自动清除通道评估 **(CCA)**
- 内置编码增益支持扩展范围和耐用性
- 数字 **RSSI** 测量

说明

CC1121 是一个完全集成的单芯片无线电收发器，为经济高效的无线系统在低功耗和低电压操作下实现高性能而设计 所有滤波器都已集成、 无需昂贵的外部 SAW 和 IF 滤波器。 该器件主要用于 ISM（工业、科学和医疗）以及处于 410-480 MHz 和 820-960 MHz 的 SRD（短程设备） 频带。

CC1121 提供扩展硬件特性，以支持数据包处理、数据缓冲和猝发传输、清除通道评估、链路质量指示和无线电唤醒。 CC1121 主要运行参数可以通过 SPI 接口控制。 在一般系统中，CC1121 将与微处理器和极少的外部无源组件配合使用。

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1 Electrical Specifications (Target Specifications)

1.1 Absolute Max Ratings

T_A = 25°C, VDD = 3.0 V if nothing else state

Parameter	Min	Typ	Max	Unit	Condition
Supply Voltage	-0.3		3.9	V	
Storage Temperature Range	-40		125	°C	
Solder Reflow Temperature			260	°C	According to IPC/JEDEC J-STD-020
ESD			2000	V	HBM
ESD			500	V	CDM
Moisture Sensitivity Level			MSL3		
Input RF level			+10	dBm	
Supply voltage ramp-up rate			TBD	V/ms	
Voltage on any digital pin	-0.3		3.9	V	
Voltage on analog pins (including “dcpl” pins)	-0.3		2.0	V	

1.2 General Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Voltage supply range	2.0		3.6	V	
Temperature range	-40		85	°C	

1.3 RF Characteristics

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Frequency bands	820		960	MHz	
	410		480	MHz	
	164		192	MHz	
Datarate	0		100	kbps	FSK, GFSK, ASK, OOK, MSK
	0		200	kbps	4-FSK, 4-GFSK
	0		100	kbps	Transparent mode
Datarate TX only			200	kbps	GFSK
FSK, GFSK, for asymmetric links where e.g. uplink is at higher rate than downlink			TBD	kbps	4-GFSK

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1.4 Regulatory Standards

Performance Mode	Frequency Band	Suitable for compliance with	Comments
High Performance Mode	820 – 960 MHz	ARIB T-96 FCC PART 101 FCC PART 24 SUBMASK D FCC PART 15.247 FCC PART 15.249 ETSI EN 300 220 class 2 ETSI EN 54-25 FCC PART 90 MASK J FCC PART 90 MASK G	Performance suitable for systems targeting maximum allowed output power in the respective bands, using a range extender like the **CC1190**
	410 – 480 MHz	ETSI EN 300 220 class 2 ARIB T-67 ARIB RCR STD-30 FCC PART 90 MASK D FCC PART 90 MASK G	Performance suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
	164 – 192 MHz	ETSI EN 300 220 class 2 FCC PART 90 MASK D	Performance suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
Low Power Mode	820 – 960 MHz	FCC PART 15.247 FCC PART 15.249 ETSI EN 300 220	
	410 – 480 MHz	ETSI EN 300 220	
	164 – 192 MHz	ETSI EN 300 220	

1.5 Current Consumption, Static Modes

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Power down with retention		0.2	1	µA	
		0.8		µA	Low-power RC oscillator running
XOFF mode		TBD		mA	

1.6 Current Consumption, Transmit Modes

High Performance Mode

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX current consumption +10 dBm		35		mA	
TX current consumption +14 dBm		45		mA	

Low Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
TX current consumption +10 dBm		30		mA	

1.7 Current Consumption, Receive Modes

High Performance Mode

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
RX wait for sync 1.2 kbps, 4 byte preamble 38.4 kbps, 4 byte preamble 50 kbps, 4 byte preamble		 3 13 16		 mA mA mA	Using RX Sniff Mode, where the receiver wakes up at user defined intervals to look for the preamble. The very fast **CC1121** receiver only requires a small amount of preamble to settle, and can spend the rest of the time idle. In RX Sniff Mode the user can do a trade-off between settling time and average power consumption. RX Sniff Mode does not reduce sensitivity, selectivity or any other RF performance parameters, only settling time of the receiver is increased
RX Peak Current 1.2 kbps 38.4 kbps 50 kbps 200 kbps		 21 21 21 22		 mA mA mA mA	Peak current consumption during packet reception
Average Current Consumption					
Check for data packet every 1 second using wake on radio		3		uA	32 kHz RC oscillator used as sleep timer

Low Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
RX wait for sync 1.2 kbps, 4 byte preamble		 2		 mA	Using RX Sniff Mode
RX Peak Current Low power RX mode 1.2 kbps 38.4 kbps 50 kbps		 15 15 15		 mA	

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1.8 Receive Parameters

High Performance Mode

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Sensitivity		-119		dBm	300 bps with coding gain (using a PN spreading sequence with 4 chips per databit)
		-122		dBm	300 bps with coding gain, and paired with the **CC1190**
		-108		dBm	38.4 kbps, DEV=50 kHz CHF=100 kHz
		-108		dBm	802.15.4g 50 kbps mandatory mode, CHF=100 kHz
		-102		dBm	200 kbps, DEV=83 kHz (outer symbols), CHF=200 kHz, 4GFSK
		TBD		dBm	1.2 kbps, DEV=4 kHz CHF=10 kHz, transmission of 32 bit Sync word only
		-108			Wireless M-BUS mode 32.768 kbps, DEV=50 kHz CHF=200 kHz
		-117			1.2 kbps, DEV=20 kHz CHF=50 kHz
Saturation		+10		dBm	
Digital Channel Filter Programmable Bandwidth	40		200	kHz	
IIP3, Normal Mode		-14		dBm	At maximum gain
IIP3, High Linearity Mode		-8		dBm	Using 6dB gain reduction in front end
Datarate offset tolerance			±12	%	
Optimum Input Impedance			TBD		170 MHz
			TBD		434 MHz
			TBD		868 MHz
			TBD		950 MHz
Spurious Emissions			TBD		

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Selectivity / Blocking at 950 MHz (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Blocking and Selectivity 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		50		dB	± 50 kHz
		51		dB	± 100 kHz
		69		dB	± 1 MHz
		73		dB	± 2 MHz
		79		dB	± 10 MHz
Blocking and Selectivity 50 kbps 2GFSK, 200 kHz channel separation, 25 kHz deviation, 100 kHz channel filter 802.15.4g Mandatory Mode		42		dB	± 200 kHz (adjacent channel)
		49		dB	± 400 kHz (alternate channel)
		62		dB	± 1 MHz
		66		dB	± 2 MHz
		73		dB	± 10 MHz
Blocking and Selectivity 200 kbps 4GFSK, 83 kHz deviation (outer symbols), 200 kHz channel filter, zero IF		32		dB	± 200 kHz
		39		dB	± 400 kHz
		51		dB	± 1 MHz
		55		dB	± 2 MHz
		57		dB	± 10 MHz
Spurious response rejection 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		58		dB	

Selectivity / Blocking at 868 MHz (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Blocking and Selectivity 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		50		dB	± 50 kHz
		51		dB	± 100 kHz
		70		dB	± 1 MHz
		74		dB	± 2 MHz
		80		dB	± 10 MHz
Blocking and Selectivity 32.768 kbps 2GFSK, 50 kHz deviation, 200 kHz channel filter Wireless M-BUS mode S		43		dB	± 200 kHz
		50		dB	± 400 kHz
		62		dB	± 1 MHz
		68		dB	± 2 MHz
		73		dB	± 10 MHz
Blocking and Selectivity 38.4 kbps 2GFSK, 20 kHz deviation, 100 kHz channel filter		38		dB	± 100 kHz
		42		dB	± 200 kHz
		63		dB	± 1 MHz
		70		dB	± 2 MHz
		74		dB	± 10 MHz
Blocking and Selectivity 50 kbps 2GFSK, 200 kHz channel separation, 25 kHz deviation, 100 kHz channel filter 802.15.4g Mandatory Mode		42		dB	± 200 kHz (adjacent channel)
		51		dB	± 400 kHz (alternate channel)
		63		dB	± 1 MHz
		70		dB	± 2 MHz
		74		dB	± 10 MHz
Blocking and Selectivity 200 kbps 4GFSK, 83 kHz deviation (outer symbols), 200 kHz channel filter, zero IF		33		dB	± 200 kHz
		40		dB	± 400 kHz
		52		dB	± 1 MHz
		56		dB	± 2 MHz
		57		dB	± 10 MHz
Spurious response rejection 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		59		dB	

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Selectivity / Blocking at 434 MHz (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Blocking and Selectivity 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		57		dB	± 50 kHz
		58		dB	± 100 kHz
		75		dB	± 1 MHz
		80		dB	± 2 MHz
		85		dB	± 10 MHz
Blocking and Selectivity 38.4 kbps 2GFSK, 20 kHz deviation, 100 kHz channel filter		49		dB	± 100 kHz
		50		dB	± 200 kHz
		65		dB	± 1 MHz
		70		dB	± 2 MHz
		76		dB	± 10 MHz
Spurious response rejection 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		62		dB	

Selectivity / Blocking at 170 MHz (High Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Blocking and Selectivity 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		61		dB	± 50 kHz
		61		dB	± 100 kHz
		76		dB	± 1 MHz
		81		dB	± 2 MHz
		85		dB	± 10 MHz
Spurious response rejection 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		65		dB	

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Low Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Sensitivity		-113		dBm	1.2 kbps, DEV=20 kHz, CHF=50 kHz
		-104		dBm	38.4kbps, DEV=50 kHz, CHF=100 kHz
		-104		dBm	802.15.4g 50 kbps mandatory mode. 200 kHz channel separation, GFSK
Saturation			+10	dBm	

Selectivity / Blocking at 868 MHz (Low Power Mode)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Blocking and Selectivity 1.2 kbps 2FSK, 20 kHz deviation, 50 kHz channel filter		45			± 50 kHz
		46			± 100 kHz
		65			± 1 MHz
		68			± 2 MHz
		78			± 10 MHz
Blocking and Selectivity 38.4 kbps 2GFSK, 20 kHz deviation, 100 kHz channel filter		37			± 100 kHz
		44			± 200 kHz
		55			± 1 MHz
		58			± 2 MHz
		68			± 10 MHz
Blocking and Selectivity 50 kbps 2GFSK, 200 kHz channel separation, 25 kHz deviation, 100 kHz channel filter 802.15.4g Mandatory Mode		37			± 200 kHz (adjacent channel)
		44			± 400 kHz (alternate channel)
		55			± 1 MHz
		58			± 2 MHz
		68			± 10 MHz

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1.9 Transmit Parameters

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Max output power		+14 +14 +15 +15 +16		dBm dBm dBm dBm dBm	At 950 MHz At 868 MHz At 433 MHz At 170 MHz At 170 MHz with VDD = 3.6V
Min output power		-11 -32		dBm dBm	Within fine step size range Coarser step size
Output power step size		0.4		dB	Within fine step size range
Spurious Emissions		TBD			
Harmonics 2nd Harm, 170 MHz 3rd Harm, 170 MHz 2nd Harm, 433 MHz 3rd Harm, 433 MHz 2nd Harm, 868 MHz 3rd Harm, 868 MHz 2nd Harm, 950 MHz 3rd Harm, 950 MHz			 -36 -54 -36 -36 -41 -41 -55 -55	dBm	Transmission at +14dBm using TI reference design
Optimum Load Impedance		TBD TBD TBD TBD			170 MHz 434 MHz 868 MHz 950 MHz

1.10 PLL Parameters

High Performance Mode

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Phase noise at 950 MHz		-99		dBc/Hz	± 10 kHz offset
		-99		dBc/Hz	± 100 kHz offset
		-123		dBc/Hz	± 1 MHz offset
Phase noise at 868 MHz		-100		dBc/Hz	± 10 kHz offset
		-100		dBc/Hz	± 100 kHz offset
		-124		dBc/Hz	± 1 MHz offset
Phase noise at 433 MHz		-106		dBc/Hz	± 10 kHz offset
		-106		dBc/Hz	± 100 kHz offset
		-130		dBc/Hz	± 1 MHz offset
Phase noise at 170 MHz		-112		dBc/Hz	± 10 kHz offset
		-112		dBc/Hz	± 100 kHz offset
		-136		dBc/Hz	± 1 MHz offset

Low Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Phase noise at 950 MHz		-96		dBc/Hz	± 10 kHz offset
		-96		dBc/Hz	± 100 kHz offset
		-116		dBc/Hz	± 1 MHz offset
Phase noise at 868 MHz		-97		dBc/Hz	± 10 kHz offset
		-97		dBc/Hz	± 100 kHz offset
		-117		dBc/Hz	± 1 MHz offset
Phase noise at 433 MHz		-103		dBc/Hz	± 10 kHz offset
		-103		dBc/Hz	± 100 kHz offset
		-123		dBc/Hz	± 1 MHz offset
Phase noise at 170 MHz		-109		dBc/Hz	± 10 kHz offset
		-109		dBc/Hz	± 100 kHz offset
		-129		dBc/Hz	± 1 MHz offset

1.11 Wake-up and Timing

T_A = 25°C, VDD = 3.0 V, f_c = 868 MHz band if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Powerdown to active		300		µs	Depends on chosen crystal
Active to RX/TX (no calibration)		160		µs	
Active to RX/TX (with calibration)		430		µs	
RX/TX turnaround		40		µs	
Frequency synthesizer calibration		360		µs	When using SCAL strobe
Required number of preamble bytes		0.5		bytes	Required for RF front end gain settling only. Digital demodulation does not require preamble for settling
Time from start RX until valid RSSI, including gain settling (function of channel bandwidth. Programmable for trade-off between speed and accuracy)			300	µs	200 kHz channels (can be reduced by approx. 50% by reducing filtering time)

1.12 32 MHz Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Crystal frequency	32		33.6	MHz	
Load Capacitance	16		20	pF	
ESR			50	Ω	
Start-up Time		300		µs	

1.13 32 MHz Clock Input (TCXO)

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Clock frequency	32		33.6	MHz	
TCXO clock input swing The TCXO clock signal must be AC coupled. It is recommended that a 18pF series capacitor is used.	0.8		3.6	Vp-p	Peak-to-peak input swing

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1.14 32 kHz clock input

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Clock frequency		32		kHz	
32kHz Clock Input Pin Input High Voltage	0.8*Vdd				
32kHz Clock Input Pin Input Low Voltage			0.2*Vdd		
32kHz Clock Input Pin Input Capacitance		TBD			

1.15 32 kHz RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Frequency		32		kHz	After Calibration
Frequency Accuracy After Calibration		±0.2		%	
Temperature Coefficient		0.4		%/°C	
Supply Voltage Coefficient		3		%/V	
Initial Calibration Time		2		ms	

1.16 I/O and reset

T_A = 25°C, VDD = 3.0 V if nothing else stated

Parameter	Min	Typ	Max	Unit	Condition
Logic Input High Voltage	0.8*Vdd			V	
Logic Input Low Voltage			0.2*Vdd	V	
I/O-pin pullup and pulldown resistors		20		kΩ	
Logic Output High Voltage	0.8*Vdd				At 4mA output load or less
Logic Output Low Voltage			0.2*Vdd		At 4mA output load or less
Power-on Reset Threshold		1		V	Voltage on dvdd pin
Brown-out threshold		1.6		V	Voltage on “dcpl” pin

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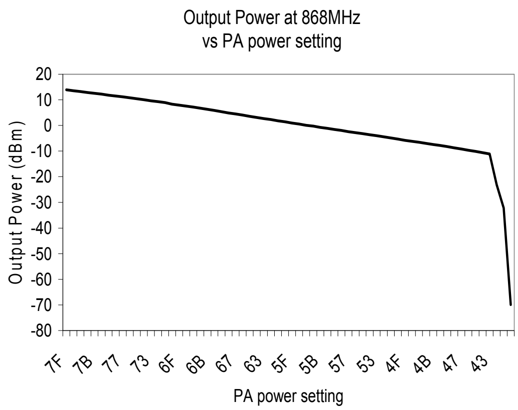
2 Typical Performance Curves



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3 Pin Configuration

The **CC1121** pin-out is shown in the table below.

Pin #	Pin name	Type / direction	Description
1	vdd_guard	Power	3.0 V VDD
2	reset_n	Digital Input	Asynchronous, active-low digital reset
3	gpio3	Digital Input/Output	General purpose IO
4	gpio2	Digital Input/Output	General purpose IO
5	dvdd	Power	3.0 V VDD to internal digital regulator
6	dcpl	Power	Digital regulator output to external C
7	si	Digital Input	Serial data in
8	sclk	Digital Input	Serial data clock
9	so(gpio1)	Digital Input/Output	Serial data out (General purpose IO)
10	gpio0	Digital Input/Output	General purpose IO
11	cs_n	Digital Input	Active-low chip-select
12	dvdd	Power	3.0 V VDD
13	avdd_if	Power	3.0 V VDD
14	rbias	Analog	External high precision R
15	avdd_rf	Power	3.0 V VDD
16	not connected		
17	pa	Analog	Single-ended TX output
18	trx_sw	Analog	TX/RX switch
19	lna_p	Analog	Differential RX input
20	lna_n	Analog	Differential RX input
21	dcpl_vco	Power	Pin for external decoupling of VCO supply regulator
22	avdd_synth1	Power	3.0 V VDD
23	lpf0	Analog	External loopfilter components
24	lpf1		External loopfilter components
25	avdd_pfd_chp	Power	3.0 V VDD
26	dcpl_pfd_chp	Power	Pin for external decoupling of PFD and CHP regulator
27	avdd_synth2	Power	3.0 V VDD
28	avdd_xosc	Power	3.0 V VDD
29	dcpl_xosc	Power	Pin for external decoupling of XOSC supply regulator
30	xosc_q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to ext_xosc is used)
31	xosc_q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to ext_xosc is used)
32	ext_xosc	Digital Input	Pin for external xosc input (must be grounded if a regular xosc connected to xosc_q1 and xosc_2 is used)

4 Block Diagram

A system block diagram of **CC1121** is shown Figure 4.1.

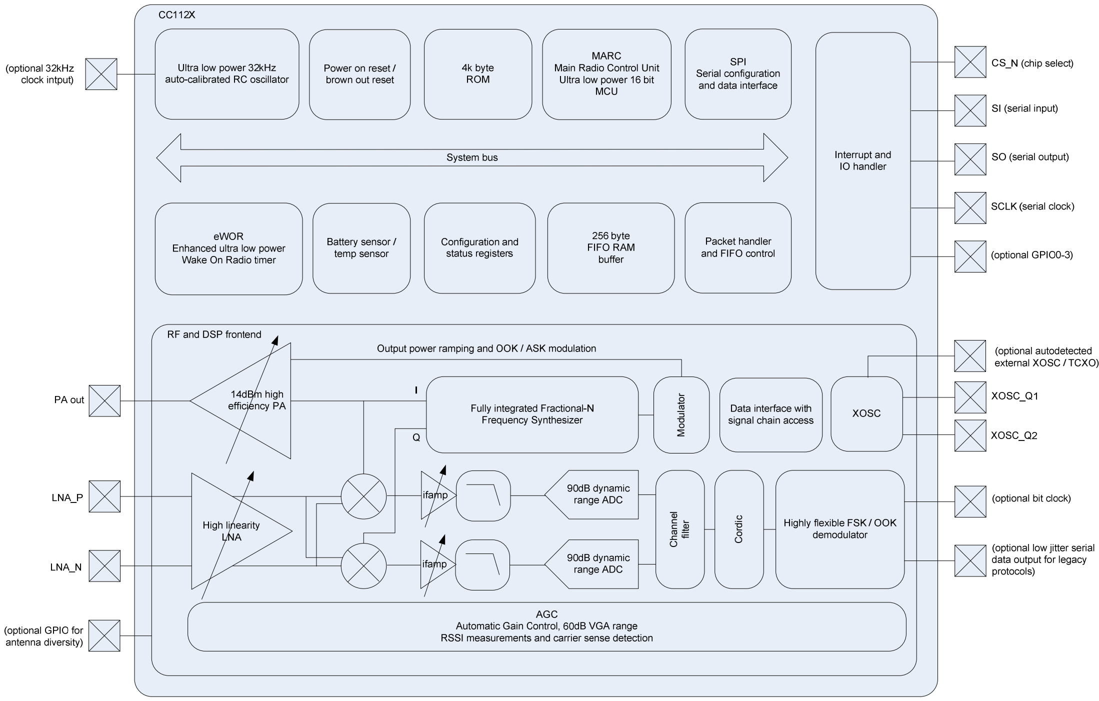

Figure 4.1 : System Block Diagram

4.1 Frequency Synthesizer

At the heart of **CC1121** there is a fully integrated, fractional-N, ultra high performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance, giving very high selectivity and blocking performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power.

Either a crystal can be connected to XOSC_Q1 and XOSC_Q2, or a TCXO can be connected to the external clock input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part. To reduce system cost, **CC1121** has high accuracy frequency estimation and compensation registers to measure and compensate for crystal inaccuracies, enabling the use of lower cost crystals. If a TCXO is used, the **CC1121** will automatically turn the TCXO on and off when needed to support low power modes and Wake-On-Radio operation.

4.2 Receiver

CC1121 features a highly flexible receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitized by the high dynamic range ADCs.

An advanced Automatic Gain Control (AGC) unit adjusts the front end gain, and enables the **CC1121** to receive both strong and weak signals, even in the presence of strong interferers. High attenuation channel and data filtering enable reception with strong neighbor channel interferers. The I/Q signal is converted to a phase / magnitude signal to support both FSK and OOK modulation schemes.

A sophisticated pattern recognition algorithm locks onto the synchronization word without need for preamble settling bytes. Receiver settling time is therefore reduced to the settling time of the

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AGC, typically 4 bits. The advanced pattern recognition also eliminates the problem of false sync triggering on noise, further reducing power consumption and improving sensitivity and reliability. The pattern recognition logic can also be used as a high performance preamble detector to reliably detect a valid preamble in the channel.

A novel I/Q compensation algorithm removes any problem of I/Q mismatch and hence avoids time consuming and costly I/Q / image calibration steps in production or in the field.

4.3 Transmitter

The **CC1121** transmitter is based on direct synthesis of the RF frequency (in-loop modulation). To achieve effective spectrum usage, **CC1121** has extensive data filtering and shaping in TX to support high throughput data communication in narrowband channels. The modulator also controls power ramping to remove issues such as spectral splattering when driving external high power RF amplifiers.

4.4 Radio Control and User Interface

The **CC1121** digital control system is built around MARC (Main Radio Control) implemented using a high performance 16 bit ultra low power MCU. MARC handles power modes, radio sequencing and protocol timing.

A 4-wire SPI serial interface is used for configuration and data buffer access. The digital baseband includes support for channel configuration, packet handling, and data buffering. The host MCU can stay in power down until a valid RF packet has been received, and then burst read the data, greatly reducing the power consumption and computing power required from the host MCU.

The **CC1121** radio control and user interface is based on the widely used **CC1101** transceiver to enable easy SW transition between the two platforms. The command strobes and the main radio states are the same on the two platforms.

For legacy formats **CC1121** also supports two serial modes. In synchronous serial mode **CC1121** does bit synchronization and provides the MCU with a bit clock with associated data. In transparent mode **CC1121** outputs the digital baseband signal using a digital interpolation filter to eliminate jitter introduced by digital filtering and demodulation.

4.5 Enhanced Wake-On-Radio (eWOR)

eWOR, using a flexible integrated sleep timer, enables automatic receiver polling with no intervention from the MCU. The **CC1121** will enter RX, listen and return to sleep if a valid RF packet is not received. The sleep interval and duty cycle can be configured to make a trade-off between network latency and power consumption. Incoming messages are time-stamped to simplify timer re-synchronization.

The eWOR timer runs off an ultra low power 32 kHz RC oscillator. To improve timing accuracy, the RC oscillator can be automatically calibrated to the RF crystal in configurable intervals.

4.6 Sniff Mode

The **CC1121** supports very quick start up time, and requires very few preamble bits. Sniff Mode uses this to dramatically reduce the current consumption while the receiver is waiting for data.

Since the **CC1121** is able to wake up and settle much faster than the length of most preambles, it is not required to be in RX continuously while waiting for a packet to arrive. Instead, the enhanced wake-on-radio feature can be used to put the device into sleep periodically. By setting an appropriate sleep time, the **CC1121** will be able to wake up and receive the packet when it arrives with no performance loss. This removes the need for accurate timing synchronization between transmitter and receiver, and allows the user to trade off current consumption between the transmitter and receiver.

4.7 Antenna Diversity

Automatic antenna diversity is supported by CC1121 to increase performance in a multi-path environment. An external antenna switch is required; the switch will be automatically controlled by CC1121 using one of the GPIO pins (also support for differential output control signal typically used in RF switches).

If antenna diversity is enabled, CC1121 will alternate between the two antennas until a valid RF input signal is detected, and then receive on this antenna. An optional acknowledge packet can be transmitted from the same antenna as the received packet.

An incoming RF signal can be validated by received signal strength, by using the automatic preamble detector, or a combination of the two. Using the preamble detector will make a more robust system and avoid the need to set a defined signal strength threshold, as this threshold will set the sensitivity limit of the system.

5 Typical Application Circuit

Very few external components are required for the operation of **CC1121**. A typical application circuit is shown below. Note that it does not show how the board layout should be done, the board layout will greatly influence the RF performance of **CC112**.

This section is meant as an introduction only. Note that decoupling capacitors for power pins are not shown in the figure below.

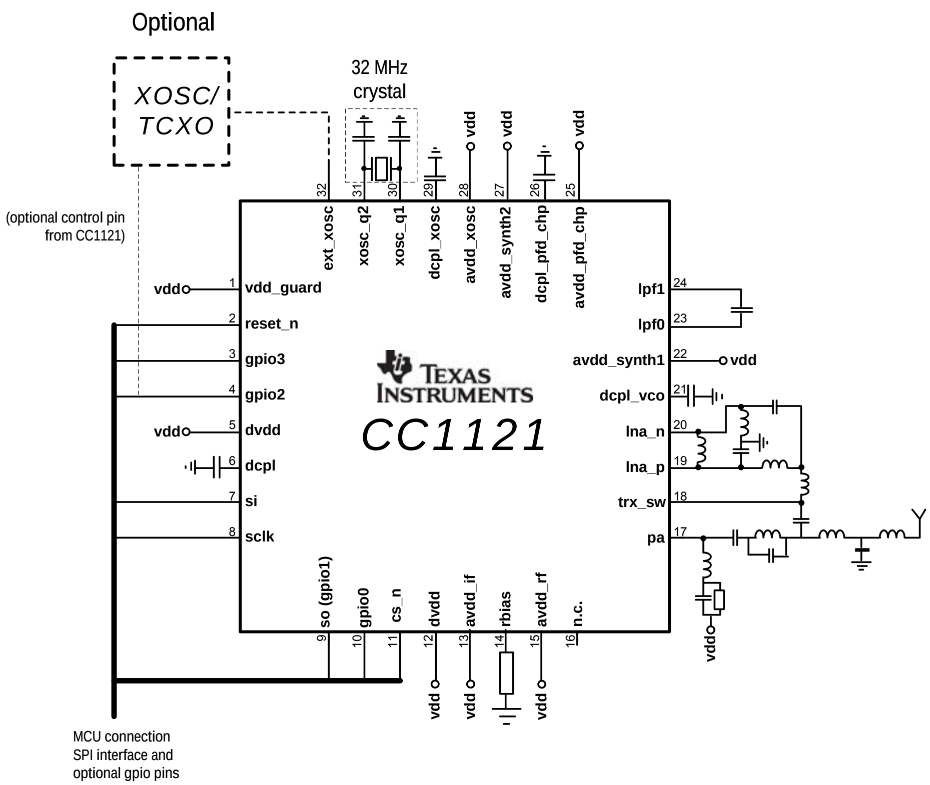

Figure 5.1 : Typical application circuit

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
CC1121RHMR	ACTIVE	QFN	RHM	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
CC1121RHMT	ACTIVE	QFN	RHM	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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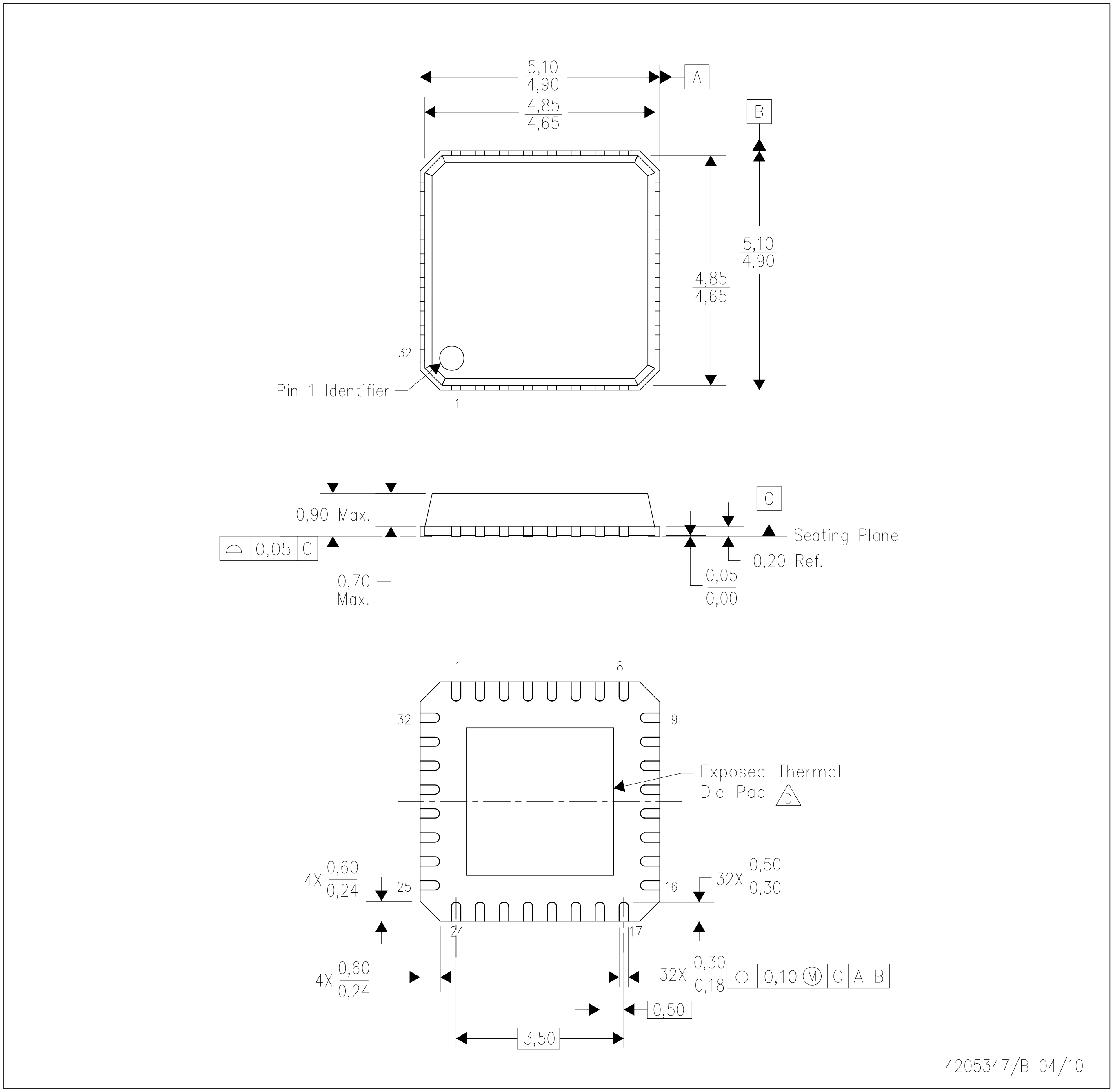
RHM (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



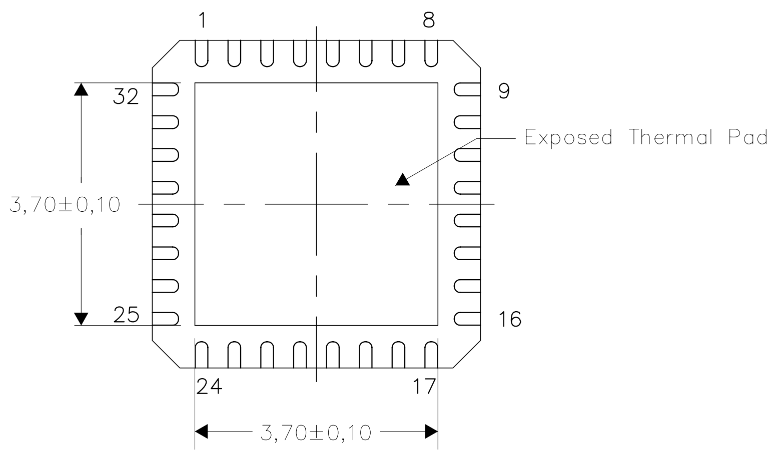
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

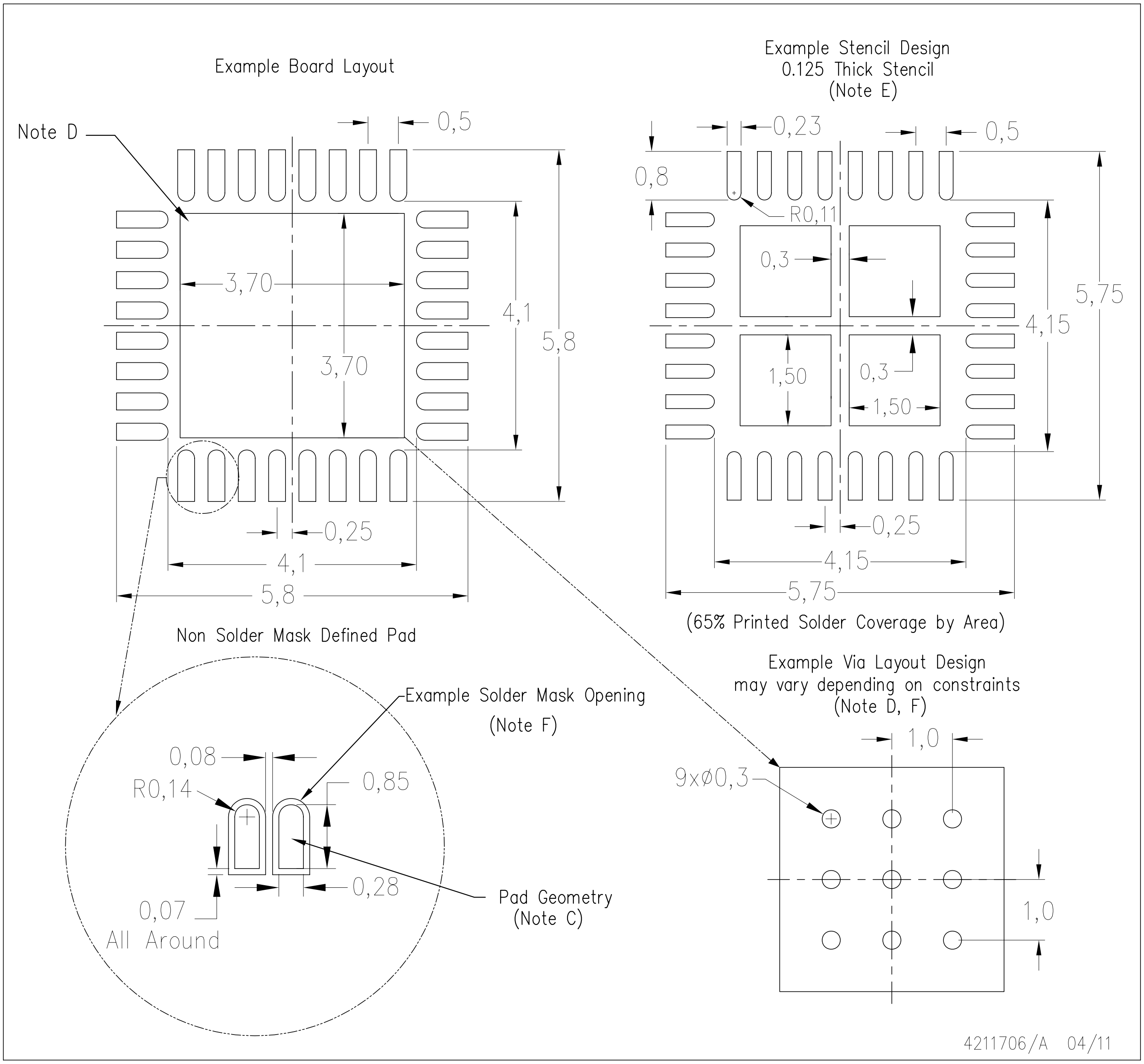


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHM (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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