TEXAS INSTRUMENTS

SCCS061B - July 1994 - Revised September 2001

CY74FCT16652T
CY74FCT162652T

16-Bit Registered Transceivers

Features

- **I_{off} supports partial-power-down mode operation**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40°C to +85°C**
- **V_{CC} = 5V ± 10%**

CY74FCT16652T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25°C**

CY74FCT162652T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A = 25°C**

Functional Description

These 16-bit, high-speed, low-power, registered transceivers that are organized as two independent 8-bit bus transceivers with three-state D-type registers and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. OEAB and $\overline{OEBA}$ control pins are provided to control the transceiver functions. SAB and SBA control pins are provided to select either real-time or stored data transfer.
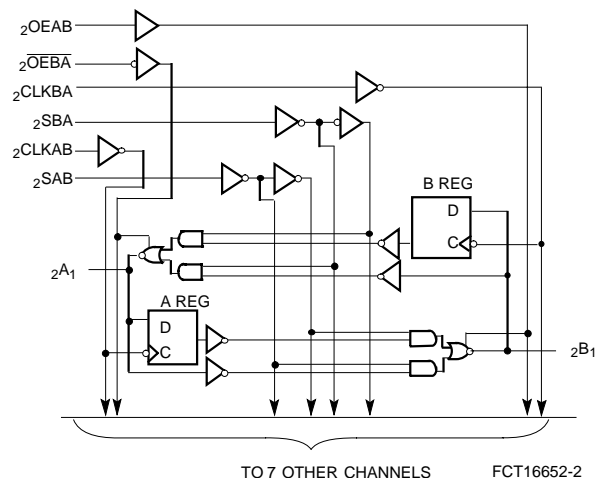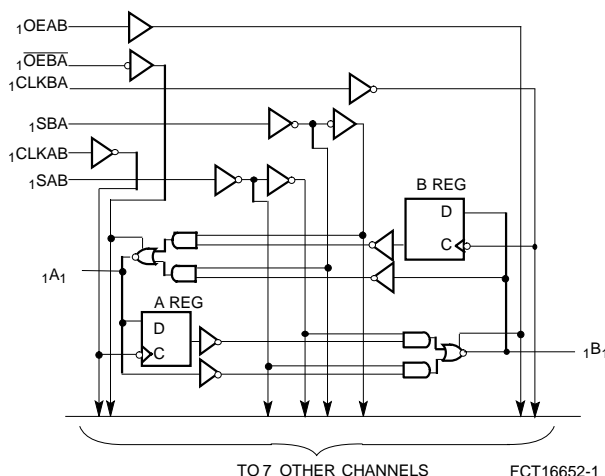
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CLKAB or CLKBA), regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16652T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162652T has 24-mA balanced output drivers with current-limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162652T is ideal for driving transmission lines.
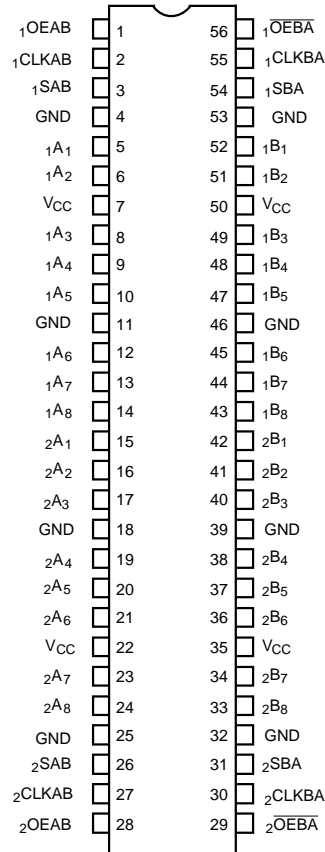
Logic Block Diagrams

TO 7 OTHER CHANNELS   FCT16652-1

TO 7 OTHER CHANNELS   FCT16652-2

Pin Configuration

SSOP/TSSOP
Top View

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           ┌──────∪──────┐
 1OEAB   □ │1          56│ □ 1OEBA
 1CLKAB  □ │2          55│ □ 1CLKBA
 1SAB    □ │3          54│ □ 1SBA
 GND     □ │4          53│ □ GND
 1A1     □ │5          52│ □ 1B1
 1A2     □ │6          51│ □ 1B2
 VCC     □ │7          50│ □ VCC
 1A3     □ │8          49│ □ 1B3
 1A4     □ │9          48│ □ 1B4
 1A5     □ │10         47│ □ 1B5
 GND     □ │11         46│ □ GND
 1A6     □ │12         45│ □ 1B6
 1A7     □ │13         44│ □ 1B7
 1A8     □ │14         43│ □ 1B8
 2A1     □ │15         42│ □ 2B1
 2A2     □ │16         41│ □ 2B2
 2A3     □ │17         40│ □ 2B3
 GND     □ │18         39│ □ GND
 2A4     □ │19         38│ □ 2B4
 2A5     □ │20         37│ □ 2B5
 2A6     □ │21         36│ □ 2B6
 VCC     □ │22         35│ □ VCC
 2A7     □ │23         34│ □ 2B7
 2A8     □ │24         33│ □ 2B8
 GND     □ │25         32│ □ GND
 2SAB    □ │26         31│ □ 2SBA
 2CLKAB  □ │27         30│ □ 2CLKBA
 2OEAB   □ │28         29│ □ 2OEBA
           └─────────────┘
              FCT16652-3
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Pin Description

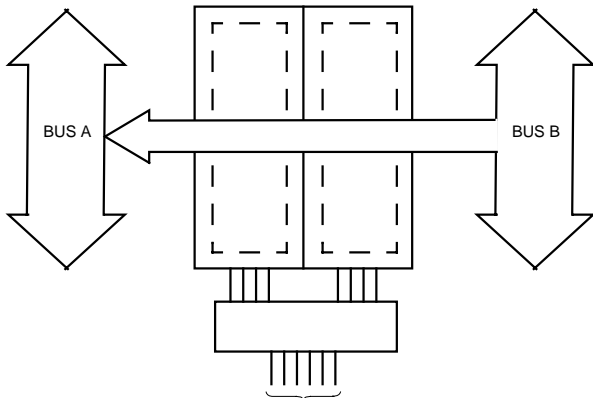| Name	Description
A	Data Register A Inputs Data Register B Outputs
B	Data Register B Inputs Data Register A Outputs
CLKAB, CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
OEAB, $\overline{OEBA}$	Output Enable Inputs

Function Table[1]

Inputs						Data I/O[2]		
OEAB	**$\overline{\text{OEBA}}$**	**CLKAB**	**CLKBA**	**SAB**	**SBA**	**A**	**B**	**Operation or Function**
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X			Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[2]	Store A, Hold B
H	H	↑	↑	X[3]	X	Input	Output	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified[2]	Input	Hold A, Store B
L	L	↑	↑	X	X[3]	Input	Input	Store B in both Registers
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
H	H	H or L	X	H	X			Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A Data to B Bus and Stored B Data to A Bus

Notes:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ =LOW-to-HIGH Transition
2. The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{\text{OEBA}}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
3. Select control=L; clocks can occur simultaneously.
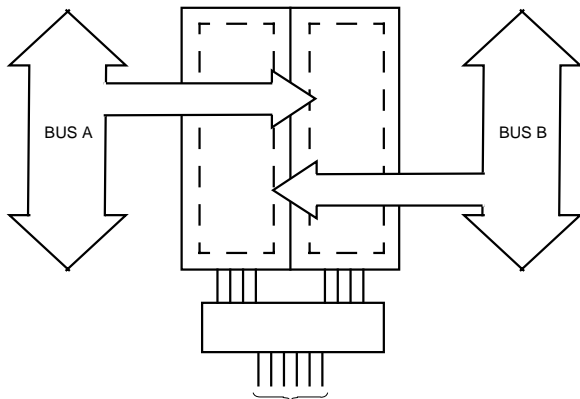   Select control=H; clocks must be staggered to load both registers.

OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
L	L	X	X	X	L

Real-Time Transfer
Bus B to Bus A
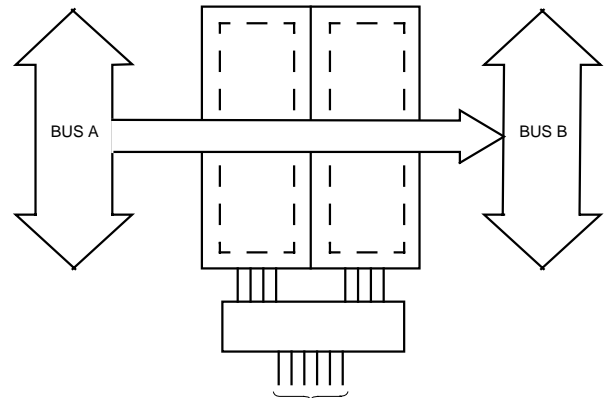
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	X	X	L	X

Real-Time Transfer
Bus A to Bus B

OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
X	H	⌐	⌐	X	X
L	X	X	X	X	X
L	H	⌐	⌐	X	X

Storage from
A and/or B
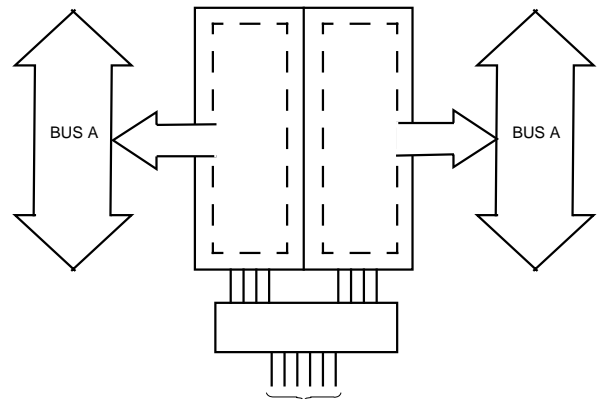
OEAB	$\overline{OEBA}$	CLKAB	CLKBA	SAB	SBA
H	L	H or L	H or L	H	H

Transfer Stored Data
to A and/or B

Maximum Ratings[4]

(Above which the useful life may be impaired. For user guide-lines, not tested.)

Storage Temperature ....Com'l −55°C to +125°C

Ambient Temperature with
Power Applied ....Com'l −55°C to +125°C

DC Input Voltage ....−0.5V to +7.0V

DC Output Voltage ....−0.5V to +7.0V

DC Output Current
(Maximum Sink Current/Pin) ....−60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage..>2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	−40°C to +85°C	5V ± 10%

Note:
4. Stresses greater than those listed under Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH Level	2.0			V
V_{IL}	Input LOW Voltage	Logic LOW Level			0.8	V
V_H	Input Hysteresis			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		−0.7	−1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[8]	V_{CC}=Max., V_{OUT}=GND	−80	−140	−200	mA
I_O	Output Drive Current[8]	V_{CC}=Max., V_{OUT}=2.5V	−50		−180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[7]			±1	µA

Output Drive Characteristics for CY74FCT16652T

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162652T

Parameter	Description	Test Conditions[5]	Min.	Typ.[6]	Max.	Unit
I_{ODL}	Output LOW Current[8]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[8]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance (T_A = +25˚C, f = 1.0 MHz)

Parameter	Description[10]	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Notes:
5. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
6. Typical values are at V_{CC}=5.0V, +25°C ambient.
7. Tested at T_A= +25°C.
8. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
9. Duration of the condition cannot exceed one second.
10. This parameter is measured at characterization but not tested.

Power Supply Characteristics

Param.	Description	Test Conditions[11]		Min.	Typ.[12]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	$V_{IN} \leq 0.2V$ $V_{IN} \geq V_{CC}-0.2V$	—	5	500	μA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN}=3.4V[13]		—	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[14]	V_{CC}=Max. Outputs Open OEAB=$\overline{OEAB}$=GND One Input Toggling 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	75	120	μA/ MHz
I_C	Total Power Supply Current[15]	V_{CC}=Max. Outputs Open f_o=10 MHz (CLKBA) 50% Duty Cycle OEAB=$\overline{OEBA}$=GND One-Bit Toggling f_1=5 MHz 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	0.8	1.7	mA
			V_{IN}=3.4V or V_{IN}=GND	—	1.3	3.2	mA
		V_{CC}=Max. Outputs Open f_o=10 MHz (CLKBA) 50% Duty Cycle OEAB=$\overline{OEBA}$=GND Sixteen Bits Toggling f_1=2.5 MHz 50% Duty Cycle	V_{IN}=V_{CC} or V_{IN}=GND	—	3.8	6.5[16]	mA
			V_{IN}=3.4V or V_{IN}=GND	—	8.3	20.0[16]	mA

Notes:

11. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
12. Typical values are at V_{CC}=5.0V +25° ambient.
13. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
14. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
15. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = $I_{CC}+\Delta I_{CC}D_H N_T+I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
16. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[17]

| Parameter | Description | CY74FCT16652AT CY74FCT162652AT | | Unit | Fig. No.[18] |
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	6.3	ns	1, 3
t_{PZH} t_{PHL}	Output Enable Time OEAB or $\overline{OEBA}$ to Bus	1.5	9.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time OEAB or $\overline{OEBA}$ to Bus	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	6.3	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus	1.5	7.7	ns	1, 5
t_{SU}	Set-Up time HIGH or LOW Bus to Clock	2.0	—	ns	4
t_{H}	Hold Time HIGH or LOW Bus to Clock	1.5	—	ns	4
t_{W}	Clock Pulse Width HIGH or LOW	5.0	—	ns	5
$t_{SK(O)}$	Output Skew[19]	—	0.5	ns	

| Parameter | Description | CY74FCT16652CT CY74FCT162652CT | | Unit | Fig. No.[18] |
		Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	1.5	5.4	ns	1, 3
t_{PZH} t_{PHL}	Output Enable Time OEAB or $\overline{OEBA}$ to Bus	1.5	7.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time OEAB or $\overline{OEBA}$ to Bus	1.5	6.3	ns	1, 7, 8
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus	1.5	5.7	ns	1, 5
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus	1.5	6.2	ns	1, 5
t_{SU}	Set-Up Time HIGH or LOW Bus to Clock	2.0	—	ns	4
t_{H}	Hold Time HIGH or LOW Bus to Clock	1.5	—	ns	4
t_{W}	Clock Pulse Width HIGH or LOW	5.0	—	ns	5
$t_{SK(O)}$	Output Skew[19]	—	0.5	ns	

Notes:
17. Minimum limits are specified, but not tested, on propagation delays.
18. See "Parameter Measurement Information" in the General Information section.
19. Skew between any two outputs of the same package switching in the same direction. This parameter ensured by design.

Ordering Information CY74FCT16652

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	CY74FCT16652CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
6.3	CY74FCT16652ATPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162652

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.4	74FCT162652CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162652CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162652CTPVCT	O56	56-Lead (300-Mil) SSOP	
6.3	CY74FCT162652ATPVC	O56	56-Lead (300-Mil) SSOP	Industrial
	74FCT162652ATPVCT	O56	56-Lead (300-Mil) SSOP	

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Package Diagrams

56-Lead Shrunk Small Outline Package O56

DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

56-Lead Thin Shrunk Small Outline Package Z56

DIMENSIONS IN INCHES $\frac{MIN.}{MAX.}$

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PACKAGE OPTION ADDENDUM
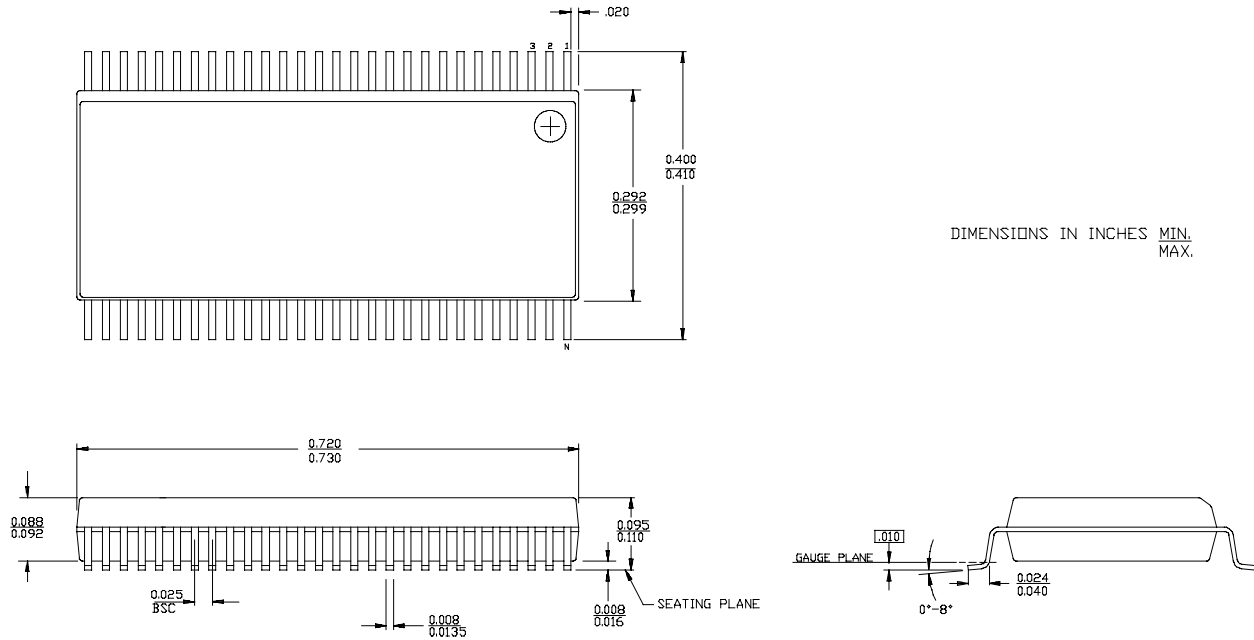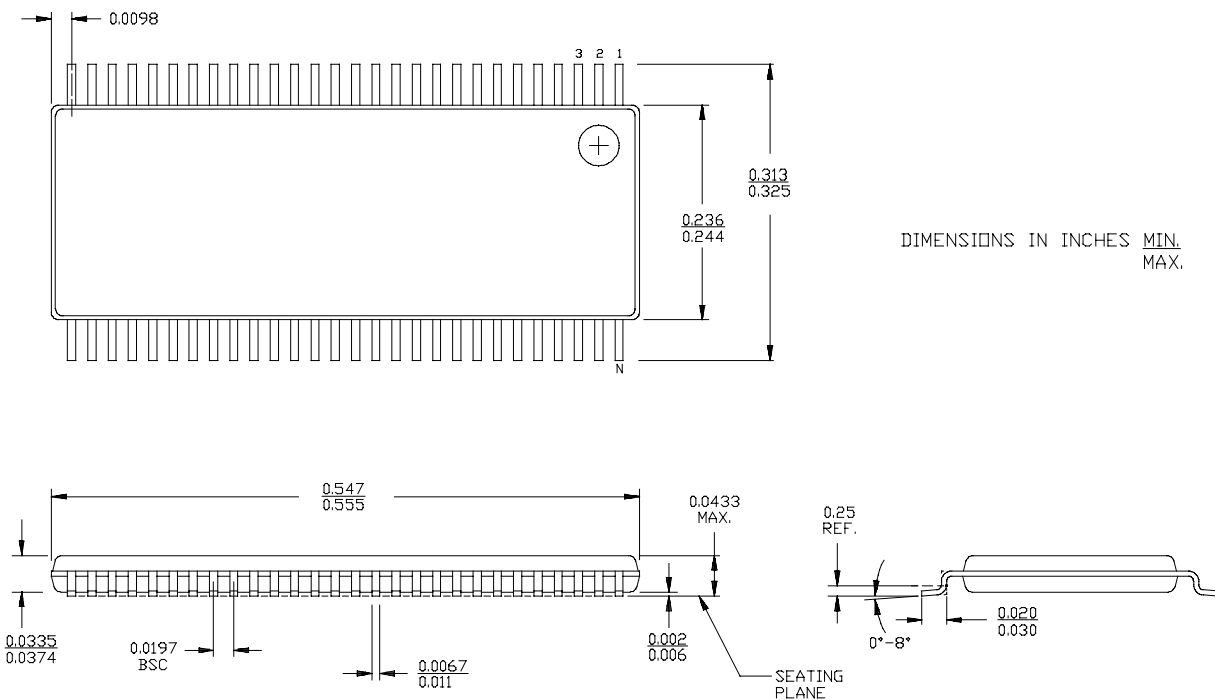
PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74FCT162652ATPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162652ATPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162652CTPACT	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162652CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT162652ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
74FCT162652ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
74FCT16652ATPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16652ATPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16652CTPVCG4	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74FCT16652CTPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162652ATPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162652CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT162652ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT162652ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16652ATPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16652ATPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16652CTPVC	ACTIVE	SSOP	DL	56	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16652CTPVCT	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CY74FCT16652ETPAC	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT16652ETPACT	OBSOLETE	TSSOP	DGG	56		TBD	Call TI	Call TI
CY74FCT16652ETPVC	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
CY74FCT16652ETPVCT	OBSOLETE	SSOP	DL	56		TBD	Call TI	Call TI
FCT162652ATPVCTG4	ACTIVE	SSOP	DL	56	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162652CTPACTE4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
FCT162652CTPACTG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

www.BDTIC.com/TI

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
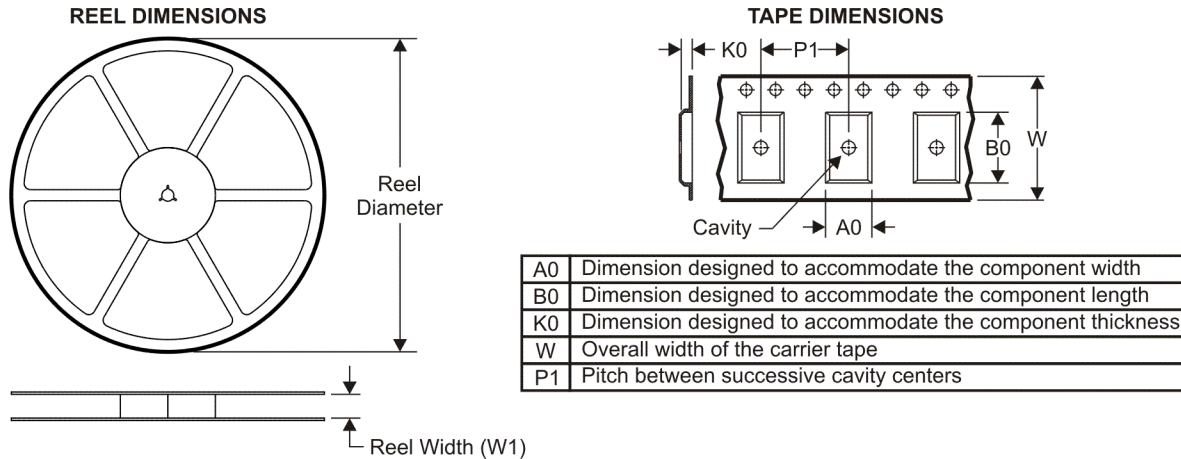
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162652ATPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
74FCT162652CTPACT	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
CY74FCT16652ATPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
CY74FCT16652CTPVCT	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162652ATPVCT	SSOP	DL	56	1000	346.0	346.0	49.0
74FCT162652CTPACT	TSSOP	DGG	56	2000	346.0	346.0	41.0
CY74FCT16652ATPVCT	SSOP	DL	56	1000	346.0	346.0	49.0
CY74FCT16652CTPVCT	SSOP	DL	56	1000	346.0	346.0	49.0

DL (R-PDSO-G**)　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0.025 (0,635)

0.0135 (0,343) / 0.008 (0,203)

⊕ 0.005 (0,13) Ⓜ

48　　　　　　25

0.010 (0,25) / 0.005 (0,13)

0.299 (7,59) / 0.291 (7,39)

0.420 (10,67) / 0.395 (10,03)

Gage Plane

0.010 (0,25)

1　　　　　　24

0°–8°

0.040 (1,02) / 0.020 (0,51)

A

0.110 (2,79) MAX　　　　0.008 (0,20) MIN

Seating Plane

△ 0.004 (0,10)

	PINS **	28	48	56
DIM				
A MAX		0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN		0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048 / E 12/01
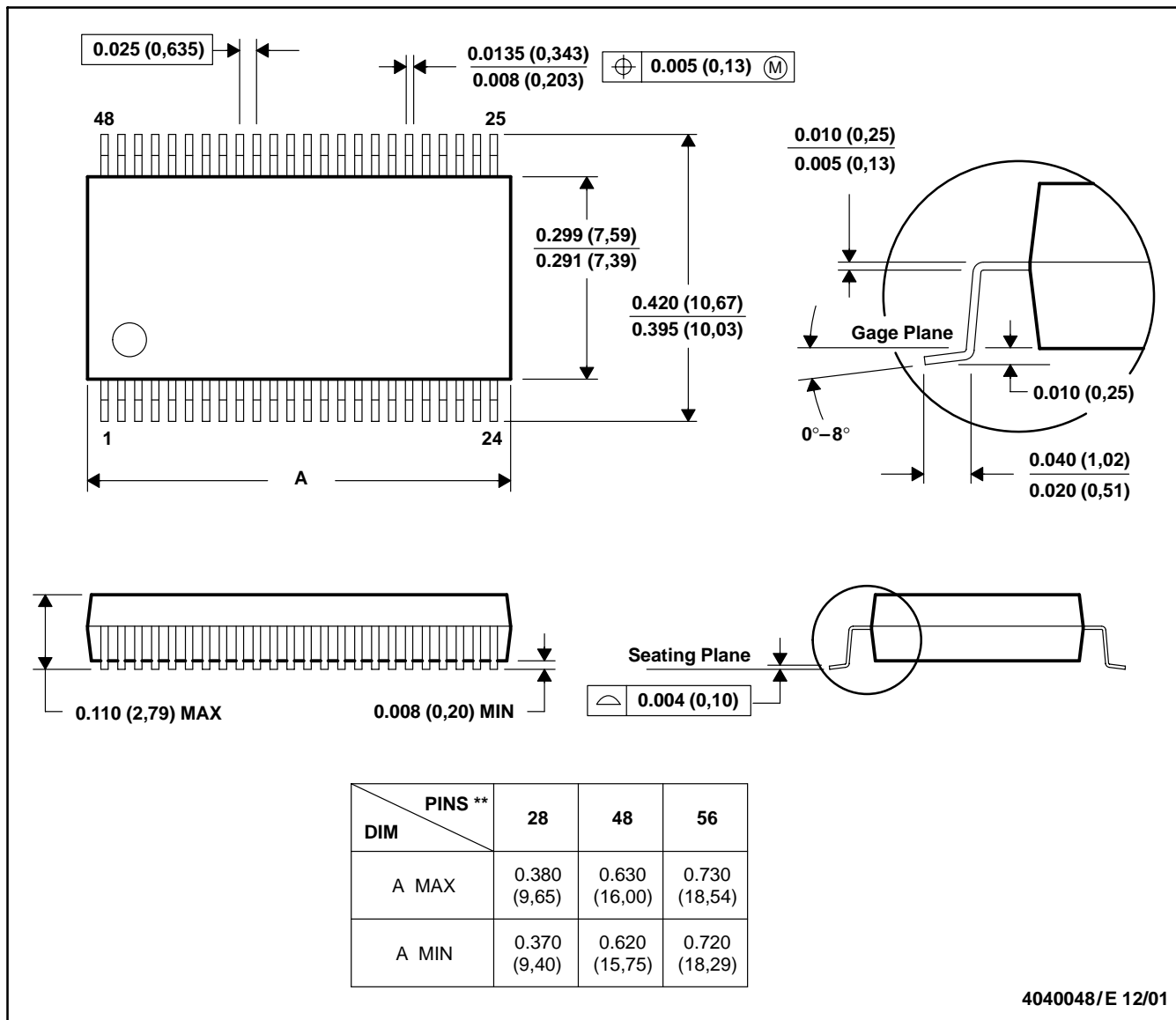
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

DGG (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

PINS ** DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97
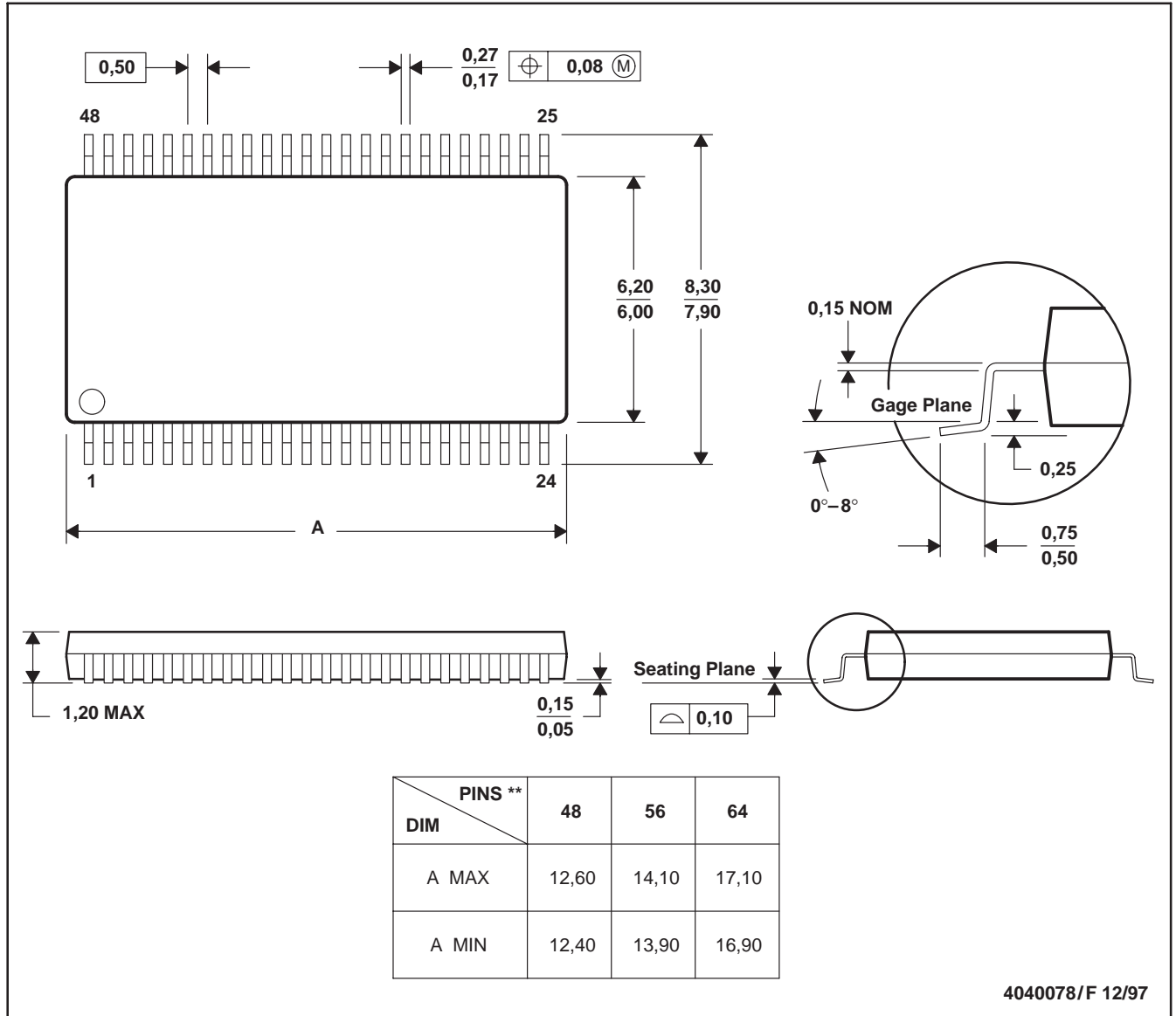
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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