

## 14-BIT 2.4-GSPS DIGITAL-TO-ANALOG CONVERTER

Check for Samples: [DAC5670-SP](#)

### FEATURES

- 14-Bit Resolution
- 2.4-GSPS Maximum Update Rate Digital to Analog Converter
- Dual Differential Input Ports
  - Even/Odd Demultiplexed Data
  - Maximum 1.2 GSPS Each Port, 2.4 GSPS Total
  - Dual 14-Bit Inputs + 1 Reference Bit
  - DDR Output Clock
  - DLL Optimized Clock Timing Synchronized to Reference Bit
  - LVDS and HyperTransport™ Voltage Level Compatible
  - Internal 100-Ω Terminations for Data and Reference Bit Inputs
- Selectable 2 Times Interpolation With  $F_s/2$  Mixing

- Differential Scalable Current Outputs: 5 mA to 30 mA
- On-Chip 1.2-V Reference
- 3.3-V Analog Supply Operation
- Power Dissipation: 2 W
- 192-Ball CBGA (GEM) Package
- QML-V Qualified, SMD 5962-07247
- Military Temperature Range (-55°C to 125°C  $T_{case}$ )

### APPLICATIONS

- Cable Modem Termination System Direct Synthesis
- Cellular Base Transceiver Station Transmit Channels
  - CDMA: W-CDMA, CDMA2000, TD-SCDMA
  - 800 to 900-MHz Direct Synthesis
- Point-to-Point Microwave
- Radar
- Satellite Communications

### DESCRIPTION

The DAC5670 is a 14-bit 2.4-GSPS digital-to-analog converter (DAC) with dual demultiplexed differential input ports. The DAC5670 is clocked at the DAC sample rate and the two input ports run at a maximum of 1.2 GSPS. An additional reference bit input sequence is used to adjust the output clock delay to the data source, optimizing the internal data latching clock relative to this reference bit with a delay lock loop (DLL).

The DAC5670 also can accept data up to 1.2 GSPS on one input port the same clock configuration. In the single port mode, repeating the input sample (A\_ONLY mode), 2 times interpolation by zero stuff (A\_ONLY\_ZS mode), or 2 times interpolation by repeating and inverting the input sample (A\_ONLY\_INV) are used to double the input sample rate up to 2.4 GSPS.

The DAC5670 operates with a single 3-V to 3.6-V supply voltage. Power dissipation is 2 W at maximum operating conditions. The DAC5670 provides a nominal full-scale differential current-output of 20 mA, supporting both single-ended and differential applications. An on-chip 1.2-V temperature-compensated bandgap reference and control amplifier allows the user to adjust the full-scale output current from the nominal 20 mA to as low as 5 mA or as high as 30 mA. The output current can be directly fed to the load with no additional external output buffer required. The device has been specifically designed for a differential transformer coupled output with a 50-Ω doubly-terminated load.

The DAC5670 is available in a 192-ball CBGA package. The device is characterized for operation over the military temperature range (-55°C to 125°C  $T_{case}$ ).



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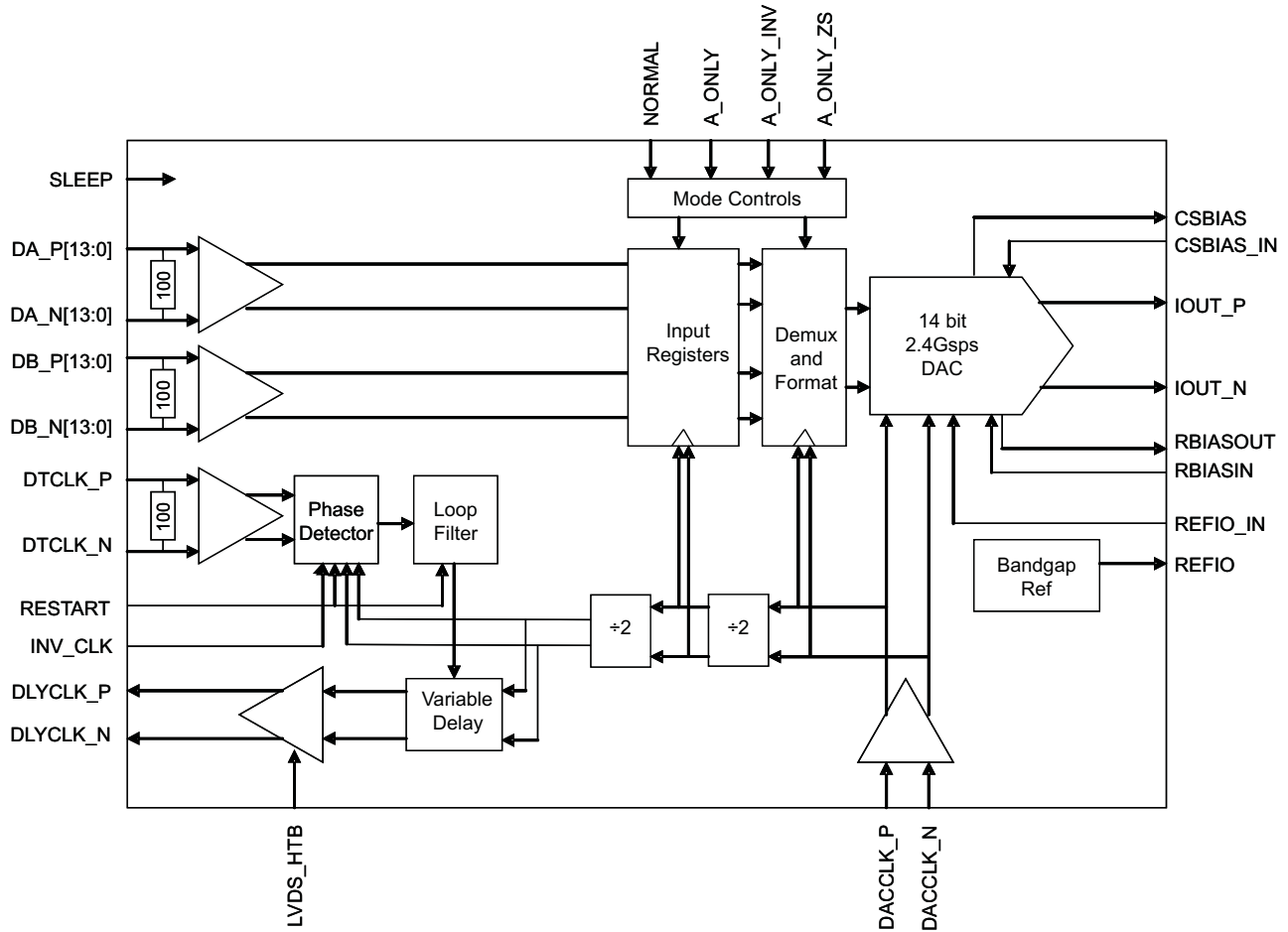
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**AVAILABLE OPTIONS**

TEMPERATURE	PACKAGE <sup>(1)</sup>	TOP SIDE SYMBOL
-55°C to 125°C T <sub>case</sub>	192-GEM	5962-0724701VXA DAC5670MGEM-V

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.



**Figure 1. Functional Block Diagram DAC5670**

**Table 1. Terminal Assignments (Top View)**

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
<b>A</b>		DB10_N	DB10_P	DB12_P	DB12_N	DLYCLK_N	DLYCLK_P	DTCLK_N	DTCLK_P	DA2_N	DA2_P	DA3_N	DA3_P	
<b>B</b>	DB9_P	GND	GND	DB11_P	DB11_N	DB13_N	DB13_P	DA0_P	DA0_N	DA1_P	DA1_N	GND	GND	DA4_P
<b>C</b>	DB9_N	DB8_P	AVDD	AVDD	AVDD	GND	GND	GND	GND	AVDD	DA7_N	DA7_P	DA5_P	DA4_N
<b>D</b>	DB7_N	DB8_N	DB6_P	DB6_N	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	DA6_N	DA6_P	DA5_N	DA8_N
<b>E</b>	DB7_P	DB5_N	AVDD	AVDD	GND	GND	GND	GND	GND	GND	AVDD	AVDD	DA9_N	DA8_P
<b>F</b>	DB3_N	DB5_P	GND	AVDD	GND	GND	GND	GND	GND	GND	AVDD	GND	DA9_P	DA10_N
<b>G</b>	DB3_P	AVDD	GND	AVDD	GND	GND	AVDD	AVDD	GND	GND	AVDD	GND	DA11_N	DA10_P
<b>H</b>	DB4_N	AVDD	GND	AVDD	GND	GND	AVDD	AVDD	GND	GND	AVDD	GND	DA11_P	DA12_N
<b>J</b>	DB4_P	DB2_P	GND	AVDD	GND	GND	GND	GND	GND	GND	AVDD	GND	DA13_P	DA12_P
<b>K</b>	DB1_P	DB2_N	AVDD	AVDD	GND	GND	GND	GND	GND	GND	AVDD	AVDD	DA13_N	Dacclk_P
<b>L</b>	DB1_N	AVDD	REFIO	REFIO_I_N	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	GND	Inv_clk	AVDD	Dacclk_N
<b>M</b>	DB0_P	GND	AVDD	AVDD	AVDD	IOUT_N	IOUT_P	GND	GND	AVDD	GND	Restart	GND	
<b>N</b>	DB0_N	GND	GND	AVDD	GND	GND	GND	GND	GND	A_only			A_only_z	GND
<b>P</b>		CSCap_IN	CSCap	RBIAS_IN	RBIAS_OUT		GND	GND	LVDS_htb	AVDD	Sleep	A_only_inv	M_Normal	

**Table 2. Terminal Assignments (Bottom View)**

	A	B	C	D	E	F	G	H	J	K	L	M	N	P
<b>1</b>		DB9_P	DB9_N	DB7_N	DB7_P	DB3_N	DB3_P	DB4_N	DB4_P	DB1_P	DB1_N	DB0_P	DB0_N	
<b>2</b>	DB10_N	GND	DB8_P	DB8_N	DB5_N	DB5_P	AVDD	AVDD	DB2_P	DB2_N	AVDD	GND	GND	CSCap_IN
<b>3</b>	DB10_P	GND	AVDD	DB6_P	AVDD	GND	GND	GND	GND	AVDD	REFIO	AVDD	GND	CSCap
<b>4</b>	DB12_P	DB11_P	AVDD	DB6_N	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	REFIO_I_N	AVDD	AVDD	RBIAS_IN
<b>5</b>	DB12_N	DB11_N	AVDD	AVDD	GND	GND	GND	GND	GND	GND	AVDD	AVDD	GND	RBIAS_OUT
<b>6</b>	DLYCLK_N	DB13_N	GND	AVDD	GND	GND	GND	GND	GND	GND	AVDD	IOUT_N	GND	
<b>7</b>	DLYCLK_P	DB13_P	GND	AVDD	GND	GND	AVDD	AVDD	GND	GND	AVDD	IOUT_P	GND	GND
<b>8</b>	DTCLK_N	DA0_P	GND	AVDD	GND	GND	AVDD	AVDD	GND	GND	AVDD	GND	GND	GND
<b>9</b>	DTCLK_P	DA0_N	GND	AVDD	GND	GND	GND	GND	GND	GND	AVDD	GND	GND	LVDS_htb
<b>10</b>	DA2_N	DA1_P	AVDD	AVDD	GND	GND	GND	GND	GND	GND	AVDD	AVDD	A_only	AVDD
<b>11</b>	DA2_P	DA1_N	DA7_N	DA6_N	AVDD	AVDD	AVDD	AVDD	AVDD	AVDD	GND	GND		Sleep
<b>12</b>	DA3_N	GND	DA7_P	DA6_P	AVDD	GND	GND	GND	GND	AVDD	Inv_clk	Restart		A_only_inv
<b>13</b>	DA3_P	GND	DA5_P	DA5_N	DA9_N	DA9_P	DA11_N	DA11_P	DA13_P	DA13_N	AVDD	GND	A_only_z	M_Normal
<b>14</b>		DA4_P	DA4_N	DA8_N	DA8_P	DA10_N	DA10_P	DA12_N	DA12_P	Dacclk_P	Dacclk_N		GND	

**TERMINAL FUNCTIONS**

TERMINAL		Type	DESCRIPTION
NAME	BALL NO.		
DACCLK_P	K14	I	External clock, sample clock for the DAC
DACCLK_N	L14	I	Complementary external clock, sample clock for the DAC
DLYCLK_P	A7	O	DDR type data clock to data source
DLYCLK_N	A6	O	DDR type data clock to data source complementary signal
DTCLK_P	A9	I	Input data toggling reference bit
DTCLK_N	A8	I	Input data toggling reference bit, complementary signal
DA_P[13]	J13	I	Port A data bit 13 (MSB)
DA_N[13]	K13	I	Port A data bit 13 complement (MSB)
DA_P[12]	J14	I	Port A data bit 12
DA_N[12]	H14	I	Port A data bit 12 complement
DA_P[11]	H13	I	Port A data bit 11
DA_N[11]	G13	I	Port A data bit 11 complement
DA_P[10]	G14	I	Port A data bit 10
DA_N[10]	F14	I	Port A data bit 10 complement
DA_P[9]	F13	I	Port A data bit 9
DA_N[9]	E13	I	Port A data bit 9 complement
DA_P[8]	E14	I	Port A data bit 8
DA_N[8]	D14	I	Port A data bit 8 complement
DA_P[7]	C12	I	Port A data bit 7
DA_N[7]	C11	I	Port A data bit 7 complement
DA_P[6]	D12	I	Port A data bit 6
DA_N[6]	D11	I	Port A data bit 6 complement
DA_P[5]	C13	I	Port A data bit 5
DA_N[5]	D13	I	Port A data bit 5 complement
DA_P[4]	B14	I	Port A data bit 4
DA_N[4]	C14	I	Port A data bit 4 complement
DA_P[3]	A13	I	Port A data bit 3
DA_N[3]	A12	I	Port A data bit 3 complement
DA_P[2]	A11	I	Port A data bit 2
DA_N[2]	A10	I	Port A data bit 2 complement
DA_P[1]	B10	I	Port A data bit 1
DA_N[1]	B11	I	Port A data bit 1 complement
DA_P[0]	B8	I	Port A data bit 0 (LSB)
DA_N[0]	B9	I	Port A data bit 0 complement (LSB)
DB_P[13]	B7		Port B data bit 13 (MSB)
DB_N[13]	B6	I	Port B data bit 13 complement (MSB)
DB_P[12]	A4	I	Port B data bit 12
DB_N[12]	A5	I	Port B data bit 12 complement
DB_P[11]	B4	I	Port B data bit 11
DB_N[11]	B5	I	Port B data bit 11 complement
DB_P[10]	A3	I	Port B data bit 10
DB_N[10]	A2	I	Port B data bit 10 complement
DB_P[9]	B1	I	Port B data bit 9
DB_N[9]	C1	I	Port B data bit 9 complement

**TERMINAL FUNCTIONS (continued)**

TERMINAL		Type	DESCRIPTION
NAME	BALL NO.		
DB_P[8]	C2	I	Port B data bit 8
DB_N[8]	D2	I	Port B data bit 8 complement
DB_P[7]	E1	I	Port B data bit 7
DB_N[7]	D1	I	Port B data bit 7 complement
DB_P[6]	D3	I	Port B data bit 6
DB_N[6]	D4	I	Port B data bit 6 complement
DB_P[5]	F2	I	Port B data bit 5
DB_N[5]	E2	I	Port B data bit 5 complement
DB_P[4]	J1	I	Port B data bit 4
DB_N[4]	H1	I	Port B data bit 4 complement
DB_P[3]	G1	I	Port B data bit 3
DB_N[3]	F1	I	Port B data bit 3 complement
DB_P[2]	J2	I	Port B data bit 2
DB_N[2]	K2	I	Port B data bit 2 complement
DB_P[1]	K1	I	Port B data bit 1
DB_N[1]	L1	I	Port B data bit 1 complement
DB_P[0]	M1	I	Port B data bit 0 (LSB)
DB_N[0]	N1	I	Port B data bit 0 complement (LSB)
IOUT_P	M7	O	DAC current output. Full scale when all input bits are set 1.
IOUT_N	M6	O	DAC complementary current output. Full scale when all input bits are 0.
RBIASOUT	P5	O	Rbias resistor current output
RBIASIN	P4	I	Rbias resistor sense input
CSCAP	P3	O	Current source bias voltage
CSCAP_IN	P2	I	Current source bias voltage sense input
REFIO	L3	O	Bandgap reference output
REFIO_IN	L4	I	Bandgap reference sense input
RESTART	M12	I	Resets DLL when high. Low for normal DLL operation.
LVDS_HTB	P9	I	DLYCLK_P/N control, lvds mode when high, ht mode when low
INV_CLK	L12	I	Inverts the DLL target clocking relationship when high. Low for normal DLL operation.
SLEEP	P11	I	Active-high sleep
NORMAL	P13	I	High for {a0,b0,a1,b1,a2,b2, ...} normal mode
A_ONLY	N10	I	High for {a0,a0,a1,a1,a2,a2, ...} A_only mode
A_ONLY_INV	P12	I	High for {a0,-a0, a1,-a1,a2,-a2, ...} A_only_inv mode
A_ONLY_ZS	N13	I	High for {a0,0,a1,0,a2,0, ...} A_only_zs mode

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	AVDD to GND		5.0	V
DA_P[13..0], DA_N[13..0], DB_P[13..0], DB_N[13..0]	Measured with respect to GND	-0.3	AVDD + 0.3	V
NORMAL, A_ONLY, A_ONLY_INV, A_ONLY_ZS	Measured with respect to GND	-0.3	AVDD + 0.3	V
DTCLK_P, DTCLK_N, DACCLK_P, DACCLK_N	Measured with respect to GND	-0.3	AVDD + 0.3	V
LVDS_HTB, INV_CLK, RESTART	Measured with respect to GND	-0.3	AVDD + 0.3	V
IOUT_P, IOUT_N	Measured with respect to GND	AVDD – 0.5	AVDD + 1.5	V
CSCAP_IN, REFIO_IN, RBIAS_IN	Measured with respect to GND	-0.3	AVDD + 0.3	V
Peak input current (any input)			20	mA
Storage temperature range		-65	150	°C
Maximum Junction Temperature			150	°C
Lead temperature 1,6 mm (1/16 in) from the case for 10 s			260	°C

- (1) Stresses above those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## DC Electrical Characteristics

$T_{C,MIN} = -55^{\circ}\text{C}$  to  $T_{C,MAX} = 125^{\circ}\text{C}$ , typical values at  $25^{\circ}\text{C}$ ,  $AV_{DD} = 3\text{ V}$  to  $3.6\text{ V}$ ,  $I_{OUTFS} = 20\text{ mA}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>Resolution</b>			14			Bits
<b>DC Accuracy</b>						
INL	Integral nonlinearity	$T_{C,MIN}$ to $T_{C,MAX}$ , $f_{DAC} = 640\text{ KHz}$ , $f_{OUT} = 10\text{ KHz}$	-7.5	$\pm 1.5$	7.5	LSB
DNL	Differential nonlinearity		-0.98	$\pm 0.8$	1.75	
<b>Monotonicity</b>			14			Bits
<b>Analog Output</b>						
	Offset error	Mid code offset	-0.45	$\pm 0.09$	0.45	%FSR
	Gain error	With external reference	-6.0	$\pm 1.6$	6.0	%FSR
	Gain error	With internal reference	-6.0	$\pm 1.6$	6.0	%FSR
	Full-scale output current				30	mA
	Output compliance range	$I_{O(FS)} = 20\text{ mA}$ , $AV_{DD} = 3.15\text{ V}$ to $3.45\text{ V}$	$AV_{DD} - 0.5$		$AV_{DD} + 0.5$	V
	Output resistance			300 <sup>(2)</sup>		k $\Omega$
	Output capacitance	IOUT_P and IOUT_N single ended		13.7 <sup>(2)</sup>		pF
<b>Reference Output</b>						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current			100		nA
<b>Reference Input</b>						
$V_{REFIO}$	Input voltage range		1.14	1.2	1.26	V
	Input resistance			1 <sup>(2)</sup>		M $\Omega$
	Small-signal bandwidth			1.4		MHz
	Input capacitance			3.2 <sup>(2)</sup>		pF
<b>Temperature Coefficients</b>						
	Offset drift			75		ppm of FSR/ $^{\circ}\text{C}$
	Gain drift	With external reference		75		ppm of FSR/ $^{\circ}\text{C}$
	Gain drift	With internal reference		75		ppm of FSR/ $^{\circ}\text{C}$
	Reference voltage drift			35		ppm/ $^{\circ}\text{C}$
<b>Power Supply</b>						
$AV_{DD}$	Analog supply voltage		3	3.3	3.6	V
$I_{AVDD}$	Analog supply current	$f_{DAC} = 2.4\text{ GHz}$ , NORMAL input mode		560	650	mA
$I_{AVDD}$	Sleep mode, $AV_{DD}$ supply current	Sleep mode (SLEEP pin high)		150	180	mA
P	Power dissipation	$f_{DAC} = 2.4\text{ GHz}$ , NORMAL input mode		1800	2350	mW
PSRR	Power-supply rejection ratio	$AV_{DD} = 3.15\text{ V}$ to $3.45\text{ V}$		0.4	1.3	%FSR/V

(1) Typicals are characterization values at  $25^{\circ}\text{C}$  and  $AV_{DD} = 3.3\text{ V}$ . These parameters are characterized but not production tested.

(2) Specified by design

**AC Electrical Characteristics**

T<sub>C,MIN</sub> = -55°C to T<sub>C,MAX</sub> = 125°C, typical values at 25°C, AVDD = 3 V to 3.6 V, I<sub>OUTFS</sub> = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>Analog Output</b>						
f <sub>DAC</sub>	Maximum output update rate		2.4			GSPS
t <sub>s(DAC)</sub>	Output setting time to 0.1%	Mid-scale transition		3.5		ns
t <sub>pd</sub>	Output propagation delay			7 DACCLK + 1.5 ns		
t <sub>r(IOUT)</sub>	Output rise time, 10% to 90%			280		ps
t <sub>f(IOUT)</sub>	Output fall time, 90% to 10%			280		ps
<b>AC Performance</b>						
SFDR	Spurious-free dynamic range	f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 100 MHz, Dual-port mode, 0 dBFS	46	55		dBc
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 200 MHz, Dual-port mode, 0 dBFS		51		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 300 MHz, Dual-port mode, 0 dBFS	31	36		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 500 MHz, Dual-port mode, 0 dBFS	35	43		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 500 MHz, Dual-port mode, -6 dBFS		47		
SNR	Signal-to-noise ratio	f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 100 MHz, Dual-port mode, 0 dBFS	58	60		dBc
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 200 MHz, Dual-port mode, 0 dBFS		60		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 300 MHz, Dual-port mode, 0 dBFS	56	62		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 500 MHz, Dual-port mode, 0 dBFS	51	58		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 500 MHz, Dual-port mode, -6 dBFS		52		
THD	Total harmonic distortion	f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 100 MHz, Dual-port mode, 0 dBFS	45	52		dBc
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 200 MHz, Dual-port mode, 0 dBFS		50		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 300 MHz, Dual-port mode, 0 dBFS	31	36		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 500 MHz, Dual-port mode, 0 dBFS	35	46		
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 500 MHz, Dual-port mode, -6 dBFS		44		
IMD3	Third-order two-tone intermodulation	f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 99 MHz and 102 MHz, Each tone at -6 dBFS, Dual-port mode.		70		dBc
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 200 MHz and 202 MHz, Each tone at -6 dBFS, Dual-port mode.		68		dBc
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 253 MHz and 257 MHz, Each tone at -6 dBFS, Dual-port mode.	47	57		dBc
		f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 299 MHz and 302 MHz, Each tone at -6 dBFS, Dual-port mode.	35	55		dBc
IMD	Four-tone intermodulation	f <sub>DAC</sub> = 2.4 GSPS, f <sub>OUT</sub> = 298 MHz, 299 MHz, 300 MHz, and 301 MHz, Each tone at -12 dBFS, Dual-port mode.	47	62.5		dBc

(1) Typicals are characterization values at 25C and AVDD = 3.3V. These parameters are characterized but not production tested



## Digital Electrical Characteristics

$T_{C,MIN} = -55^{\circ}C$  to  $T_{C,MAX} = 125^{\circ}C$ , typical values at  $25^{\circ}C$ ,  $AVDD = 3V$  to  $3.6V$ ,  $I_{outFS} = 20mA$  (unless otherwise noted)

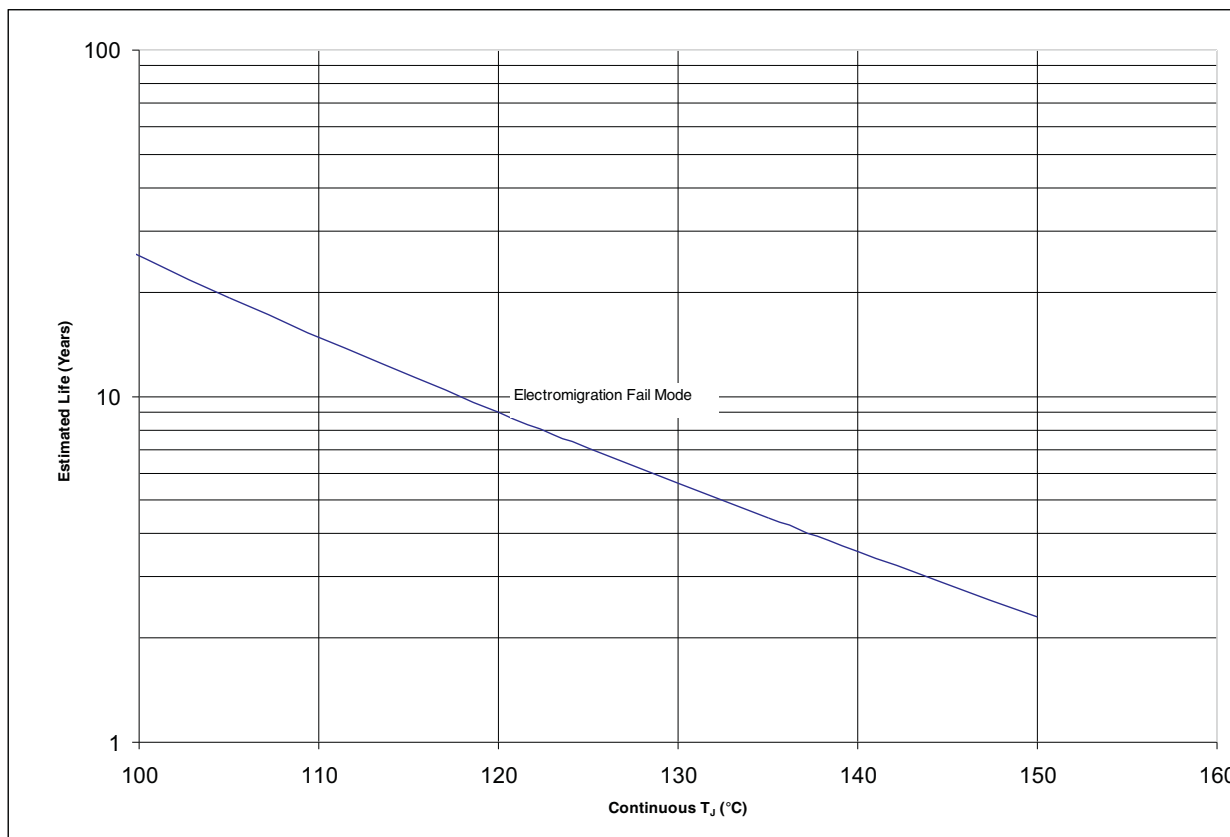
PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>CMOS Interface (SLEEP, RESTART, INV_CLK, NORMAL, A_ONLY, A_ONLY_INV, A_ONLY_ZS)</b>						
$V_{IH}$	High-level input voltage		2	3		V
$V_{IL}$	Low-level input voltage		0	0	0.8	V
$I_{IH}$	High-level input current			0.2	10	$\mu A$
$I_{IL}$	Low-level input current		-10	-0.2		$\mu A$
	Input capacitance			2.5 <sup>(2)</sup>		pF
<b>Differential Data Interface (DA_P[13:0], DA_N[13:0], DB_P[13:0], DB_N[13:0], DTCLK_P, DTCLK_N)</b>						
$V_{ITH}$	Differential input threshold		-100		100	mV
$Z_T$	Internal termination impedance		80	100	125	$\Omega$
$V_{ICOM}$	Input common mode		0.6		1.4	V
$C_i$	Input capacitance			2.6 <sup>(2)</sup>		pF
<b>Clock Inputs (DACCLK_P, DACCLK_N)</b>						
$ DACCLK\_P - DACCLK\_N $	Clock differential input voltage		200		1000	mV
	Clock duty cycle		40		60	%
VCLKCM	Clock common mode		1.0		1.4	V

(1) Typicals are characterization values at  $25^{\circ}C$  and  $AVDD = 3.3V$ . These parameters are characterized but not production tested

(2) Specified by design

**Table 3. Thermal Information**

Parameter		TEST CONDITIONS	TYPICAL	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Non-thermally enhanced JEDEC standard PCB, per JESD-51, 51-3	41.3	$^{\circ}C/W$
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 test method 1012	3.8	$^{\circ}C/W$



- A. See data sheet for absolute maximum and minimum recommended operating conditions.
- B. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

**Figure 2. DAC5670MGEM-V - 192/GEM Package Operating Life Derating Chart**

### TYPICAL CHARACTERISTICS

Single-Tone Spectrum Power  
vs  
Frequency

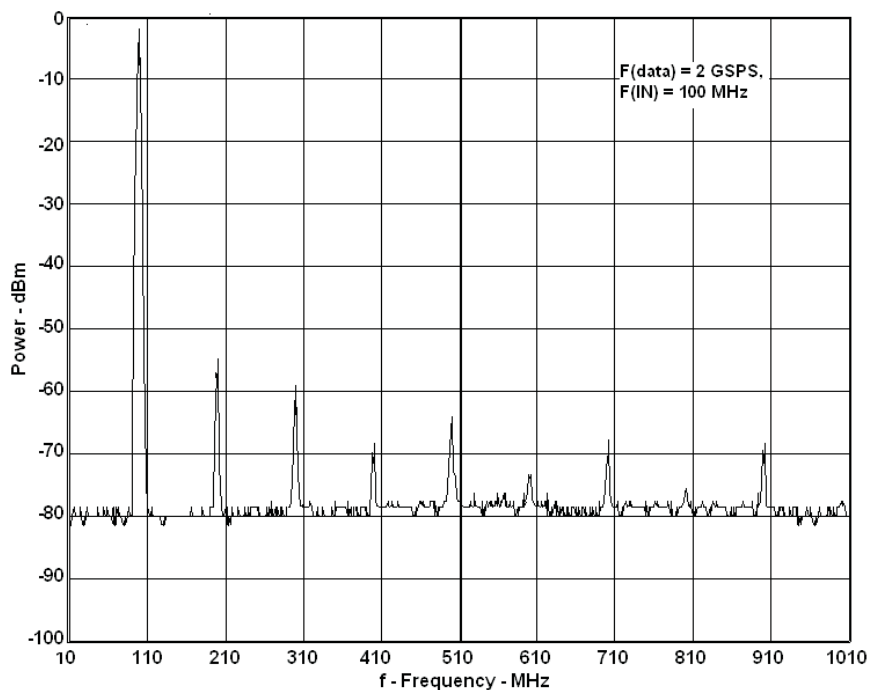


Figure 3.

Two-Tone IMD (Power)  
vs  
Frequency

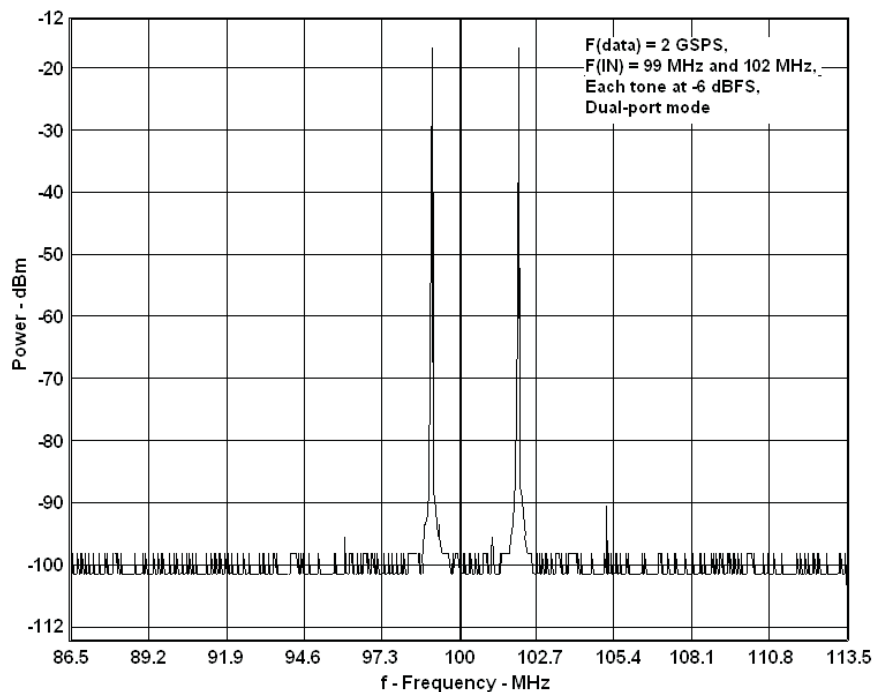


Figure 4.

**TYPICAL CHARACTERISTICS (continued)**

**W-CDMA TM1 Single Carrier Power  
vs  
Frequency**

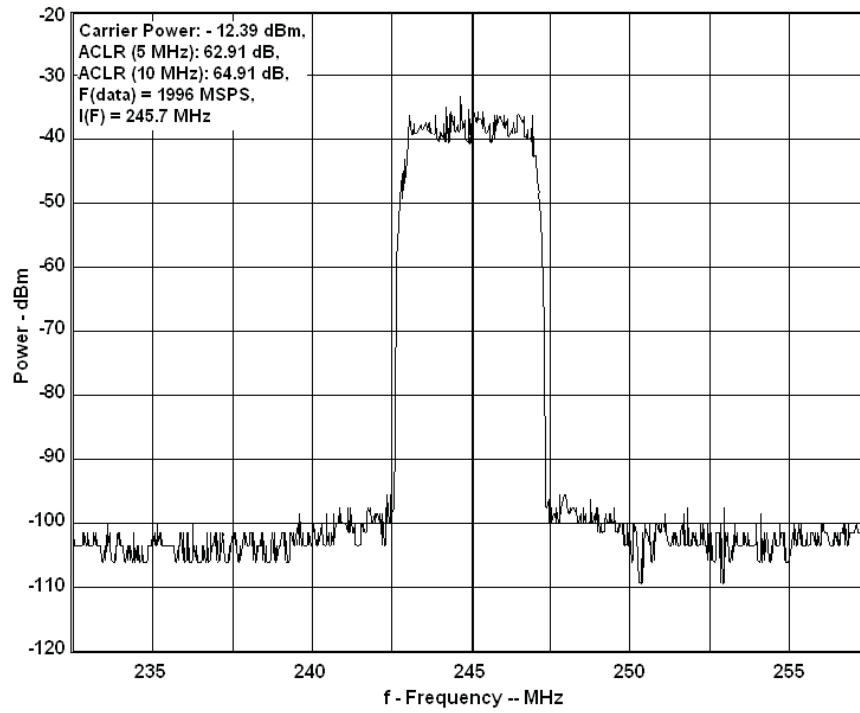
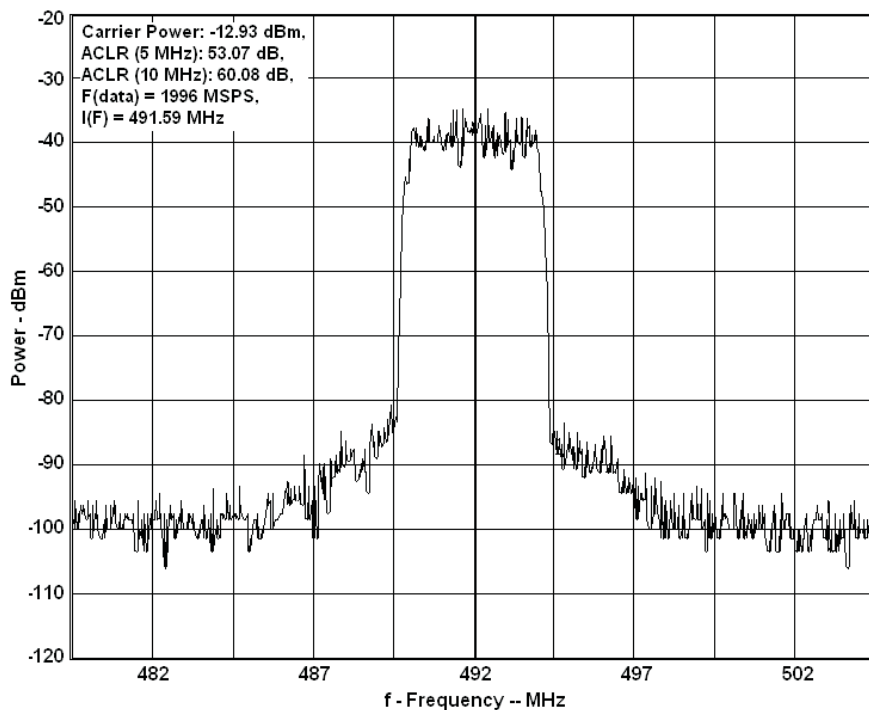


Figure 5.

**TYPICAL CHARACTERISTICS (continued)**

**W-CDMA TM1 Single Carrier Power  
vs  
Frequency**



**Figure 6.**

### TYPICAL CHARACTERISTICS (continued)

W-CDMA TM1 Dual Carrier Power  
vs  
Frequency

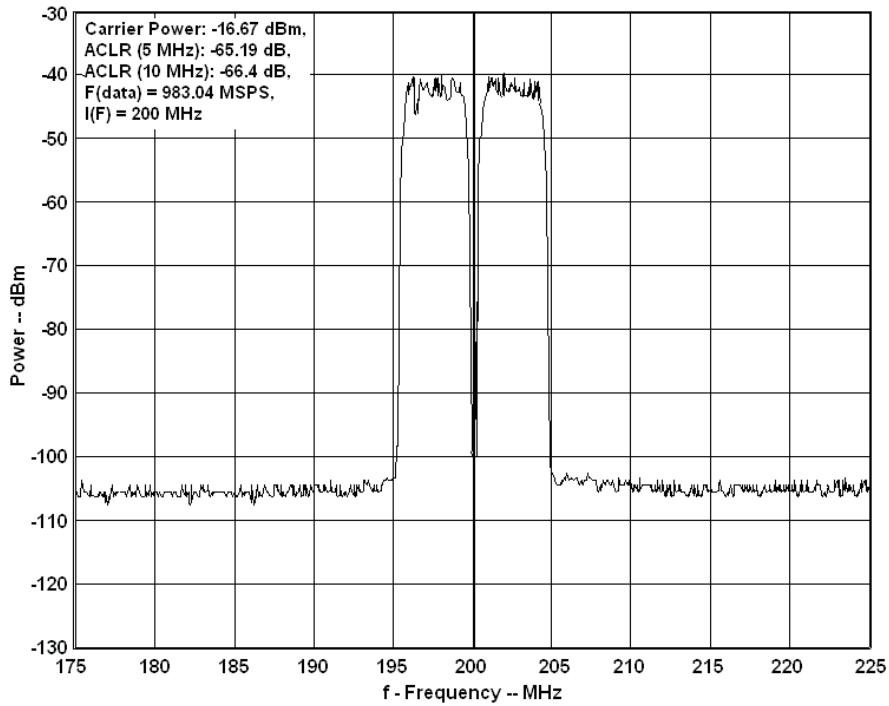


Figure 7.

### TYPICAL CHARACTERISTICS (continued)

W-CDMA TM1 Three Carrier Power  
vs  
Frequency

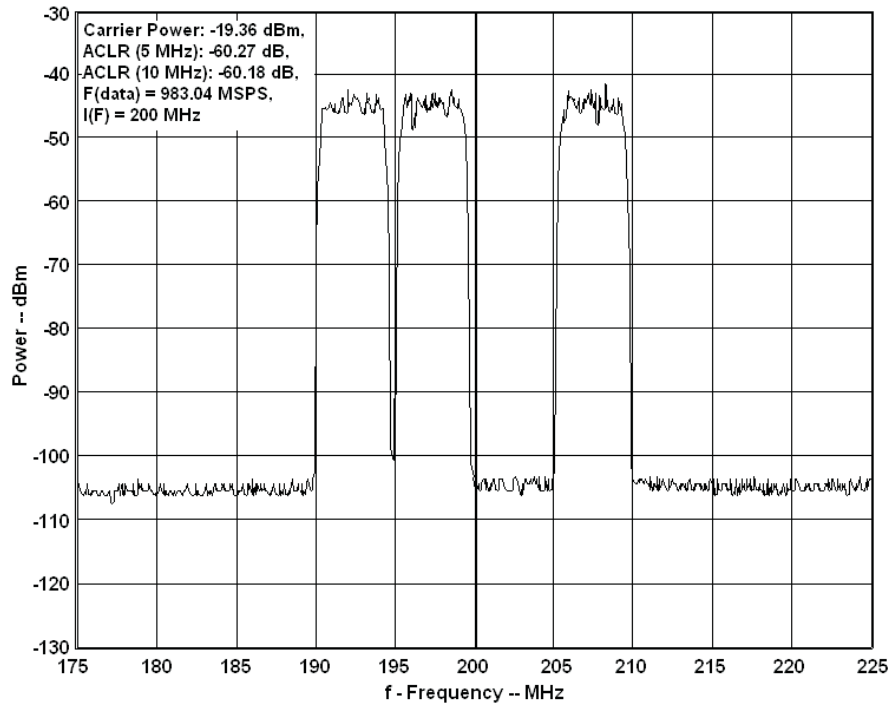


Figure 8.

**TYPICAL CHARACTERISTICS (continued)**

**W-CDMA TM1 Four Carrier Power  
vs  
Frequency**

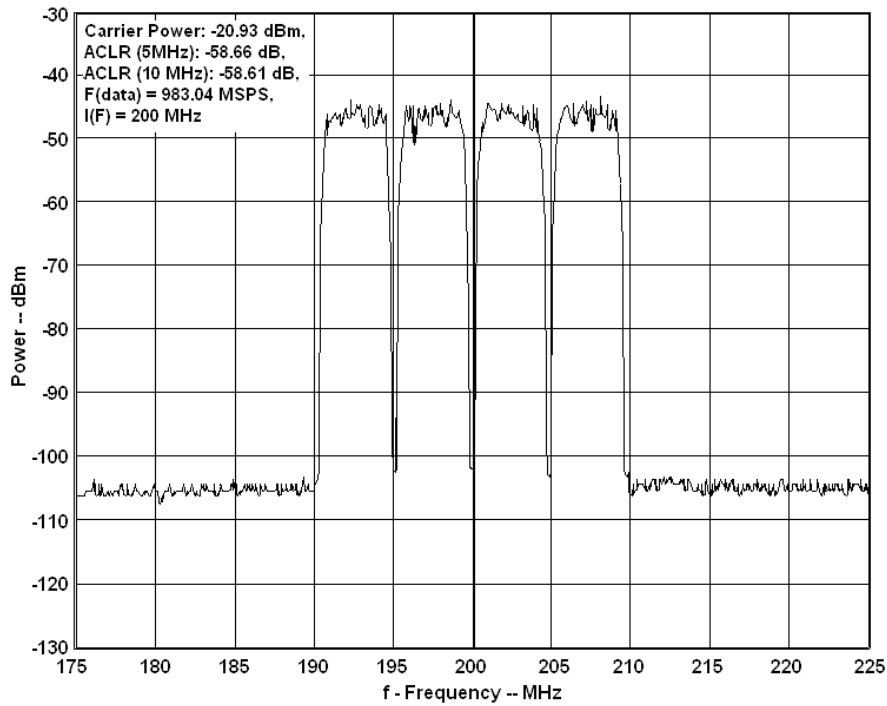


Figure 9.



APPLICATION INFORMATION

Detailed Description

Figure 10 shows a simplified block diagram of the current steering DAC5670. The DAC5670 consists of a segmented array of NPN-transistor current sinks, capable of delivering a full-scale output current up to 30mA. Differential current switches direct the current of each current sink to either one of the complementary output nodes IOUT\_P or IOUT\_N. The complementary current output enables differential operation, canceling out common-mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, and even-order distortion components, and doubling signal output power.

The full-scale output current is set using an external resistor (RBIAS) in combination with an on-chip bandgap voltage reference source (1.2V) and control amplifier. The current (IBIAS) through resistor RBIAS is mirrored internally to provide a full-scale output current equal to 32 times IBIAS. The full-scale current is adjustable from 30mA down to 5mA by using the appropriate bias resistor value.

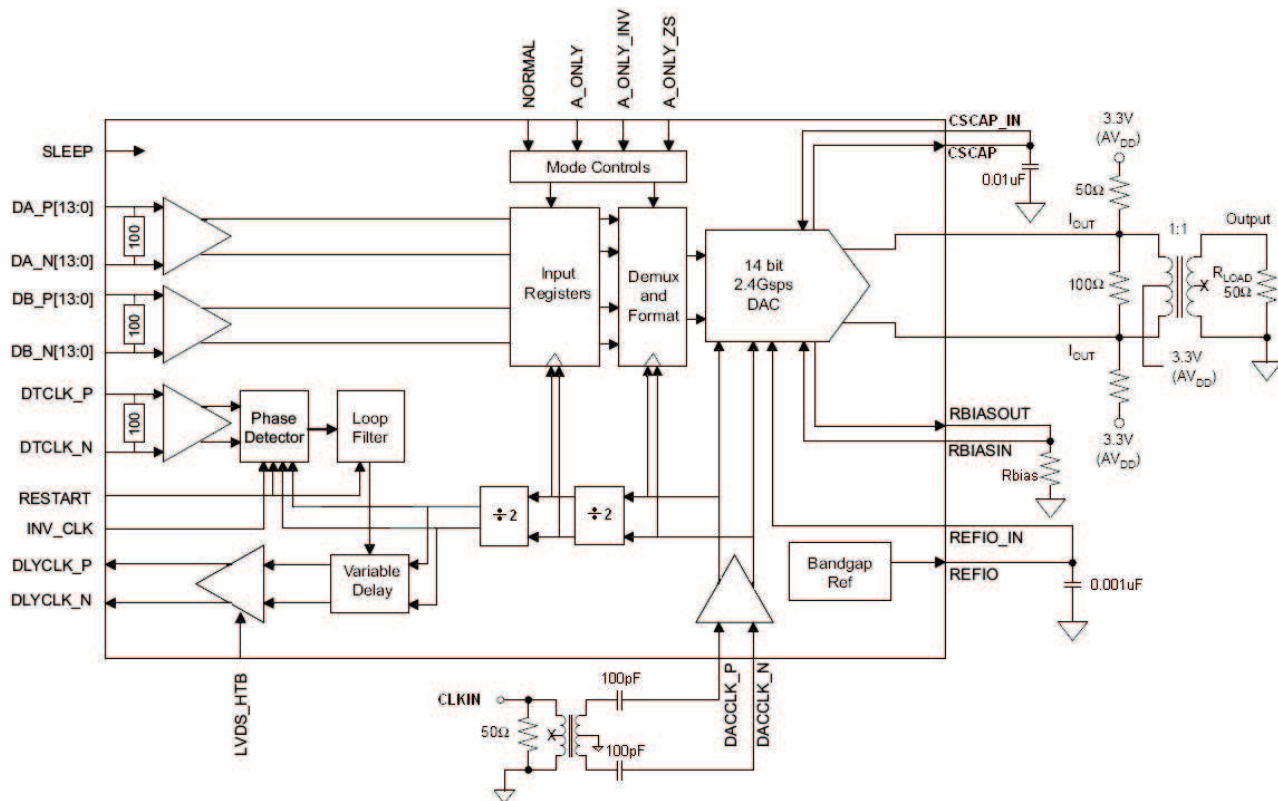
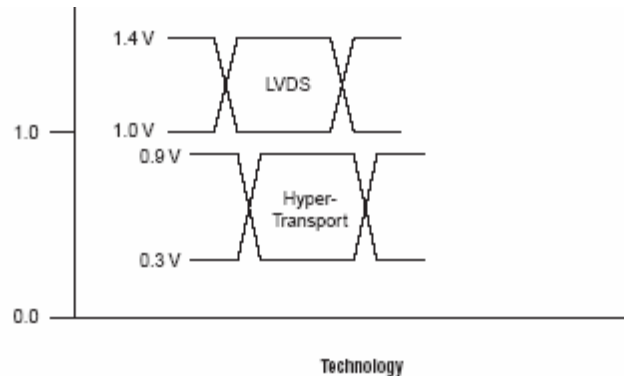


Figure 10. Current Steering DAC5670

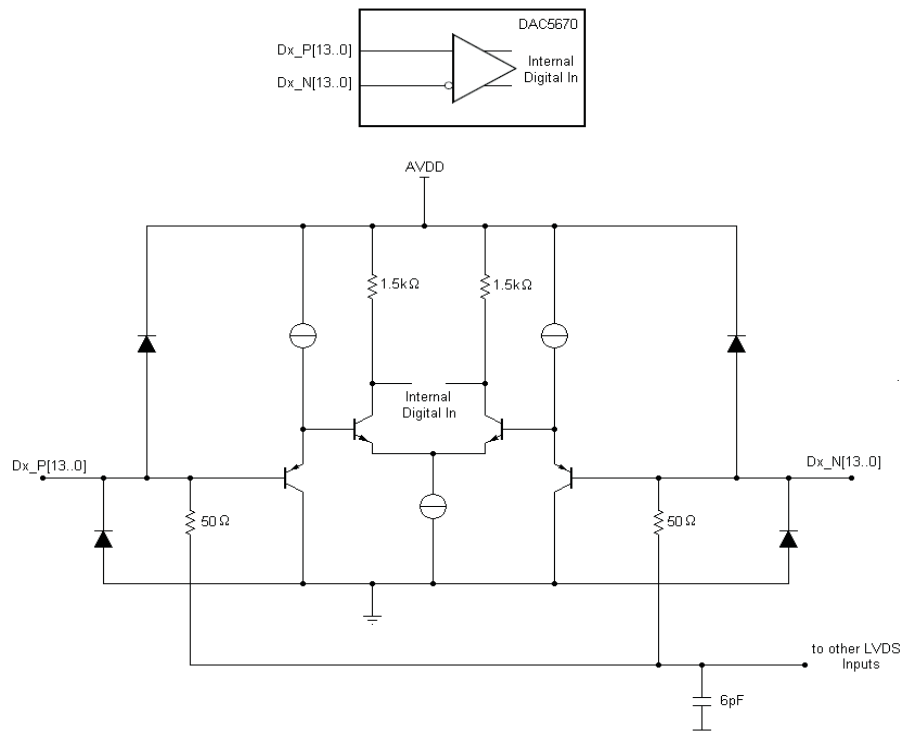
**Digital Inputs**

The DAC5670 differential digital inputs are compatible with LVDS and HyperTransport voltage levels.



**Figure 11. Digital Input Voltage Options**

The DAC5670 uses low voltage differential signaling (LVDS and Hyper-Transport) for the bus input interface. The LVDS and Hyper-Transport input modes feature a low differential voltage swing. The differential characteristic of LVDS and Hyper-Transport modes allow for high-speed data transmission with low electromagnetic interference (EMI) levels. Figure 12 shows the equivalent complementary digital input interface for the DAC5670, valid for pins DA\_P[13:0], DA\_N[13:0], DB\_P[13:0], and DB\_N[13:0].



**Figure 12.**

Figure 13 shows a schematic of the equivalent CMOS/TTL-compatible digital inputs of the DAC5670, valid for the following pins: RESTART, LVDS\_HTB, INV\_CLK, SLEEP, NORMAL, A\_ONLY, A\_ONLY\_INV, and A\_ONLY\_ZS.

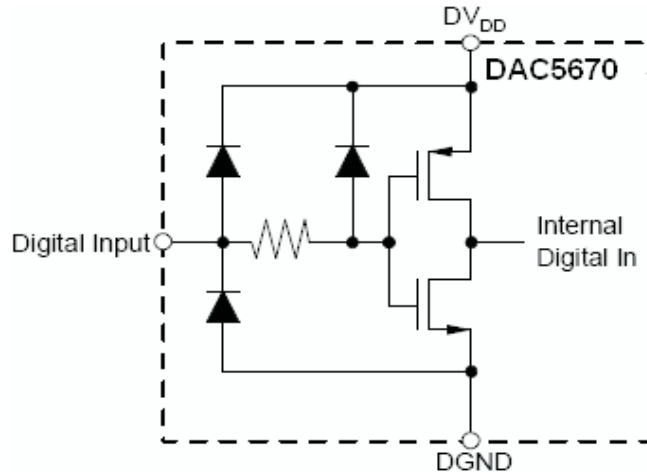


Figure 13.

The DAC5670 is clocked at the DAC sample rate. Each input port runs at a maximum of 1.2 GSPS. The DAC5670 provides an output clock at one-half the input port data rate (DACCLK/4), monitors an additional reference bit input sequence, and adjusts the output clock delay to optimize the data latch relative to the reference bit with a DLL. The DLL delay automatically adjusts for drift over temperature and time.

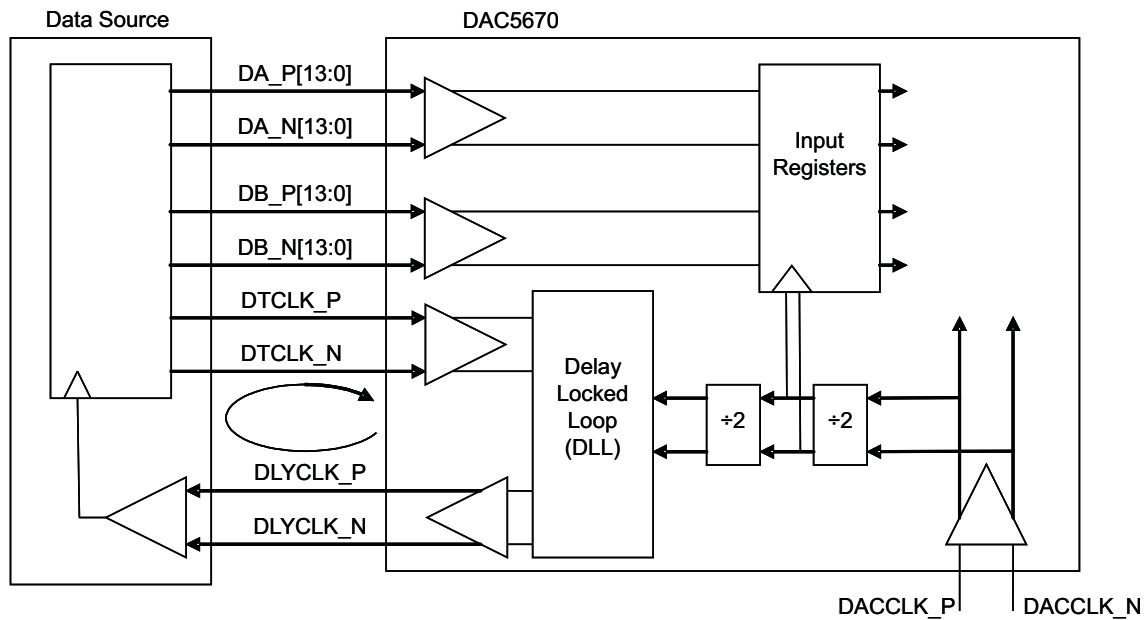


Figure 14. DLL Input Loop Simplified Block Diagram

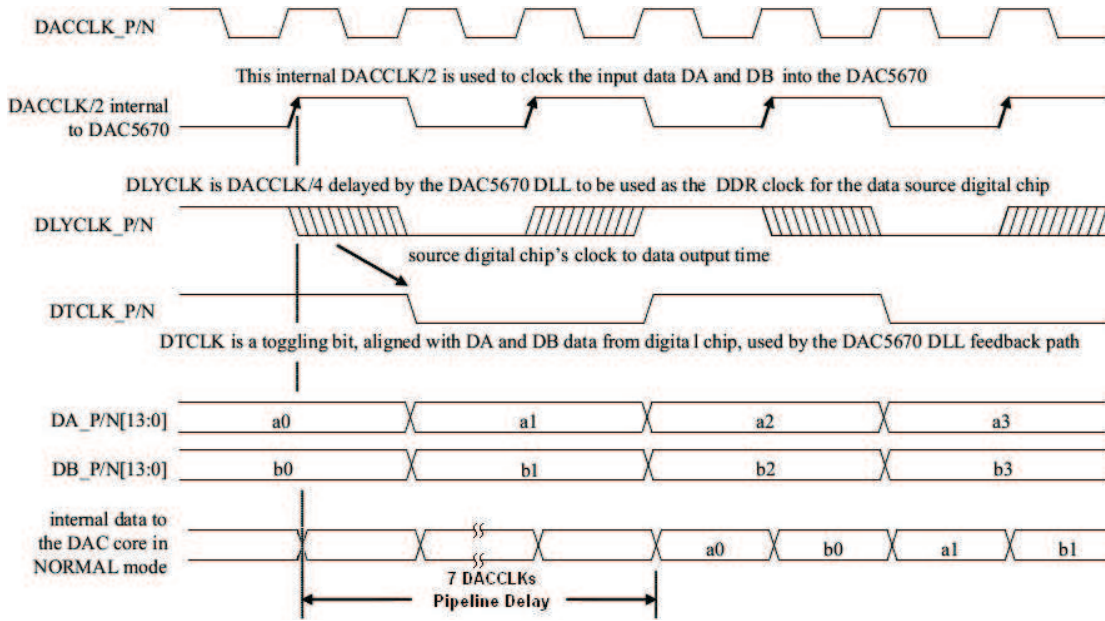


Figure 15. DLL Input Loop Functional Timing

**Input Format**

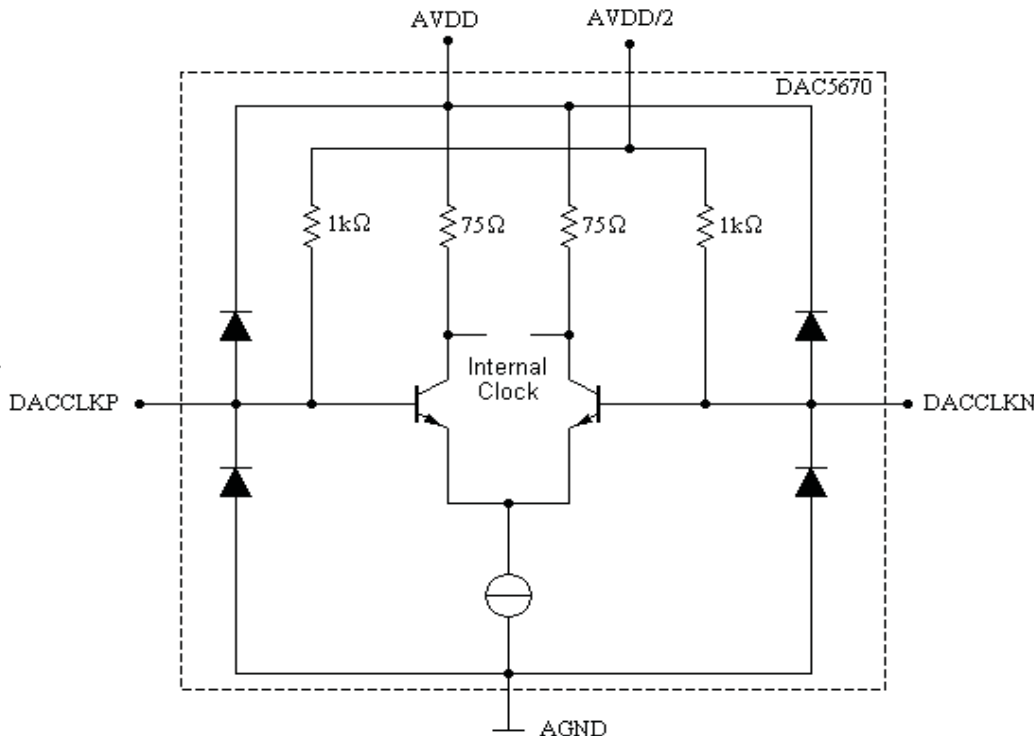
The DAC5670 has four input modes selected by the four mutually exclusive configuration pins: NORMAL, A\_ONLY, A\_ONLY\_INV, and A\_ONLY\_ZS. Table 4 lists the input modes, the input sample rates, the maximum DAC sample rate (CLK input) and resulting DAC output sequence for each configuration. For all configurations, the DLYCLK\_P/N outputs and DTCLK\_P/N inputs are DACCLK\_P/N frequency divided by four.

Table 4. DAC5670 Input Formats

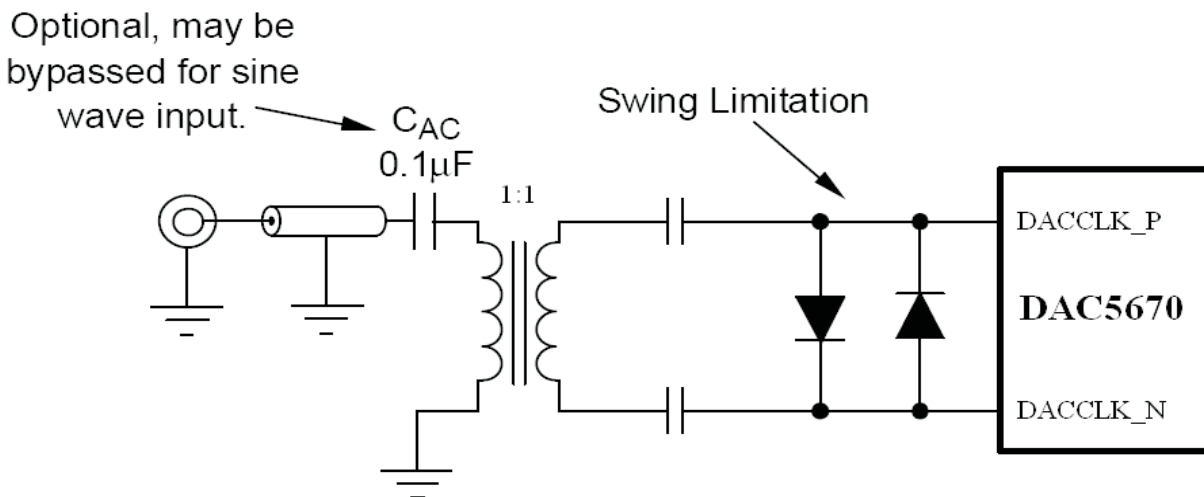
NORMAL	A_ONLY	A_ONLY_INV	A_ONLY_ZS	FinA/Fdac	FinB/Fdac	f <sub>DAC</sub> MAX (MHz)	DLYCLK_P/N AND DTCLK_P/N FREQ (MHz)	DAC OUTPUT SEQUENCE
1	0	0	0	1/2	1/2	2400	F <sub>dac</sub> /4	A0, B0, A1, B1, A2, B2, . . .
0	1	0	0	1/2	Off	2400	F <sub>dac</sub> /4	A0, A0, A1, A1, A2, A2, . . .
0	0	1	0	1/2	Off	2400	F <sub>dac</sub> /4	A0, -A0, A1, -A1, A2, -A2, . . .
0	0	0	1	1/2	Off	2400	F <sub>dac</sub> /4	A0, 0, A1, 0, A2, 0, . . .

**Clock Input**

The DAC5670 features differential, LVPECL compatible clock inputs (DACCLK\_P, DACCLK\_N). Figure 16 shows the equivalent schematic of the clock input buffer. The internal biasing resistors set the input common-mode voltage to AVDD/2, while the input resistance is typically 1 kΩ. A variety of clock sources can be ac-coupled to the device, including a sine wave source (see Figure 17).



**Figure 16. Clock Equivalent Input**



**Figure 17. Driving the DAC5670 with a Single-Ended Clock Source Using a Transformer**

To obtain best ac performance the DAC5670 clock input should be driven with a differential LVPECL or sine wave source as shown in Figure 18 and Figure 19. Here, the potential of VTT should be set to the termination voltage required by the driver along with the proper termination resistors (RT). The DAC5670 clock input can also be driven single-ended for slower clock rates using TTL/CMOS levels; this is shown in Figure 20.

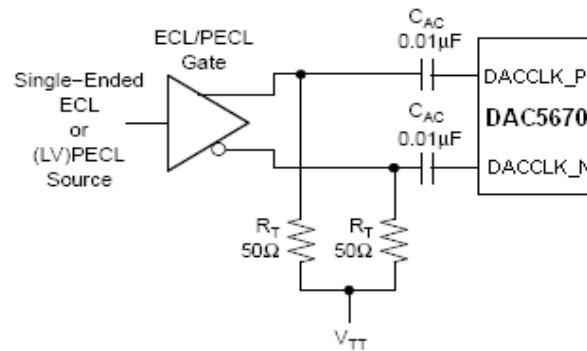


Figure 18. Driving the DAC5670 with a Single-Ended ECL/PECL Clock Source

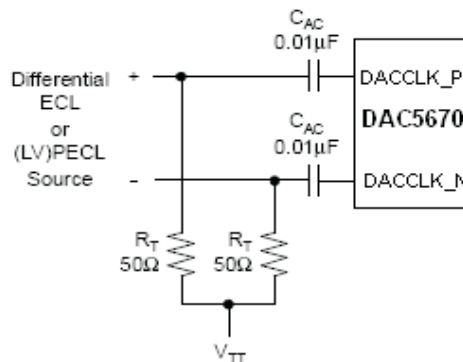


Figure 19. Driving the DAC5670 with a Differential ECL/PECL Clock Source

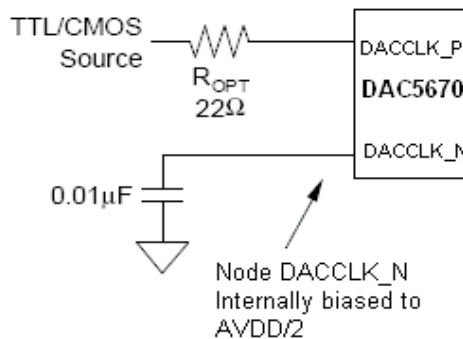


Figure 20. Driving the DAC5670 with a Single-Ended TTL/CMOS Clock Source

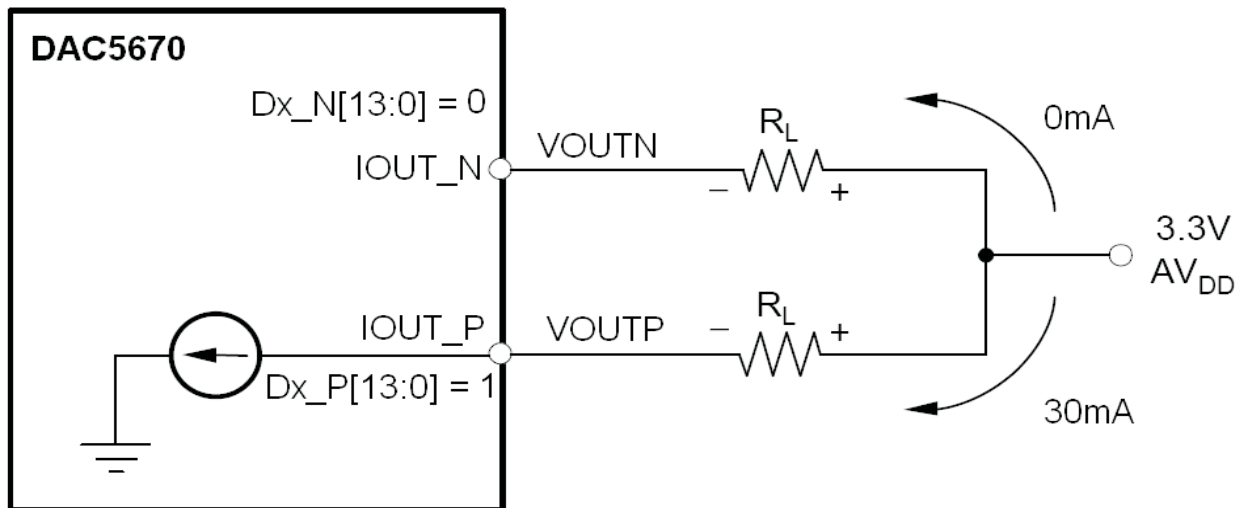
## DAC Transfer Function

The DAC5670 has a current sink output. The current flow through IOUT\_P and IOUT\_N is controlled by Dx\_P[13:0] and Dx\_N[13:0]. For ease of use, we denote D[13:0] as the logical bit equivalent of Dx\_P[13:0] and its complement Dx\_N[13:0]. The DAC5670 supports straight binary coding with D13 being the MSB and D0 the LSB. Full-scale current flows through IOUT\_P when all D[13:0] inputs are set high and through IOUT\_N when all D[13:0] inputs are set low. The relationship between IOUT\_P and IOUT\_N can be expressed as [Equation 1](#):

$$IOUT\_N = IO_{(FS)} - IOUT\_P \quad (1)$$

$IO_{(FS)}$  is the full-scale output current sink (5 mA to 30 mA). Since the output stage is a current sink, the current can only flow from AVDD through the load resistors  $R_L$  into the IOUT\_N and IOUT\_P pins.

The output current flow in each pin driving a resistive load can be expressed as shown in [Figure 21](#), as well as in [Equation 2](#) and [Equation 3](#).



**Figure 21. Relationship between D[13:0], IOUT\_N and IOUT\_P**

$$IOUT\_N = (IOUT_{(FS)} \times (16384 - CODE)) / 16384 \quad (2)$$

$$IOUT\_P = (IOUT_{(FS)} \times CODE) / 16384 \quad (3)$$

where CODE is the decimal representation of the DAC input word. This would translate into single-ended voltages at IOUT\_N and IOUT\_P, as shown in [Equation 4](#) and [Equation 5](#):

$$VOUTN = AVDD - IOUT\_N \times R_L \quad (4)$$

$$VOUTP = AVDD - IOUT\_P \times R_L \quad (5)$$

For example, assuming that D[13:0] = 1 and that  $R_L$  is 50  $\Omega$ , the differential voltage between pins IOUT\_N and IOUT\_P can be expressed as shown in [Equation 6](#) through [Equation 8](#) where  $IO_{(FS)} = 20$  mA:

$$VOUTN = 3.3 \text{ V} - 0 \text{ mA} \times 50 \ \Omega = 3.3 \text{ V} \quad (6)$$

$$VOUTP = 3.3 \text{ V} - 20 \text{ mA} \times 50 \ \Omega = 2.3 \text{ V} \quad (7)$$

$$VDIFF = VOUTN - VOUTP = 1 \text{ V} \quad (8)$$

If D[13:0] = 0, then IOUT\_P = 0 mA and IOUT\_N = 20 mA and the differential voltage VDIFF = -1 V.

The output currents and voltages in IOUT\_N and IOUT\_P are complementary. The voltage, when measured differentially, will be doubled compared to measuring each output individually. Care must be taken not to exceed the compliance voltages at the IOUT\_N and IOUT\_P pins in order to keep signal distortion low.

Reference Operation

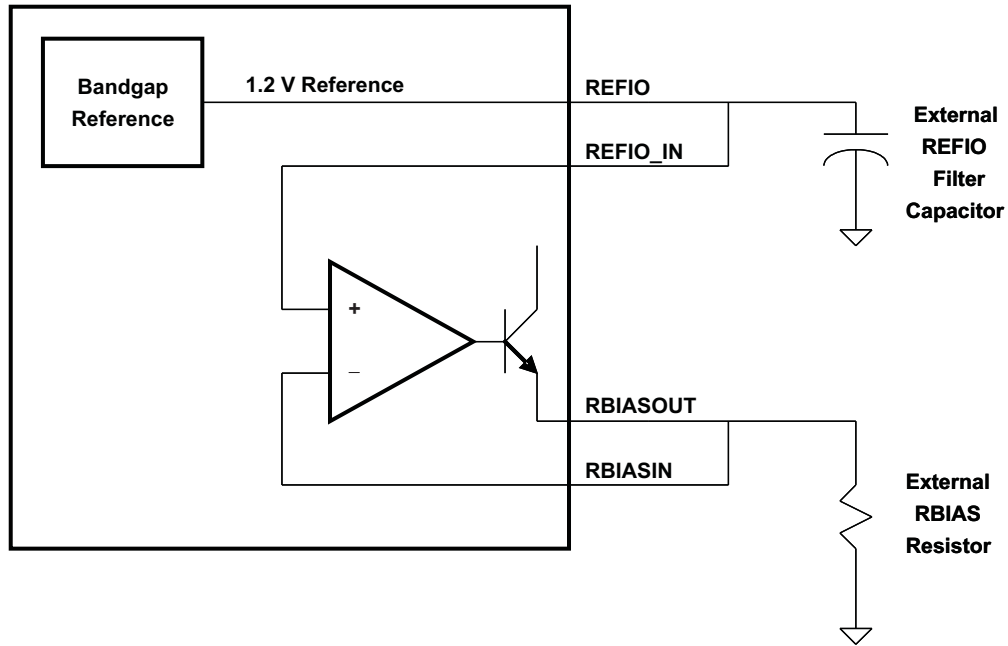


Figure 22. Reference Circuit

The DAC5670 comprises a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor  $R_{BIAS}$  to pins RBIASOUT and RBIASIN. The bias current  $I_{BIAS}$  through resistor  $R_{BIAS}$  is defined by the on-chip bandgap reference voltage and control amplifier. The full-scale output current equals 32 times this bias current. The full-scale output current  $I_{OUT_{FS}}$  can thus be expressed as:

$$I_{OUT_{FS}} = 32 \times I_{BIAS} = 32 \times V_{REFIO}/R_{BIAS} \tag{9}$$

Where:

$V_{REFIO}$  Voltage at terminals REFIO and REFIO\_IN

The bandgap reference voltage delivers an accurate voltage of 1.2 V. An external REFIO filter capacitor of 0.1  $\mu$ F should be connected externally to the terminals REFIO and REFIO\_IN for compensation.

The full-scale output current can be adjusted from 30 mA down to 5 mA by varying external resistor  $R_{BIAS}$ .



### Analog Current Outputs

Figure 23 is a simplified schematic of the current sink array output with corresponding switches. Differential NPN switches direct the current of each individual NPN current sink to either the positive output node IOOUT\_P or its complementary negative output node IOOUT\_N. The input data presented at the DA\_P[13:0], DA\_N[13:0], DB\_P[13:0] and DB\_N[13:0] is decoded to control the sw\_p(N) and sw\_n(N) current switches.

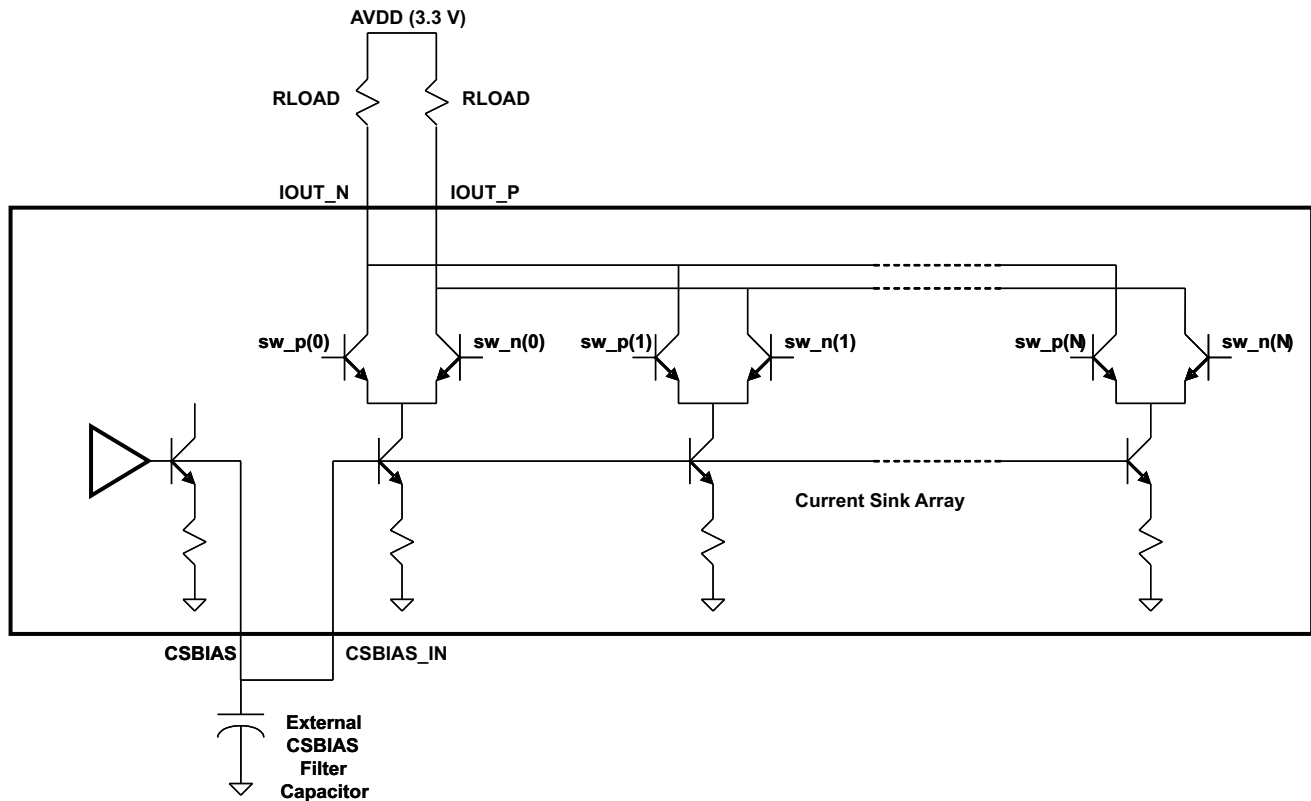


Figure 23. Current Sink Array

The external output resistors  $R_{LOAD}$  are connected to the positive supply, AVDD.

The DAC5670 can easily be configured to drive a doubly-terminated 50  $\Omega$  cable using a properly selected transformer. Figure 24 and Figure 25 show the 1:1 and 4:1 impedance ratio configuration, respectively. These configurations provide maximum rejection of common-mode noise sources and even-order distortion components, thereby doubling the power of the DAC to the output. The center tap on the primary side of the transformer is terminated to AVDD, enabling a dc current flow for both IOOUT\_N and IOOUT\_P.

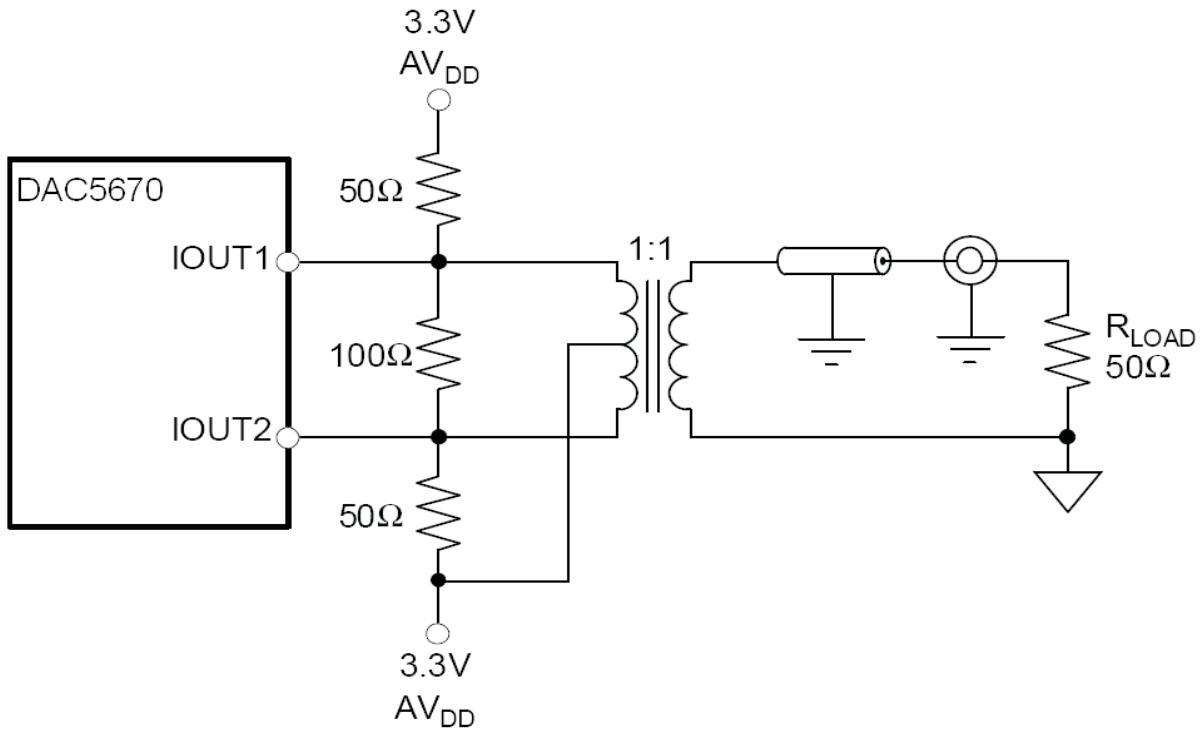


Figure 24.

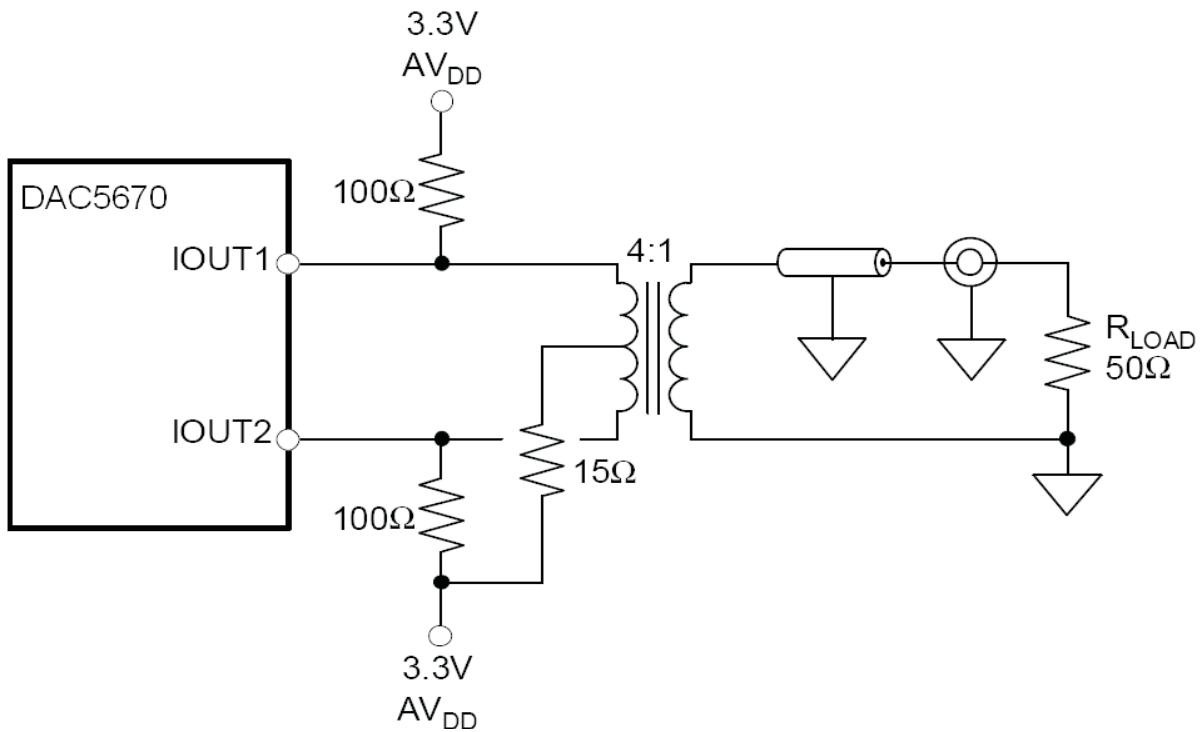


Figure 25.

**Sleep Mode**

When the SLEEP pin is asserted (high), the DAC5670 enters a lower-power mode.

## Definitions of Specifications and Terminology

**Differential Nonlinearity (DNL):** Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

**Gain Drift:** Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at 25°C to values over the full operating temperature range.

**Gain Error:** Defined as the percentage error in the ratio between the measured full-scale output current and the value of the ideal full-scale output ( $32 \times V_{\text{REFIO}}/R_{\text{BIAS}}$ ). A  $V_{\text{REFIO}}$  of 1.2V is used to measure the gain error with an external reference voltage applied. With an internal reference, this error includes the deviation of  $V_{\text{REFIO}}$  (internal bandgap reference voltage) from the typical value of 1.2V.

**Integral Nonlinearity (INL):** Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

**Intermodulation Distortion (IMD3, IMD):** The two-tone IMD3 or four-tone IMD is defined as the ratio (in dBc) of the worst 3rd-order (or higher) intermodulation distortion product to either fundamental output tone.

**Offset Drift:** Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at 25°C to values over the full operating temperature range.

**Offset Error:** Defined as the percentage error in the ratio of the differential output current ( $I_{\text{OUT}_P} - I_{\text{OUT}_N}$ ) to half of the full-scale output current for input code 8192.

**Output Compliance Range:** Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result in reduced reliability of the device or adversely affecting distortion performance.

**Power Supply Rejection Ratio (PSSR):** Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

**Reference Voltage Drift:** Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

**Spurious Free Dynamic Range (SFDR):** Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

**Signal to Noise Ratio (SNR):** Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

**Total Harmonic Distortion (THD):** Defined as the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental output signal.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
5962-0724701VXA	ACTIVE	CBGA	GEM	192	84	TBD	Call TI	Call TI	

<sup>(1)</sup> The marketing status values are defined as follows:

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**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

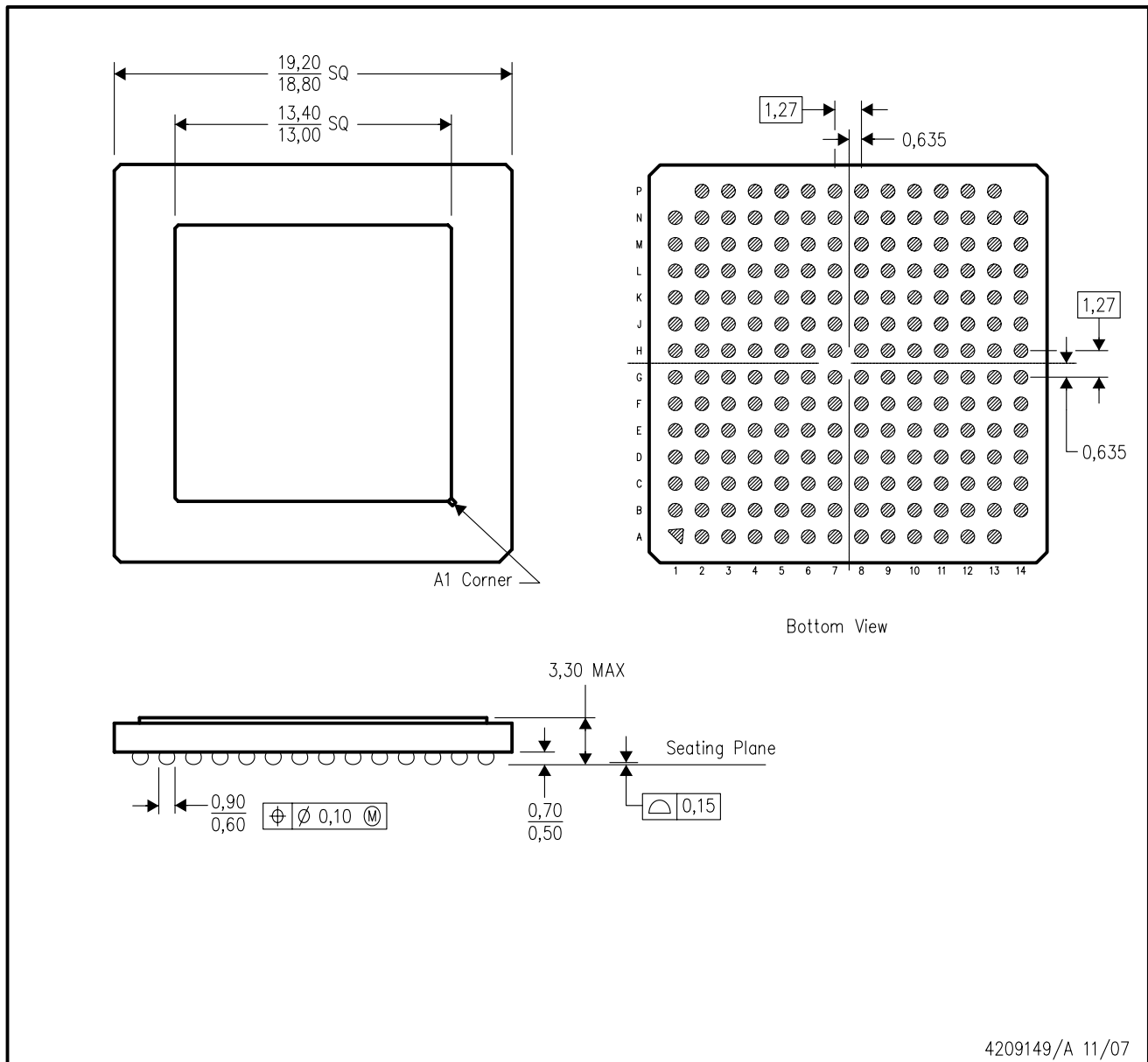
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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GEM (S-CBGA-N192)

CERAMIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Metal Lid Hermetic Package.
  - D. Falls within JEDEC MO-156

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OMAP Mobile Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
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Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
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Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
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