LM48821

LM48821 Direct Coupled, Ultra Low Noise, 52mW Differential Input Stereo HeadphoneAmplifier with I2C Volume Control

TEXAS INSTRUMENTS

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National Semiconductor

LM48821 Boomer® Audio Power Amplifier Series
Direct Coupled, Ultra Low Noise, 52mW Differential Input Stereo Headphone Amplifier with I2C Volume Control

General Description

With its directly-coupled output technology, the LM48821 is a variable gain audio power amplifier capable of delivering $52mW_{RMS}$ per channel into a 16Ω single-ended load with less than 1% THD+N from a 3V power supply. The I^2C volume control has a range of –76dB to 18dB.

The LM48821's Tru-GND technology utilizes advanced charge pump technology to generate the LM48821's negative supply voltage. This eliminates the need for output-coupling capacitors typically used with single-ended loads.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. The LM48821 does not require output coupling capacitors or bootstrap capacitors, and therefore is ideally suited for mobile phone and other low voltage applications where minimal power consumption is a primary requirement.

The LM48821 incorporates selectable low-power consumption shutdown and channel select modes.

The LM48821 contains advanced output transient suppression circuitry that eliminates noises which would otherwise occur during turn-on and turn-off transitions.

Key Specifications

■ Improved PSRR at 217Hz	82dB (typ)
■ Stereo Output Power at V_{DD} = 3V, R_L = 16Ω, THD+N = 1%	52mW (typ)
■ Mono Output Power at V_{DD} = 3V, R_L = 16Ω, THD+N = 1%	93mW (typ)
■ Shutdown current	0.1µA (typ)

Features

- Ground referenced outputs
- Differential Inputs
- I^2C Volume and mode controls
- Available in space-saving micro SMD package
- Ultra low current shutdown mode
- Advanced output transient suppression circuitry eliminates noises during turn-on and turn-off transitions
- 2.0V to 4.0V operation (PV_{DD} and SV_{DD})
- 1.8 to 4.0V operation (I^2CV_{DD})
- No output coupling capacitors, snubber networks, bootstrap capacitors, or gain-setting resistors required

Applications

- Notebook PCs
- Desktop PCs
- Mobile Phones
- PDAs
- Portable Electronic Devices
- MP3 Players

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Tru-GND is a trademark of National Semiconductor Corporation.

Typical Application

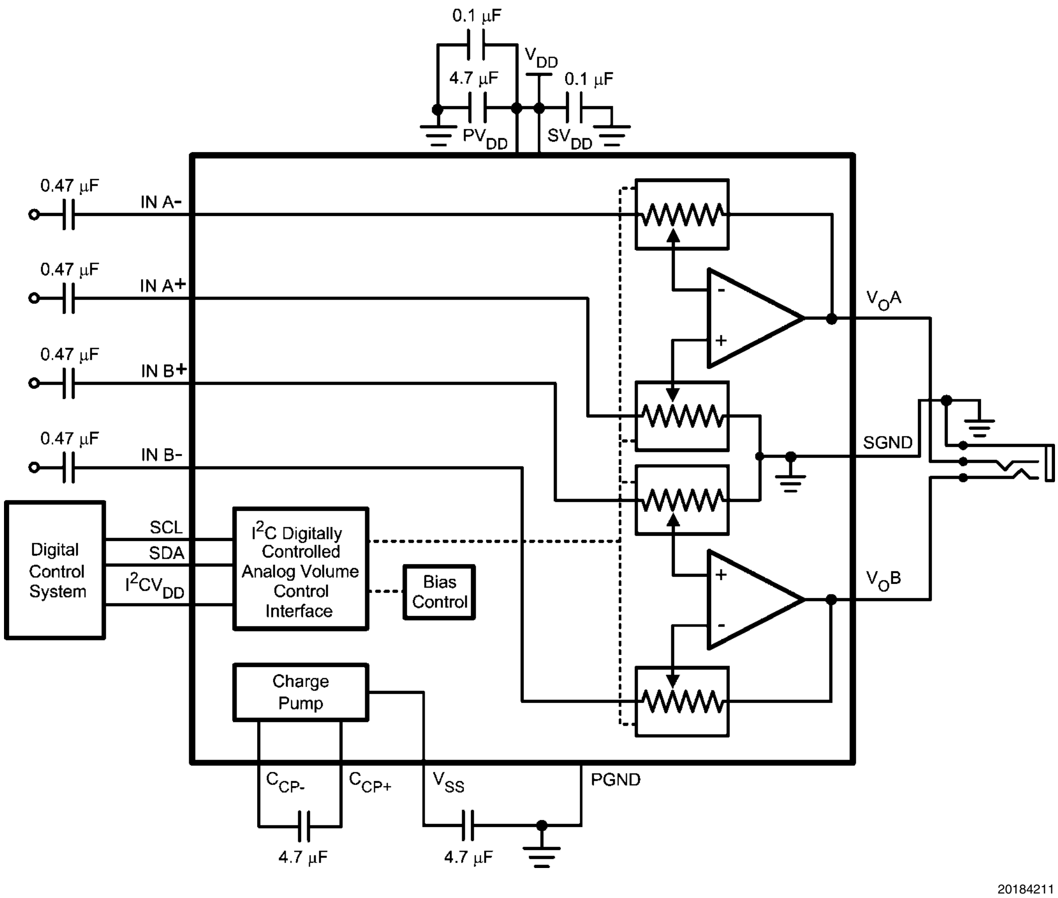
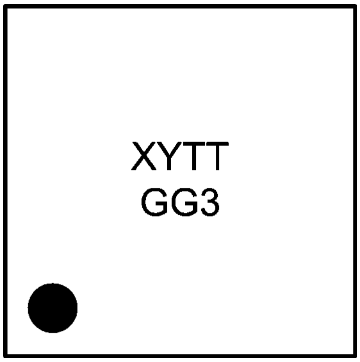


FIGURE 1. Typical Audio Amplifier Application Circuit

Connection Diagrams

micro SMD Package



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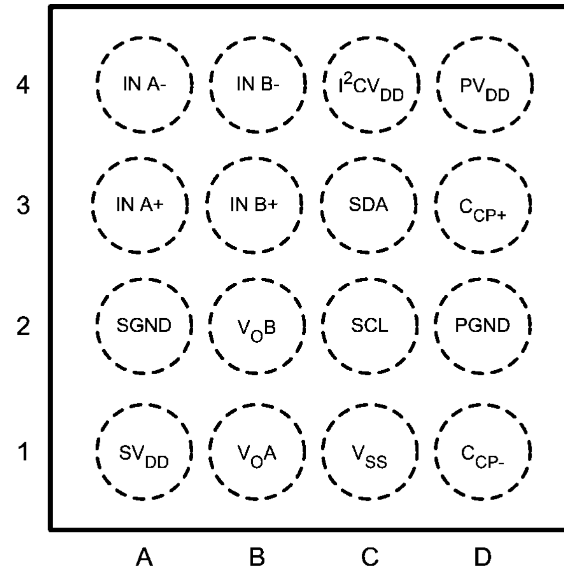
Top View
Order Number TLA1611A
See NS Package Number TLA1611A

micro SMD Marking



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Top View
XY - Date Code
TT - Lot Traceability
GG3 – LM48821

Pin Descriptions

Pin Designator	Pin Name	Pin Function
A1	SV_{DD}	Signal power supply input
A2	SGND	Signal ground
A3	IN A+	Left non-inverting input
A4	IN A-	Left inverting input
B1	V_OA	Left output
B2	V_OB	Right output
B3	IN B+	Right non-inverting input
B4	IN B-	Right inverting input
C1	V_{SS}	DC to DC converter output
C2	SCL	I^2C serial clock input
C3	SDA	I^2C serial data input
C4	I^2CV_{DD}	I^2C supply voltage input
D1	C_{CP-}	DC to DC converter flying capacitor inverting input
D2	PGND	Power ground
D3	C_{CP+}	DC to DC converter flying capacitor non-inverting input
D4	PV_{DD}	DC to DC converter power supply input

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	4.5V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (Note 3)	Internally Limited
ESD Susceptibility (Note 4)	2000V
ESD Susceptibility (Note 5)	200V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (typ) - (TLA1611A) (Note 3)	105°C/W

Operating Ratings

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	
PV_{DD} and SV_{DD}	$2.0V \le V_{DD} \le 4.0V$
I^2CV_{DD}	$1.8V \le I^2CV_{DD} \le 4.0V$

Audio Amplifier Electrical Characteristics V_{DD} = 3V (Notes 1, 2)

The following specifications apply for V_{DD} = 3V, R_L = 16Ω, A_V = 0dB, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48821		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, inputs terminated, both channels enabled	3.0	4.5	mA (max)
		V_{IN} = 0V, inputs terminated, one channel enabled	2.0	3.0	mA
I_{SD}	Shutdown Current	Right and Left Enable bits set to 0	0.1	1.2	μA (max)
V_{OS}	Output Offset Voltage	R_L = 32Ω	0.5	2.5	mV (max)
A_V	Volume Control Range	[B0:B4] = 00000	–76		dB
		[B0:B4] = 11111	+18		dB
ΔA_V	Channel-to-Channel Gain Match		±0.015		dB
A_{V-MUTE}	Mute Gain		–76		dB
R_{IN}	Input Resistance	Gain = 18dB	9	5 15	kΩ (min) kΩ (max)
		Gain = –76dB	81		kΩ
P_{OUT}	Output Power	THD+N = 1% (max); f_{IN} = 1kHz, R_L = 16Ω, per channel	52	43	mW (min)
		THD+N = 1% (max); f_{IN} = 1kHz, R_L = 32Ω, per channel	53	45	mW (min)
		THD+N = 1% (max); f_{IN} = 1kHz, R_L = 16Ω, single channel driven	93	80	mW (min)
		THD+N = 1% (max); f_{IN} = 1kHz, R_L = 32Ω, single channel driven	79		mW
THD+N	Total Harmonic Distortion + Noise	P_{OUT} = 50mW, f = 1kHz R_L = 16Ω, single channel	0.022		%
		P_{OUT} = 50mW, f = 1kHz R_L = 32Ω, single channel	0.011		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV$_{P-P}$, input referred			
		f = 217Hz f = 1kHz f = 20kHz	82 80 55	65	dB (min) dB dB
CMRR	Common Mode Rejection Ratio	V_{RIPPLE} = 200mV$_{p-p}$, Input referred f = 2kHz	65		dB
SNR	Signal-to-Noise-Ratio	R_L = 32Ω, P_{OUT} = 20mW, f = 1kHz, BW = 20Hz to 22kHz	100		dB
T_{WU}	Charge Pump Wake-Up Time		400		μs

Symbol	Parameter	Conditions	LM48821		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
X_{TALK}	Crosstalk	$R_L = 16\Omega$, $P_{OUT} = 1.6mW$, f = 1kHz, A-weighted filter	82		dB
Z_{OUT}	Output Impedance	Right and Left Enable bits set to 0	41		kΩ

Control Interface Electrical Characteristics (Notes 1, 2)

The following specifications apply for 1.8V ≤ I^2CV_{DD} ≤ 4.0V, unless otherwise specified. Limits apply for T_A = 25°C. See Figure 2.

Symbol	Parameter	Conditions	LM48821		Units (Limits)
			Typical (Note 6)	Limits (Notes 7, 8)	
t_1	SCL period			2.5	µs (min)
t_2	SDA Setup Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}	Logic High Input Threshold			0.7 x I^2CV_{DD}	V (min)
V_{IL}	Logic Low Input Threshold			0.3 x I^2CV_{DD}	V (max)

Note 1: All voltages are measured with respect to the GND pin unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower. For the LM48821, see power derating currents for more information.

Note 4: Human body model, 100pF discharged through a 1.5kΩ resistor.

Note 5: Machine Model, 220pF - 240pF discharged through all pins.

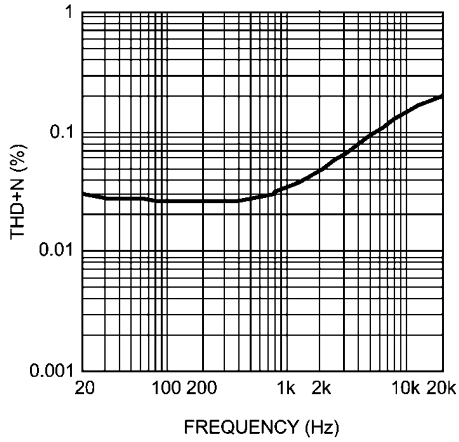
Note 6: Typicals are measured at +25°C and represent the parametric norm.

Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

Typical Performance Characteristics

THD+N vs Frequency
V_{DD} = 2V, P_O = 6mW,
R_L = 16Ω, Stereo



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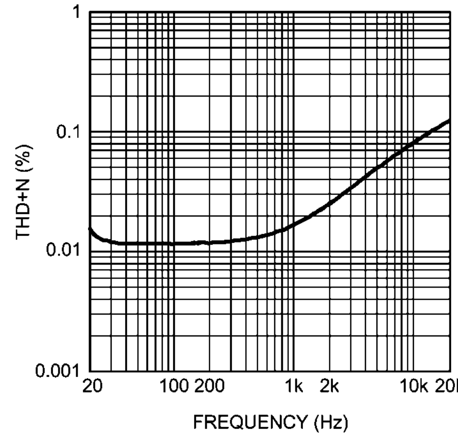
THD+N vs Frequency
V_{DD} = 2V, P_O = 10mW,
R_L = 32Ω, Stereo



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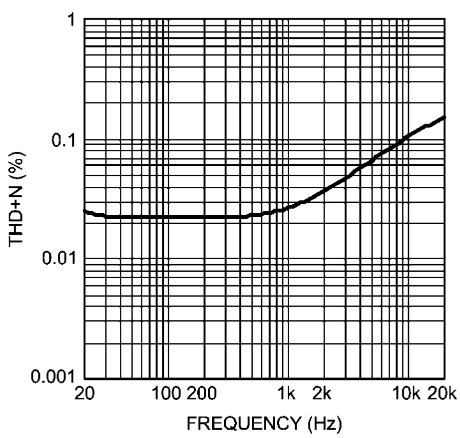
THD+N vs Frequency
V_{DD} = 2V, P_O = 16mW,
R_L = 16Ω, Mono Left



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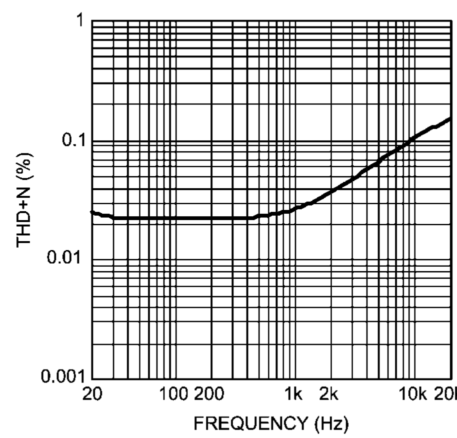
THD+N vs Frequency
V_{DD} = 2V, P_O = 16mW,
R_L = 16Ω, Mono Right



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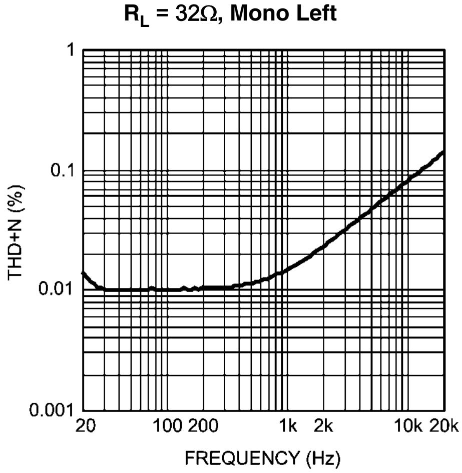
THD+N vs Frequency
V_{DD} = 2V, P_O = 18mW,
R_L = 32Ω, Mono Left



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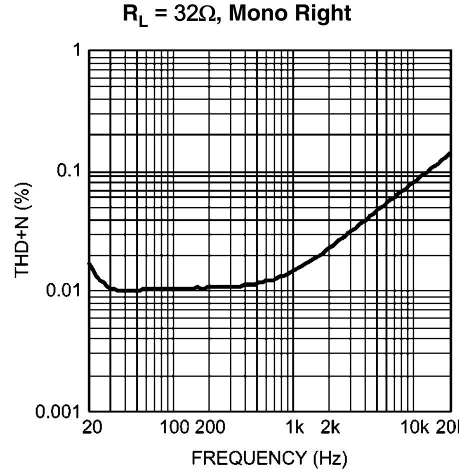
THD+N vs Frequency
V_{DD} = 2V, P_O = 18mW,
R_L = 32Ω, Mono Right



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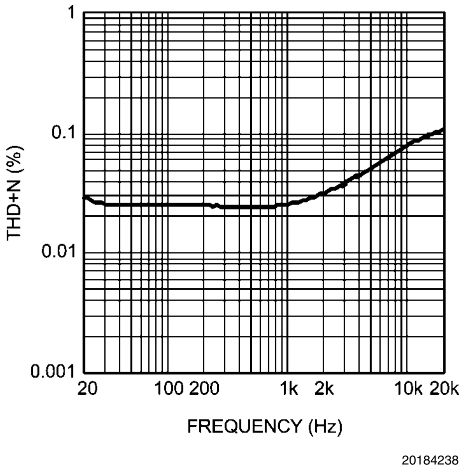
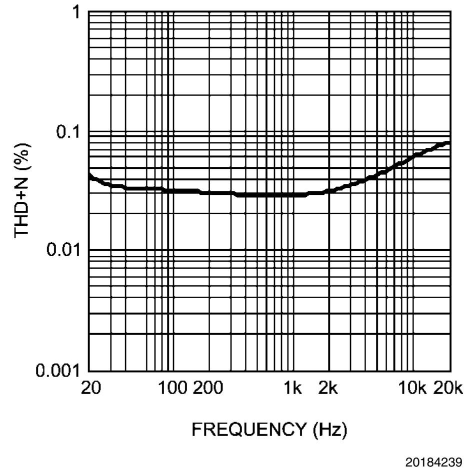
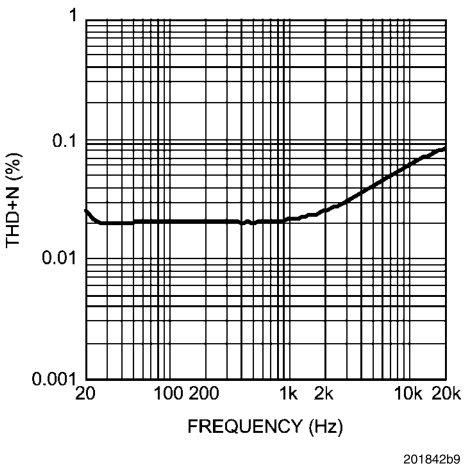
THD+N vs Frequency
V_{DD} = 3V, P_O = 35mW,
R_L = 16Ω, Stereo



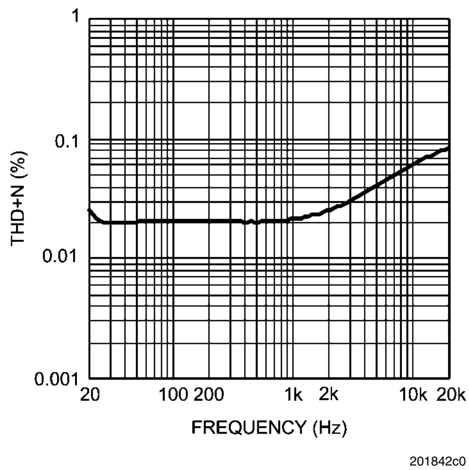
THD+N vs Frequency
V_{DD} = 4V, P_O = 50mW,
R_L = 16Ω, Stereo



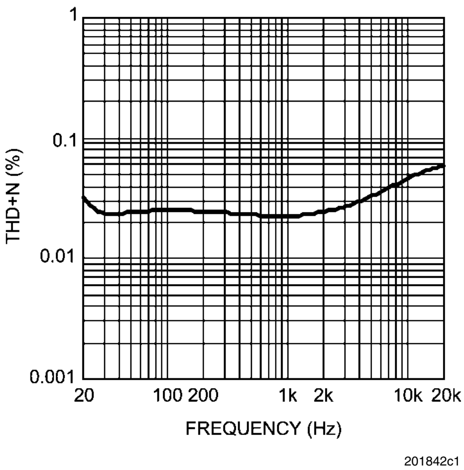
THD+N vs Frequency
V_{DD} = 3V, P_O = 70mW,
R_L = 16Ω, Mono Left



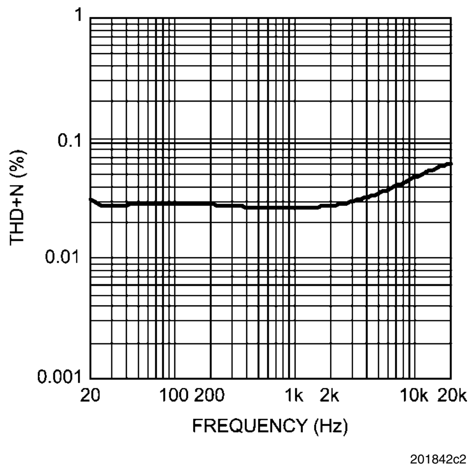
THD+N vs Frequency
V_{DD} = 3V, P_O = 70mW,
R_L = 16Ω, Mono Right



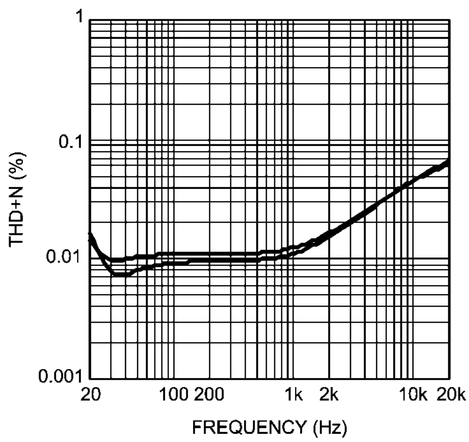
THD+N vs Frequency
V_{DD} = 4V, P_O = 160mW,
R_L = 16Ω, Mono Left



THD+N vs Frequency
V_{DD} = 4V, P_O = 160mW,
R_L = 16Ω, Mono Right



THD+N vs Frequency
V_{DD} = 3V, P_O = 40mW,
R_L = 32Ω, Stereo



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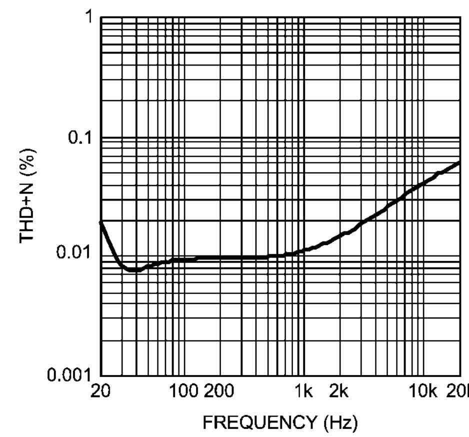
THD+N vs Frequency
V_{DD} = 3V, P_O = 60mW,
R_L = 32Ω, Mono Left



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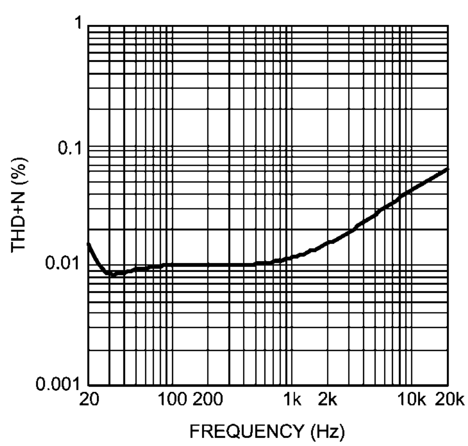
THD+N vs Frequency
V_{DD} = 3V, P_O = 60mW,
R_L = 32Ω, Mono Right



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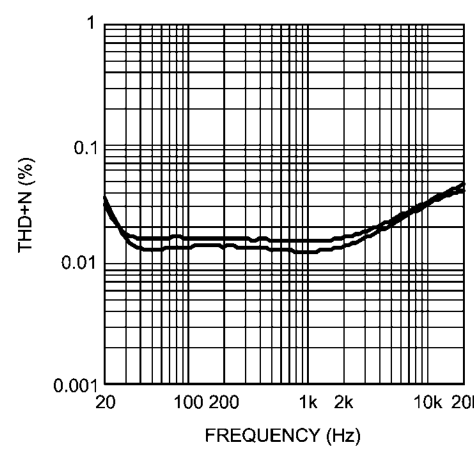
THD+N vs Frequency
V_{DD} = 4V, P_O = 90mW,
R_L = 32Ω, Stereo



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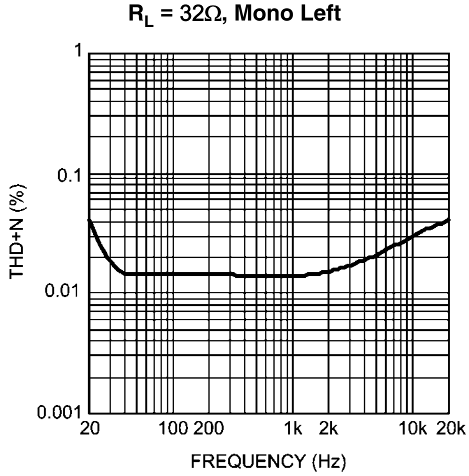
THD+N vs Frequency
V_{DD} = 4V, P_O = 120mW,
R_L = 32Ω, Mono Left



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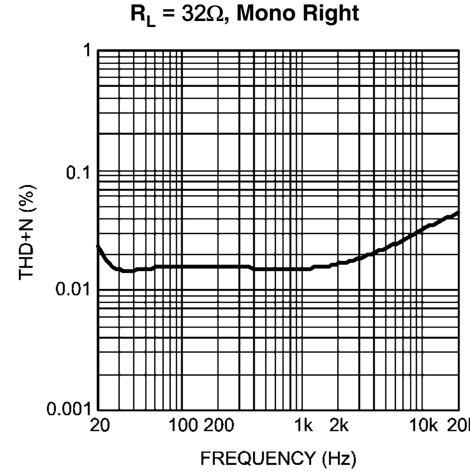
THD+N vs Frequency
V_{DD} = 4V, P_O = 120mW,
R_L = 32Ω, Mono Right



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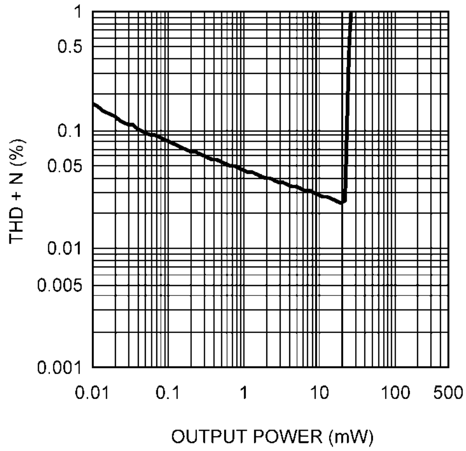
THD+N vs Output Power
V_{DD} = 2V, R_L = 16Ω,
f = 1kHz, Mono Left



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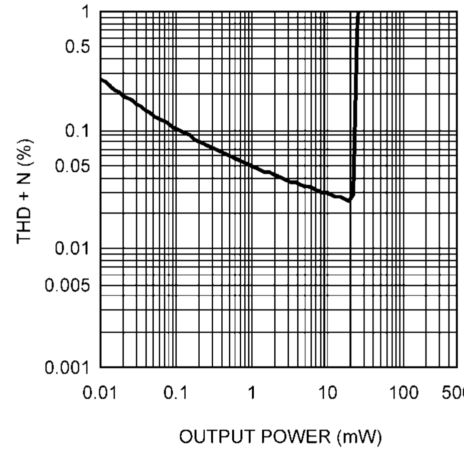
THD+N vs Output Power
V_{DD} = 2V, R_L = 16Ω,
f = 1kHz, Mono Right



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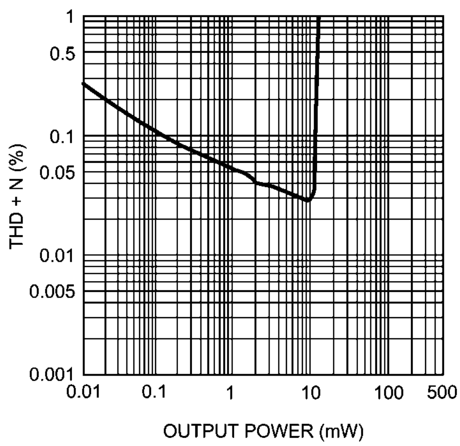
THD+N vs Output Power
V_{DD} = 2V, R_L = 16Ω,
f = 1kHz, Stereo



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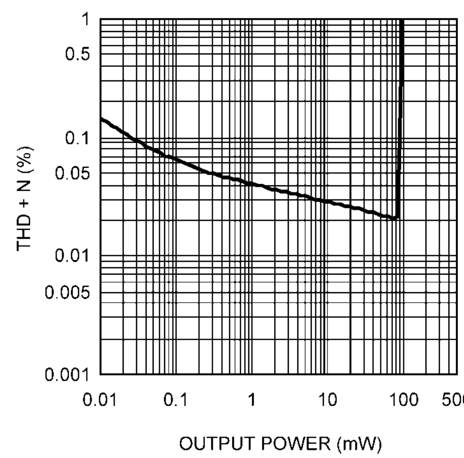
THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω,
f = 1kHz, Mono Left



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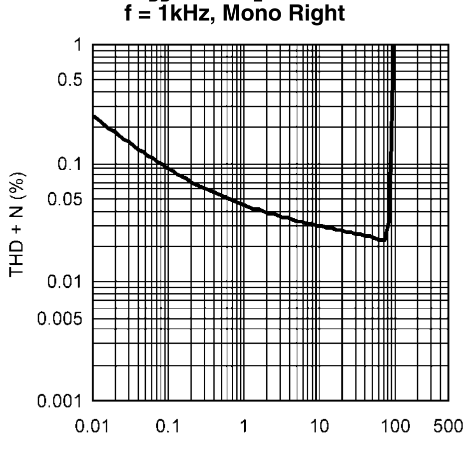
THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω,
f = 1kHz, Mono Right



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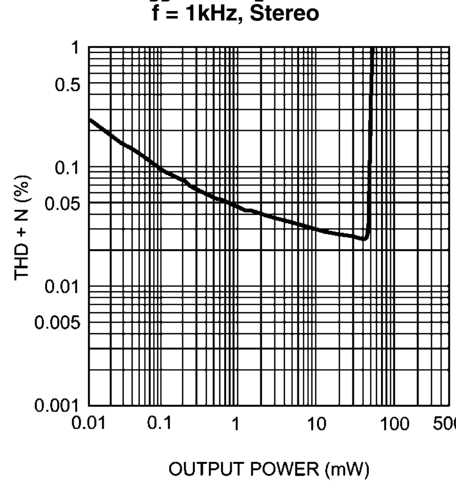
THD+N vs Output Power
V_{DD} = 3V, R_L = 16Ω,
f = 1kHz, Stereo



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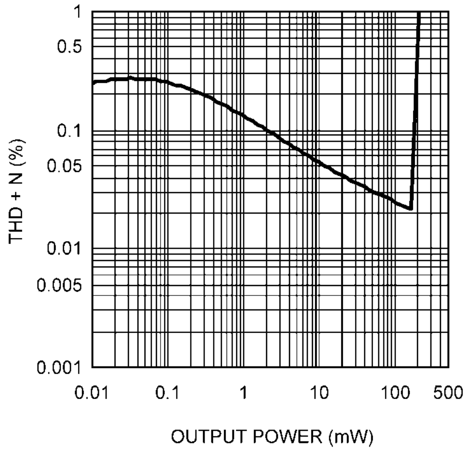
THD+N vs Output Power
V_{DD} = 4V, R_L = 16Ω,
f = 1kHz, Mono Left



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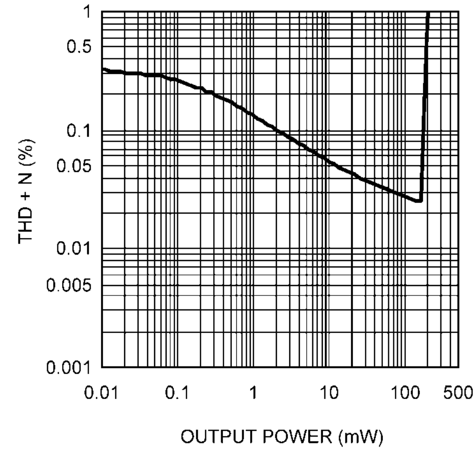
THD+N vs Output Power
V_{DD} = 4V, R_L = 16Ω,
f = 1kHz, Mono Right



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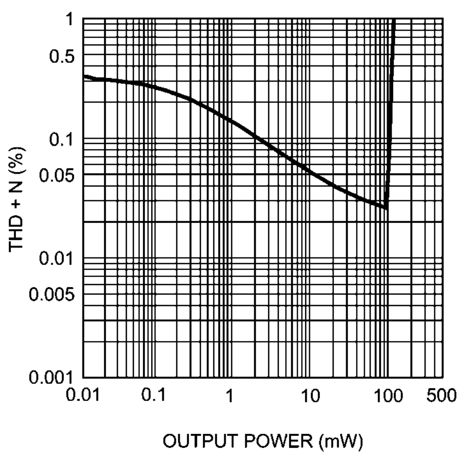
THD+N vs Output Power
V_{DD} = 4V, R_L = 16Ω,
f = 1kHz, Stereo



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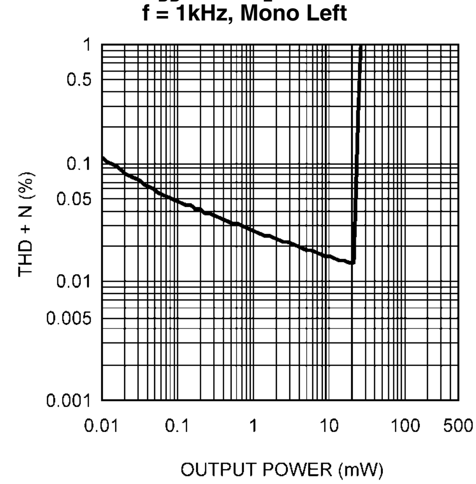
THD+N vs Output Power
V_{DD} = 2V, R_L = 32Ω,
f = 1kHz, Mono Left



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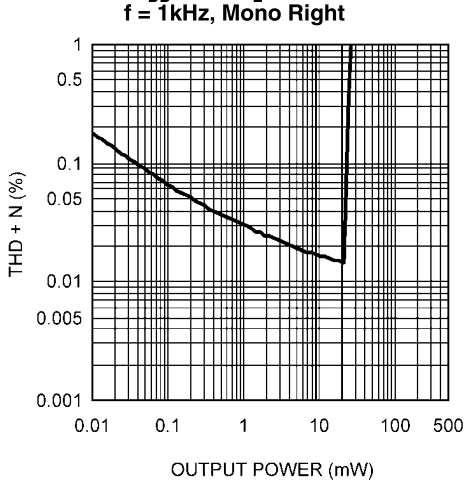
THD+N vs Output Power
V_{DD} = 2V, R_L = 32Ω,
f = 1kHz, Mono Right



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THD+N vs Output Power
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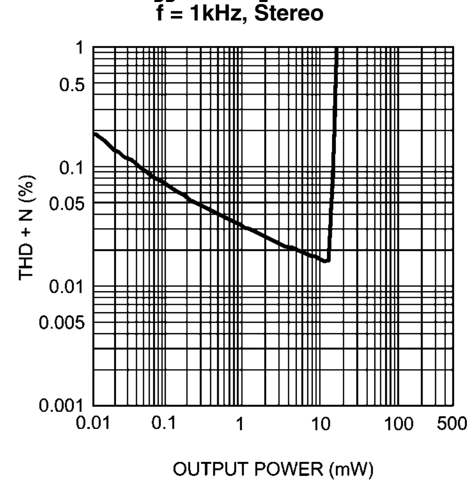
f = 1kHz, Stereo



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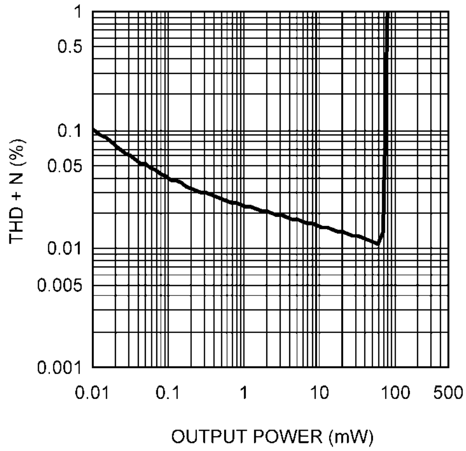
THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω,
f = 1kHz, Mono Left



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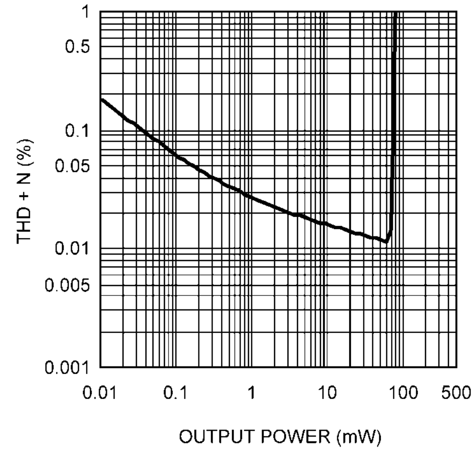
THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω,
f = 1kHz, Mono Right



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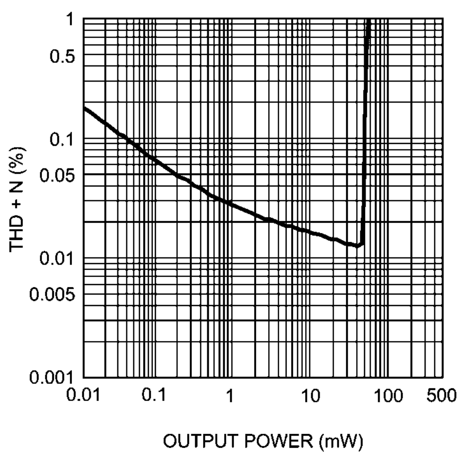
THD+N vs Output Power
V_{DD} = 3V, R_L = 32Ω,
f = 1kHz, Stereo



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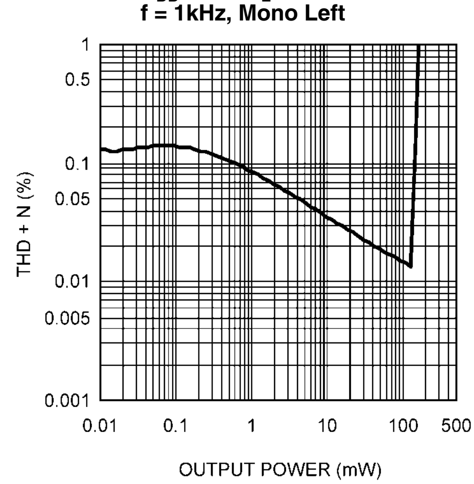
THD+N vs Output Power
V_{DD} = 4V, R_L = 32Ω,
f = 1kHz, Mono Left



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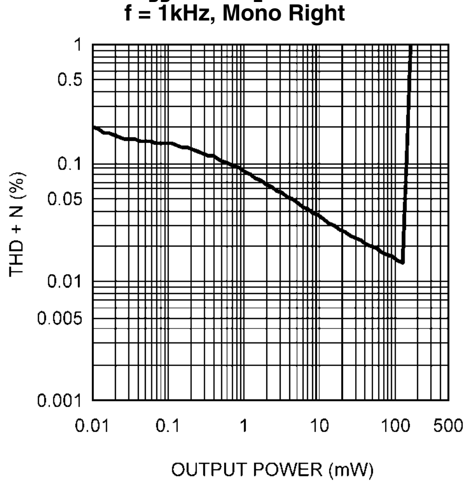
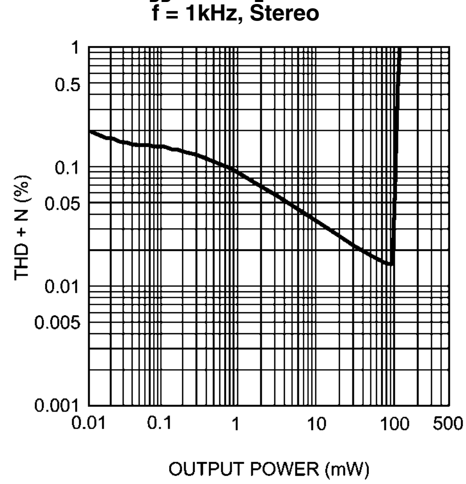
THD+N vs Output Power
V_{DD} = 4V, R_L = 32Ω,
f = 1kHz, Mono Right



20184255

THD+N vs Output Power
V_{DD} = 4V, R_L = 32Ω,
f = 1kHz, Stereo



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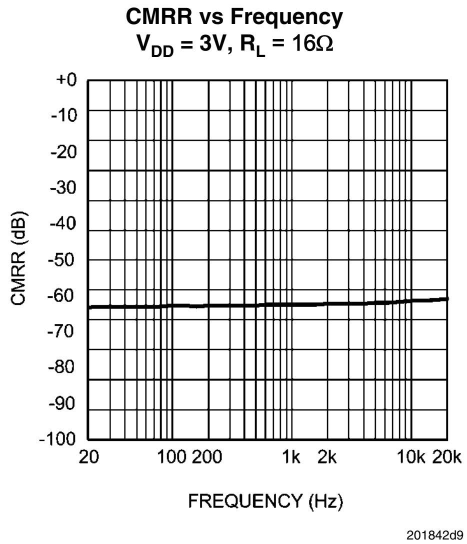
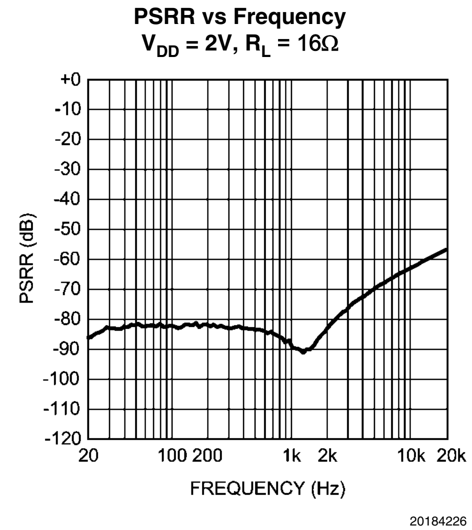
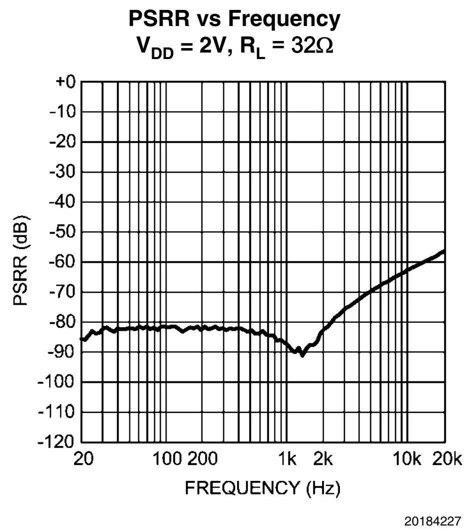
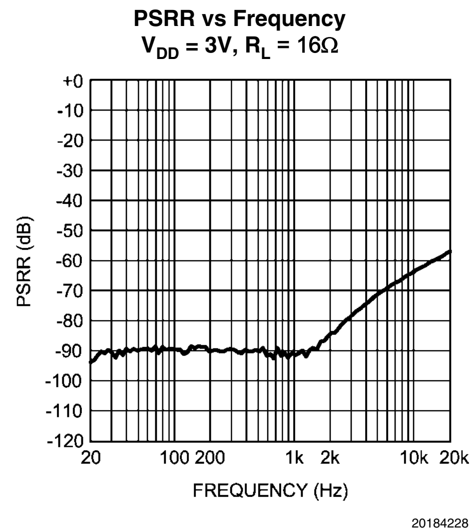
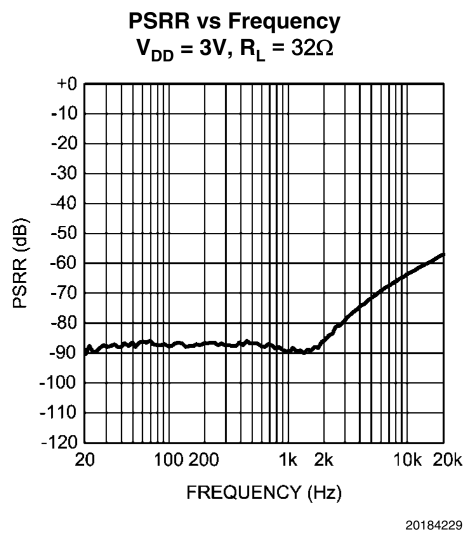
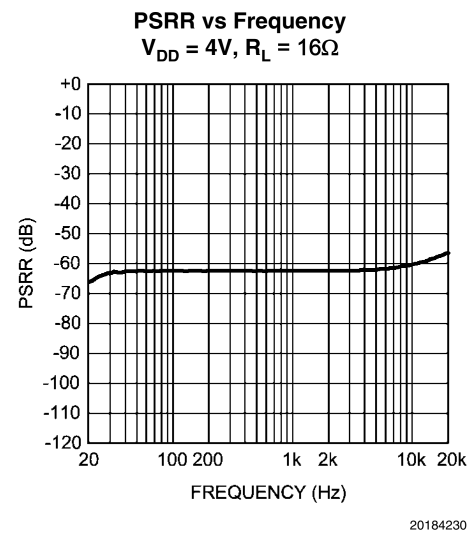

CMRR vs Frequency
V_{DD} = 3V, R_L = 16Ω
+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
CMRR (dB)
20
100 200
1k 2k
10k 20k
FREQUENCY (Hz)
201842d9


PSRR vs Frequency
V_{DD} = 2V, R_L = 16Ω
+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
PSRR (dB)
20
100 200
1k 2k
10k 20k
FREQUENCY (Hz)
20184226

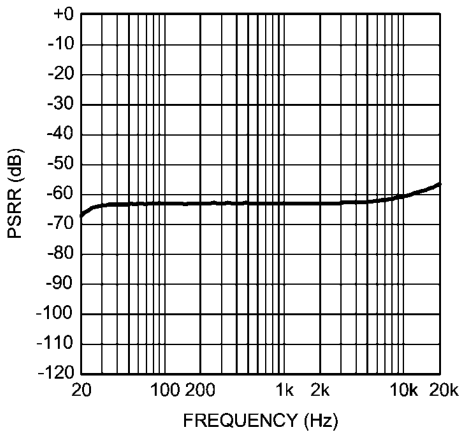

PSRR vs Frequency
V_{DD} = 2V, R_L = 32Ω
+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
PSRR (dB)
20
100 200
1k 2k
10k 20k
FREQUENCY (Hz)
20184227


PSRR vs Frequency
V_{DD} = 3V, R_L = 16Ω
+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
PSRR (dB)
20
100 200
1k 2k
10k 20k
FREQUENCY (Hz)
20184228


PSRR vs Frequency
V_{DD} = 3V, R_L = 32Ω
+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
PSRR (dB)
20
100 200
1k 2k
10k 20k
FREQUENCY (Hz)
20184229

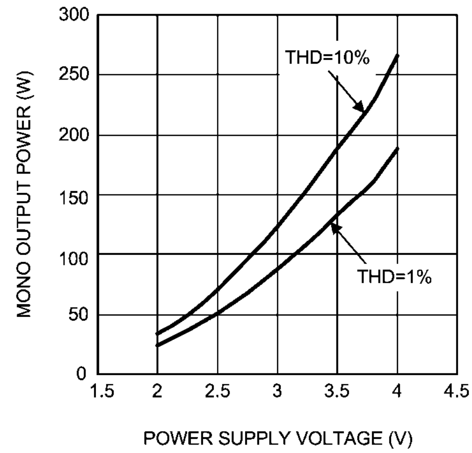

PSRR vs Frequency
V_{DD} = 4V, R_L = 16Ω
+0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
PSRR (dB)
20
100 200
1k 2k
10k 20k
FREQUENCY (Hz)
20184230

PSRR vs Frequency
V_{DD} = 4V, R_L = 32Ω



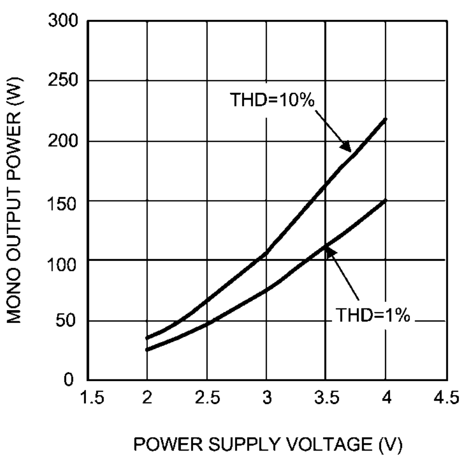
20184231

Output Power vs Voltage Supply
R_L = 16Ω, Mono



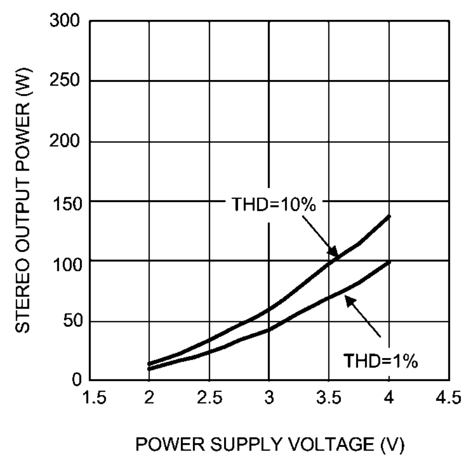
20184212

Output Power vs Voltage Supply
R_L = 32Ω, Mono



20184213

Output Power vs Voltage Supply
R_L = 16Ω, Stereo



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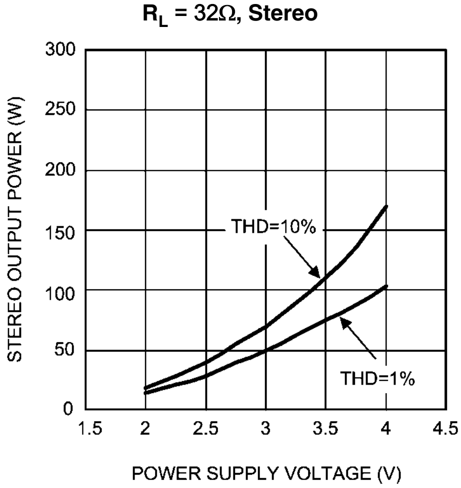
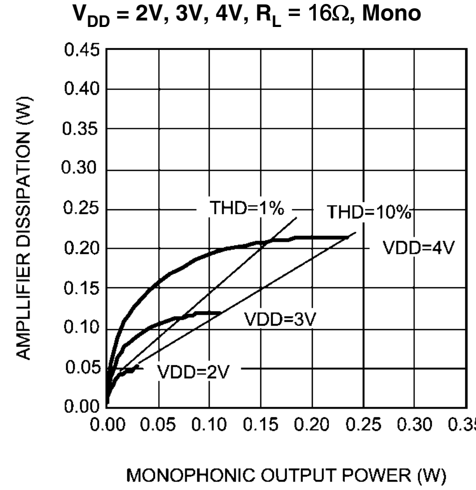
Output Power vs Voltage Supply
R_L = 32Ω, Stereo



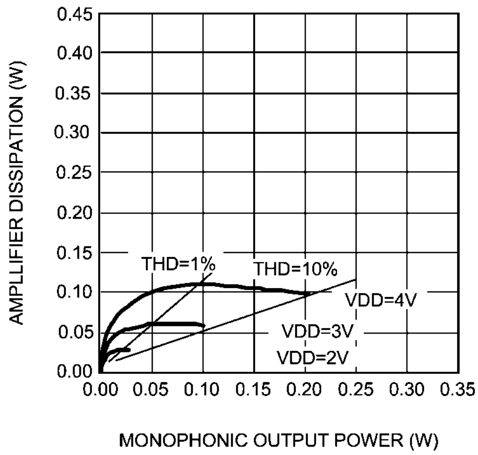
20184217

Output Power vs Power Dissipation
V_{DD} = 2V, 3V, 4V, R_L = 16Ω, Mono



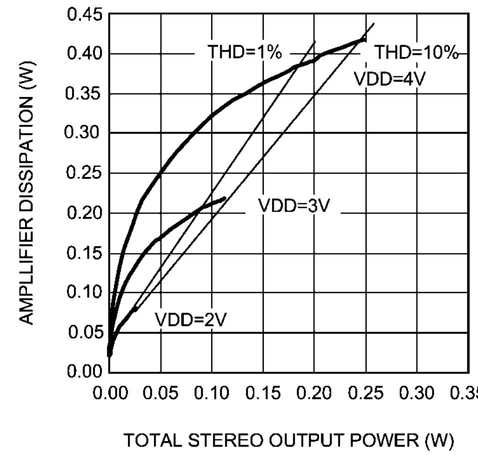
20184214

Output Power vs Power Dissipation
V_{DD} = 2V, 3V, 4V, R_L = 32Ω, Mono



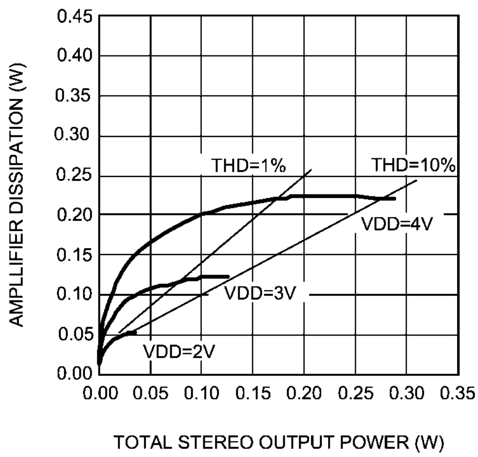
20184215

Output Power vs Power Dissipation
V_{DD} = 2V, 3V, 4V, R_L = 16Ω, Stereo



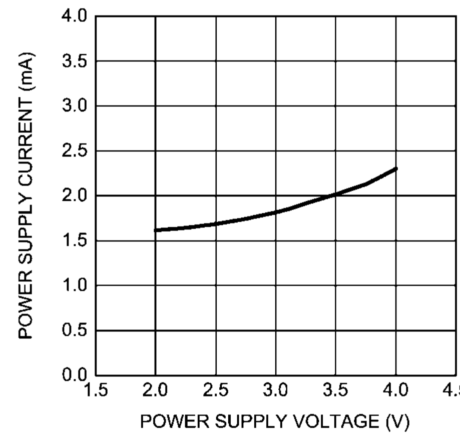
20184218

Output Power vs Power Dissipation
V_{DD} = 2V, 3V, 4V, R_L = 32Ω, Stereo



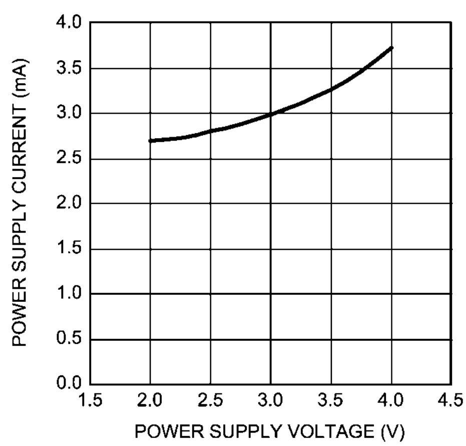
20184219

Supply Current vs Supply Voltage
Mono



20184209

Supply Current vs Supply Voltage
Stereo



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Application Information

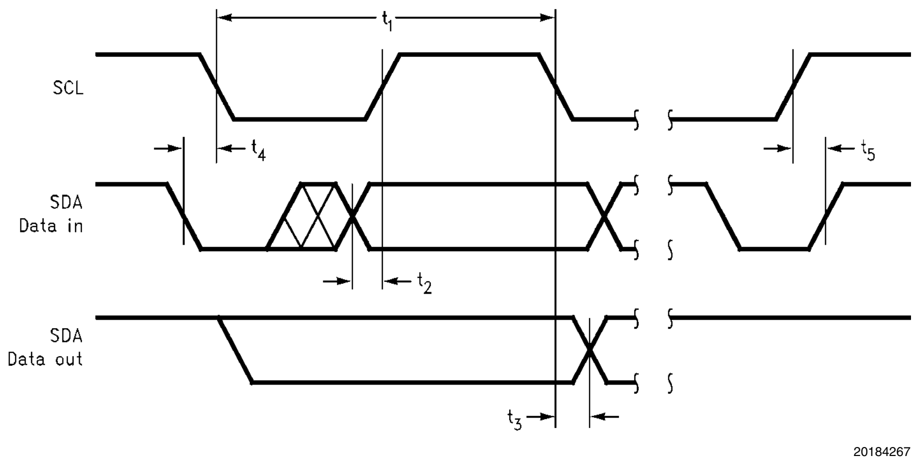


FIGURE 2. I²C Timing Diagram

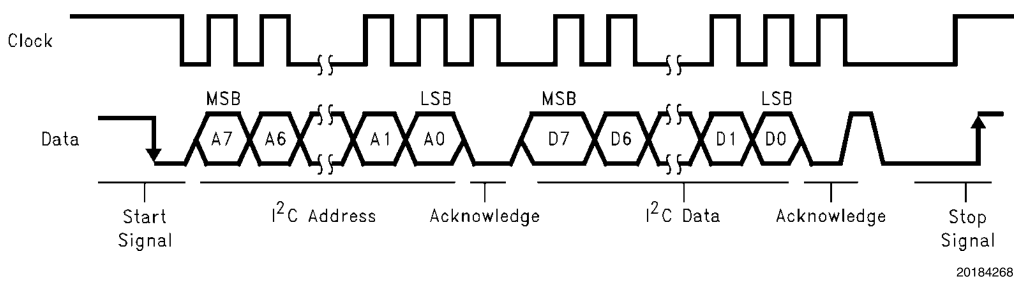


FIGURE 3. I²C Bus Format

TABLE 1. Chip Address

	D7	D6	D5	D4	D3	D2	D1	D0
Chip Address	1	1	1	0	1	1	0	0

TABLE 2. Control Registers

	D7	D6	D5	D4	D3	D2	D1	D0
Volume Control	VD4	VD3	VD2	VD1	VD0	MUTE	LF ENABLE	RT ENABLE

I²C VOLUME CONTROL

The LM48821 can be configured in 32 different gain steps by forcing I²C volume control bits to a desired gain according to the table below:

TABLE 3. Volume Control

VD4	VD3	VD2	VD1	VD0	Gain (dB)
0	0	0	0	0	–76
0	0	0	0	1	–62
0	0	0	1	0	–52
0	0	0	1	1	–44
0	0	1	0	0	–38
0	0	1	0	1	–34
0	0	1	1	0	–30
0	0	1	1	1	–27
0	1	0	0	0	–24
0	1	0	0	1	–21
0	1	0	1	0	–18
0	1	0	1	1	–16
0	1	1	0	0	–14
0	1	1	0	1	–12
0	1	1	1	0	–10
0	1	1	1	1	–8
1	0	0	0	0	–6
1	0	0	0	1	–4
1	0	0	1	0	–2
1	0	0	1	1	0
1	0	1	0	0	2
1	0	1	0	1	4
1	0	1	1	0	6
1	0	1	1	1	8
1	1	0	0	0	10
1	1	0	0	1	12
1	1	0	1	0	13
1	1	0	1	1	14
1	1	1	0	0	15
1	1	1	0	1	16
1	1	1	1	0	17
1	1	1	1	1	18

I²C COMPATIBLE INTERFACE

The LM48821 uses a serial data bus that conforms to the I²C protocol. Controlling the chip's functions is accomplished with two wires: serial clock (SCL) and serial data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I²C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM48821.

The bus format for the I²C interface is shown in Figure 3. The bus format diagram is broken up into six major sections: The Start Signal, the I²C Address, an Acknowledge bit, the I²C data, second Acknowledge bit, and the Stop Signal.

The start signal is generated by lowering the data signal while the clock signal is high. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is high.

After the last bit of the address bit is sent, the master releases the data line high (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM48821 has received the address correctly, then it holds the data line low during the clock pulse. If the data line is not held low during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM48821. The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable high.

After the data byte is sent, the master must check for another acknowledge to see if the LM48821 received the data.

If the master has more data bytes to send to the LM48821, then the master can repeat the previous two steps until all data bytes have been sent.

The stop signal ends the transfer. To signal stop , the data signal goes high while the clock signal is high. The data line should be held high when not in use.

The LM48821's I²C address is shown in Table 1. The I²C data register and its control bit names are shown in Table 2. The data values for the volume control are shown in Table 3.

I²C INTERFACE POWER SUPPLY PIN (I^2CV_{DD})

The LM48821's I²C interface is powered up through the I^2CV_{DD} pin. The LM48821's I²C interface operates at a voltage level set by the I^2CV_{DD} pin. This voltage can be independent from the main power supply pin (V_{DD}). This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 3.3V voltage regulator typically use a 10μF in parallel with a 0.1μF filter capacitors to stabilize the regulator's output, reduce noise on the regulated supply lines, and improve the regulator's transient response. However, their presence does not eliminate the need for a local 1.0μF tantalum bypass capacitance connected between the LM48821's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM48821's power supply pins and ground as short as possible.

ELIMINATING THE OUTPUT COUPLING CAPACITOR

The LM48821 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the LM48821 to reference its amplifier outputs to ground instead of a half-supply voltage, like traditional capacitivel-coupled headphone amplifiers. Because there is no DC bias voltage associated with either stereo output, the large DC blocking capacitors (typically 220μF) are not necessary. The coupling capacitors are replaced by two, small ceramic charge pump capacitors, saving board space and cost.

Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor form a high pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM48821 does not require the output coupling capacitors, the low frequency response of the device is not degraded.

In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the output voltage swing and available dynamic range of the LM48821 when compared to a traditional capacitively-coupled output headphone amplifier operating from the same supply voltage.

OUTPUT TRANSIENT ELIMINATED

The LM48821 contains advanced circuitry that virtually eliminates output transients ('clicks' and 'pops'). This circuitry attenuates output transients when the supply voltage is first applied or when the part resumes operation after using the shutdown mode.

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. Equation 1 states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (2V_{DD})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM48821 has two power amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from Equation 1. Even with large internal power dissipation, the LM48821 does not require heat sinking over a large range of ambient temperatures. The maximum power dissipation point obtained must not be greater than the power dissipation that results from Equation 2:

$$P_{DMAX} = (T_{JMAX} - T_A) / (\theta_{JA}) \quad (2)$$

For the micro SMD package, θ_{JA} = 105°C/W. T_{JMAX} = 150°C for the LM48821. Depending on the ambient temperature, T_A, of the system surroundings, Equation 2 can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of Equation 1 is greater than that of Equation 2, then either the supply voltage must be decreased, the load impedance increased or T_A reduced. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly.

SELECTING EXTERNAL COMPONENTS

Optimizing the LM48821's performance requires properly selecting external components. Though the LM48821 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

Charge Pump Capacitor Selection

Use low ESR (equivalent series resistance) (<100mΩ) ceramic capacitors with an X7R dielectric for best performance. Low ESR capacitors keep the charge pump output impedance to a minimum, extending the headroom on the negative supply. Higher ESR capacitors result in reduced output power from the audio amplifiers.

Charge pump load regulation and output impedance are affected by the value of the flying capacitor (connected between the C_{CP-} and C_{CP+} pins). A larger valued C_1 (up to 4.7µF) improves load regulation and minimizes charge pump output resistance. Beyond 4.7µF, the switchon-resistance dominates the output impedance.

The output ripple is affected by the value and ESR of the output capacitor (connected between the V_{SS} and PGND pins). Larger capacitors reduce output ripple on the negative power supply. Lower ESR capacitors minimize the output ripple and reduce the output impedance of the charge pump.

The LM48821 charge pump design is optimized for 4.7µF, low ESR, ceramic, flying, and output capacitors.

Power Supply Bypass Capacitor

For good THD+N and low noise performance and to ensure correct power-on behavior at the maximum allowed power supply voltage, a local 4.7µF power supply bypass capacitor should be connected as physically closed as possible to the PV_{DD} pin.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitors (the 0.47µF capacitors in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using high value input and output capacitors.

Besides affecting system cost and size, the input coupling capacitor value has an effect on the LM48821's click and pop performance. The magnitude of the pop is directly proportional to the input capacitor's size. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired -3dB frequency.

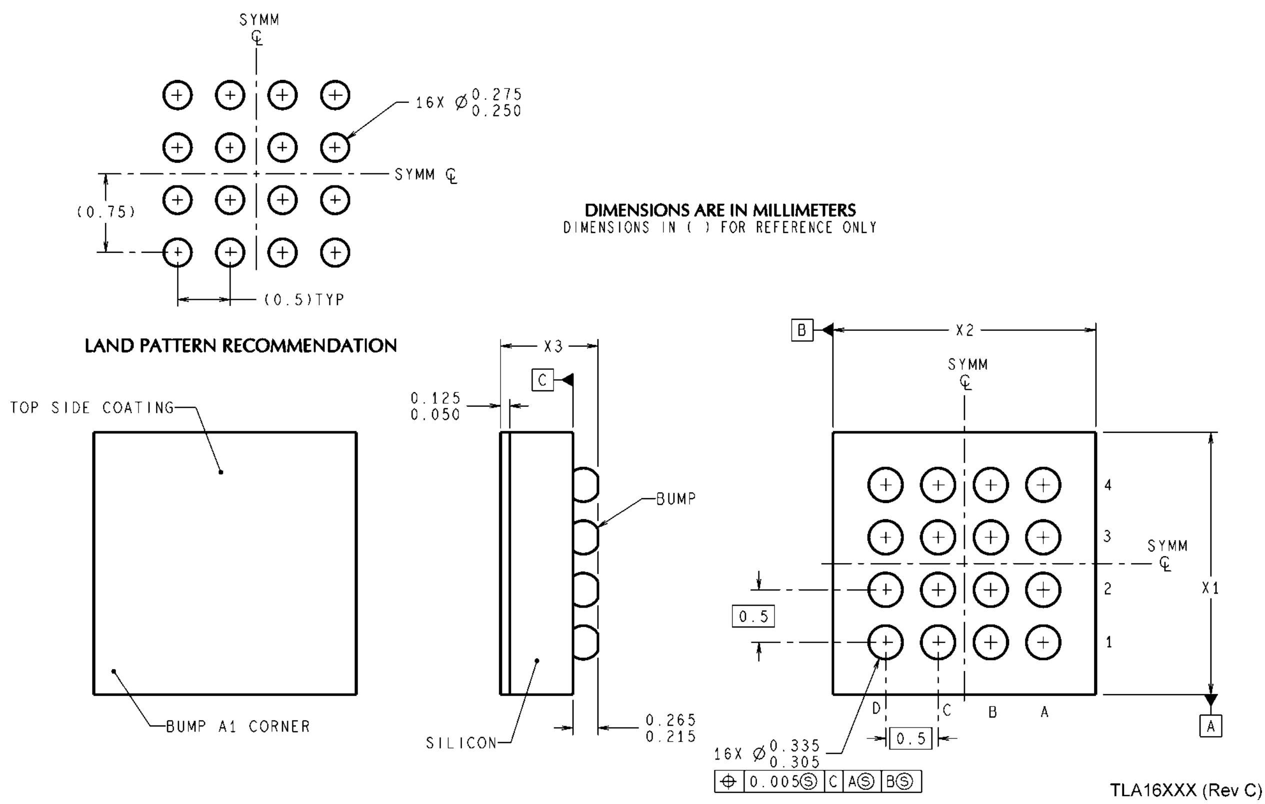
The LM48821's nominal input resistance at full volume is 10kΩ and a minimum of 5kΩ. This input resistance and the input coupling capacitor value produce a -3dB high pass filter cutoff frequency that is found using Equation 3.

$$f_{-3dB} = 1/2\pi R_i C_i \quad (3)$$

Revision History

Rev	Date	Description
1.0	06/06/07	Initial release.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Bump micro SMD
Order Number LM48821TL
NS Package Number TLA1611A
X_1 = 1.970± 0.03 X_2 = 1.970 ± 0.03 X_3 = 0.6 ± 0.075

Notes

Notes

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