

# LM4946

*LM4946 Output Capacitor-Less Audio Subsystem with Programmable National 3D*



Literature Number: SNAS335E

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# LM4946 Boomer<sup>®</sup> Audio Power Amplifier Series

## Output Capacitor-Less Audio Subsystem with Programmable National 3D

### General Description

The LM4946 is an audio power amplifier capable of delivering 540mW of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N, 35mW per channel of continuous average power into stereo 32Ω single-ended (SE) loads with 1% THD+N, or an output capacitor-less (OCL) configuration with identical specifications as the SE configuration, from a 3.3V power supply.

The LM4946 has three input channels: one pair for a two-channel stereo signal and the third for a differential single-channel mono input. The LM4946 features a 32-step digital volume control and eight distinct output modes. The digital volume control, 3D enhancement, and output modes (mono/SE/OCL) are programmed through a two-wire I<sup>2</sup>C or a three-wire SPI compatible interface that allows flexibility in routing and mixing audio channels.

The LM4946 is designed for cellular phone, PDA, and other portable handheld applications. It delivers high quality output power from a surface-mount package and requires only seven external components in the OCL mode (two additional components in SE mode).

### Key Specifications

■ THD+N at 1kHz, 540mW into 8Ω BTL (3.3V)	1.0% (typ)
■ THD+N at 1kHz, 35mW into 32Ω SE (3.3V)	1.0% (typ)
■ Single Supply Operation (V <sub>DD</sub> )	2.7 to 5.5V
■ I <sup>2</sup> C/SPI Single Supply Operation	
LLP	2.2 to 5.5V
micro SMD	1.7 to 5.5V

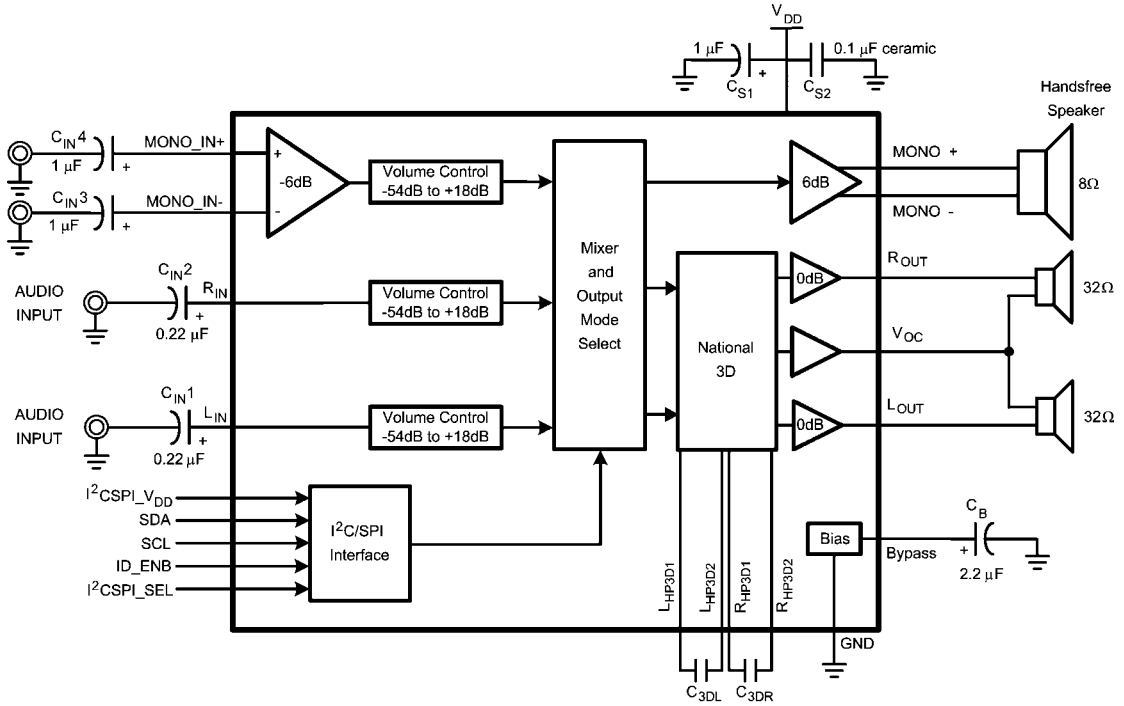
### Features

- I<sup>2</sup>C/SPI Control Interface
- I<sup>2</sup>C/SPI programmable National 3D Audio
- I<sup>2</sup>C/SPI controlled 32 step digital volume control (-54dB to +18dB)
- Three independent volume channels (Left, Right, Mono)
- Eight distinct output modes
- LLP and microSMD surface mount packaging
- "Click and Pop" suppression circuitry
- Thermal shutdown protection
- Low shutdown current (0.02uA, typ)
- RF immunity topology

### Applications

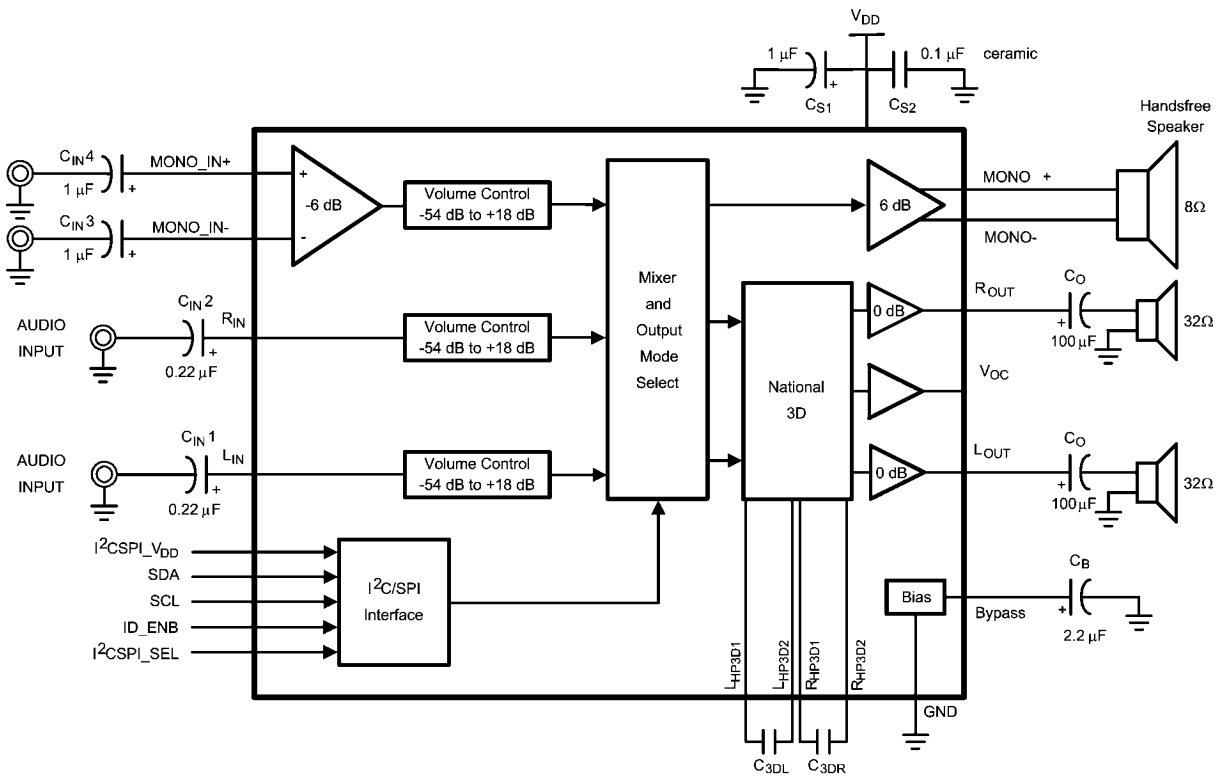
- Mobile Phones
- PDAs

# Typical Application



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FIGURE 1. Typical Audio Amplifier Application Circuit-Output Capacitor-less

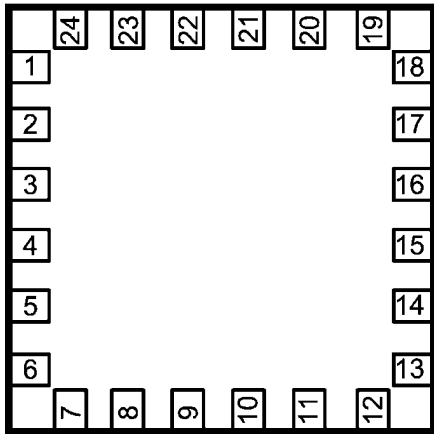


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FIGURE 2. Typical Audio Amplifier Application Circuit-Single Ended

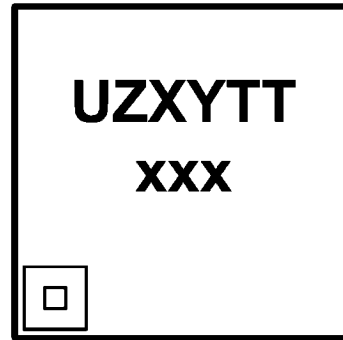
# Connection Diagrams

24 Lead LLP Package



Top View

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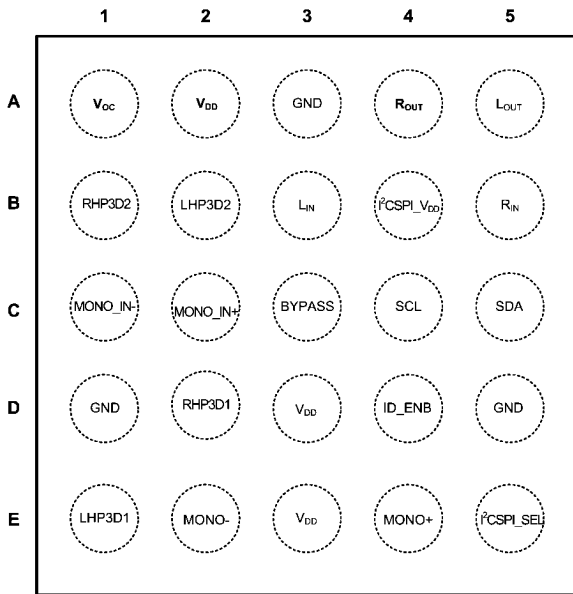


Pin 1

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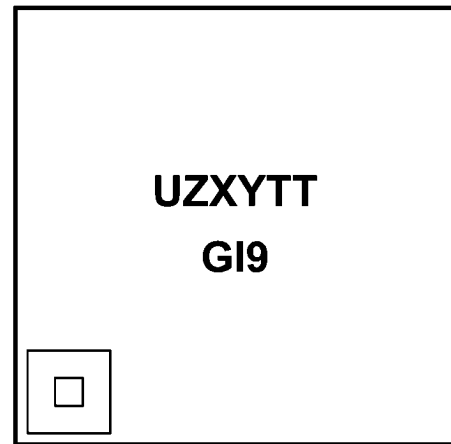
Top View  
 U - Wafer Fab Code  
 Z - Assembly Plant Code  
 XY - Date Code  
 TT - Die Traceability  
 xxx - L4946SQ

25 Bump micro SMD Package



Top View

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Bump A1

201628n3

Top View  
 U - Wafer Fab Code  
 Z - Assembly Plant Code  
 XY - Date Code  
 TT - Die Traceability  
 G - Boomer  
 I9 - LM4946TM

## Pin Descriptions

Pin Number (LLP)	Bump (Mirco SMD)	Name	Description
1	B2	LHP3D2	Left Headphone 3D Input 1
2	A1	V <sub>OC</sub>	Center Amplifier Output
3	A2	V <sub>DD</sub>	Voltage Supply
4	A3	GND	Ground
5	A4	R <sub>OUT</sub>	Right Headphone Output
6	A5	L <sub>OUT</sub>	Left Headphone Output
7	B4	I <sup>2</sup> C/SPI_V <sub>DD</sub>	I <sup>2</sup> C or SPI Interface Voltage Supply
8	B5	R <sub>IN</sub>	Right Input Channel
9	B3	L <sub>IN</sub>	Left Input Channel
10	C5	SDA	Data
11	C4	SCL	Clock
12	D5	GND	Ground
13	D4	ID_ENB	Address Identification/Enable Bar
14	E5	I <sup>2</sup> C/SPI_SEL	I <sup>2</sup> C or SPI Select
15	E4	MONO+	Loudspeaker Output Positive
16	D3	V <sub>DD</sub>	Voltage Supply
17	E2	MONO-	Loudspeaker Output Negative
18	E1	LHP3D1	Left Headphone 3D Input 2
19	D2	RHP3D1	Right Headphone 3D Input 1
20	D1	GND	Ground
21	C3	BYPASS	Half-Supply Bypass
22	C1	MONO_IN-	Loudspeaker Negative Input
23	C2	MONO_IN+	Loudspeaker Positive Input
24	B1	RHP3D2	Right Headphone 3D Input 2
	E3	V <sub>DD</sub>	Voltage Supply

**Absolute Maximum Ratings** (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3 to $V_{DD} + 0.3$
ESD Susceptibility (Note 3)	2.0kV
ESD Machine model (Note 6)	200V
Junction Temperature	150°C
Solder Information (Note 1)	
Vapor Phase (60 sec.)	215°C

Infrared (15 sec.)	220°C
Thermal Resistance (Note 8)	
$\theta_{JA}$ (typ) - SQA24A	46°C/W
$\theta_{JA}$ (typ) - TMD25A	49°C/W

**Operating Ratings**

Temperature Range	-40°C to 85°C
Supply Voltage ( $V_{DD}$ )	$2.7V \leq V_{DD} \leq 5.5V$
Supply Voltage (I <sup>2</sup> C/SPI) (Note 10)	$I^2CSPI\_V_{DD} \leq V_{DD}$
LLP	$2.2V \leq I^2CSPI\_V_{DD} \leq 5.5V$
micro SMD	$1.7V \leq I^2CSPI\_V_{DD} \leq 5.5V$

**Electrical Characteristics 3.3V** (Notes 2, 7)

The following specifications apply for  $V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$ , all volume controls set to 0dB, unless otherwise specified.

Symbol	Parameter	Conditions	LM4946		Units (Limits)
			Typical (Note 4)	Limits (Note 5)	
$I_{DD}$	Supply Current	Output Modes 2, 4, 6 $V_{IN} = 0V$ ; No load, SE Headphone	3.25		mA
		Output Modes 1, 3, 5, 7 $V_{IN} = 0V$ ; No load, SE Headphone	5.65		mA
		Output Modes 2, 4, 6 $V_{IN} = 0V$ ; No load, OCL Headphone	4	6.5	mA (max)
		Output Modes 1, 3, 5, OCL Headphone	5		mA
		Output Modes 7 $V_{IN} = 0V$ ; No load, OCL Headphone	6.5	10.5	mA (max)
$I_{SD}$	Shutdown Current	Output Mode 0	0.02	1	$\mu A$ (max)
$V_{OS}$	Output Offset Voltage	$V_{IN} = 0V$ , Mode 7 Mono	12	50	mV (max)
		$V_{IN} = 0V$ , Mode 7 Headphones (Note 11)	3	15	
$P_O$	Output Power	MONO <sub>OUT</sub> ; $R_L = 8\Omega$ THD+N = 1%; f = 1kHz, BTL, Mode 1	540	500	mW (min)
		$R_{OUT}$ and $L_{OUT}$ ; $R_L = 32\Omega$ THD+N = 1%; f = 1kHz, SE, Mode 4	35	30	mW (min)
THD+N	Total Harmonic Distortion + Noise	MONO <sub>OUT</sub> f = 1kHz $P_{OUT} = 250mW$ ; $R_L = 8\Omega$ , BTL, Mode 1	0.05		%
		$R_{OUT}$ and $L_{OUT}$ f = 1kHz $P_{OUT} = 12mW$ ; $R_L = 32\Omega$ , SE, Mode 4	0.015		%

Symbol	Parameter	Conditions	LM4946		Units (Limits)	
			Typical (Note 4)	Limits (Note 5)		
N <sub>OUT</sub>	Output Noise	A-weighted, inputs terminated to GND, output referred				
		Speaker; Mode 1	17		μV	
		Speaker; Mode 3, 7	27		μV	
		Speaker; Mode 5	33		μV	
		Headphone; SE, Mode 2	8		μV	
		Headphone; SE, Mode 4, 7	8		μV	
		Headphone; SE, Mode 6	12		μV	
		Headphone; OCL, Mode 2	8		μV	
		Headphone; OCL, Mode 4, 7	9		μV	
		Headphone; OCL, Mode 6	12		μV	
PSRR	Power Supply Rejection Ratio MONO <sub>OUT</sub>	V <sub>RIPPLE</sub> = 200mV <sub>PP</sub> ; f = 217Hz, R <sub>L</sub> = 8Ω C <sub>B</sub> = 2.2μF, BTL All audio inputs terminated to GND; output referred				
		BTL, Output Mode 1	76		dB	
		BTL, Output Mode 3, 7	65		dB	
		BTL, Output Mode 5	63		dB	
	Power Supply Rejection Ratio R <sub>OUT</sub> and L <sub>OUT</sub>	V <sub>RIPPLE</sub> = 200mV <sub>PP</sub> ; f = 217Hz, R <sub>L</sub> = 32Ω C <sub>B</sub> = 2.2μF, All audio inputs terminated to GND output referred				
		SE, Output Mode 2	78		dB	
		SE, Output Mode 4,7	82		dB	
		SE, Output Mode 6	78		dB	
		OCL, Output Mode 2	84		dB	
OCL, Output Mode 4, 7	78		dB			
OCL, Output Mode 6	77		dB			
	Volume Control Step Size Error		±0.2		dB	
	Digital Volume Control Range	Maximum attenuation	-54	-56 -52	dB (max) dB (min)	
Maximum gain		18	17.4 18.6	dB (min) dB (max)		
	HP(SE) Mute Attenuation	Output Mode 1, 3, 5	96		dB	
	MONO_IN Input Impedance R <sub>IN</sub> and L <sub>IN</sub> Input Impedance	Maximum gain setting	12.5	10 15	kΩ (min) kΩ (max)	
		Maximum attenuation setting	110	90 130	kΩ (min) kΩ (max)	
CMRR	Common-Mode Rejection Ratio	f = 217Hz, V <sub>CM</sub> = 1V <sub>pp</sub> , Mode 1, BTL, R <sub>L</sub> = 8Ω	61		dB	
		f = 217Hz, V <sub>CM</sub> = 1V <sub>pp</sub> , Mode 2, R <sub>L</sub> = 32Ω	66			
XTALK	Crosstalk	Headphone; P <sub>O</sub> = 12mW f = 1kHz, OCL, Mode 4	-54		dB	
		Headphone; P <sub>O</sub> = 12mW f = 1kHz, SE, Mode 4	-72		dB	
T <sub>WU</sub>	Wake-Up Time from Shutdown	C <sub>B</sub> = 2.2μF, OCL	100		ms	
		C <sub>B</sub> = 2.2μF, SE	135		ms	

## Electrical Characteristics 5.0V (Notes 2, 7)

The following specifications apply for  $V_{DD} = 5.0V$ ,  $T_A = 25^\circ C$ , all volume controls set to 0dB, unless otherwise specified.

Symbol	Parameter	Conditions	LM4946		Units (Limits)
			Typical (Note 4)	Limits (Note 5)	
$I_{DD}$	Supply Current	Output Modes 2, 4, 6 $V_{IN} = 0V$ ; No load SE Headphone	3.8		mA
		Output Modes 1, 3, 5, 7 $V_{IN} = 0V$ ; No Load, SE Headphone	6.6		mA
		Output Modes 2, 4, 6 $V_{IN} = 0V$ ; No load, OCL Headphone	4.6		mA
		Output Modes 1, 3, 5 $V_{IN} = 0V$ ; No Load, OCL Headphone	6		mA
		Output Modes 7 $V_{IN} = 0V$ ; No Load, OCL Headphone	7.4		mA
$I_{SD}$	Shutdown Current	Output Mode 0	0.05		$\mu A$
$V_{OS}$	Output Offset Voltage	$V_{IN} = 0V$ , Mode 7 Mono	12		mV
		$V_{IN} = 0V$ , Mode 7 Headphones	3		
$P_O$	Output Power	MONO <sub>OUT</sub> ; $R_L = 8\Omega$ THD+N = 1%; $f = 1kHz$ , BTL, Mode 1	1.3		W
		$R_{OUT}$ and $L_{OUT}$ ; $R_L = 32\Omega$ THD+N = 1%; $f = 1kHz$ , SE, Mode 4	85		mW
THD+N	Total Harmonic Distortion + Noise	MONO <sub>OUT</sub> , $f = 1kHz$ $P_{OUT} = 500mW$ ; $R_L = 8\Omega$ , BTL, Mode 1	0.05		%
		$R_{OUT}$ and $L_{OUT}$ , $f = 1kHz$ $P_{OUT} = 30mW$ ; $R_L = 32\Omega$ , SE, Mode 4	0.012		%
$N_{OUT}$	Output Noise	A-weighted, inputs terminated to GND, output referred Speaker; Mode 1	17		$\mu V$
		Speaker; Mode 3, 7	27		$\mu V$
		Speaker; Mode 5	33		$\mu V$
		Headphone; SE, Mode 2	8		$\mu V$
		Headphone; SE, Mode 4, 7	8		$\mu V$
		Headphone; SE, Mode 6	12		$\mu V$
		Headphone; OCL, Mode 2	8		$\mu V$
		Headphone; OCL, Mode 4, 7	9		$\mu V$
		Headphone; OCL, Mode 6	12		$\mu V$
PSRR	Power Supply rejection Ratio MONO <sub>OUT</sub>	$V_{RIPPLE} = 200mV_{PP}$ ; $f = 217Hz$ , $R_L = 8\Omega$ $C_B = 2.2\mu F$ , BTL All audio inputs terminated to GND; output referred			
		BTL, Output Mode 1	69		dB
		BTL, Output Mode 3, 7	60		dB
		BTL, Output Mode 5	58		dB



Symbol	Parameter	Conditions	LM4946		Units (Limits)
			Typical (Note 4)	Limits (Note 5)	
PSRR	Power Supply Rejection Ratio $R_{OUT}$ and $L_{OUT}$	$V_{RIPPLE} = 200mV_{PP}$ ; $f = 217Hz$ , $R_L = 32\Omega$ $C_B = 2.2\mu F$ , BTL All audio inputs terminated to GND; output referred			
		SE, Output Mode 2	75		dB
		SE, Output Mode 4,7	75		dB
		SE, Output Mode 6	72		dB
		OCL, Output Mode 2	75		dB
		OCL, Output Mode 4, 7	79		dB
		OCL, Output Mode 6	72		dB
	Digital Volume Control Range	Maximum attenuation	-54	-56 -52	dB (max) dB (min)
		Maximum gain	18	17.4 18.6	dB (min) dB (max)
	HP(SE) Mute Attenuation	Output Mode 1, 3, 5	96		dB
	MONO_IN Input Impedance $R_{IN}$ and $L_{IN}$ Input Impedance	Maximum gain setting	12.5	10 15	k $\Omega$ (min) k $\Omega$ (max)
		Maximum attenuation setting	110	90 130	k $\Omega$ (min) k $\Omega$ (max)
CMRR	Common-Mode Rejection Ratio	$f = 217Hz$ , $V_{CM} = 1V_{pp}$ , 0dB gain Mode 1, BTL, $R_L = 8\Omega$	61		dB
		$f = 217Hz$ , $V_{CM} = 1V_{pp}$ , 0dB gain Mode 2, $R_L = 32\Omega$	66		
XTALK	Crosstalk	Headphone; $P_O = 30mW$ , OCL, Mode 4	-55		dB
		Headphone; $P_O = 30mW$ , SE, Mode 4	-72		dB
TWU	Wake-Up Time from Shutdown	$C_B = 2.2\mu F$ , OCL	135		ms
		$C_B = 2.2\mu F$ , SE	180		ms

**I<sup>2</sup>C/SPI LLP/micro SMD** (Notes 2, 7)

The following specifications apply for  $V_{DD} = 5.0V$  and  $3.3V$ ,  $T_A = 25^\circ C$ ,  $2.2V \leq I^2CSPI\_V_{DD} \leq 5.5V$ , unless otherwise specified.

Symbol	Parameter	Conditions	LM4946		Units (Limits)
			Typical (Note 4)	Limits (Notes 5, 7)	
$t_1$	I <sup>2</sup> C Clock Period			2.5	$\mu s$ (min)
$t_2$	I <sup>2</sup> C Data Setup Time			100	ns (min)
$t_3$	I <sup>2</sup> C Data Stable Time			0	ns (min)
$t_4$	Start Condition Time			100	ns (min)
$t_5$	Stop Condition Time			100	ns (min)
$t_6$	I <sup>2</sup> C Data Hold Time			100	ns (min)
$f_{SPI}$	Maximum SPI Frequency			1000	kHz (max)
$t_{EL}$	SPI ENB High Time			100	ns (min)
$t_{DS}$	SPI Data Setup Time			100	ns (min)
$t_{ES}$	SPI ENB Setup Time			100	ns (min)
$t_{DH}$	SPI Data Hold Time			100	ns (min)
$t_{EH}$	SPI Enable Hold Time			100	ns (min)
$t_{CL}$	SPI Clock Low Time			500	ns (min)
$t_{CH}$	SPI Clock High Time			500	ns (min)
$V_{IH}$	I <sup>2</sup> C/SPI Input Voltage High			$0.7 \times I^2CSPI$ $V_{DD}$	V (min)
$V_{IL}$	I <sup>2</sup> C/SPI Input Voltage Low			$0.3 \times I^2CSPI$ $V_{DD}$	V (max)

**I<sup>2</sup>C/SPI micro SMD only** (Notes 2, 7)

The following specifications apply for  $V_{DD} = 5.0V$  and  $3.3V$ ,  $T_A = 25^\circ C$ ,  $1.7V \leq I^2CSPI\_V_{DD} \leq 2.2V$ , unless otherwise specified.

Symbol	Parameter	Conditions	LM4946		Units (Limits)
			Typical (Note 4)	Limits (Notes 5, 7)	
$t_1$	I <sup>2</sup> C Clock Period			2.5	$\mu s$ (min)
$t_2$	I <sup>2</sup> C Data Setup Time			250	ns (min)
$t_3$	I <sup>2</sup> C Data Stable Time			0	ns (min)
$t_4$	Start Condition Time			250	ns (min)
$t_5$	Stop Condition Time			250	ns (min)
$t_6$	I <sup>2</sup> C Data Hold Time			250	ns (min)
$f_{SPI}$	Maximum SPI Frequency			250	kHz (max)
$t_{EL}$	SPI ENB High Time			250	ns (min)
$t_{DS}$	SPI Data Setup Time			250	ns (min)
$t_{ES}$	SPI ENB Setup Time			250	ns (min)
$t_{DH}$	SPI Data Hold Time			250	ns (min)
$t_{EH}$	SPI Enable Hold Time			250	ns (min)
$t_{CL}$	SPI Clock Low Time			500	ns (min)
$t_{CH}$	SPI Clock High Time			500	ns (min)
$V_{IH}$	I <sup>2</sup> C/SPI Input Voltage High			$0.7 \times I^2CSPI$ $V_{DD}$	V (min)
$V_{IL}$	I <sup>2</sup> C/SPI Input Voltage Low			$0.25 \times I^2CSPI$ $V_{DD}$	V (max)

**Note 1:** See AN-450 "Surface Mounting and their effects on Product Reliability" for other methods of soldering surface mount devices.

**Note 2:** Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 3:** Human body model, 100pF discharged through a 1.5k $\Omega$  resistor.

**Note 4:** Typical specifications are specified at +25°C and represent the most likely parametric norm.

**Note 5:** Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

**Note 6:** Machine Model ESD test is covered by specification EIAJ IC-121-1981. A 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (resistance of discharge path must be under 50 $\Omega$ ).

**Note 7:** All voltages are measured with respect to the ground pin, unless otherwise specified.

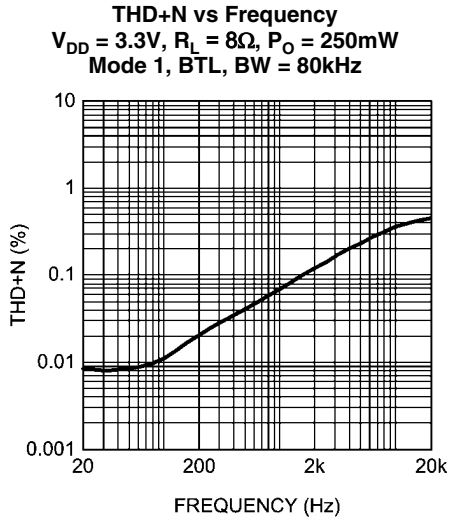
**Note 8:** The given  $\theta_{JA}$  for an LM4946SQ mounted on a demonstration board with a 9in<sup>2</sup> area of 1oz printed circuit board copper ground plane.

**Note 9:** Datasheet min/max specifications are guaranteed by design, test, or statistical analysis.

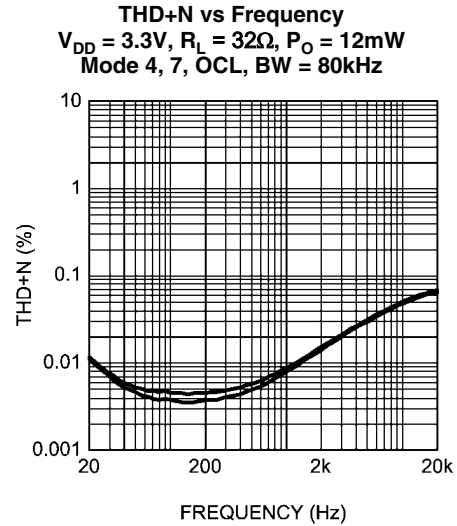
**Note 10:** Refer to table on page 9.

**Note 11:** For LM4946 LLP package, revised specification goes into effect starting with date code 79. Existing specification is per datasheet rev 1.0

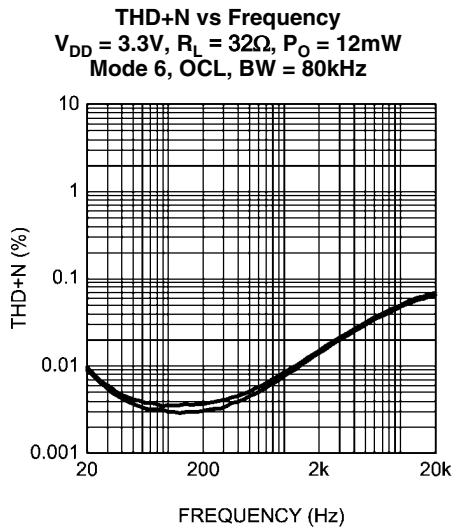
## Typical Performance Characteristics



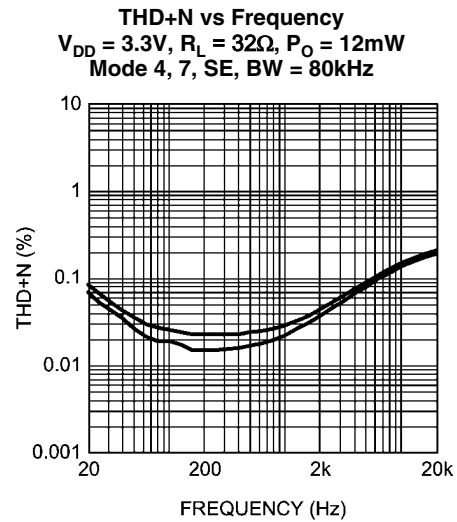
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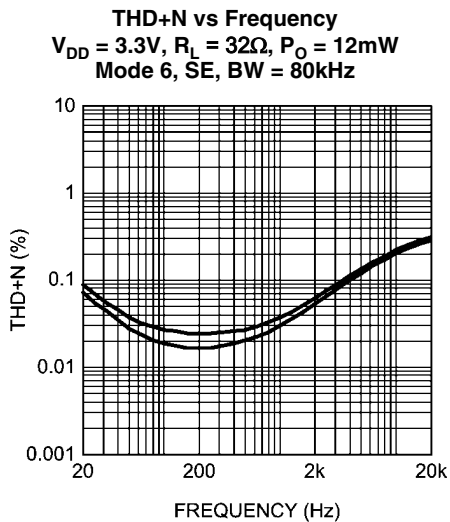
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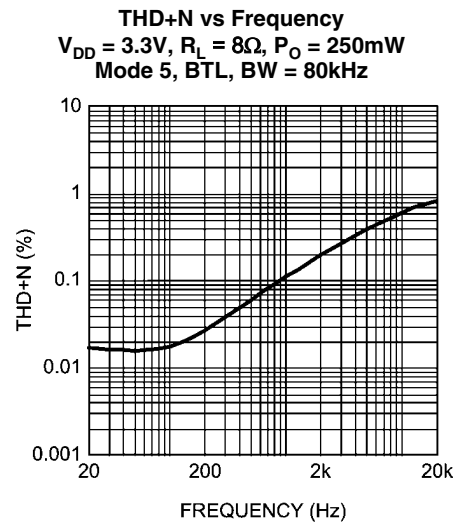
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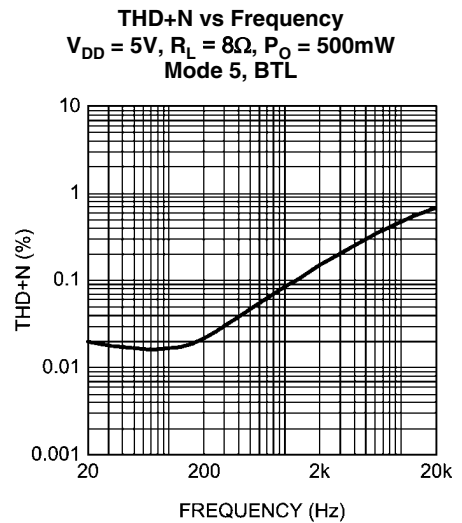
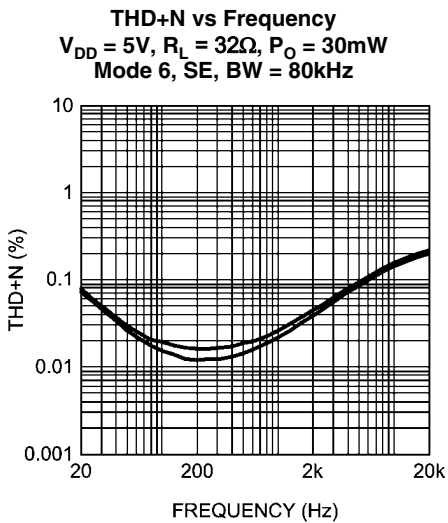
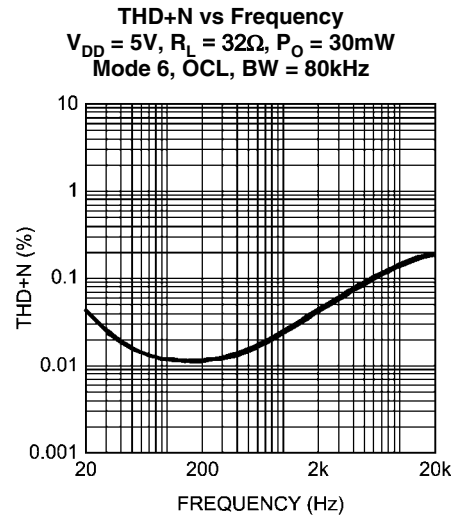
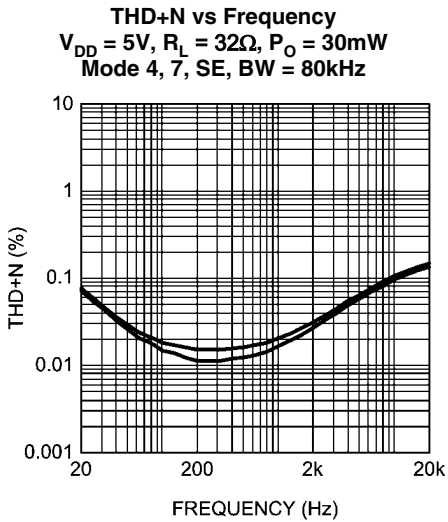
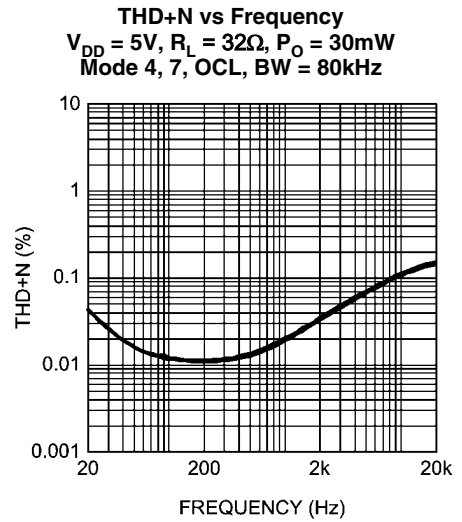
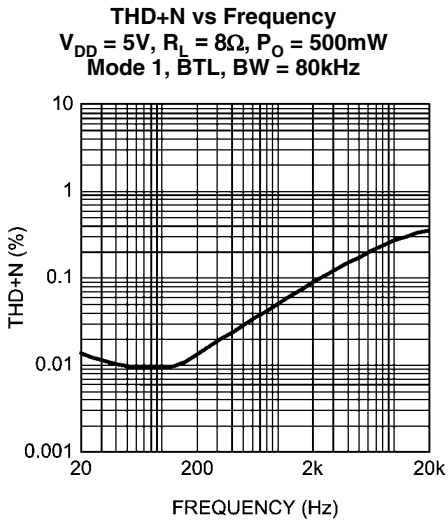
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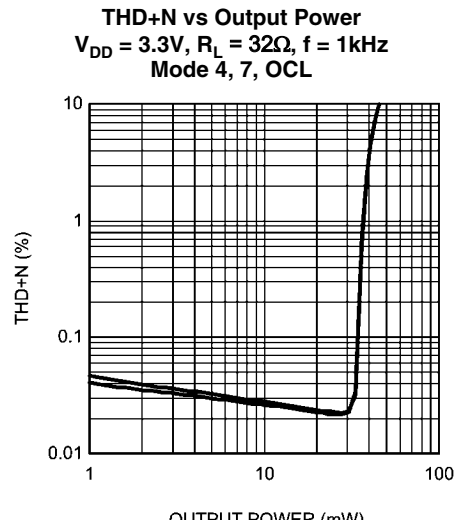
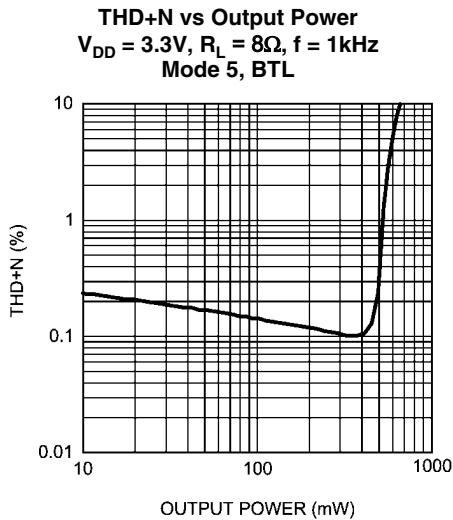
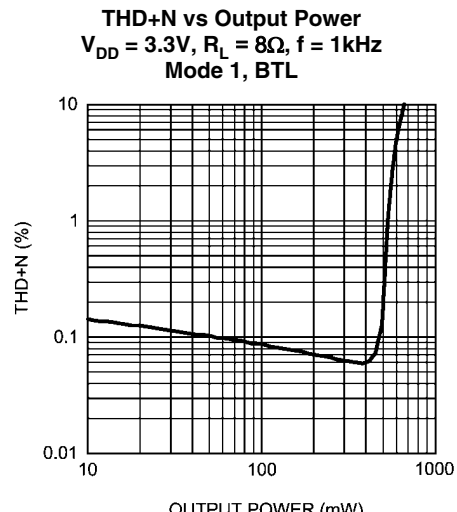
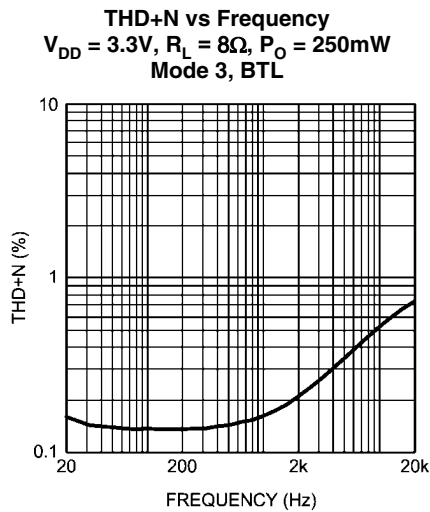
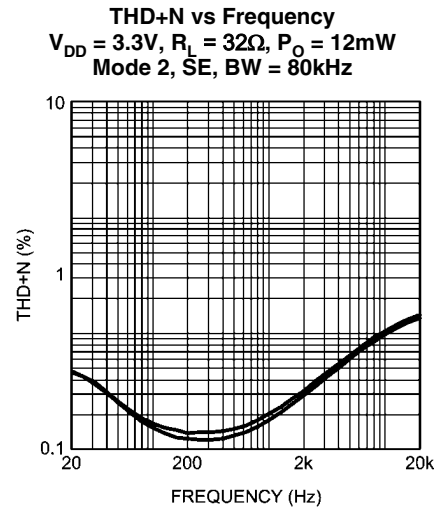
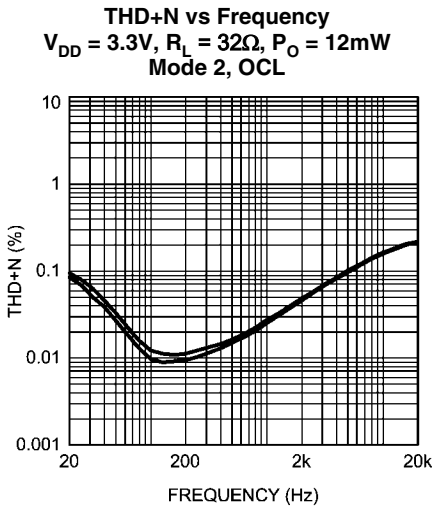


20162834

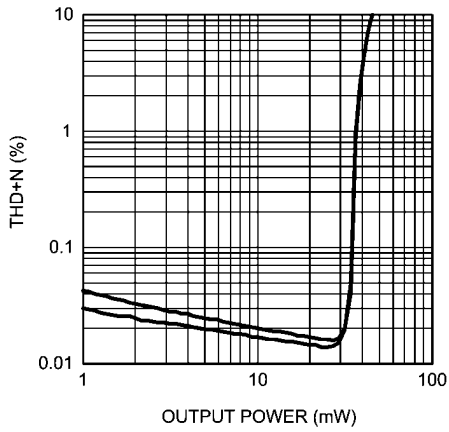


20162827



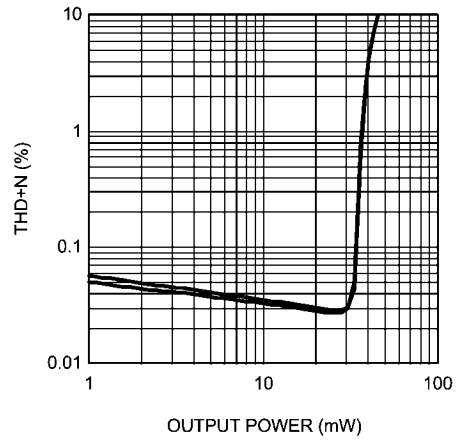


**THD+N vs Output Power**  
 $V_{DD} = 3.3V, R_L = 32\Omega, f = 1kHz$   
 Mode 4, 7, SE



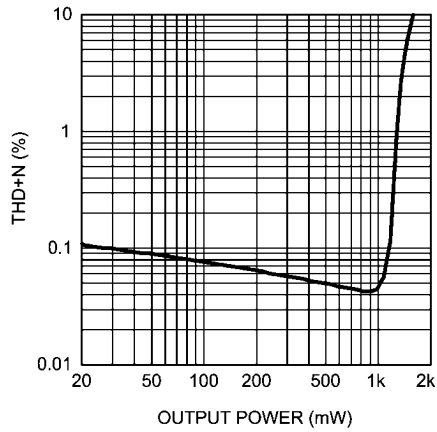
201628b1

**THD+N vs Output Power**  
 $V_{DD} = 3.3V, R_L = 32\Omega, f = 1kHz$   
 Mode 6, SE



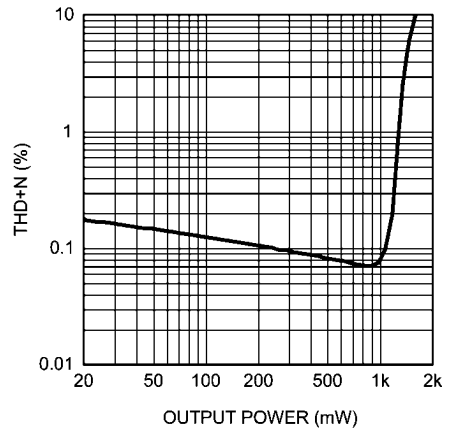
201628e7

**THD+N vs Output Power**  
 $V_{DD} = 5V, R_L = 8\Omega, f = 1kHz$   
 Mode 1, BTL



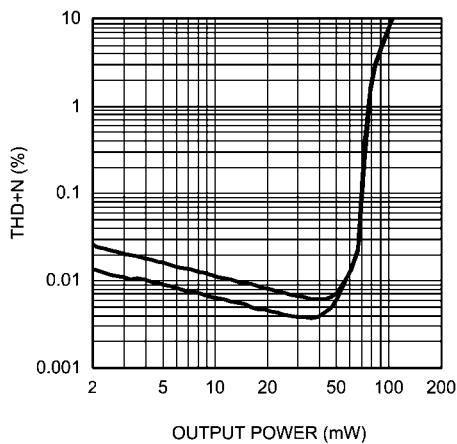
201628b2

**THD+N vs Output Power**  
 $V_{DD} = 5V, R_L = 8\Omega, f = 1kHz$   
 Mode 5, BTL



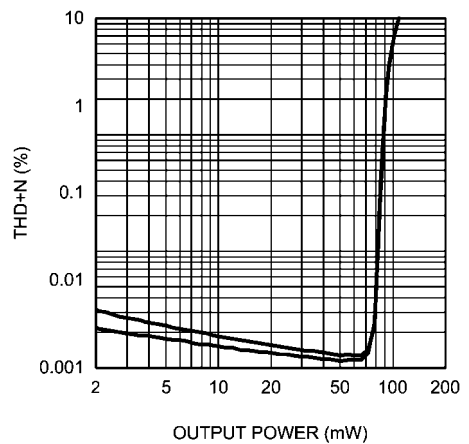
201628b6

**THD+N vs Output Power**  
 $V_{DD} = 5V, R_L = 32\Omega, f = 1kHz$   
 Mode 4, 7, OCL



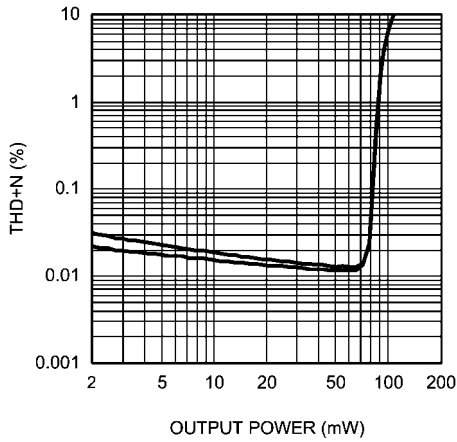
201628c0

**THD+N vs Output Power**  
 $V_{DD} = 5V, R_L = 32\Omega, f = 1kHz$   
 Mode 4, 7, SE



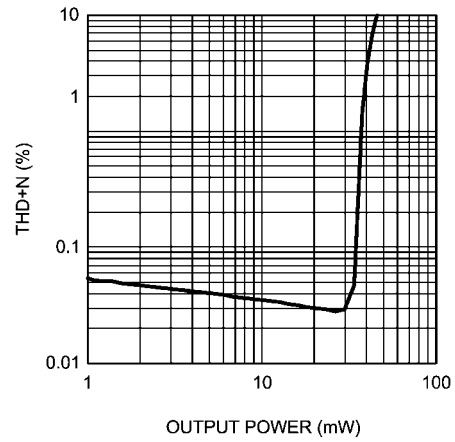
201628b3

**THD+N vs Output Power**  
 $V_{DD} = 5V, R_L = 32\Omega, f = 1kHz$   
 Mode 6, SE



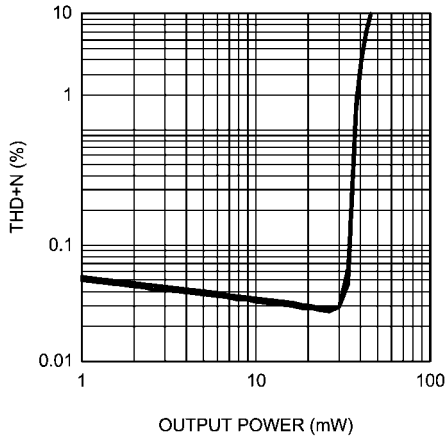
201628c1

**THD+N vs Output Power**  
 $V_{DD} = 3.3V, R_L = 32\Omega, f = 1kHz$   
 Mode 6, Mono Input, OCL



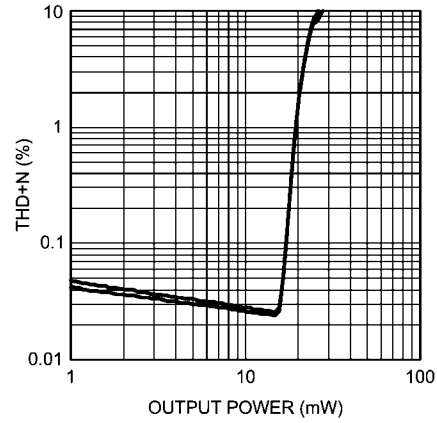
201628m1

**THD+N vs Output Power**  
 $V_{DD} = 3.3V, R_L = 32\Omega, f = 1kHz$   
 Mode 6, Stereo Input, OCL



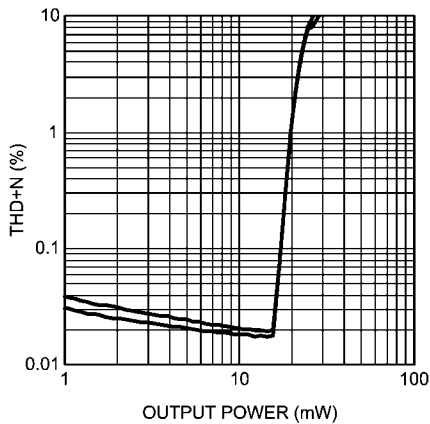
201628m2

**THD+N vs Output Power**  
 $V_{DD} = 3.3V, R_L = 32\Omega, f = 1kHz$   
 Mode 2, OCL



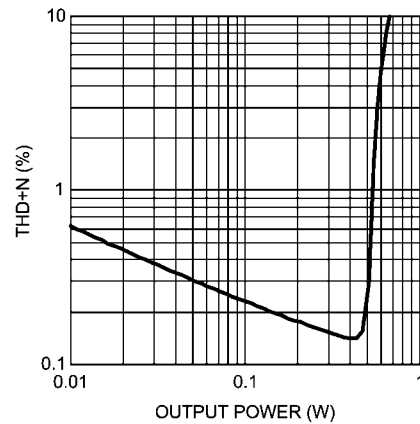
201628m6

**THD+N vs Output Power**  
 $V_{DD} = 3.3V, R_L = 32\Omega, f = 1kHz$   
 Mode 2, SE



201628m7

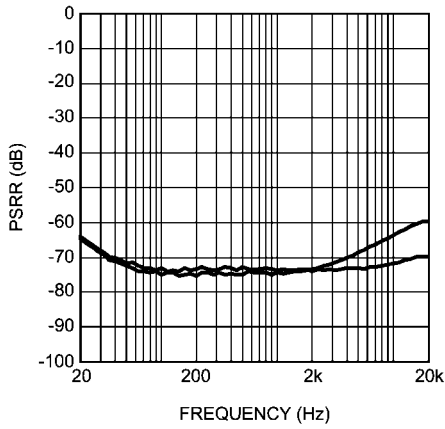
**THD+N vs Output Power**  
 $V_{DD} = 3.3V, R_L = 8\Omega, f = 1kHz$   
 Mode 3, BTL



201628m8

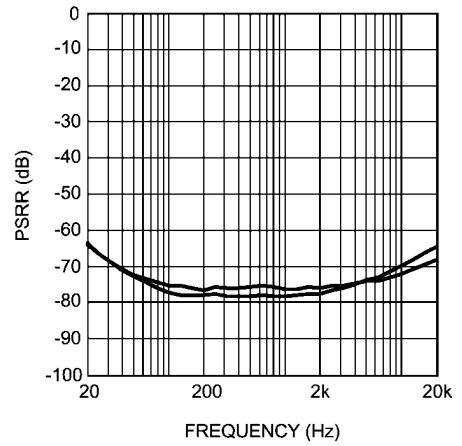


**PSRR vs Frequency**  
 $V_{DD} = 3.3V, 0dB$   
 Mode 4, 7, OCL



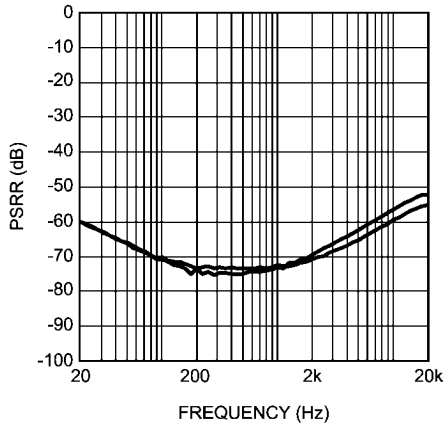
20162819

**PSRR vs Frequency**  
 $V_{DD} = 3.3V, 0dB$   
 Mode 4, 7, SE



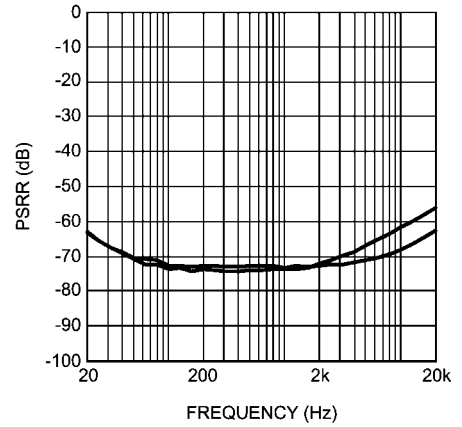
20162820

**PSRR vs Frequency**  
 $V_{DD} = 3.3V, 0dB$   
 Mode 6, OCL



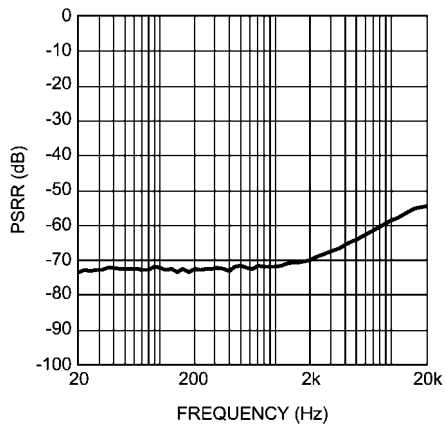
20162821

**PSRR vs Frequency**  
 $V_{DD} = 3.3V, 0dB$   
 Mode 6, SE



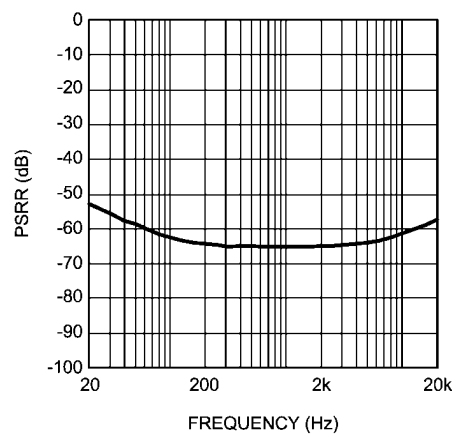
20162822

**PSRR vs Frequency**  
 $V_{DD} = 3.3V, 6dB$   
 Mode 1, BTL

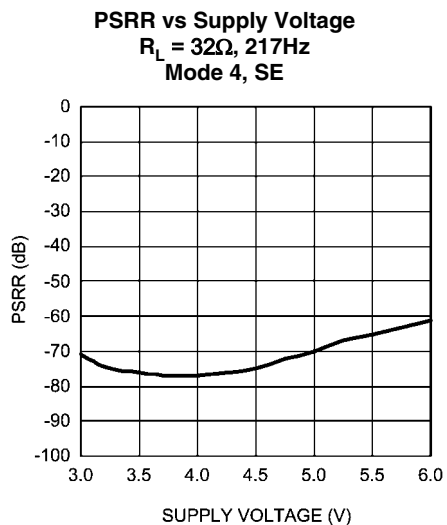
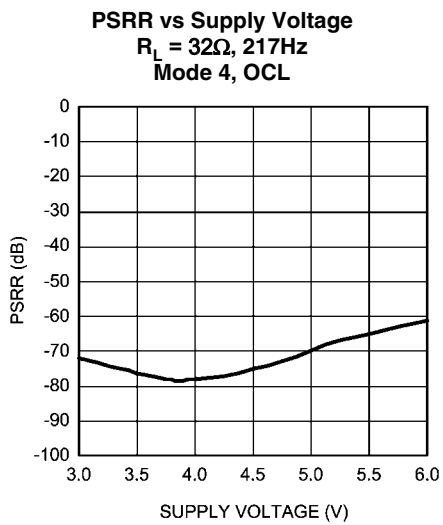
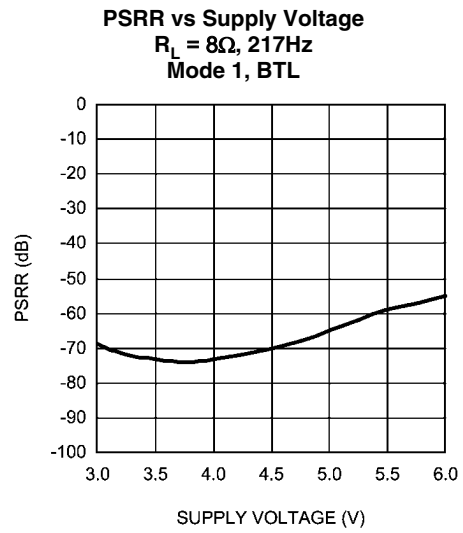
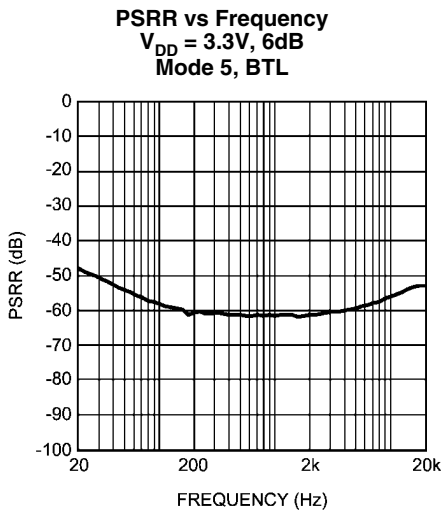
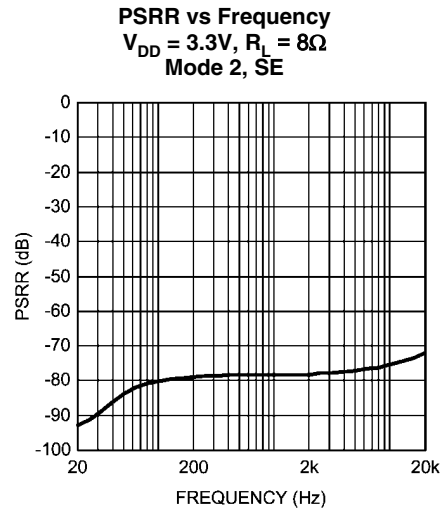
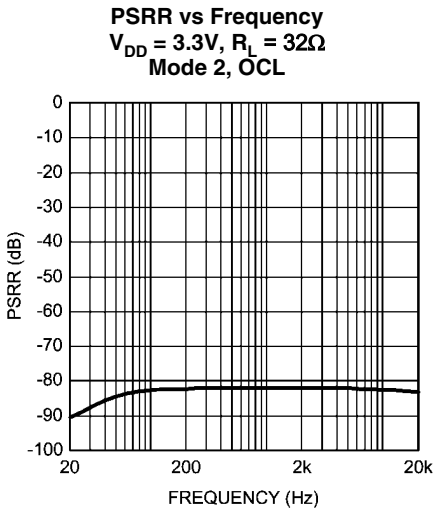


20162823

**PSRR vs Frequency**  
 $V_{DD} = 3.3V, R_L = 8\Omega$   
 Mode 3, 7, BTL

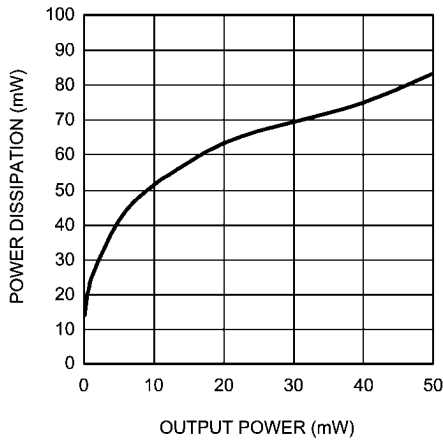


20162877



**Power Dissipation vs Output Power**

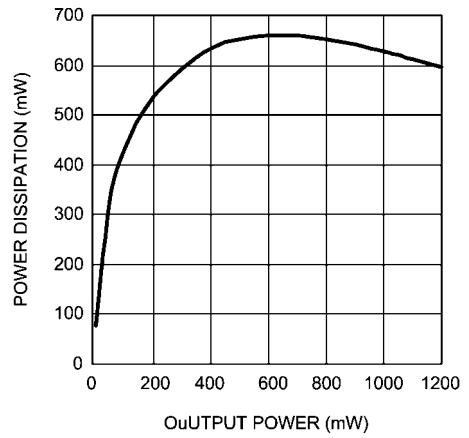
$V_{DD} = 3.3V$ ,  $R_L = 32\Omega$   
 $f = 1kHz$ , Mode 2, 4, 6, SE



201628g0

**Power Dissipation vs Output Power**

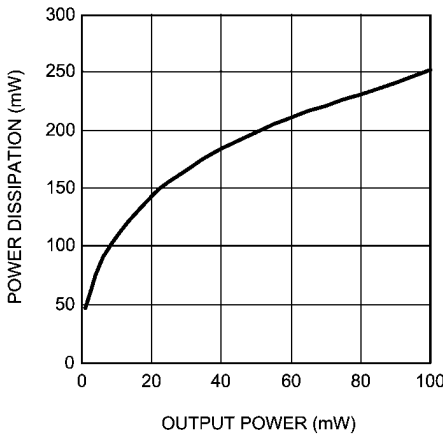
$V_{DD} = 5V$ ,  $R_L = 8\Omega$   
 $f = 1kHz$ , Mode 1, 3, 5, BTL



201628c5

**Power Dissipation vs Output Power**

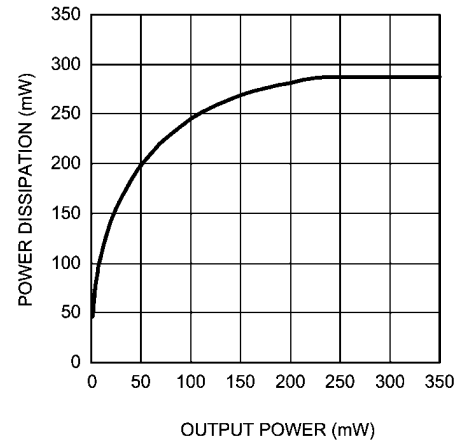
$V_{DD} = 5V$ ,  $R_L = 32\Omega$   
 $f = 1kHz$ , Mode 2, 4, 6, OCL



201628c6

**Power Dissipation vs Output Power**

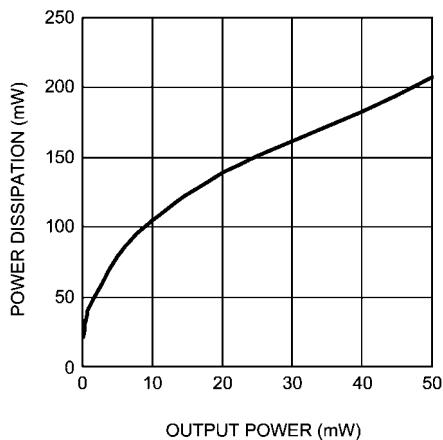
$V_{DD} = 3.3V$ ,  $R_L = 8\Omega$ ,  $f = 1kHz$ ,  
 Modes 1, 3, 5, BTL



201628k5

**Power Dissipation vs Output Power**

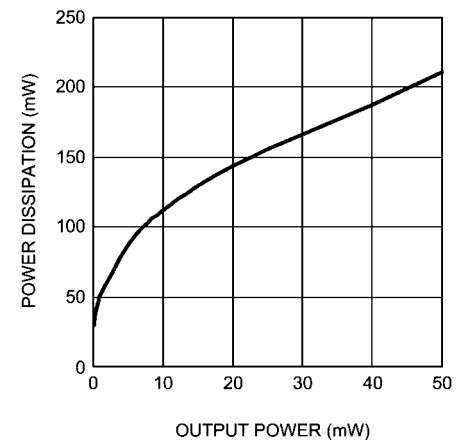
$V_{DD} = 3.3V$ ,  $R_L = 32\Omega$ ,  $f = 1kHz$ ,  
 Modes 2, 4, 6, OCL



201628k6

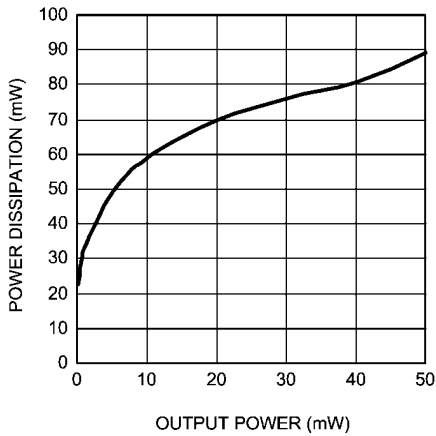
**Power Dissipation vs Output Power**

$V_{DD} = 3.3V$ ,  $R_L = 8\Omega$ ,  $f = 1kHz$ ,  
 Mode 7, OCL



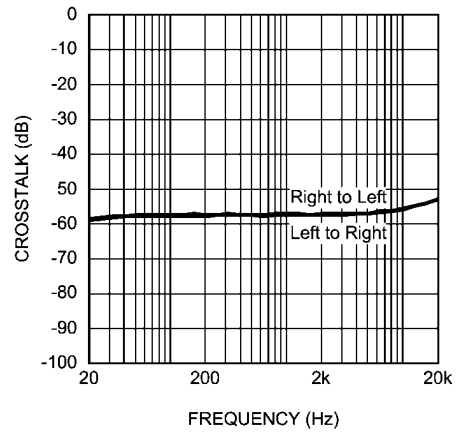
201628k7

**Power Dissipation vs Output Power**  
 $V_{DD} = 3.3V, R_L = 32\Omega, f = 1kHz,$   
**Mode 7, SE**



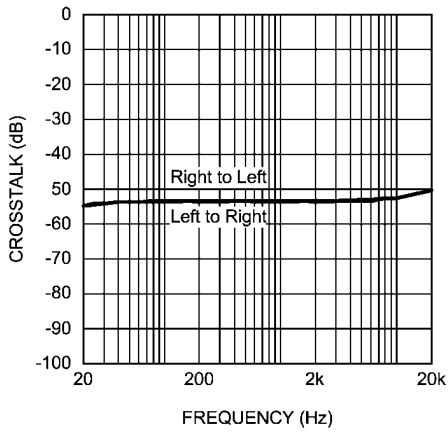
201628k9

**Crosstalk vs Frequency**  
 $V_{DD} = 3.3V, R_L = 32\Omega, P_O = 12mW$   
**Right-Left, Mode 4, OCL**



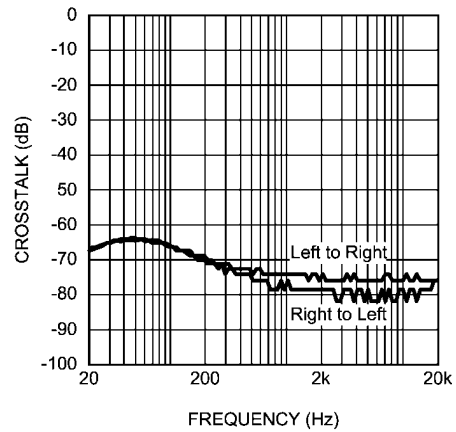
201628e9

**Crosstalk vs Frequency**  
 $V_{DD} = 5V, R_L = 32\Omega, P_O = 30mW$   
**Left-Right, Mode 4, OCL**



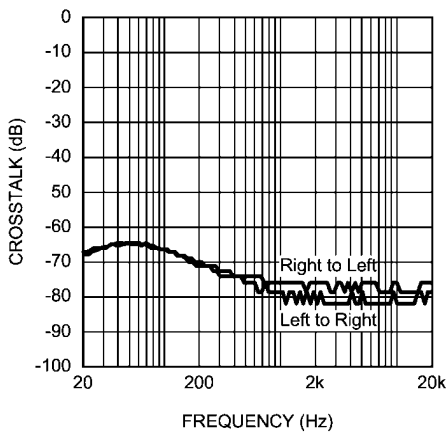
201628f1

**Crosstalk vs Frequency**  
 $V_{DD} = 3.3V, R_L = 32\Omega, P_O = 12mW$   
**Mode 4, SE**



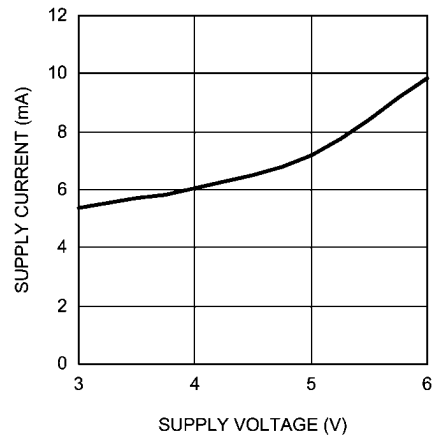
201628f0

**Crosstalk vs Frequency**  
 $V_{DD} = 5V, R_L = 32\Omega, P_O = 30mW$   
**Mode 4, SE**



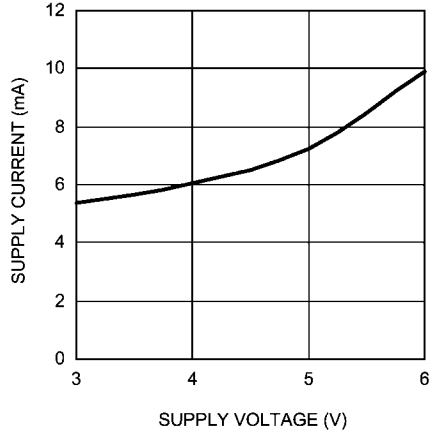
201628f2

**Supply Current vs Supply Voltage**  
**No Load, Mode 7**



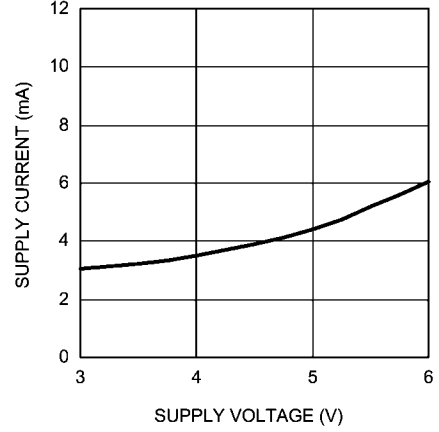
201628k2

**Supply Current vs Supply Voltage**  
 $V_{DD} = 3.3V$ , No Load, Modes 1, 3, 5



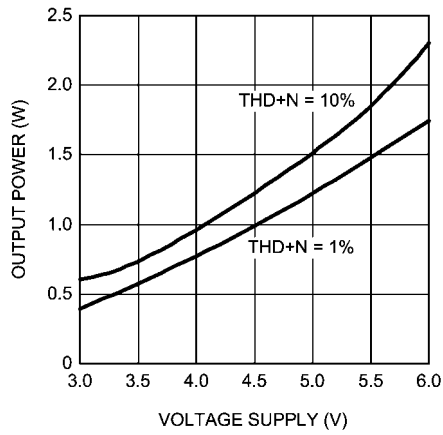
201628k3

**Supply Current vs Supply Voltage**  
 No Load, Modes 2, 4, 6



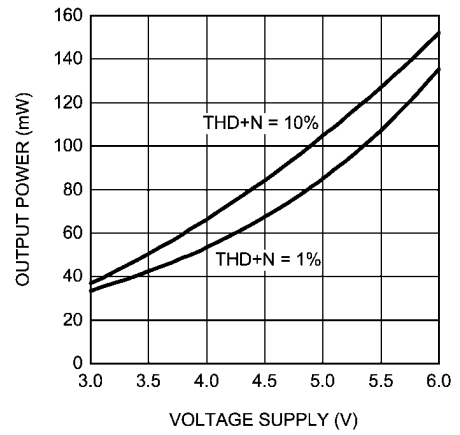
201628k4

**Output Power vs Supply Voltage**  
 $R_L = 8\Omega$ ,  $f = 1kHz$ , Mono, Mode 1



201628n0

**Output Power vs Supply Voltage**  
 $R_L = 32\Omega$ ,  $f = 1kHz$ , OCL, Mode 4



201628n1

## Application Information

### I<sup>2</sup>C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ID\_ENB: This is the address select input pin.

I<sup>2</sup>CSPI\_SEL: This is tied LOW for I<sup>2</sup>C mode.

### I<sup>2</sup>C COMPATIBLE INTERFACE

The LM4946 uses a serial bus which conforms to the I<sup>2</sup>C protocol to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The maximum clock frequency specified by the I<sup>2</sup>C standard is 400kHz. In this discussion, the master is the controlling microcontroller and the slave is the LM4946.

The I<sup>2</sup>C address for the LM4946 is determined using the ID\_ENB pin. The LM4946's two possible I<sup>2</sup>C chip addresses are of the form 111110X<sub>1</sub>0 (binary), where X<sub>1</sub> = 0, if ID\_ENB is logic LOW; and X<sub>1</sub> = 1, if ID\_ENB is logic HIGH. If the I<sup>2</sup>C interface is used to address a number of chips in a system, the LM4946's chip address can be changed to avoid any possible address conflicts.

The bus format for the I<sup>2</sup>C interface is shown in Figure 3. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is HIGH. The start signal will alert all devices attached to the I<sup>2</sup>C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is HIGH.

For I<sup>2</sup>C interface operation, the I<sup>2</sup>CSPI\_SEL pin needs to be tied LOW (and tied high for SPI operation).

After the last bit of the address bit is sent, the master releases the data line HIGH (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM4946 has received the address correctly, then it holds the data line LOW during the clock pulse. If the data line is not held LOW during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM4946.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable HIGH.

After the data byte is sent, the master must check for another acknowledge to see if the LM4946 received the data.

If the master has more data bytes to send to the LM4946, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes HIGH while the clock signal is HIGH. The data line should be held HIGH when not in use.

### I<sup>2</sup>C INTERFACE POWER SUPPLY PIN (I<sup>2</sup>CSPI\_V<sub>DD</sub>)

The LM4946's I<sup>2</sup>C interface is powered up through the I<sup>2</sup>CSPI\_V<sub>DD</sub> pin. The LM4946's I<sup>2</sup>C interface operates at a voltage level set by the I<sup>2</sup>CV<sub>DD</sub> pin which can be set independent to that of the main power supply pin V<sub>DD</sub>. This is ideal whenever logic levels for the I<sup>2</sup>C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

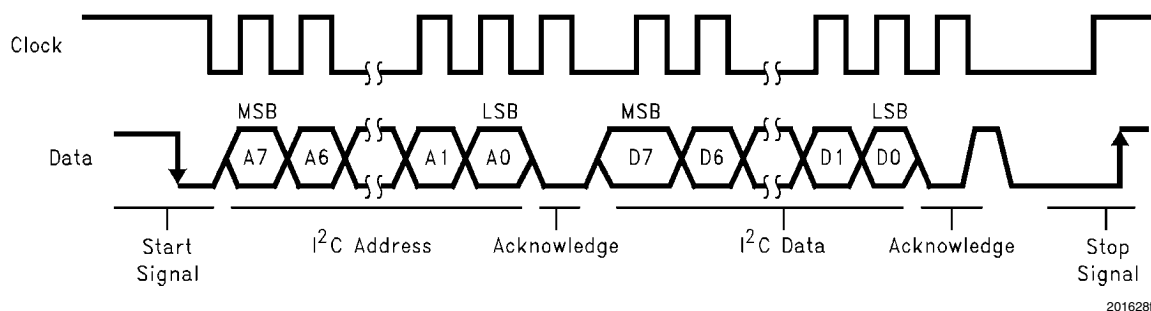
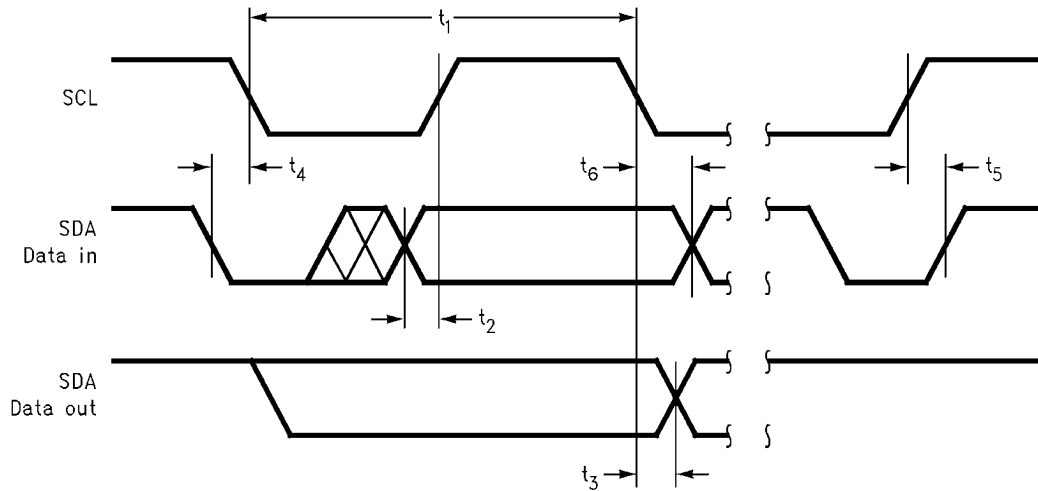


FIGURE 3. I<sup>2</sup>C Bus Format

20162815



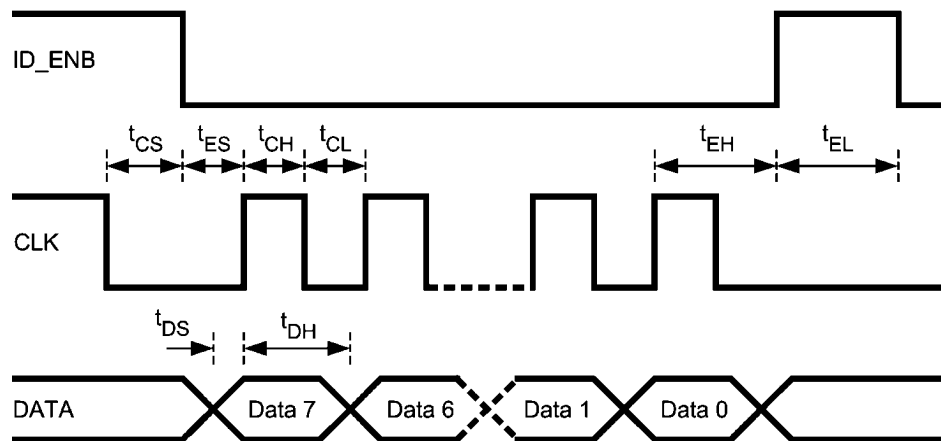
201628f4

FIGURE 4. I<sup>2</sup>C Timing Diagram**SPI DESCRIPTION**

(For  $2.2V \leq I^2CSPI\_V_{DD} \leq 5.5V$ , see page 9 for more information).

0. I<sup>2</sup>CSPI\_SEL: This pin is tied HIGH for SPI mode.
1. The data bits are transmitted with the MSB first.
2. The maximum clock rate is 1MHz for the CLK pin.
3. CLK must remain HIGH for at least 500ns ( $t_{CH}$ ) after the rising edge of CLK, and CLK must remain LOW for at least 500ns ( $t_{CL}$ ) after the falling edge of CLK.
4. The serial data bits are sampled at the rising edge of CLK. Any transition on DATA must occur at least 100ns ( $t_{DS}$ ) before the rising edge of CLK. Also, any transition on DATA must occur at least 100ns ( $t_{DH}$ ) after the rising edge of CLK and stabilize before the next rising edge of CLK.
5. ID\_ENB should be LOW only during serial data transmission.

6. ID\_ENB must be LOW at least 100ns ( $t_{ES}$ ) before the first rising edge of CLK, and ID\_ENB has to remain LOW at least 100ns ( $t_{EH}$ ) after the eighth rising edge of CLK.
7. If ID\_ENB remains HIGH for more than 100ns before all 8 bits are transmitted then the data latch will be aborted.
8. If ID\_ENB is LOW for more than 8 CLK pulses then only the first 8 data bits will be latched and activated when ID\_ENB transitions to logic-high.
9. ID\_ENB must remain HIGH for at least 100ns ( $t_{EL}$ ) to latch in the data.
10. Coincidental rising or falling edges of CLK and ID\_ENB are not allowed. If CLK is to be held HIGH after the data transmission, the falling edge of CLK must occur at least 100ns ( $t_{CS}$ ) before ID\_ENB transitions to LOW for the next set of data.



20162824

FIGURE 5. SPI Timing Diagram

TABLE 1. Chip Address

	A7	A6	A5	A4	A3	A2	A1	A0
Chip Address	1	1	1	1	1	0	EC	0
ID_ENB = 0	1	1	1	1	1	0	0	0
ID_ENB = 1	1	1	1	1	1	0	1	0

EC — Externally Controlled

TABLE 2. Control Registers

	D7	D6	D5	D4	D3	D2	D1	D0
Mode Control	0	0	0	0	OCL	MC2	MC1	MC0
Programmable 3D	0	1	0	0	N3D3	N3D2	N3D1	N3D0
Mono Volume Control	1	0	0	MVC4	MVC3	MVC2	MVC1	MVC0
Left Volume Control	1	1	0	LVC4	LVC3	LVC2	LVC1	LVC0
Right Volume Control	1	1	1	RVC4	RVC3	RVC2	RVC1	RVC0

1. Bits MVC0 — MVC4 control 32 step volume control for MONO input
2. Bits LVC0 — LVC4 control 32 step volume control for LEFT input
3. Bits RVC0 — RVC4 control 32 step volume control for RIGHT input
4. Bits MC0 — MC2 control 8 distinct modes
5. Bits N3D3, N3D2, N3D1, N3D0 control programmable 3D function
6. N3D0 turns the 3D function ON (N3D0 = 1) or OFF (N3D0 = 0), and N3D1 = 0 provides a "wider" aural effect or N3D1 = 1 a "narrower" aural effect
7. Bit OCL selects between SE with output capacitor (OCL = 0) or SE without output capacitors (OCL = 1). **Default is OCL = 0**

TABLE 3. Programmable National 3D Audio

	N3D3	N3D2
Low	0	0
Medium	0	1
High	1	0
Maximum	1	1

TABLE 4. Output Mode Selection

Output Mode Number	MC2	MC1	MC0	Handsfree Speaker Output	Right HP Output	Left HP Output
0	0	0	0	SD	SD	SD
1	0	0	1	$G_P \times P$	MUTE	MUTE
2	0	1	0	SD	$G_P \times P/2$	$G_P \times P/2$
3	0	1	1	$2 \times (G_L \times L + G_R \times R)$	MUTE	MUTE
4	1	0	0	SD	$G_R \times R$	$G_L \times L$
5	1	0	1	$2 \times (G_L \times L + G_R \times R) + G_P \times P$	MUTE	MUTE
6	1	1	0	SD	$G_R \times R + G_P \times P/2$	$G_L \times L + G_P \times P/2$
7	1	1	1	$2 \times (G_R \times R + G_L \times L)$	$G_R \times R$	$G_L \times L$

On initial POWER ON, the default mode is 000

P = Phone-in (Mono)

R =  $R_{IN}$ L =  $L_{IN}$ 

SD = Shutdown

MUTE = Mute Mode

 $G_P$  = Phone In (Mono) volume control gain $G_R$  = Right stereo volume control gain $G_L$  = Left stereo volume control gain



TABLE 5. Volume Control Table

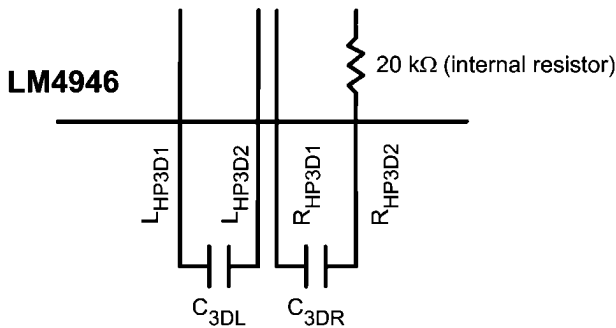
Volume Step	xVC4	xVC3	xVC2	xVC1	xVC0	Gain,dB
1	0	0	0	0	0	-54.00
2	0	0	0	0	1	-46.50
3	0	0	0	1	0	-40.50
4	0	0	0	1	1	-34.50
5	0	0	1	0	0	-30.00
6	0	0	1	0	1	-27.00
7	0	0	1	1	0	-24.00
8	0	0	1	1	1	-21.00
9	0	1	0	0	0	-18.00
10	0	1	0	0	1	-15.00
11	0	1	0	1	0	-13.50
12	0	1	0	1	1	-12.00
13	0	1	1	0	0	-10.50
14	0	1	1	0	1	-9.00
15	0	1	1	1	0	-7.50
16	0	1	1	1	1	-6.00
17	1	0	0	0	0	-4.50
18	1	0	0	0	1	-3.00
19	1	0	0	1	0	-1.50
20	1	0	0	1	1	0.00
21	1	0	1	0	0	1.50
22	1	0	1	0	1	3.00
23	1	0	1	1	0	4.50
24	1	0	1	1	1	6.00
25	1	1	0	0	0	7.50
26	1	1	0	0	1	9.00
27	1	1	0	1	0	10.50
28	1	1	0	1	1	12.00
29	1	1	1	0	0	13.50
30	1	1	1	0	1	15.00
31	1	1	1	1	0	16.50
32	1	1	1	1	1	18.00

1. x = M, L, or R
2. Gain / Attenuation is from input to output

**NATIONAL 3D ENHANCEMENT**

The LM4946 features a stereo headphone, 3D audio enhancement effect that widens the perceived soundstage from a stereo audio signal. The 3D audio enhancement creates a perceived spatial effect optimized for stereo headphone listening. The LM4946 can be programmed for a “narrow” or “wide” soundstage perception. The narrow soundstage has a more focused approaching sound direction, while the wide soundstage has a spatial, theater-like effect. Within each of these two modes, four discrete levels of 3D effect that can be programmed: low, medium, high, and maximum (Table 2, 3), each level with an ever increasing aural effect, respectively. The difference between each level is 3dB.

The external capacitors, shown in Figure 6, are required to enable the 3D effect. The value of the capacitors set the cutoff frequency of the 3D effect, as shown by Equations 1 and 2. Note that the internal 20kΩ resistor is nominal.



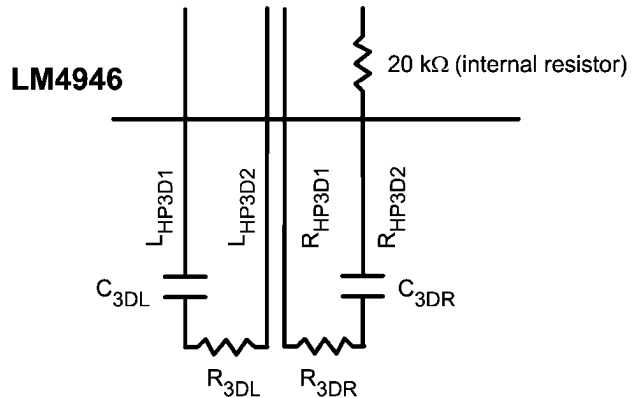
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**FIGURE 6. External 3D Effect Capacitors**

$$f_{3DL(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DL} \quad (1)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * 20k\Omega * C_{3DR} \quad (2)$$

Optional resistors  $R_{3DL}$  and  $R_{3DR}$  can also be added (Figure 7) to affect the -3dB frequency and 3D magnitude.



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**FIGURE 7. External RC Network with Optional  $R_{3DL}$  and  $R_{3DR}$  Resistors**

$$f_{3DL(-3dB)} = 1 / 2\pi * (20k\Omega + R_{3DL}) * C_{3DL} \quad (3)$$

$$f_{3DR(-3dB)} = 1 / 2\pi * (20k\Omega + R_{3DR}) * C_{3DR} \quad (4)$$

$\Delta AV$  (change in AC gain) =  $1 / 1 + M$ , where M represents some ratio of the nominal internal resistor, 20kΩ (see example below).

$$f_{3dB(3D)} = 1 / 2\pi (1 + M)(20k\Omega * C_{3D}) \quad (5)$$

$$C_{Equivalent(new)} = C_{3D} / 1 + M \quad (6)$$

**TABLE 6. Pole Locations**

$R_{3D}$ (kΩ) (optional)	$C_{3D}$ (nF)	M	$\Delta AV$ (dB)	f-3dB (3D) (Hz)	Value of $C_{3D}$ to keep same pole location (nF)	new Pole Location (Hz)
0	68	0	0	117		
1	68	0.05	-0.4	111	64.8	117
5	68	0.25	-1.9	94	54.4	117
10	68	0.50	-3.5	78	45.3	117
20	68	1.00	-6.0	59	34.0	117

## PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 8Ω LOAD

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by an 8Ω load from 158.3mW to 156.4mW. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

### BRIDGE CONFIGURATION EXPLANATION

The LM4946 drives a load, such as a speaker, connected between outputs, MONO+ and MONO-.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between MONO- and MONO+ and driven differentially (commonly referred to as "bridge mode"). This results in a differential or BTL gain of:

$$A_{VD} = 2(R_f / R_i) = 2 \quad (7)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing MONO- and MONO+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

### POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM4946 has a pair of bridged-tied amplifiers driving a handsfree speaker, MONO. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation (8), assuming a 5V power

supply and an 8Ω load, the maximum MONO power dissipation is 634mW.

$$P_{\text{DMAX-SPKROUT}} = 4(V_{\text{DD}})^2 / (2\pi^2 R_L): \text{Bridge Mode} \quad (8)$$

The LM4946 also has a pair of single-ended amplifiers driving stereo headphones, R<sub>OUT</sub> and L<sub>OUT</sub>. The maximum internal power dissipation for R<sub>OUT</sub> and L<sub>OUT</sub> is given by equation (9) and (10). From Equations (9) and (10), assuming a 5V power supply and a 32Ω load, the maximum power dissipation for L<sub>OUT</sub> and R<sub>OUT</sub> is 40mW, or 80mW total.

$$P_{\text{DMAX-LOUT}} = (V_{\text{DD}})^2 / (2\pi^2 R_L): \text{Single-ended Mode} \quad (9)$$

$$P_{\text{DMAX-ROUT}} = (V_{\text{DD}})^2 / (2\pi^2 R_L): \text{Single-ended Mode} \quad (10)$$

The maximum internal power dissipation of the LM4946 occurs when all three amplifiers pairs are simultaneously on; and is given by Equation (11).

$$P_{\text{DMAX-TOTAL}} = P_{\text{DMAX-SPKROUT}} + P_{\text{DMAX-LOUT}} + P_{\text{DMAX-ROUT}} \quad (11)$$

The maximum power dissipation point given by Equation (11) must not exceed the power dissipation given by Equation (12):

$$P_{\text{DMAX}} = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}} \quad (12)$$

The LM4946's T<sub>JMAX</sub> = 150°C. In the SQ package, the LM4946's θ<sub>JA</sub> is 46°C/W. At any given ambient temperature T<sub>A</sub>, use Equation (12) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (12) and substituting P<sub>DMAX-TOTAL</sub> for P<sub>DMAX</sub> results in Equation (13). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM4946's maximum junction temperature.

$$T_A = T_{\text{JMAX}} - P_{\text{DMAX-TOTAL}} \theta_{\text{JA}} \quad (13)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum mono power dissipation without exceeding the maximum junction temperature is approximately 121°C for the SQ package.

$$T_{\text{JMAX}} = P_{\text{DMAX-TOTAL}} \theta_{\text{JA}} + T_A \quad (14)$$

Equation (14) gives the maximum junction temperature T<sub>JMAX</sub>. If the result violates the LM4946's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation (11) is greater than that of Equation (12), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ<sub>JA</sub>. The heat sink can be created using additional copper area around the package, with connections to

the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the  $\theta_{JA}$  is the sum of  $\theta_{JC}$ ,  $\theta_{CS}$ , and  $\theta_{SA}$ . ( $\theta_{JC}$  is the junction-to-case thermal impedance,  $\theta_{CS}$  is the case-to-sink thermal impedance, and  $\theta_{SA}$  is the sink-to-ambient thermal impedance). Refer to the Typical Performance Characteristics curves for power dissipation information at lower output power levels.

#### POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a  $1\mu\text{F}$  in parallel with a  $0.1\mu\text{F}$  filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local  $1.0\mu\text{F}$  tantalum bypass capacitor and a parallel  $0.1\mu\text{F}$  ceramic capacitor connected between the LM4946's supply pin and ground. Keep the length of leads and traces that connect capacitors between the LM4946's power supply pin and ground as short as possible.

#### SELECTING EXTERNAL COMPONENTS

##### Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor ( $C_i$  in Figures 1 & 2). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz.

Applications using speakers with this limited frequency response reap little improvement by using large input capacitor. The internal input resistor ( $R_i$ ), minimum  $10\text{k}\Omega$ , and the input capacitor ( $C_i$ ) produce a high pass filter cutoff frequency that is found using Equation (15).

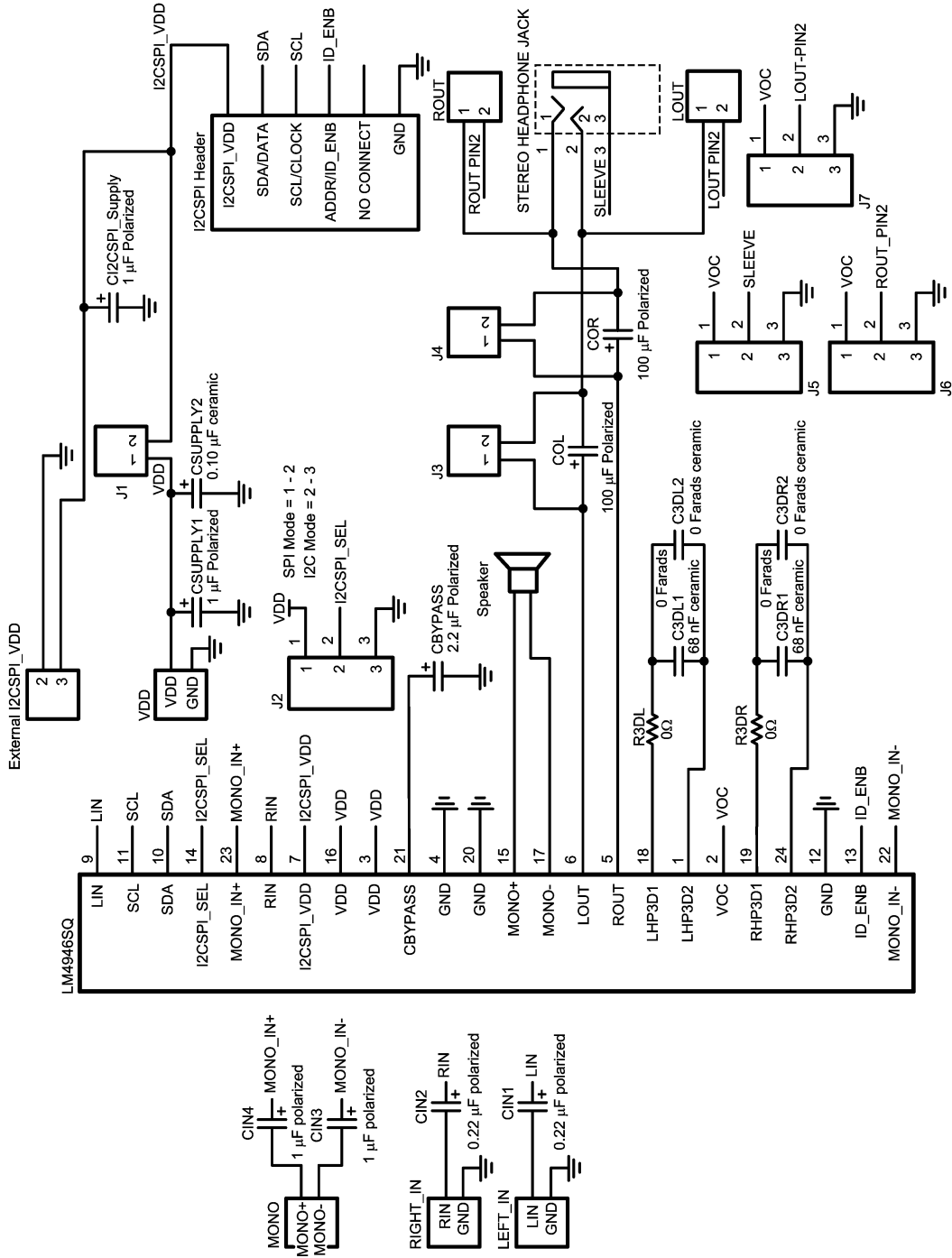
$$f_c = 1 / (2\pi R_i C_i) \quad (15)$$

As an example when using a speaker with a low frequency limit of 150Hz,  $C_i$ , using Equation (15) is  $0.106\mu\text{F}$ . The  $0.22\mu\text{F}$   $C_i$  shown in *Figure 1* allows the LM4946 to drive high efficiency, full range speaker whose response extends below 40Hz.

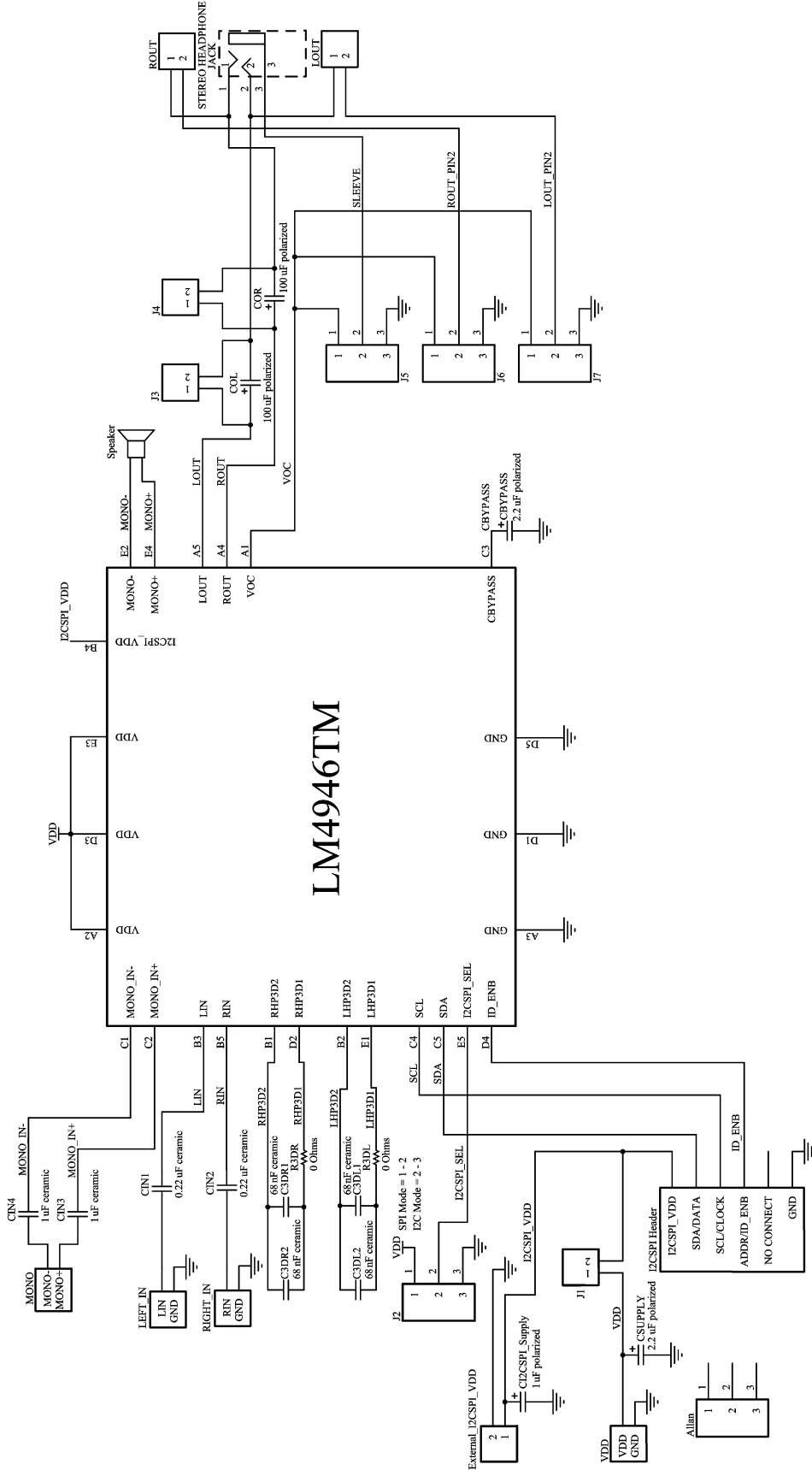
##### Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of  $C_B$ , the capacitor connected to the BYPASS pin. Since  $C_B$  determines how fast the LM4946 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4946's outputs ramp to their quiescent DC voltage (nominally  $V_{DD}/2$ ), the smaller the turn-on pop. Choosing  $C_B$  equal to  $2.2\mu\text{F}$  along with a small value of  $C_i$  (in the range of  $0.1\mu\text{F}$  to  $0.33\mu\text{F}$ ), produces a click-less and pop-less shutdown function. As discussed above, choosing  $C_i$  no larger than necessary for the desired bandwidth helps minimize clicks and pops.  $C_B$ 's value should be in the range of 7 to 10 times the value of  $C_i$ . This ensures that output transients are eliminated when power is first applied or the LM4946 resumes operation after shutdown.

# Demo Board Schematic Diagram



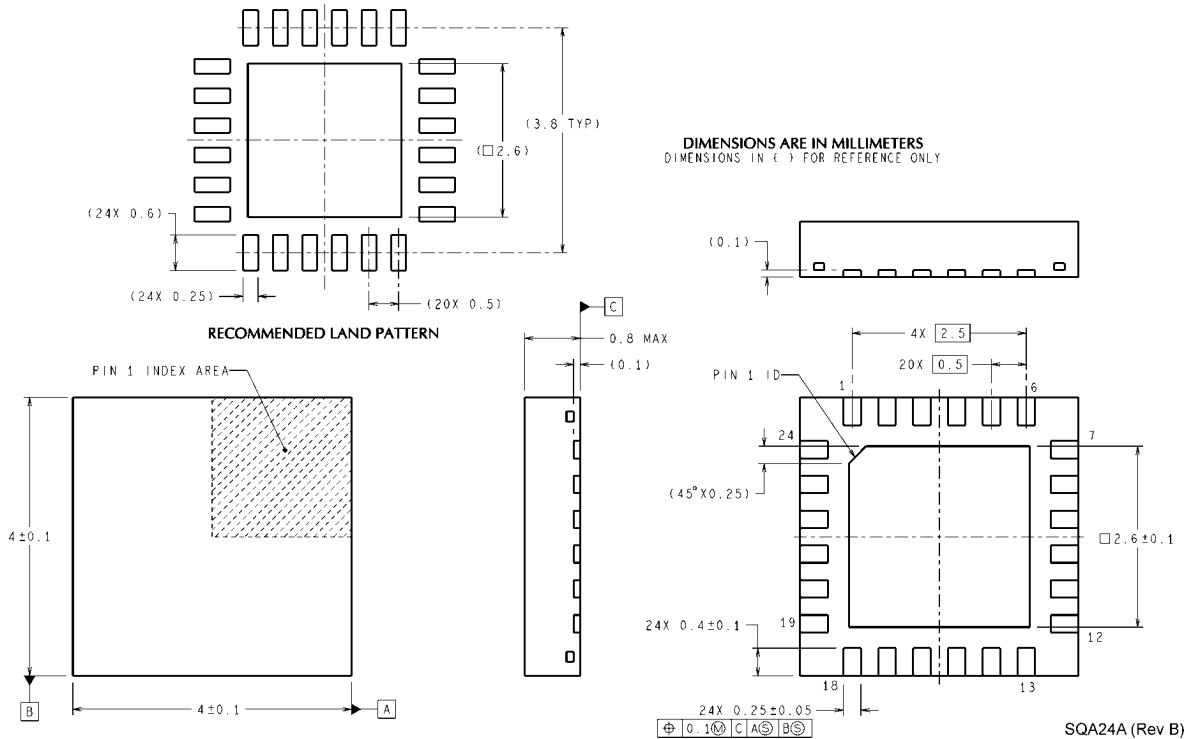
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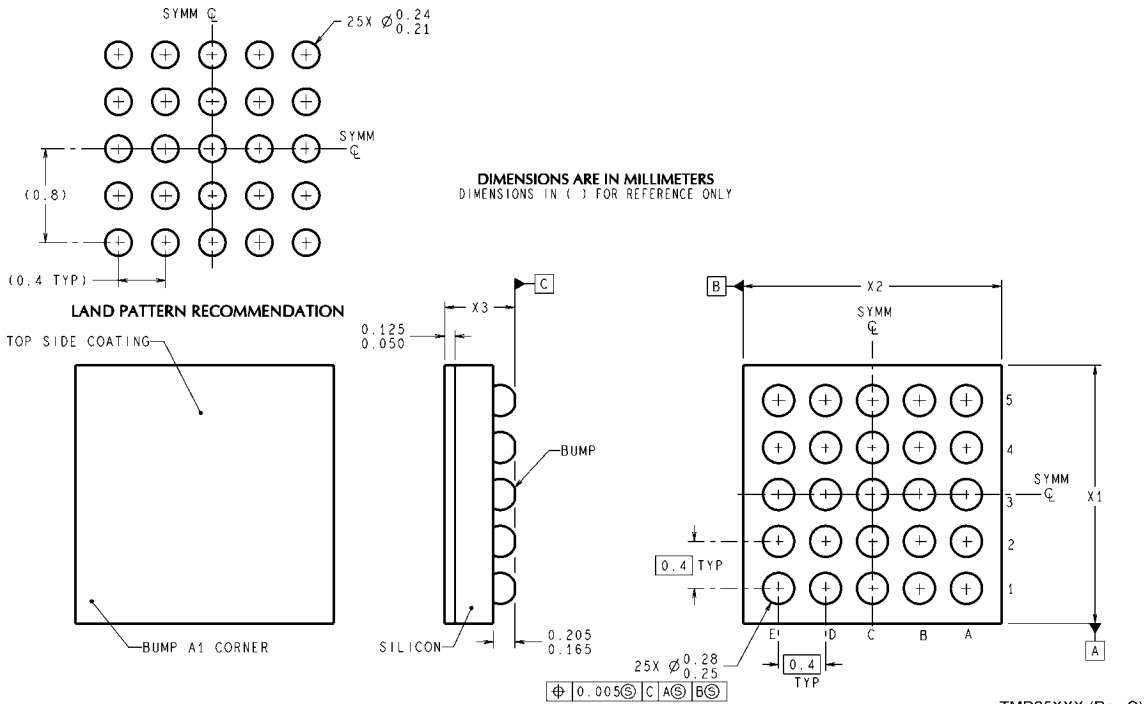
## Revision History

Rev	Date	Description
1.0	01/23/06	Initial release.
1.1	03/05/07	Added the TMD25XXX package.
1.2	03/13/07	Edited the 25-pin micro SMD connection diagram.
1.3	04/24/07	Added the I2C/SPI (1.7V 2.2V) table.
1.4	04/26/07	Added the numerical values for the X1, X2, and X3 in the Physical Dimension section.
1.5	05/02/07	Text edits. Added the TM package.
1.6	05/15/07	Added the TM board schematic and input some text edits.
1.7	05/16/07	More text edits.
1.8	06/06/07	Added Note 11 and more text edits.
1.9	07/31/07	Edited the 5.0V EC table (MONO_IN Input Impedance and Rin/Lin Input Impedance).

**Physical Dimensions** inches (millimeters) unless otherwise noted



**24 Lead LLP Package**  
**Order Number LM4946SQ**  
**NS Package Number SQA24A**  
**Dimensions are in millimeters**  
 $X_1 = 4 \pm 0.1$   $X_2 = 4 \pm 0.1$   $X_3 = 0.8 \pm 0.1$



**25 Bump micro SMD Package**  
**Order Number LM4946TM**  
**NS Package Number TMD25ABA**  
 $X_1 = 2015\mu\text{m}$ ,  $X_2 = 2047\mu\text{m}$ ,  $X_3 = 600\mu\text{m}$



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