LMV1099

LMV1099 Uplink Far Field Noise Suppression & Downlink SNR Enhancing Microphone Amplifier with Earpiece Driver

Texas Instruments

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General Description

The LMV1099 is an uplink and downlink voice intelligibility enhancing analog IC, ideally suited for mobile handsets. Uplink voice intelligibility is improved by rejecting far-field noise through a unique two-microphone solution. Downlink voice intelligibility is improved by enhancing the SNR (Signal-to-Noise Ratio) between the downlink voice and the ambient noise environment at the user's earpiece.

The LMV1099 preserves uplink near-field voice signals within close range of the microphones while rejecting far-field acoustic noise greater than 0.5m from the microphones.

The LMV1099 also enhances downlink voice intelligibility by improving near-field SNR based on the user's environment. The analog circuitry adapts dynamically to both the user's ambient noise environment as well as the downlink signal amplitude to ensure optimum SNRI (signal-to-noise ratio improvement). The downlink path also provides uplink noise attenuation through an adjustable high pass filter before the SNR enhanced downlink voice reaches the user's earpiece.

Unlike digital-based noise reduction solutions, the all-analog low power consuming LMV1099 increases both uplink and downlink voice intelligibility without DSP-type artifacts, distortions or processing delays.

Key Specifications

■ Uplink Far Field Noise Suppression (Electrical $FFNS_E$ at f = 1kHz)	33dB (typ)
■ Near-Field SNR Enhancement	6 to 18dB (typ)
■ Downlink $SNRI_E$	16dB (typ)
■ Supply voltage range	2.7V to 5.5V
■ Supply current (V_{DD} = 3.6V)	3.8mA (typ)
■ Shutdown current	0.06μA (typ)
■ Uplink PSRR (f = 217Hz)	106dB (typ)
■ Downlink SNR (A-weighted)	102dB (typ)
■ Downlink THD+N	0.03% (typ)
■ Earpiece output power (R_L = 32Ω)	83mW (typ)

Features

- Noise reduction without DSP-type artifacts.
- Adapting AGC (Automatic Gain Control) on ambient noise level & downlink signal strength
- Downlink adjustable noise-reducing high pass filter
- Separate Uplink & Downlink Enable Functions
- No added process delays
- Low power consumption
- Shutdown function
- Maximum AGC Limiter
- Differential inputs & outputs for noise immunity
- Earpiece amplifier
- Available in a 25-bump micro SMD

Applications

- Mobile Handsets
- Mobile and handheld two-way radios
- Bluetooth and other power headsets

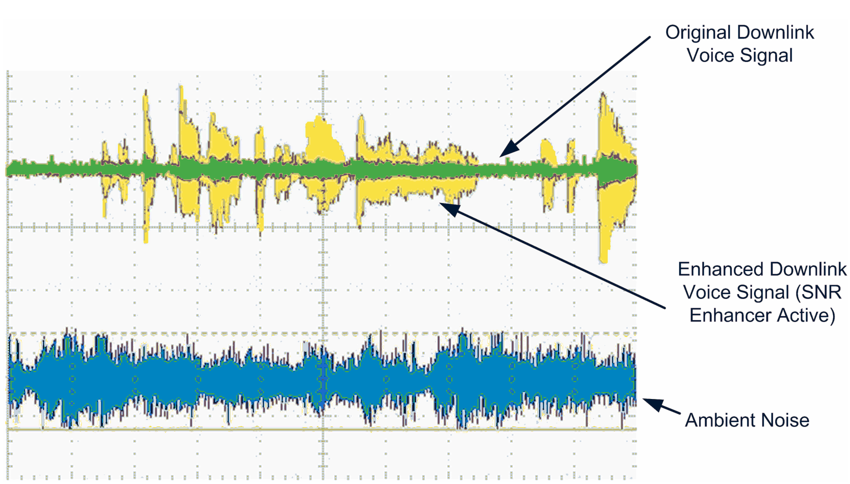
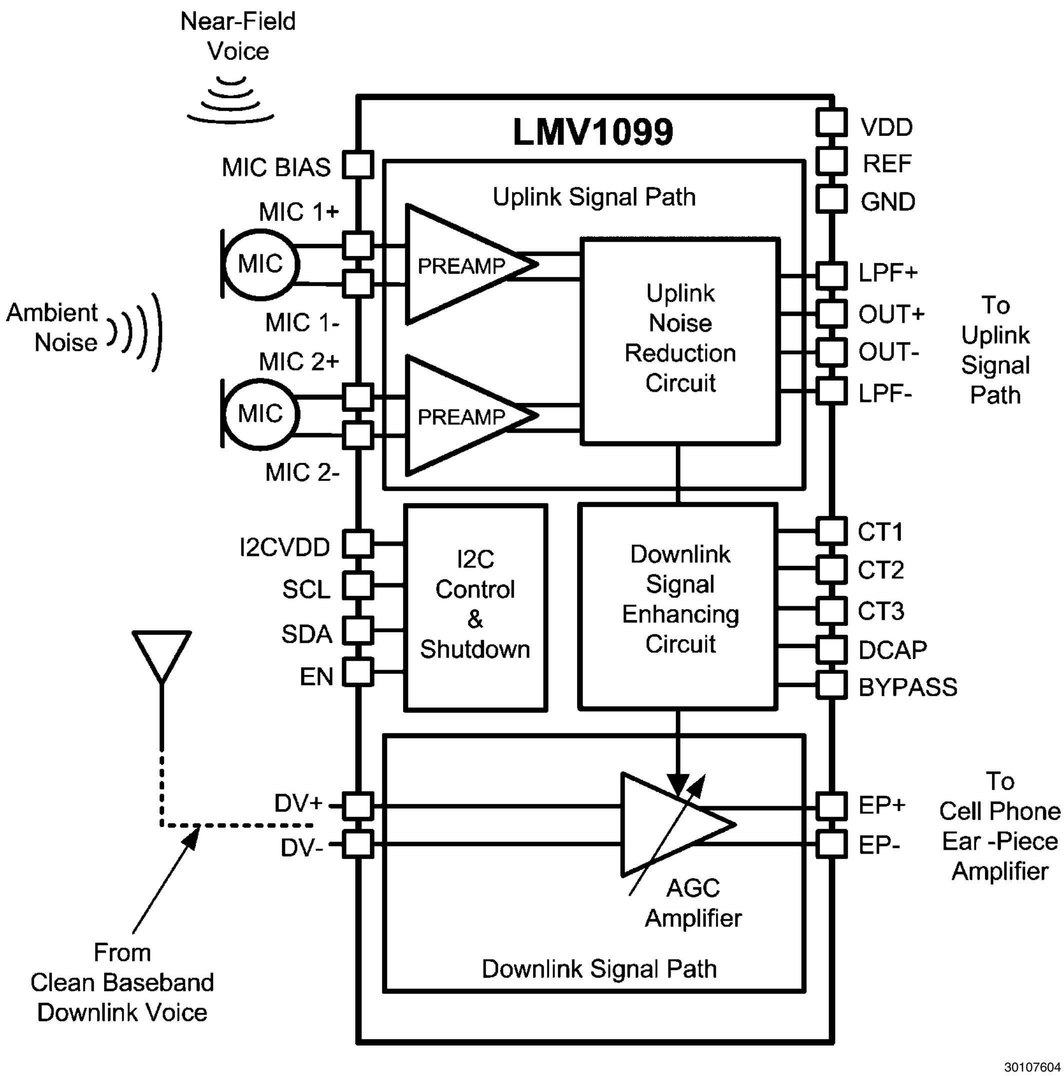


FIGURE 1. Voice Enhanced Signal

Block Diagram



Typical Application

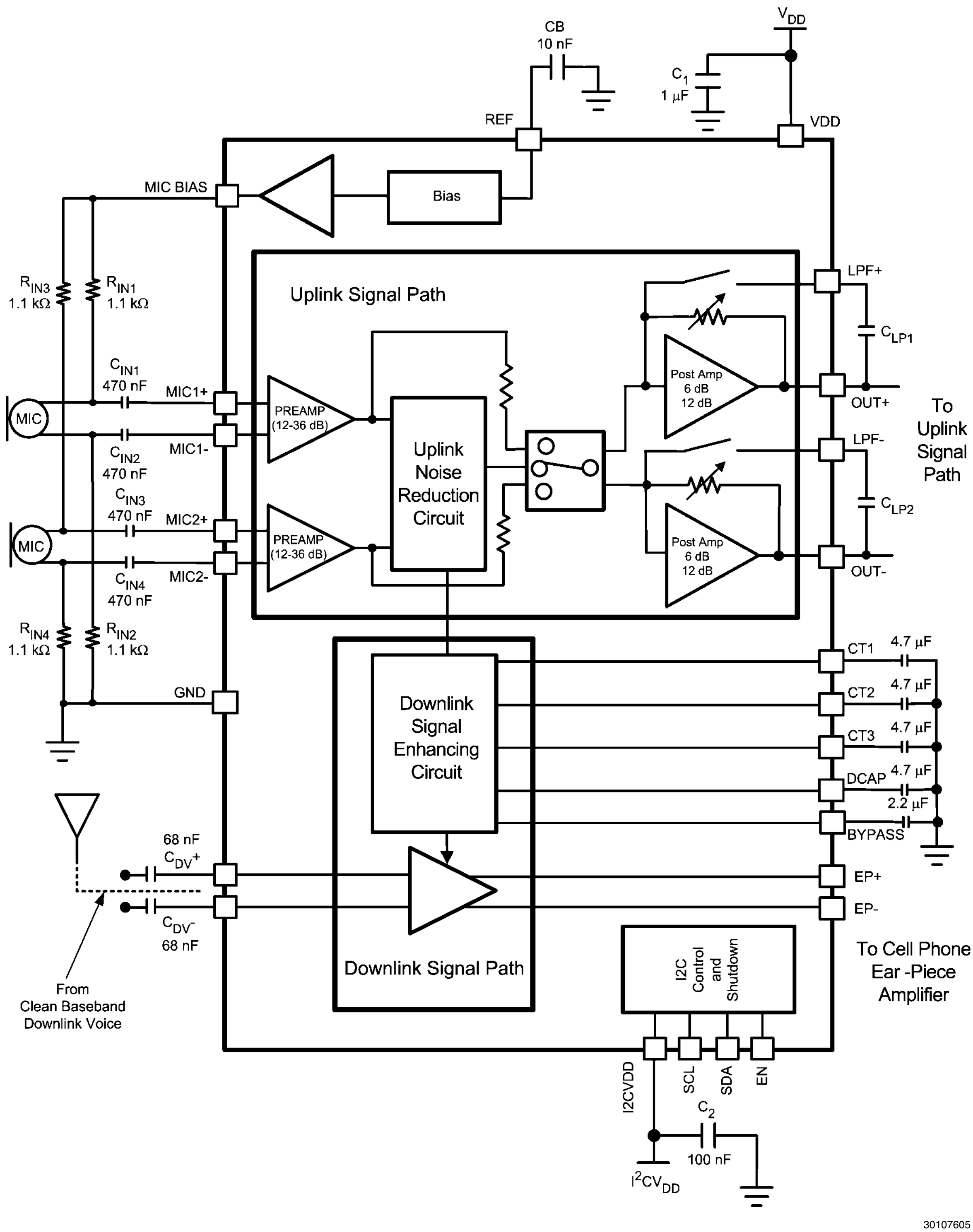
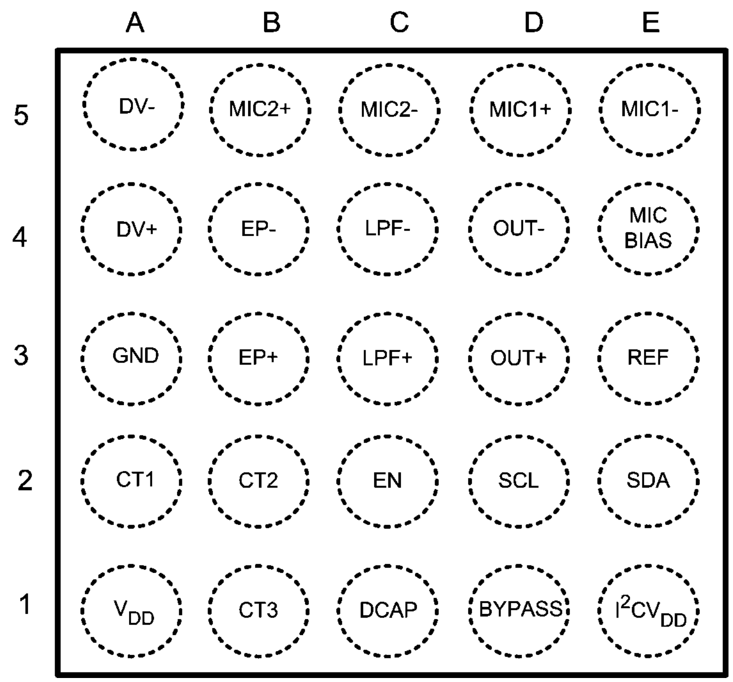


FIGURE 2. Typical Application Circuit Diagram

Connection Diagrams

25 – Bump micro SMD package



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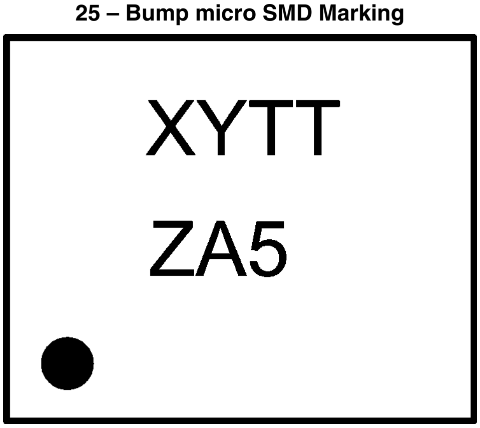
Top View
Order Number LMV1099TL
See NS Package Number TLA25GMA

25 – Bump micro SMD Marking



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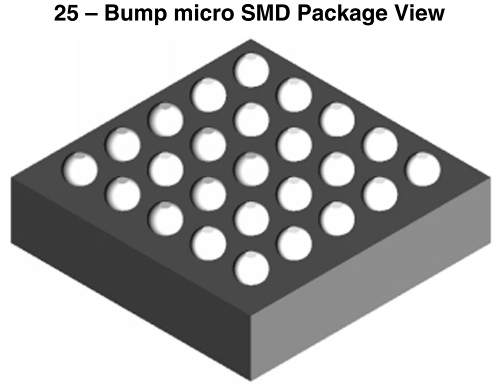
Top View
X = Plant Code
Y = Date Code
TT = Die Traceability
ZA5 = LMV1099TL

25 – Bump micro SMD Package View



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Bottom View
Order Number LMV1099TL
See NS Package Number TLA25GMA

Ordering Information

Order Number	Package	Package Drawing Number	Device Marking	Transport Media
LMV1099TL	25 Bump microSMD	TLA25GMA	XYTTZA5	250 TNR
LMV1099TLX	25 Bump microSMD	TLA25GMA	XYTTZA5	3k TNR

Pin Descriptions

TABLE 1. Pin Name and Function

PIN	NAME	TYPE	UPLINK PIN DESCRIPTIONS
D5	MIC1+	Analog Input	Uplink Voice Positive Microphone #1 Input
E5	MIC1-	Analog Input	Uplink Voice Negative Microphone #1 Input
B5	MIC2+	Analog Input	Uplink Voice Positive Microphone #2 Input
C5	MIC2-	Analog Input	Uplink Voice Negative Microphone #2 Input
E4	MIC BIAS	Analog Output	Microphone DC Bias Voltage Output
E3	REF	Analog Ref	Microphone Reference Bypass Pin
D3	OUT+	Analog Output	Uplink Positive Output (To Baseband Chipset)
C3	LPF+	Analog Input	Uplink-Output Low Pass Filter Positive Feedback Input
D4	OUT-	Analog Output	Uplink Negative Output (To Baseband Chipset)
C4	LPF-	Analog Input	Uplink-Output Low Pass Filter Negative Feedback Input
PIN	**NAME**	**TYPE**	**DOWNLINK PIN DESCRIPTIONS**
A4	DV+	Analog Input	Downlink Voice Positive Input
A5	DV-	Analog Input	Downlink Voice Negative Input
A2	CT1	Analog Ref	Control Signal Timing Capacitor
B2	CT2	Analog Ref	Control Signal Timing Capacitor
B1	CT3	Analog Ref	Control Signal Timing Capacitor
A3	GND	Ground	Power Supply Ground Pin
D1	Bypass	Analog Ref	Earpiece Reference Bypass Pin
B3	EP+	Analog Output	Ear Speaker Positive Output (To Ear Piece Speaker)
B4	EP-	Analog Output	Ear Speaker Negative Output (To Ear Piece Speaker)
PIN	**NAME**	**TYPE**	**DIGITAL INTERFACE & SUPPLY PIN DESCRIPTIONS**
D2	SCL	Digital Input	I²C Serial Clock Digital Input
C2	EN	Digital Input	I²C Chip Enable Digital Input
E2	SDA	Digital I/O	I²C Serial Data Address Digital Input/Output Pin
E1	I^2CV_{DD}	Digital Supply	I²C Digital Supply Voltage Pin
A1	V_{DD}	Supply	Power Supply Voltage Pin
C1	DCAP	Analog Ref	Voice Signal Detection Capacitor

Note: Pin assignment subject to change.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	6.0V
Storage Temperature	-85°C to +150°C
ESD Rating (HBM) (Note 4)	2000V
ESD Rating (MM) (Note 5)	200V
ESD Rating (CDM) (Note 6)	750V
Junction Temperature (T_{JMAX})	150°C
Mounting Temperature Infrared or Convection (20 sec.)	235°C

Thermal Resistance

θ_{JA} (microSMD) (Note 3)	70°C/W

Soldering Information

See AN-112 "microSMD Wafers Level Chip Scale Package."

Operating Ratings (Note 1)

Supply Voltage	$2.7V \le V_{DD} \le 5.5V$
I^2CV_{DD}	$1.7V \le I^2CV_{DD} \le 5.5V$ $I^2CV_{DD} \le V_{DD}$
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$

Electrical Characteristics V_{DD} = 3.6V (Note 2)

Unless otherwise specified, all limits guaranteed for T_A = 25°C, V_{DD} = 3.6V, EN = V_{DD}. For Uplink tests, unless otherwise specified, preamplifier gain = 20dB, post amplifier gain = 6dB, V_{IN} = 18mV_{P-P}, f = 1kHz, R_L = 100kΩ, C_L = 4.7pF and in pass-through mode. For Downlink tests, unless otherwise specified, f = 1kHz, R_L = 32Ω, AGC_{AV} = 0dB.

Symbol	Parameter	Conditions	LMV1099 Typical (Note 7)	LMV1099 Limit (Note 8)	Units (Limits)
		GENERAL SPECIFICATIONS			
I_{DDQ}	Supply Quiescent Current	V_{IN} = 0V	3.8	4.5	mA (max)
I_{SD}	Shutdown Current	EN pin is Low	0.06	1	μA (max)
T_{ON}	IC Wake-up Time		27	40	ms (max)
V_{IH}	Logic High Input Threshold	EN, SCL, SDA		$0.7xI^2CV_{DD}$	V (min)
V_{IL}	Logic Low Input Threshold	EN, SCL, SDA		$0.3xI^2CV_{DD}$	V (max)
		UPLINK SPECIFICATIONS			
$FFNS_E$	Far Field Noise Suppression (Electrical)	f = 1kHz (See Test Method) f = 300Hz (See Test Method)	33 42	27.5	dB (min) dB (min)
$SNRI_E$	Signal-to-Noise Ratio Improvement (Electrical)	f = 1khz (See Test Method) f = 300Hz (See Test Method)	25 33	19.5	dB (min) dB (min)
V_{IN}	Maximum Input Signal	THD+N < 1%, Pre Amp Gain = 12dB	435	395	mV_{PP} (min)
V_{OUT}	Maximum AC Output Voltage	Differential Output, f = 1kHz THD+N < 1%	1.25	1.10	V_{RMS} (min)
	DC Level at Outputs	V_{IN} = GND	825		mV
V_{OS}	Output Offset Voltage	$V_{IN(Mic1/Mic2)}$ = 0V, Input Referred	0.7	5.0	mV (max)
THD+N	Total Harmonic Distortion + Noise	Differential Output	0.1	0.3	% (max)
FR	Frequency Response	30Hz – 12kHz (without Filter)	±0.5		dB
SNR	Signal-to-Noise Ratio	V_{IN} = 18mV_{P-P}, A-Weighted, audio band	65		dB
e_N	Input Referred Noise level	A-Weighted	7		μV_{RMS}
Z_{IN}	Input Impedance		150	127 173	kΩ (min) kΩ max)
Z_{OUT}	Output Impedance		235		Ω
Z_{LOAD}	Allowable Load Impedance	R_{LOAD} C_{LOAD}		10 100	kΩ (min) pF (max)
A_M	Microphone Pre Amplifier Gain Range	Minimum setting Maximum setting	12 36		dB
A_{MR}	Microphone Pre Amplifier Gain Resolution		2	1.7 2.3	dB (min) dB (max)
A_P	Post Amplifier Gain Range	Minimum setting Maximum setting	6 12		dB
A_{PR}	Post Amplifier Gain Resolution		6.0	5.8 6.2	dB (min) dB (max)

Symbol	Parameter	Conditions	LMV1099 Typical (Note 7)	LMV1099 Limit (Note 8)	Units (Limits)
PSRR	Power Supply Rejection Ratio	Input Referred, Input AC Grounded (470nF)			
		f = 217Hz, V_{RIPPLE} = 200mV_{PP}	106	92	dB (min)
		f = 1kHz, V_{RIPPLE} = 200mV_{PP}	102	91	dB (min)
CMRR	Common Mode Rejection Ratio	Input referred	60		dB
V_{BM}	Microphone Bias Supply Voltage	I_{BM} = 1mA	2.0	1.85 2.15	V (max) V (min)
e_{VBM}	Microphone Bias Supply Noise	A-Weighted, C_B = 10nF	5.5		μV_{RMS}
I_{BMAX}	Maximum Microphone Reference Output Current			1.2	mA (max)
DOWNLINK SPECIFICATIONS					
$V_{IN(DV)}$	Maximum Input Signal (Differential)	THD+N < 1%, AGC_{AV} = 0dB	4.7	4.1	$V_{PP(DIFF)}$ (min)
V_{OS}	Output Offset Voltage	$V_{IN(DV)}$ = 0V, R_L = 32Ω, Input Referred	0.7	5.0	mV (max)
e_N	Output Noise level	A-Weighted, $V_{IN(DV)}$ = 0V, AGC_{AV} = 0dB	8.9		μV_{RMS}
SNR	Downlink Signal-to-Noise Ratio	P_O = 35mW, A-Weighted	102		dB
P_{OUT}	Output Power	THD+N<1%, f = 1kHz, R_L = 32Ω	83	65	mW (min)
V_{LIMIT}	Output Voltage Limit	PLEV = 0	3.6		V_{P-P}
		PLEV = 1	4.1		V_{P-P}
THD+N	Total Harmonic Distortion + Noise	f = 1kHz, P_O = 35mW, R_L = 32Ω	0.03	0.05	% (max)
FR	Frequency Response	30Hz – 17kHz (without Filter)	±0.5		dB
PSRR	Power Supply Rejection Ratio	Input AC Grounded (68nF)			
		f = 217Hz, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω	93	82	dB (min)
		f = 1kHz, V_{RIPPLE} = 200mV_{P-P}, R_L = 32Ω	92	81	dB (min)
CMRR	Common Mode Rejection Ratio	V_{IN} = 200mV_{P-P}, f = 217Hz, R_L = 32Ω	50		dB
		V_{IN} = 200mV_{P-P}, f = 1kHz, R_L = 32Ω	60		dB
ZIN(DL)	Downlink Input Impedance	(See Register Map, *Table 7*)	6.5 9.5 57		kΩ kΩ kΩ
SNR ENHANCEMENT SPECIFICATIONS					
AGC_{AV}	Automatic Gain Control Range	Minimum setting Maximum setting	0 18		dB
ΔAGC_{AV}	0dB Gain Accuracy	AGC_{AV} = 0dB, f = 1kHz, V_{DV} = 1V, V_{AN}= 0V	±0.05		dB
$SNRI_E$	Signal-To-Noise Ratio Improvement (Electrical)*	f_{DV} = f_{AN} = 300Hz			
		V_{DV} = 100mV_{P-P}, V_{AN}= 0.8mV_{P-P}	6		dB
		V_{DV} = 100mV_{P-P}, V_{AN} = 2mV_{P-P}	16		dB
		f_{DV} = f_{AN} = 1kHz			
		V_{DV} = 100mV_{P-P}, V_{AN} = 1.4mV_{P-P}	12		dB (min)
		V_{DV} = 100mV_{P-P}, V_{AN} = 2mV_{P-P}	16		dB (min)

* f_{DV} = Frequency of Downlink signal
f_{AN} = Frequency of Ambient Noise signal
V_{DV} = Voltage swing of Downlink signal
V_{AN} = Voltage swing of Ambient signal

I²C Interface Characteristics V_{DD} = 3.3V, 1.8V ≤ I^2CV_{DD} ≤ 5.5V (Note 1, Note 2)

The following specifications apply for LS and HP VOLUMEGAIN = 0dB LSGAIN = 12B, HPGAIN = 0dB, EPGAIN = 0dB, R_L = 8Ω +30μH (Loudspeaker), R_L = 32Ω (Headphone), R_L = 32Ω (Earpiece), CSET = 0.1μF, ALC disabled, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C. (Note 7).

Symbol	Parameter	Conditions	LMV1099		Units (Limits)
			Typical	Limits (Note 7)	
t_1	SCL Period			2.5	μs (min)
t_2	SDA Setup Time			250	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			250	ns (min)
t_5	Stop Condition Time			250	ns (min)
t_6	SDA Data Hold Time			250	ns (min)
V_{IH}	Input High Voltage			$0.7xI^2CV_{DD}$	V (min)
V_{IL}	Input Low Voltage			$0.3xI^2CV_{DD}$	V (max)

Note 1: "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum* Ratings or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: *The Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

Note 3: The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JC}, and the ambient temperature T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} – T_A) / \theta_{JA}$ or the number given in the *Absolute Maximum Ratings*, whichever is lower.

Note 4: Human body model, applicable std. JESD22-A114C.

Note 5: Machine model, applicable std. JESD22-A115-A.

Note 6: Charge device model, applicable std. JESD22-C101D.

Note 7: Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

Note 8: Datasheet min/max specification limits are guaranteed by test or statistical analysis.

Test Methods

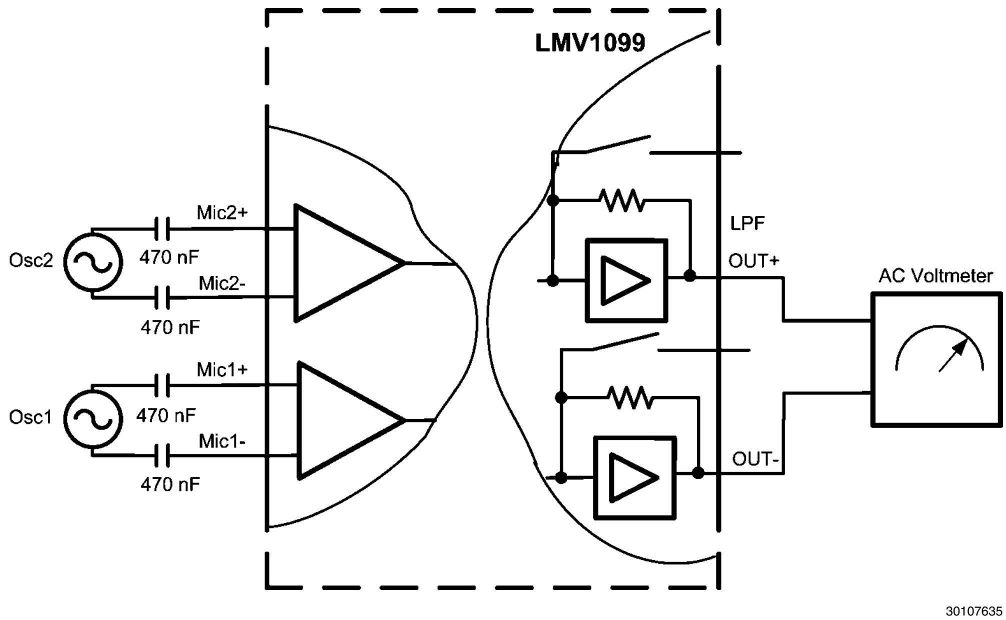


FIGURE 3. $FFNS_E$, $NFSL_E$, $SNRI_E$ Test Circuit

FAR FIELD NOISE SUPPRESSION ($FFNS_E$)

For optimum noise suppression the far field noise should be in a broadside array configuration from the two microphones, see *Figure 10*. Which means the far field sound source is equidistance from the two microphones. This configuration allows the amplitude of the far field signal to be equal at the two microphone inputs, however a slight phase difference may still exist. To simulate a real world application a slight phase delay was added to the $FFNS_E$ test. The block diagram from Figure 3 is used with the following procedure to measure the $FFNS_E$.

1. A sine wave with equal frequency and amplitude ($25mV_{P-P}$) is applied to Mic1 and Mic2. Using a signal generator, the phase of Mic 2 is delayed by 1.1° for 1kHz, or 0.33° for 300Hz, when compared with Mic1.
2. Measure the output level in dBV (X)
3. Mute the signal from Mic2
4. Measure the output level in dBV (Y)
5. $FFNS_E$ = Y - X dB

NEAR FIELD SPEECH LOSS ($NFSL_E$)

For optimum near field speech preservation, the sound source should be in an endfire array configuration from the two microphones (see *Figure 11*). In this configuration the speech signal at the microphone closest to the sound source will have greater amplitude than the microphone further away. Additionally the signal at microphone further away will experience a phase lag when compared with the closer microphone. To simulate this, phase delay as well as amplitude shift was added to the $NFSL_E$ test. The schematic from Figure 3 is used with the following procedure to measure the $NFSL_E$.

1. A $25mV_{P-P}$ and $17.25mV_{P-P}$ ($0.69*25mV_{P-P}$) sine wave is applied to Mic1 and Mic2 respectively. Once again, a signal generator is used to delay the phase of Mic2 by 15.9° for 1Khz, or 4.8° for 300Hz, when compared with Mic1.
2. Measure the output level in dBV (X)
3. Mute the signal from Mic2
4. Measure the output level in dBV (Y)
5. $NFSL_E$ = Y - X dB

SINGLE TO NOISE RATIO IMPROVEMENT ELECTRICAL ($SNRI_E$)

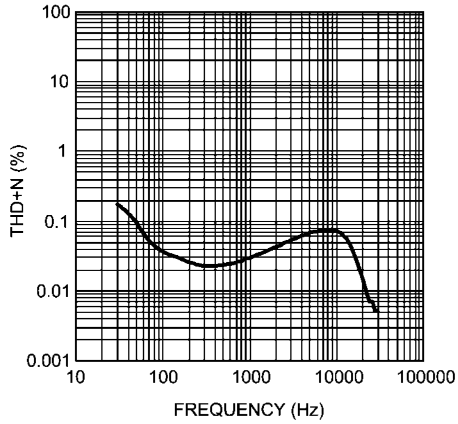
The $SNRI_E$ is the ratio of $FFNS_E$ to $NFSL_E$ and is defined as:

$$SNRI_E = FFNS_E - NFSL_E$$

Typical Performance Characteristics

Unless otherwise specified, T_J = 25°C, V_{DD} = 3.6V. Uplink Path: Input Voltage = 18mV$_{P-P}$, f =1 kHz, pass through mode (Note 8), Pre Amp gain = 20dB, Post Amp gain = 6dB, R_L = 100kΩ, and C_L = 4.7pf. Downlink Path: R_L = 32Ω, f = 1kHz, SNR Enhancer disabled.

THD+N vs Frequency
V_{DD} = 3.6V, P_{OUT} = 50mW
Downlink Path



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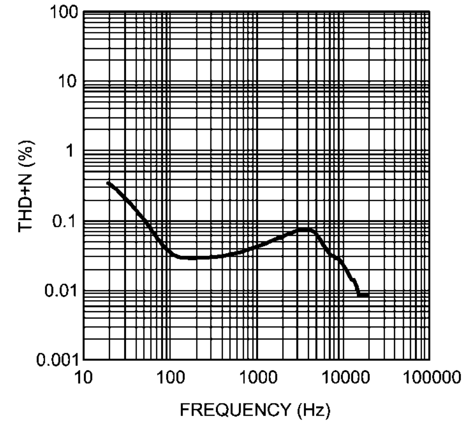
THD+N vs Frequency
V_{DD} = 5V, P_{OUT} = 150mW
Downlink Path



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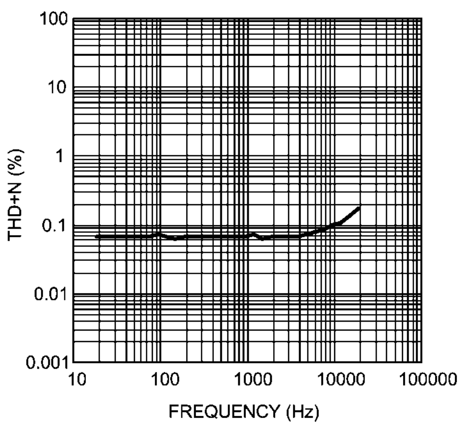
THD+N vs Frequency
Mic1 = 36mV$_{P-P}$, Mic2 = AC GND
Noise Cancelling Mode, Uplink Path



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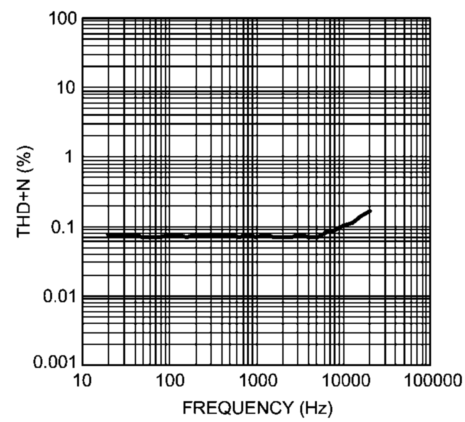
THD+N vs Frequency
Mic1 = 36mV$_{P-P}$, Mic2 = AC GND
Noise Cancelling Mode, Uplink Path



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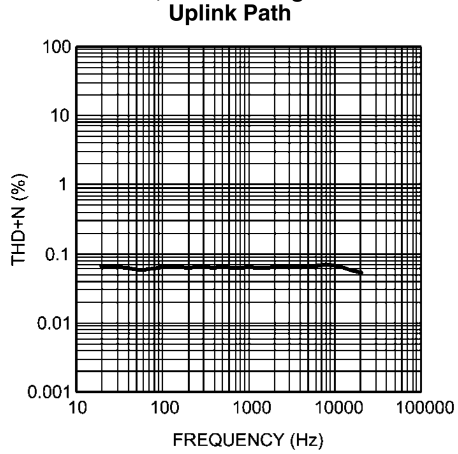
THD+N vs Frequency
Mic1 = 36mV, Pass Through Mode Mic1
Uplink Path



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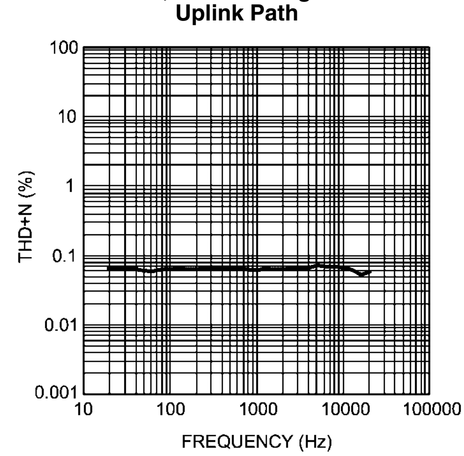
THD+N vs Frequency
Mic2 = 36mV, Pass Through Mode Mic2
Uplink Path



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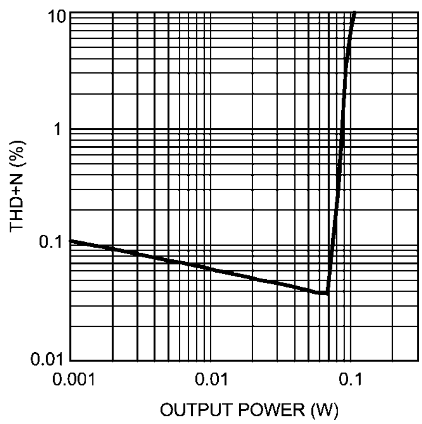
THD+N vs Output Power
V_{DD} = 3.6V, Downlink Path



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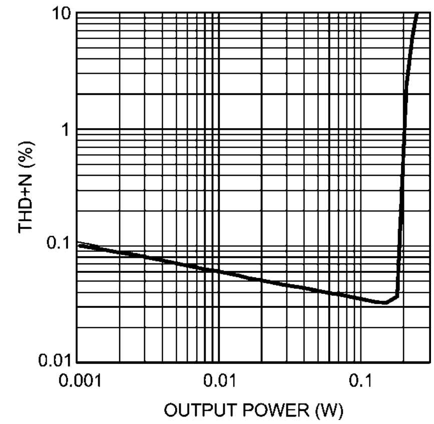
THD+N vs Output Power
V_{DD} = 5V, Downlink Path



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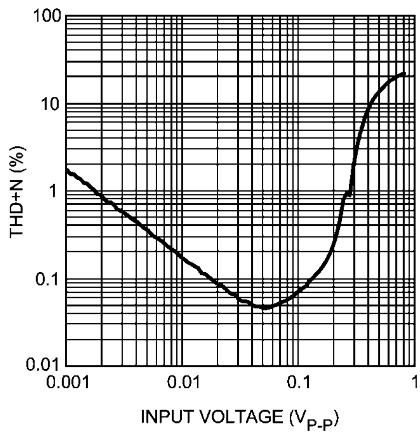
THD+N vs Input Voltage
Mic1 Noise Cancelling Mode
Mic2 = AC GND, Uplink Path



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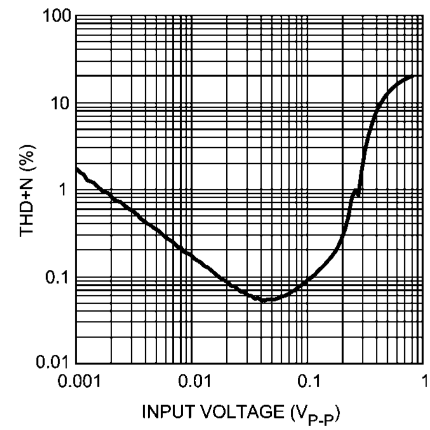
THD+N vs Input Voltage
Mic2 Noise Cancelling Mode
Mic1 = AC GND, Uplink Path



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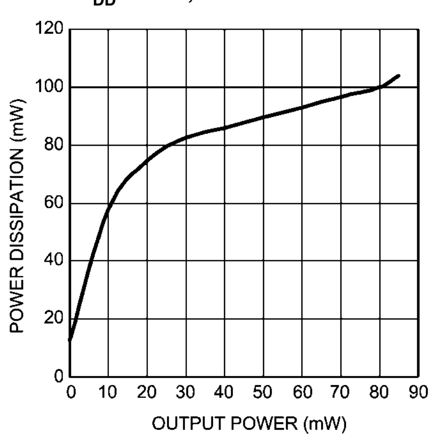
Output Power vs Power Dissipation
V_{DD} = 3.6V, Downlink Path



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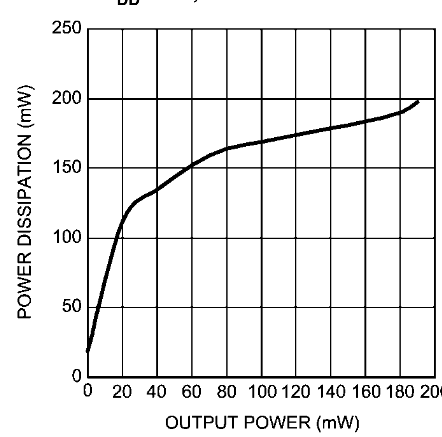
Output Power vs Power Dissipation
V_{DD} = 5V, Downlink Path



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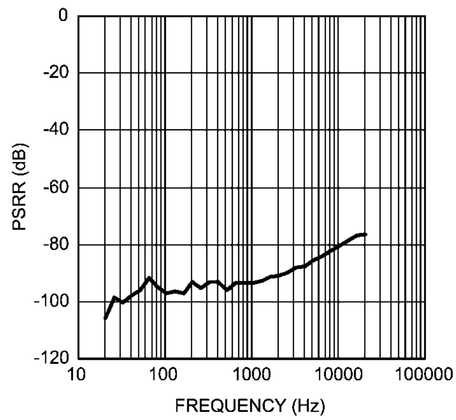
PSRR vs Frequency
V_{DD} = 3.6V, V_{RIPPLE} = 200mV_{P-P}
Input Referred, Input = AC Ground
Downlink Path



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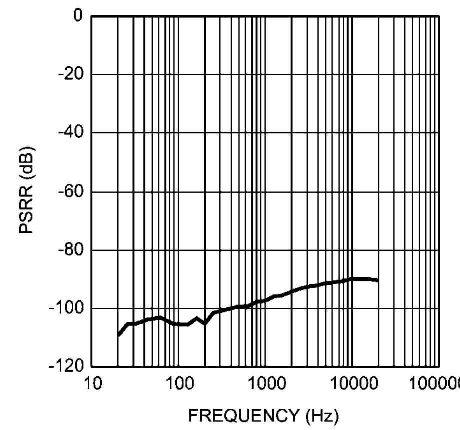
PSRR vs Frequency
Input Referred, V_{RIPPLE} = 200mV_{P-P}
Passthrough Mode, Input = AC Ground
Uplink Path



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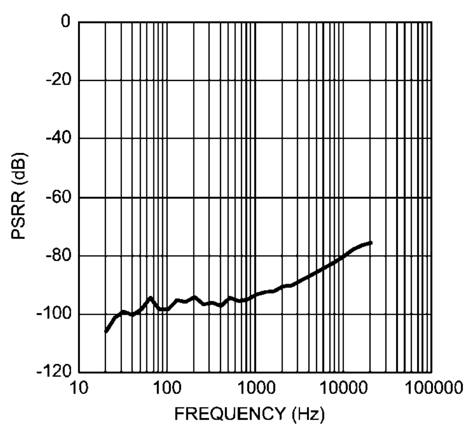
PSRR vs Frequency
V_{DD} = 5V
Input Referred, V_{RIPPLE} = 200mV_{P-P}
Input = AC Ground, Downlink Path



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Application Data

UPLINK FAR-FIELD NOISE REDUCTION OVERVIEW

The uplink portion of the LMV1099 is a fully analog solution to reduce the far field noise picked up by microphones in a communication system. A simplified block diagram is provided in *Figure 4*.

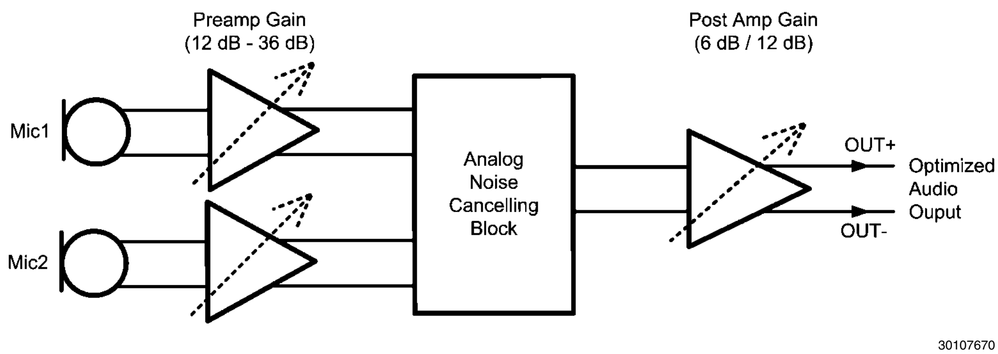


FIGURE 4. Simplified Block Diagram of the LMV1099 Uplink path

The output signal of the microphones is amplified by a preamplifier with adjustable gain between 12dB and 36dB. The matched signals are then routed through the Analog Noise Cancelling block which suppresses the far-field signal. The output of the analog noise cancelling processor is amplified in the post amplifier with selectable gain, 6dB or 12dB. For optimum noise and EMI immunity, the microphones have a differential connection to the LMV1099 and the uplink output is also differential. The adjustable gain functions can be controlled via I²C.

POWER SUPPLY CIRCUITS

A low drop-out (LDO) voltage regulator in the LMV1099 allows the device to be independent of supply voltage variations.

The Power On Reset (POR) circuitry in the LMV1099 requires the supply voltage to rise from 0V to V_{DD} in less than 100ms.

The Mic Bias output is provided as a low noise supply source for the electret microphones. The noise voltage on the Mic Bias microphone supply output pin depends on the noise voltage on the internal the reference node. The de-coupling capacitor on the V_{REF} pin determines the noise voltage on this internal reference. This capacitor should be larger than 1nF; having a larger capacitor value will result in a lower noise voltage on the Mic Bias output.

GAIN BALANCE AND GAIN BUDGET

In systems where input signals have a high dynamic range, critical noise levels or where the dynamic range of the output voltage is also limited, careful gain balancing is essential for the best performance. Too low of a gain setting in the preamplifier can result in higher noise levels, while too high of a gain setting in the preamplifier will result in saturation of the noise cancelling processor and output stages.

The gain ranges and maximum signal levels for the different functional blocks are shown in *Figure 5*. Two examples are given as a guideline on how to select proper gain settings.

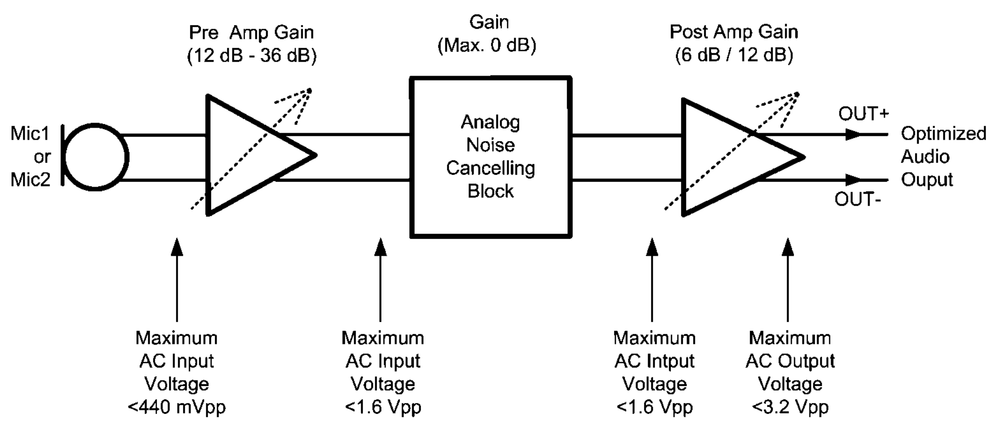


FIGURE 5. Maximum Signal Levels

Example 1:

An application using microphones with 50mV$_{P-P}$ maximum output voltage, and a baseband chip after the LMV1099 with 1.5V$_{P-P}$ maximum input voltage.

For optimum noise performance, the gain of the input stage should be set to the maximum.

1. 50mV$_{P-P}$ + 36dB = 3.1V$_{P-P}$.
2. 3.1V$_{P-P}$ is higher than the maximum 1.5V$_{P-P}$ allowed for the Noise Cancelling Block (NCB). This means a gain lower than 29.5dB should be selected.
3. Select the nearest lower gain from the gain settings shown in *Table 6*, 28dB is selected. This will prevent the NCB from being overloaded by the microphone. With this setting, the resulting output level of the Pre Amplifier will be 1.26V$_{P-P}$.
4. The NCB has a gain of 0dB which will result in 1.26V$_{P-P}$ at the output of the LMV1099. This level is less than the maximum level that is allowed at the input of the post amp of the LMV1099.
5. The baseband chip limits the maximum output voltage to 1.5V$_{P-P}$ with the minimum of 6dB post amp gain, this results in requiring a lower level at the input of the post amp of 0.75V$_{P-P}$. Now calculating this for a maximum preamp gain, the output of the preamp must be no more than 0.75mV$_{P-P}$.
6. Calculating the new gain for the preamp will result in <23.5dB gain.
7. The nearest lower gain will be 22dB.

So using preamp gain = 22dB and postamp gain = 6dB is the optimum for this application.

Example 2:

An application using microphones with 10mV$_{P-P}$ maximum output voltage, and a baseband chip after the LMV1099 with 3.3V$_{P-P}$ maximum input voltage.

For optimum noise performance we would like to have the maximum gain at the input stage.

1. 10mV$_{P-P}$ + 36dB = 631mV$_{P-P}$.
2. This is lower than the maximum 1.5V$_{P-P}$, so this is OK.
3. The NCB has a gain of 0dB which will result in 1.5V$_{P-P}$ at the output of the LMV1099. This level is lower than the maximum level that is allowed at the input of the Post Amp of the LMV1099.
4. With a Post Amp gain setting of 6dB the output of the Post Amp will be 3V$_{P-P}$ which is OK for the baseband.
5. The nearest lower Post Amp gain will be 6dB.

So using preamp gain = 36dB and postamp gain = 6dB is optimum for this application.

I²C Compatible Interface

The LMV1099 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open-collector) although the LMV1099 does not write to the I²C bus. The LMV1099 and the master can communicate at clock rates up to 400kHz. Figure 5 shows the I²C Interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LMV1099 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 6). The data line is 8 bits long and is always followed by an acknowledge pulse (Figure 7).

I²C Compatible Interface Power Supply Pin (I²CV$_{DD}$)

The LMV1099 I²C interface is powered up through the I²CV$_{DD}$ pin. The LMV1099 I²C interface operates at a voltage level set by the I²CV$_{DD}$ pin which can be set independent to that of the main power supply pin V$_{DD}$. This is ideal whenever logic levels for the I²C Interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

I²C Bus Format

The I²C bus format is shown in Figure 7. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH is generated, alerting all devices on the bus that a device address is being written to the bus. The 7-bit device address is written to the bus, most significant bit (MSB) first followed by the R/W bit, R/W = 0 indicates the master is writing to the slave device, R/W = 1 indicates the master wants to read data from the slave device. Set R/W = 0; the LMV1099 is a WRITE-ONLY device and will not respond to the R/W = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the mater device release SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LMV1099 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK)

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LMV1099 sends another ACK bit. Following the acknowledgement of the last register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

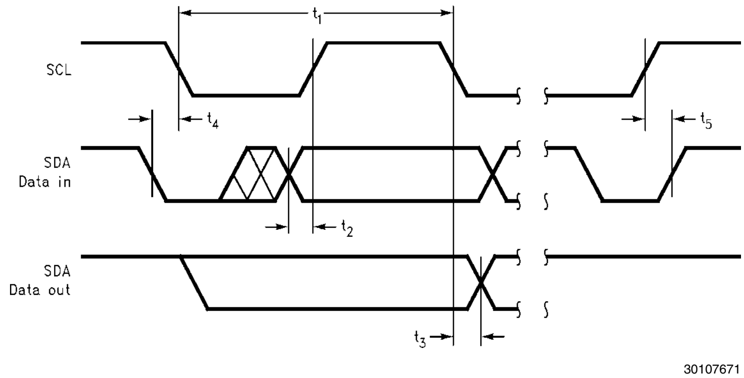


FIGURE 6. I²C Timing Diagram

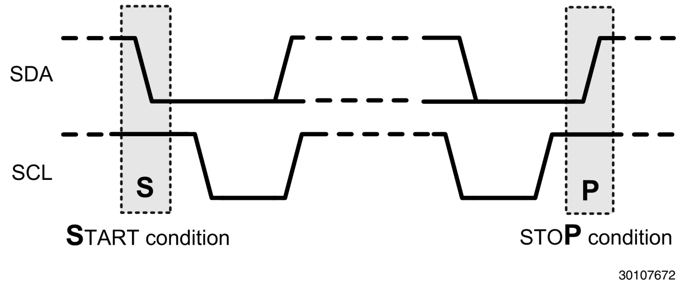


FIGURE 7. I²C Start Stop Conditions

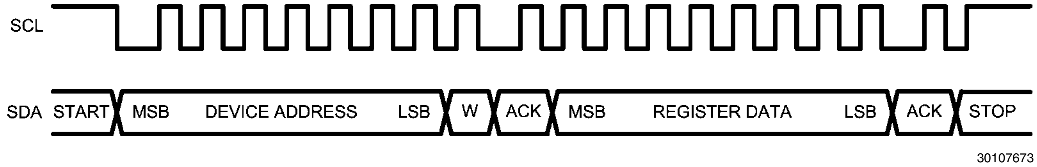


FIGURE 8. Start and Stop Diagram

I²C RESET PIN

When the I²C RESET pin is pulled low, the device will go into shutdown and the Power_on bit (see Table 3) in the shutdown control register will reset. The device will remain in shutdown until an I²C command brings the device out of shutdown (see timing diagram in *Figure 9*). This pin can be connected to the I²CV_{DD} pin to prevent undefined and unwanted state changes that may occur when the I²C supply voltage is cycled.

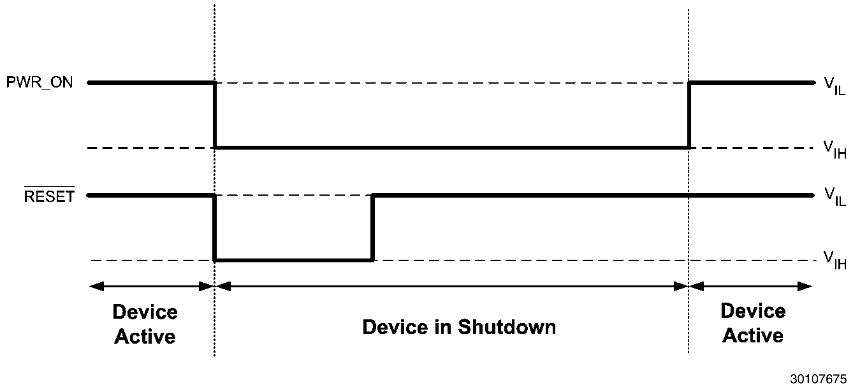


FIGURE 9. I²C Reset Timing Diagram

TABLE 2. Chip Address

	B7	B6	B5	B4	B3	B2	B1	B0/$\overline{W}$
Chip Address	1	1	0	0	1	1	1	0

NOTE: The 7th Bit (B7) of the Register Data determines whether it will activate Register A or Register B.

TABLE 3. Control Registers

Register Name	Register Address B<6:5>	B<4>	B<3>	B<2>	B<1>	B<0>
Shutdown control	00	x	x	enable_ep	I^2CV_{DD}_sd	power_on
Mic mode control	01	mic_sel1	mic_sel0	agc_mic_mute	mute_mic2	mute_mic1
Mic Gain control	10	mic_post_gain	mic_pre_gain3	mic_pre_gain2	mic_pre_gain1	mic_pre_gain0
EP	11	ep_mute	plev	ep_bypass_agc	ep_ri1	ep_ri0

TABLE 4. Shutdown Control Register

BIT	NAME	DESCRIPTION	
B2	enable_ep	0	Disable earpiece
		1	Enable earpiece
B1	I^2CV_{DD}_SD	0	I^2CV_{DD} is an active low RESET input. If I^2CV_{DD} drops below 1.1V the device resets and the I^2C registers are restored to their default state
		1	Normal operation. I^2CV_{DD} voltage does not reset the device
B0	power_on	0	Device disable
		1	Device enable

TABLE 5. LMV1099 Microphone Mode Control Register

BIT	NAME	DESCRIPTION		
B4:B3	mic_sel<4> mic_sel<3>	B4	B3	
		0	0	Noise canceling mode
		0	1	Only mic1 enabled (pass through)
		1	0	Only mic2 enabled (pass through)
		1	1	(mic1+mic2)/2
B2	agc_mic_mute	0		mic1 & mic2 mute not allowed
		1		mic1 & mic2 mute allowed
B1	mute_mic2*	0		mic2 on
		1		mic2 mute
B0	mute_mic1*	0		mic1 on
		1		mic1 mute

* agc_mic_mute overrides mute_mic1 and mute_mic2

TABLE 6. LMV1099 Microphone Gain Control Register

BIT	NAME	DESCRIPTION				
B4	mic_post_gain	0				6dB
		1				12dB
B3:B0	mic_pre_gain<3> mic_pre_gain<2> mic_pre_gain<1> mic_pre_gain<0>	B3	B2	B1	B0	
		0	0	0	0	12dB
		0	0	0	1	12dB
		0	0	1	0	12dB
		0	0	1	1	12dB
		0	1	0	0	14dB
		0	1	0	1	16dB
		0	1	1	0	18dB
		0	1	1	1	20dB
		1	0	0	0	22dB
		1	0	0	1	24dB
		1	0	1	0	26dB
		1	0	1	1	28dB
		1	1	0	0	30dB
		1	1	0	1	32dB
		1	1	1	0	34dB
		1	1	1	1	36dB

TABLE 7. LMV1099 Earpiece Control Register

BIT	NAME	DESCRIPTION		
B4	ep_mute	0		EP on
		1		EP mute
B3	plev	0		3.6V_{P-P} Earpiece Output Level (50mW with 32Ω load)
		1		4.1V_{P-P} Earpiece Output Level (70mW with 32Ω load)
B2	ep_bypass_agc	0		Normal operation
		1		Downlink SNR Enhancer Circuit bypassed (earpiece is still active)
B1:B0	ep_ri<1> ep_ri<0>	B1	B0	
		0	0	60kΩ input impedance
		0	1	9kΩ input impedance
		1	0	6kΩ input impedance
		1	1	6kΩ input impedance

Shutdown Function

As part of the Powerwise™ family, the LMV1099 consumes only 0.50mA of current. In many applications the part does not need to be continuously operational. To further reduce the power consumption in the inactive period, the LMV1099 provides two individual microphone power down functions (controlled through the mode control registers B3:B4). When either one of the shutdown functions is activated the part will go into shutdown mode consuming only a few µA of supply current. Shutdown functions can be controlled via the I²C interface or a hardware pin.

SHUTDOWN VIA HARDWARE PIN

The hardware shutdown function is operated via the EN pin. In normal operation the EN pin must be at a 'high' level (V_{DD}). Whenever a 'low' level (GND) is applied to the EN pin the part will go into shutdown mode disabling all internal circuits.

Microphone Mode Control

The LMV1099 features four Microphone modes, Noise Cancellation Mode, Mic 1 pass through, Mic 2 pass through, and (Mic1+Mic2)/2. When in Noise Cancellation mode, it is imperative that Mic 1 and Mic 2 are NOT muted. If the mute function for either microphone path is enabled, the noise cancellation circuitry will be disabled. In mic1/mic2 pass through mode the noise canceling block is bypassed, and the LMV1099 is simply used as a microphone amplifier where the microphone signal passes through the pre and post amplifier gain stages. The last mode provides an average of the two microphone pass through signals (noise cancelling block is bypassed).

The microphone input paths can be muted individually via I²C (Mic mode control register B1:B0). To enable the mute function, set bit B2 of the microphone mode control register to 1. If B2 is set to 0, the mute function will not activate.

Signal-to-Noise Ratio Enhancer (SNR Enhancer)

The SNR Enhancer in the LMV1099 is designed to provide excellent voice intelligibility in noisy environments. The control signal for the output gain adjustment is dependent on both the level and the type of ambient noise, compared with the signal energy of the downlink voice. The system was designed to operate transparently to the user, such that the gain changes are not evident but provide excellent voice intelligibility.

National has invested considerable amount of time evaluating the acoustic effects of different ambient noise source types along with their practical SPL levels to determine optimum timing capacitor values for the proprietary downlink solution. These timing capacitor values should not be changed. We recommend using standard ceramic chip type capacitors with a low leakage rating. Electrolytic capacitors should not be used.

The SNR enhancing circuit will analyze the various energy levels for different frequency ranges and weight the AGC's gain change accordingly such that the downlink voice will remain intelligent. The overall intent of the circuit is for the gain changes to be transparent. Great care has gone into ensuring that gain changes won't be too perceptible or obnoxious. The system with have more dynamic gain change capability at low ambient noise levels in order to respond to fast changing noise sources. At the other extreme the system will have less dynamic gain change at high ambient noise levels since the environment will constantly be affecting intelligibility.

Earpiece Control Registers

OUTPUT POWER LIMIT (PLEV)

While National has done extensive ambient SPL analysis, there will always be unusual circumstances that may cause the amplifier to be at its maximum 18dB setting. LMV1099 features an Output Voltage Limit function to limit the output power delivered to a speaker. When the SNR enhancer is active, the Output Voltage Limit works to protect the loudspeaker in conditions where a large downlink input signal is present. The Output Voltage Limit can be set to a selectable ($3.6V_{P-P}$ or $4.1V_{P-P}$) output level to avoid violating the maximum power limitation of the transducer.

SNR ENHANCER BYPASS (EP_BYPASS_AGC)

The SNR enhancer can be bypassed by setting B4 of the Earpiece Control Register to 1. When the SNR enhancer is bypassed, the earpiece amplifier has a fixed 0dB gain.

EP_RI (INPUT IMPEDANCE)

The earpiece input of the LMV1099 features three input impedance options, this impedance in conjunction with the input capacitor creates a high-pass filter. The three options provide various cutoff frequencies for the high-pass filter. *Table 8* shows the respective cutoff frequencies for each of the input impedance options when using a 68nF input capacitor.

TABLE 8. Input Impedance options

Input Impedance	f_C
60kΩ	40Hz
9kΩ	260Hz
6kΩ	390Hz

Changing the input coupling capacitor will affect the filters –3dB point through the simple RC equation shown below:

$$f = 1 / 2\pi RC$$

Microphone Placement

Because the LMV1099 is a microphone array Far Field Noise Reduction solution, proper microphone placement is critical for optimum performance. Two things need to be considered: The spacing between the two microphones and the position of the two microphones relative to near field source.

If the spacing between the two microphones is too small near field speech will be canceled along with the far field noise. Conversely, if the spacing between the two microphones is large, the far field noise reduction performance will be degraded. The optimum spacing between mic1 and mic2 is 1.5-2.5cm. This range provides a balance of minimal near field speech loss and maximum far field noise reduction. The microphones should be in line with the desired sound source 'near speech' and configured in an endfire array (see *Figure 11*) orientation from the sound source. If the 'near speech' (desired sound source) is equidistant to the source like a broadside array (see *Figure 10*) the result will be a great deal of near field speech loss.

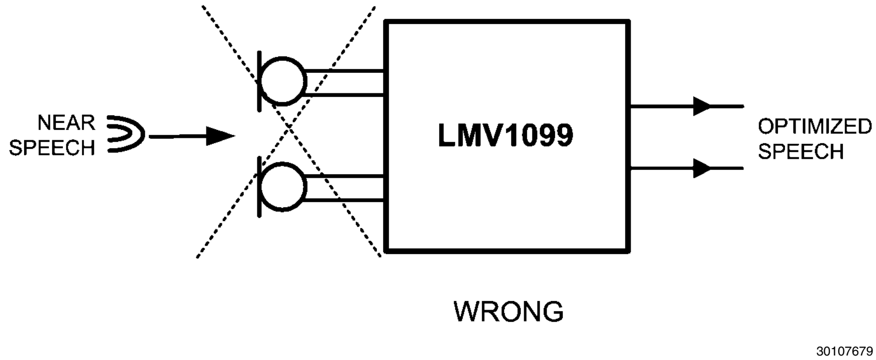


FIGURE 10. Broadside Array (WRONG)

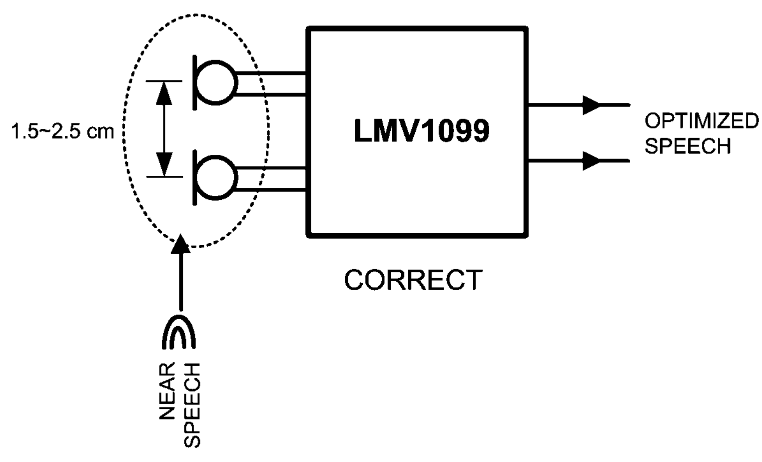


FIGURE 11. Endfire Array (CORRECT)

Low-Pass Filter At The Output

At the output of the LMV1099 there is a provision to create a 1st order low-pass filter (only enabled in 'Noise Cancelling' mode). This low-pass filter can be used to compensate for the change in frequency response that results from the noise cancellation process. The change in frequency response resembles a first-order high-pass filter, and for many of the applications it can be compensated by a first-order low-pass filter with cutoff frequency between 1.5kHz and 2.5kHz.

The transfer function of the low-pass filter is derived as:

$$H(s) = \frac{\text{Post Amplifier gain}}{sR_fC_f+1}$$

This low-pass filter is created by connecting a capacitor between the LPF pin and the OUT pin of the LMV1099. The value of this capacitor also depends on the selected output gain. For different gains the feedback resistance in the low-pass filter network changes as shown in .

This will result in the following values for a cutoff frequency of 2000 Hz:

TABLE 9. Low-Pass Filter Capacitor For 2kHz

Post Amplifier Gain Setting (dB)	R_f (kΩ)	C_f (nF)
6	20	3.9
12	40	2.0

A-Weighted Filter

The human ear is sensitive for acoustic signals within a frequency range from about 20Hz to 20kHz. Within this range the sensitivity of the human ear is not equal for each frequency. To approach the hearing response, weighting filters are introduced. One of those filters is the A-weighted filter.

The A-weighted filter is used in signal to noise measurements, where the wanted audio signal is compared to device noise and distortion.

The use of this filter improves the correlation of the measured values to the way these ratios are perceived by the human ear.

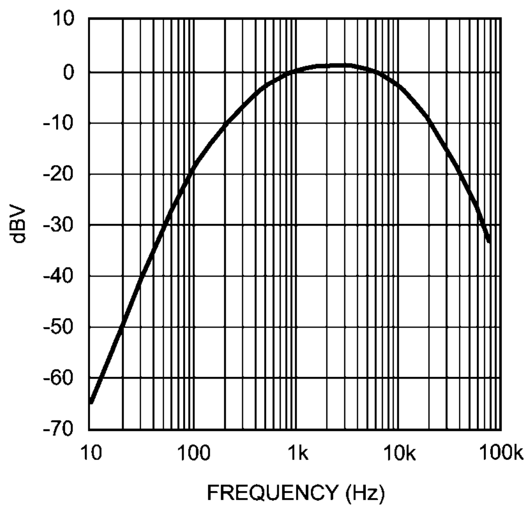


FIGURE 12. A-Weighted Filter

Measuring Uplink Noise and SNR

The overall noise of the LMV1099 is measured within the frequency band from 10Hz to 22kHz using an A-weighted filter.

The Mic+ and Mic- inputs of the LMV1099 are AC shorted between the input capacitors, see *Figure 13*.

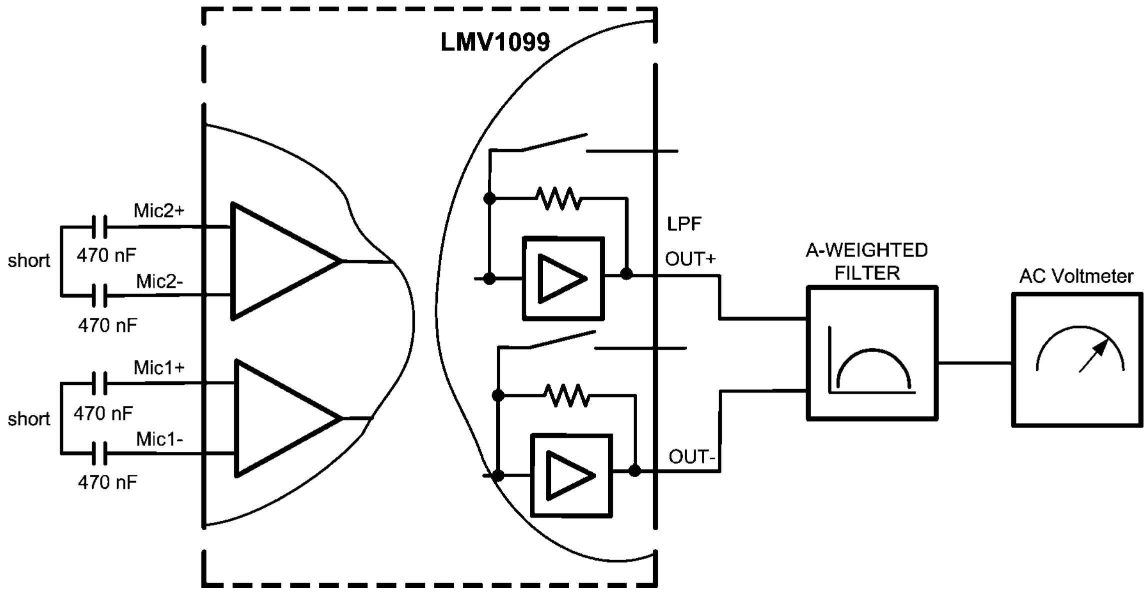


FIGURE 13. Noise Measurement Setup

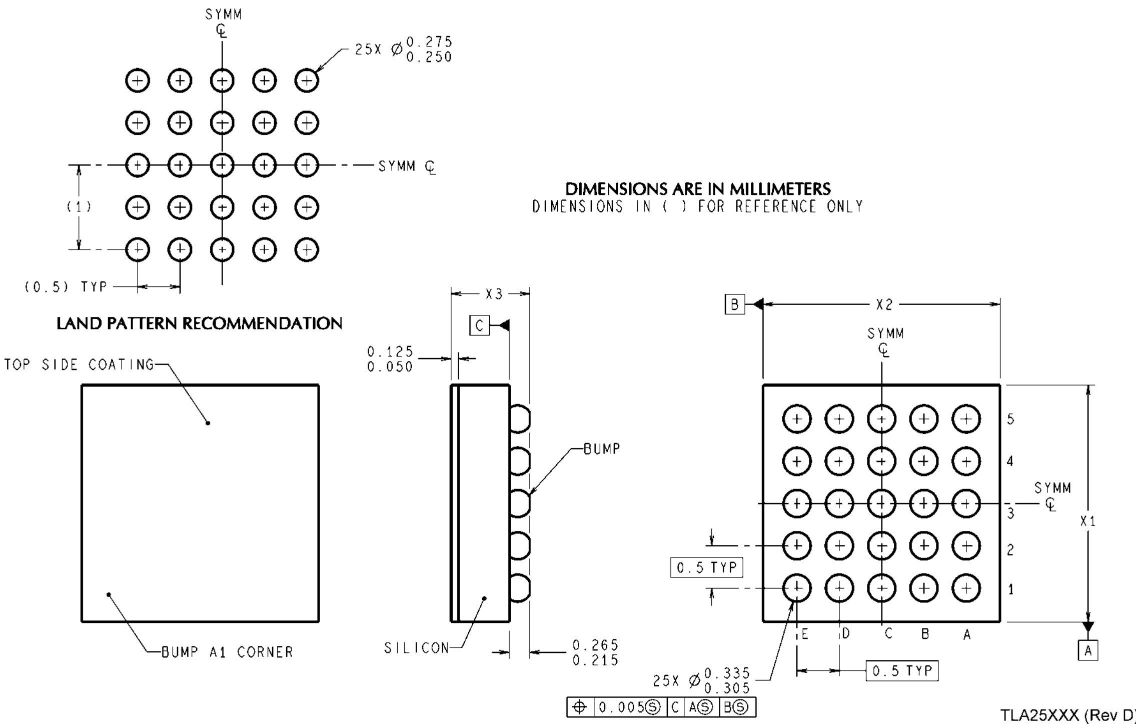
For the signal to noise ratio (SNR) the signal level at the output is measured with a 1kHz input signal of 18mV$_{P-P}$ using an A-weighted filter. This voltage represents the output voltage of a typical electret condenser microphone at a sound pressure level of 94dB SPL, which is the standard level for these measurements. The LMV1099 is programmed for 26dB of total gain (20dB preamplifier and 6dB postamplifier) with only mic1 or mic2 used. (See also *I²C Compatible* Interface).

The input signal is applied differentially between the Mic+ and Mic-. Because the part is in Pass Through mode the low-pass filter at the output of the LMV1099 is disabled.

Revision History

Rev	Date	Description
1.0	08/12/10	Initial release.
1.01	12/10/10	Added the X1, X2, and X3 values of the mktg outline.
1.02	03/30/11	Edited Table 3 (Control Registers).

Physical Dimensions inches (millimeters) unless otherwise noted



25 Bump micro SMD Technology
NS Package Number TLA25GMA
X1 = 2.644±0.030mm, X2 = 2.771±0.030mm, X3 = 0.600±0.075mm,

Notes

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LVDS	www.national.com/lvds	Packaging	www.national.com/packaging
Power Management	www.national.com/power	Green Compliance	www.national.com/quality/green
Switching Regulators	www.national.com/switchers	Distributors	www.national.com/contacts
LDOs	www.national.com/ldo	Quality and Reliability	www.national.com/quality
LED Lighting	www.national.com/led	Feedback/Support	www.national.com/feedback
Voltage References	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Applications & Markets	www.national.com/solutions
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Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
		TI E2E Community Home Page	e2e.ti.com

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