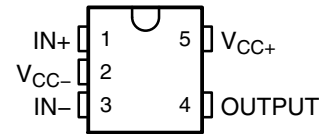


LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

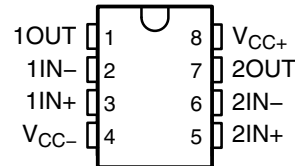
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- 2.7-V and 5-V Performance
- -40°C to 125°C Specification at 5 V
- No Crossover Distortion
- Gain Bandwidth of 152 kHz
- Low Supply Current
 - LPV321 . . . 9 μA
 - LPV358 . . . 15 μA
 - LPV324 . . . 28 μA
- Rail-to-Rail Output Swing at 100-k Ω Load
 - $V_{\text{CC}+}$ – 3.5 mV
 - $V_{\text{CC}-}$ + 90 mV
- V_{ICR} . . . -0.2 V to $V_{\text{CC}+}$ – 0.8 V
- Stable With Capacitive Load of 1000 pF
- Applications
 - Active Filters
 - General-Purpose, Low-Voltage Applications
 - Low-Power and/or Portable Applications
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

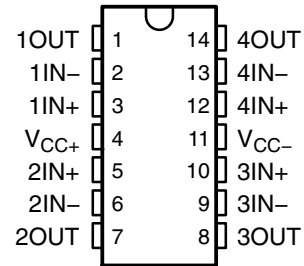
LPV321 . . . DBV OR DCK PACKAGE
(TOP VIEW)



LPV358 . . . D, DDU, OR DGK PACKAGE
(TOP VIEW)



LPV324 . . . D OR PW PACKAGE
(TOP VIEW)



description/ordering information

The LPV321/358/324 devices are low-power (9 μA per channel at 5 V) versions of the LMV321/358/324 operational amplifiers. These are additions to the LMV321/358/324 family of commodity operational amplifiers.

The LPV321/358/324 devices are the most cost-effective solutions for applications where low voltage, low-power operation, space saving, and low price are needed. These devices have rail-to-rail output-swing capability, and the input common-mode voltage range includes ground. They all exhibit excellent speed-power ratios, achieving 152 kHz of bandwidth, with a supply current of only 9 μA typical.

The LPV321, LPV358, and LPV324 are characterized for operation from -40°C to 85°C . The LPV321I, LPV358I, and LPV324I are characterized for operation from -40°C to 125°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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description/ordering information (continued)

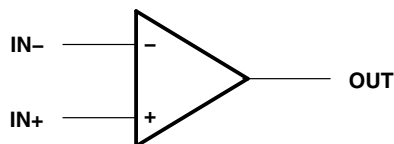
ORDERING INFORMATION

T_A	PACKAGE†			ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	Single	SOT23-5 (DBV)	Reel of 3000	LPV321DBVR	5C7_
			Reel of 250	LPV321DBVT	PREVIEW
		SC-70 (DCK)	Reel of 3000	LPV321DCKR	52_
			Reel of 250	LPV321DCKT	PREVIEW
	Dual	SOIC-8 (D)	Tube of 75	LPV358D	PV358
			Reel of 2500	LPV358DR	
		VSSOP-8 (DDU)	Reel of 3000	LPV358DDUR	5A56
			Reel of 2500	LPV358DGKR	546
		VSSOP-8 (DGK)	Reel of 250	LPV358DGKT	PREVIEW
–40°C to 125°C	Single	SOT23-5 (DBV)	Reel of 3000	LPV321IDBVR	5C1_
			Reel of 250	LPV321IDBVT	PREVIEW
		SC-70 (DCK)	Reel of 3000	LPV321IDCKR	53_
			Reel of 250	LPV321IDCKT	PREVIEW
	Dual	SOIC-8 (D)	Tube of 75	LPV358ID	PV358I
			Reel of 2500	LPV358IDR	
		VSSOP-8 (DDU)	Reel of 3000	LPV358IDDUR	5AE6
			Reel of 2500	LPV358IDGKR	556
		VSSOP-8 (DGK)	Reel of 250	LPV358IDGKT	PREVIEW
	Quad	SOIC-14 (D)	Tube of 50	LPV324ID	LPV324I
			Reel of 2500	LPV324IDR	
		TSSOP-14 (PW)	Tube of 90	LPV324IPW	PV324I
			Reel of 2000	LPV324IPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

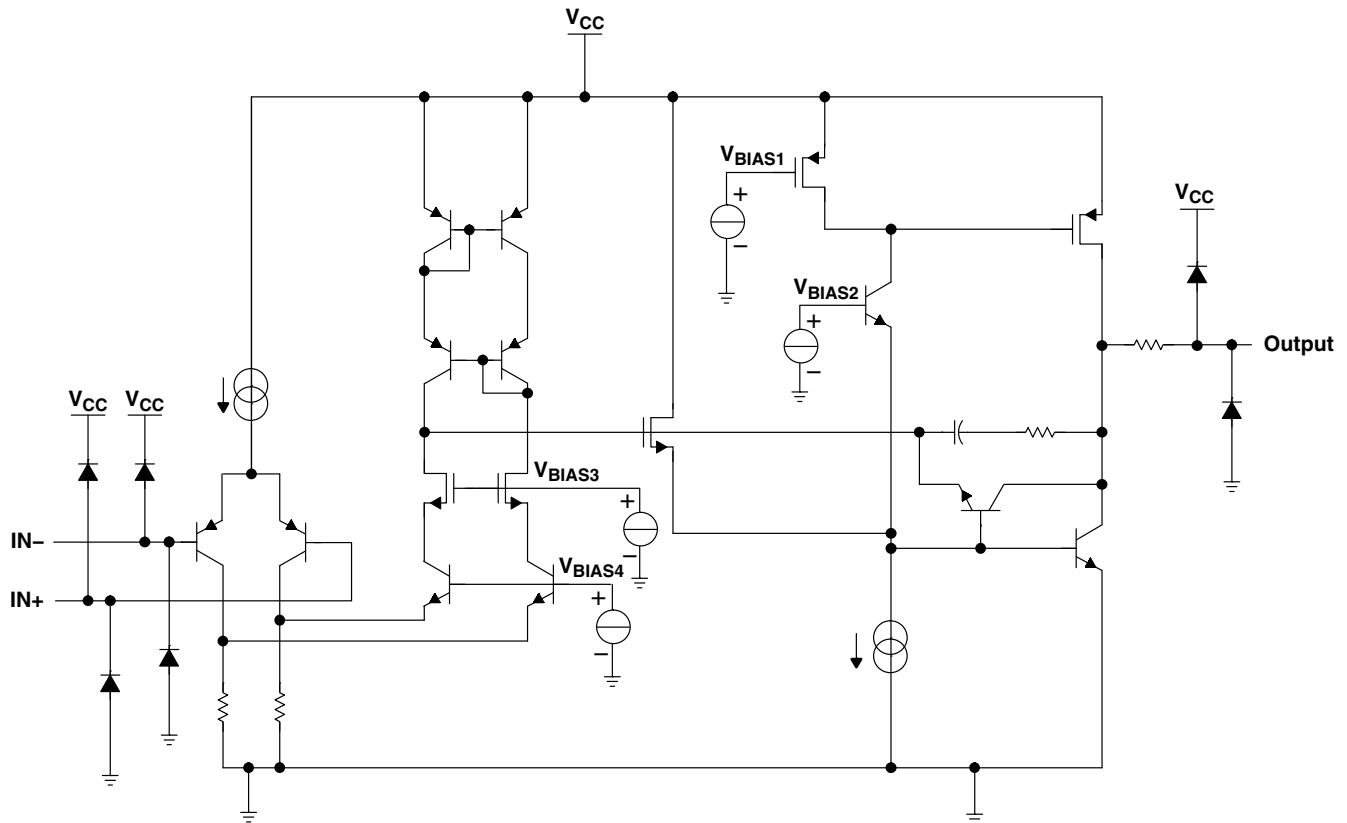
symbol (each amplifier)



LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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LPV324 simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, $V_{CC+} - V_{CC-}$ (see Note 1)	5.5 V
Differential input voltage, V_{ID} (see Note 2)	$\pm V_{CC}$
Input voltage range, V_I (either input)	V_{CC-} to $V_{CC+} - 1$ V
Package thermal impedance, θ_{JA} (see Notes 3 and 4):	
5-pin DBV package	206°C/W
5-pin DCK package	252°C/W
8-pin D package	97°C/W
8-pin DDU package	TBD°C/W
8-pin DGK package	172°C/W
14-pin D package	86°C/W
14-pin PW package	113°C/W
Maximum junction temperature, T_J	150°C
Storage temperature range, T_{stg}	-65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages and V_{CC} specified for the measurement of I_{OS} , are with respect to the network GND.
 2. Differential voltages are at IN+ with respect to IN-.
 3. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Selecting the maximum of 150°C can affect reliability.
 4. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.7	5	V
T _A	Operating free-air temperature	LPV3xx	−40	85	°C
		LPV3xxI	−40	125	

ESD protection

TEST CONDITIONS	TYP	UNIT
Human-Body Model	2	kV
Machine model	200	V
Charged-Device Model	1	kV



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**LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD
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2.7-V electrical characteristics

$T_A = 25^\circ\text{C}$, $V_{CC+} = 2.7\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{IC} = 1\text{ V}$, $V_O = V_{CC+}/2$, and $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IO} Input offset voltage			1.2	7	mV
α_{VIO} Average temperature coefficient of input offset voltage			4		$\mu\text{V}/^\circ\text{C}$
I_{IB} Input bias current			1.7	50	nA
I_{IO} Input offset current			0.6	40	nA
CMRR Common-mode rejection ratio	$0 \leq V_{IC} \leq 1.7\text{ V}$	50	70		dB
k_{SVR} Supply-voltage rejection ratio	$2.7\text{ V} \leq V_{CC+} \leq 5\text{ V}$, $V_{IC} = 1\text{ V}$, $V_O = 1\text{ V}$	50	65		dB
V_{ICR} Common-mode input voltage range	CMRR $\geq 50\text{ dB}$	0 to 1.7	–0.2 to 1.9		V
V_O Output swing	$R_L = 100\text{ k}\Omega$ to 1.35 V	High level	$V_{CC+} - 0.100$	$V_{CC+} - 0.003$	V
		Low level	0.080	0.180	
I_{CC} Supply current	LPV321		4	8	μA
	LPV358 (both amplifiers)		8	16	
	LPV324 (all four amplifiers)		16	24	
SR Slew rate‡			0.1		V/ μs
GBW Gain bandwidth product	$C_L = 22\text{ pF}$ (see Note 5)		205		kHz
Φ_m Phase margin	$C_L = 22\text{ pF}$ (see Note 5)		71		deg
Gain margin	$C_L = 22\text{ pF}$ (see Note 5)		11		dB
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$		178		$\text{nV}/\sqrt{\text{Hz}}$
I_n Equivalent input noise current	$f = 1\text{ kHz}$		0.5		$\text{pA}/\sqrt{\text{Hz}}$

† All typical values are at $V_{CC} = 2.7\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Number specified is the slower of the positive and negative slew rates.

NOTE 5: Closed-loop gain = 18 dB, $V_{IC} = V_{CC+}/2$

LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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5-V electrical characteristics

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{IC} = 2\text{ V}$, $V_O = V_{CC+}/2$, and $R_L > 1\text{ M}\Omega$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T _A	MIN	TYP†	MAX	UNIT
V _{IO}	Input offset voltage			25°C		1.5	7	mV
				−40°C to 85°C			10	
				−40°C to 125°C			11	
α _{VIO}	Average temperature coefficient of input offset voltage			25°C		4		μV/°C
I _{IB}	Input bias current			25°C		2	50	nA
				−40°C to 85°C			60	
				−40°C to 125°C			65	
CMRR	Common-mode rejection ratio	0 ≤ V _{IC} ≤ 4 V		25°C	50	71		dB
k _{SVR}	Supply-voltage rejection ratio	2.7 V ≤ V _{CC+} ≤ 5 V, V _{IC} = 1 V, V _O = 1 V		25°C	50	65		dB
V _{ICR}	Common-mode input voltage range	CMRR ≥ 50 dB		25°C	0 to 4	−0.2 to 4.2		V
I _{IO}	Input offset current			25°C		0.6	40	nA
				−40°C to 85°C			50	
				−40°C to 125°C			55	
V _O	Output swing	R _L = 100 kΩ to 2.5 V	High level	25°C	V _{CC+} − 0.100	V _{CC+} − 0.0035		V
				−40°C to 85°C	V _{CC+} − 0.200			
				−40°C to 125°C	V _{CC+} − 0.225			
			Low level	25°C	0.090		0.180	
				−40°C to 85°C			0.220	
				−40°C to 125°C			0.240	
I _{OS}	Output short-circuit current	Sourcing, V _O = 0 V		25°C	2	17	mA	
		Sinking, V _O = 5 V			20	72		
I _{CC}	Supply current	LPV321		25°C		9	12	μA
				−40°C to 85°C			15	
				−40°C to 125°C			40	
		LPV358 (both amplifiers)		25°C		15	20	
				−40°C to 85°C			24	
				−40°C to 125°C			80	
		LPV324 (all four amplifiers)		25°C		28	42	
				−40°C to 85°C			46	
				−40°C to 125°C			125	
A _V ‡	Large-signal voltage gain	R _L = 100 kΩ		25°C	15	100	V/mV	
				−40°C to 85°C	10			
				−40°C to 125°C	10			
SR§	Slew rate			25°C		0.1		V/μs

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ R_L is connected to V_{CC-} . The output voltage is $0.5\text{ V} \leq V_O \leq 4.5\text{ V}$.

§ Number specified is the slower of the positive and negative slew rates. Connected as a voltage follower with 3-V step input.

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5-V electrical characteristics

$T_A = 25^\circ\text{C}$, $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $V_{IC} = 2\text{ V}$, $V_O = V_{CC+}/2$, and $R_L > 1\text{ M}\Omega$ (unless otherwise noted)
(continued)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP [†]	MAX	UNIT
GBW	Gain bandwidth product	$C_L = 22\text{ pF}$ (see Note 5)	25°C		237		kHz
Φ_m	Phase margin	$C_L = 22\text{ pF}$ (see Note 5)	25°C		74		deg
	Gain margin	$C_L = 22\text{ pF}$ (see Note 5)	25°C		12		dB
V_n	Equivalent input noise voltage	$f = 1\text{ kHz}$	25°C		146		$\text{nV}/\sqrt{\text{Hz}}$
I_n	Equivalent input noise current	$f = 1\text{ kHz}$	25°C		0.3		$\text{pA}/\sqrt{\text{Hz}}$

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

NOTE 5: Closed-loop gain = 18 dB, $V_{IC} = V_{CC+}/2$

LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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**SUPPLY CURRENT
vs
SUPPLY VOLTAGE
(LPV324 – All Channels)**

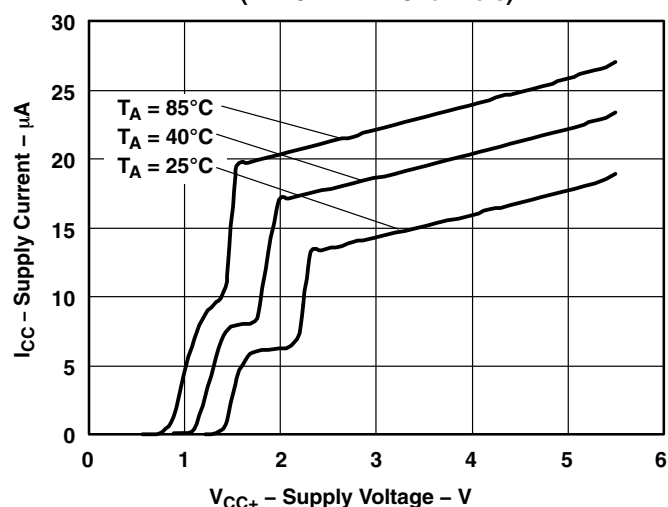


Figure 1

**INPUT BIAS CURRENT
vs
TEMPERATURE**

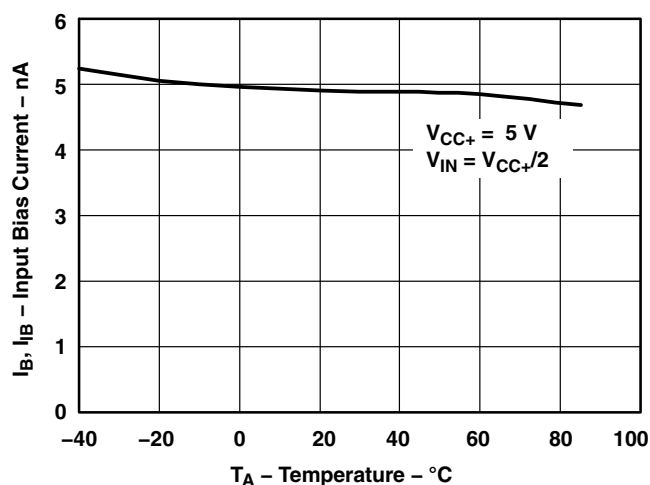


Figure 2

**SOURCING CURRENT
vs
OUTPUT VOLTAGE**

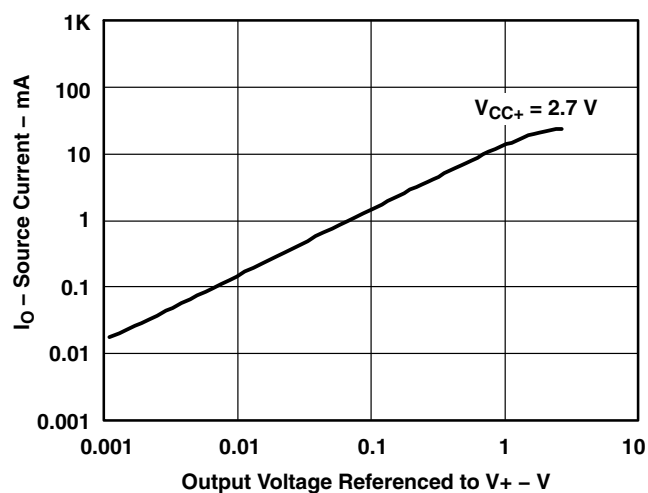


Figure 3

**SOURCING CURRENT
vs
OUTPUT VOLTAGE**

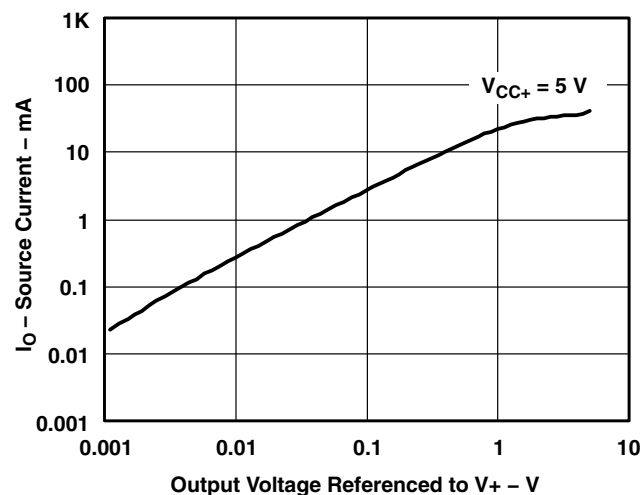


Figure 4

**LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD
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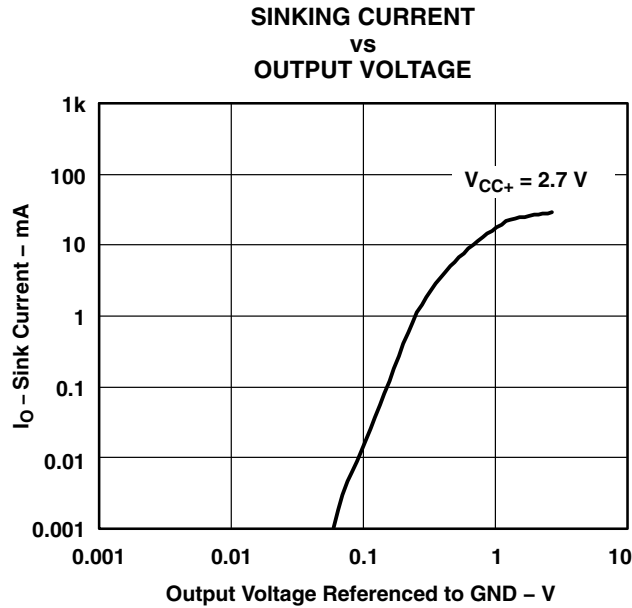


Figure 5

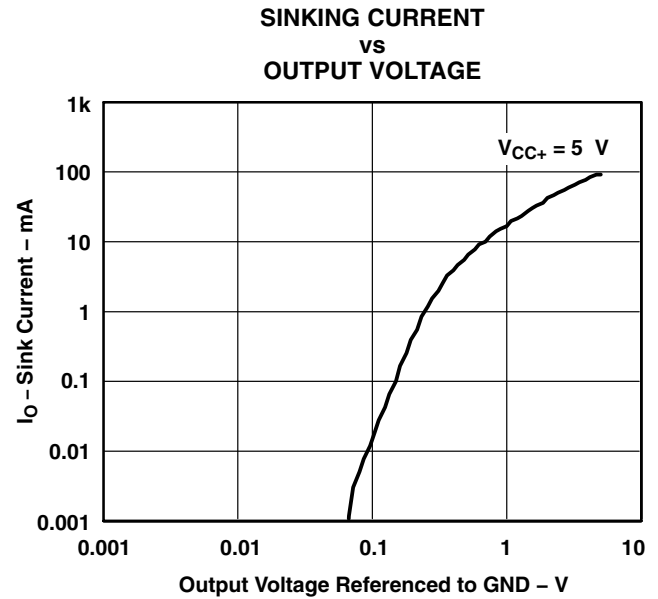


Figure 6

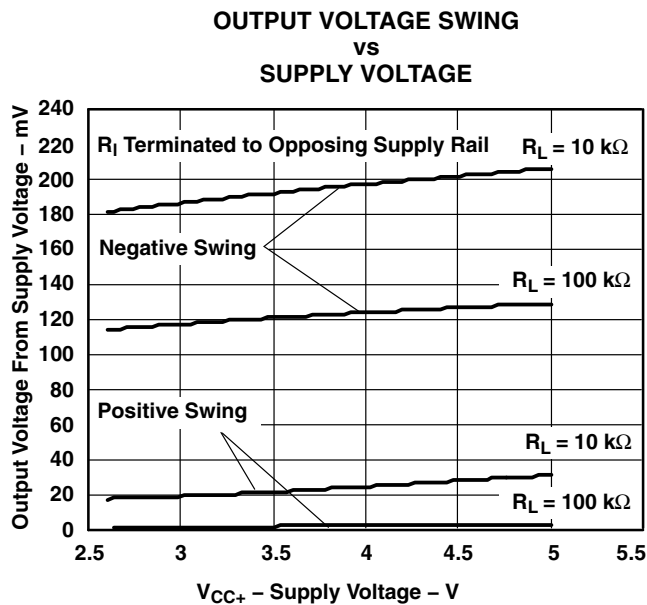


Figure 7

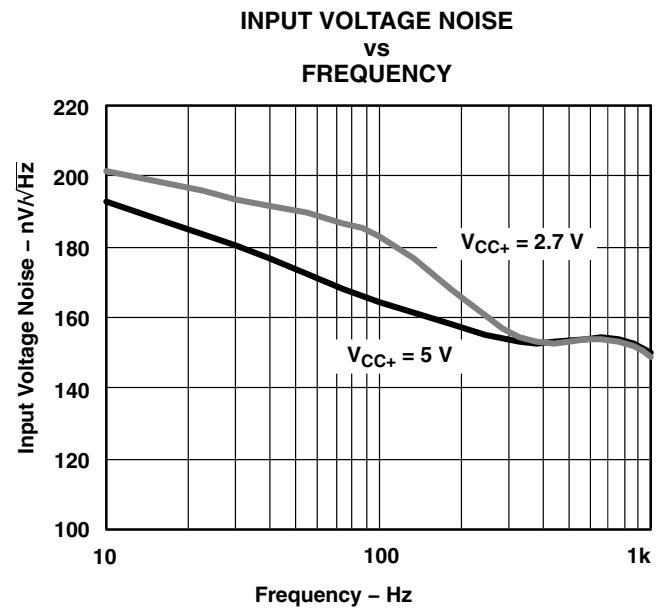


Figure 8

LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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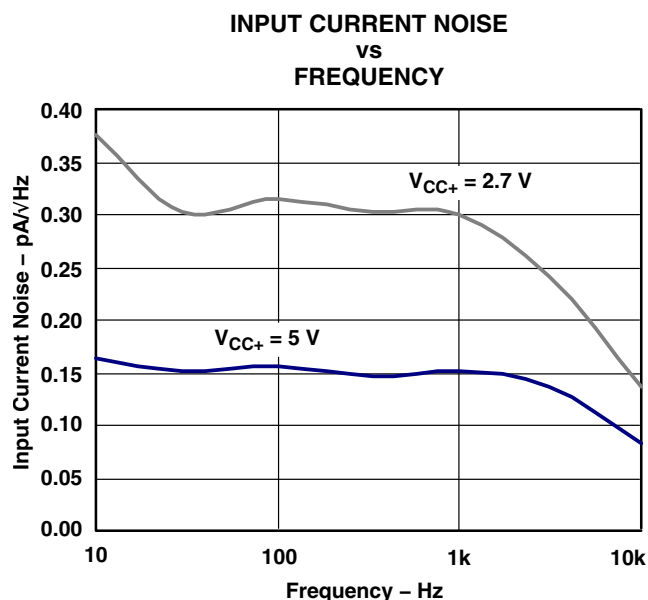


Figure 9

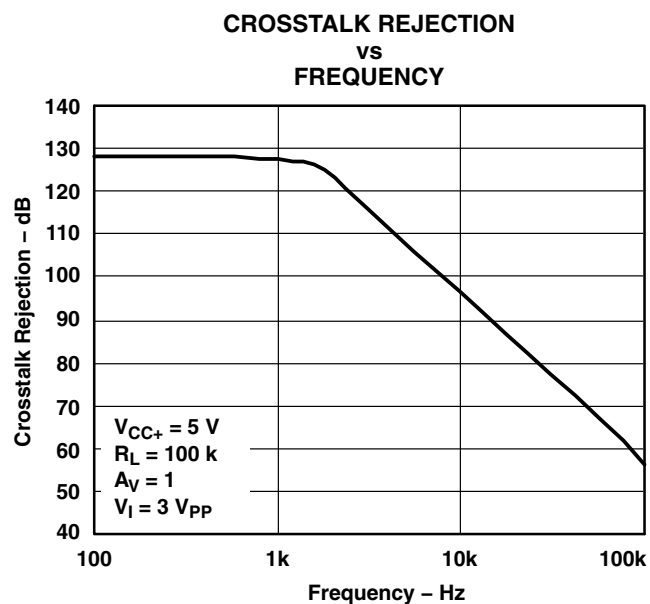


Figure 10

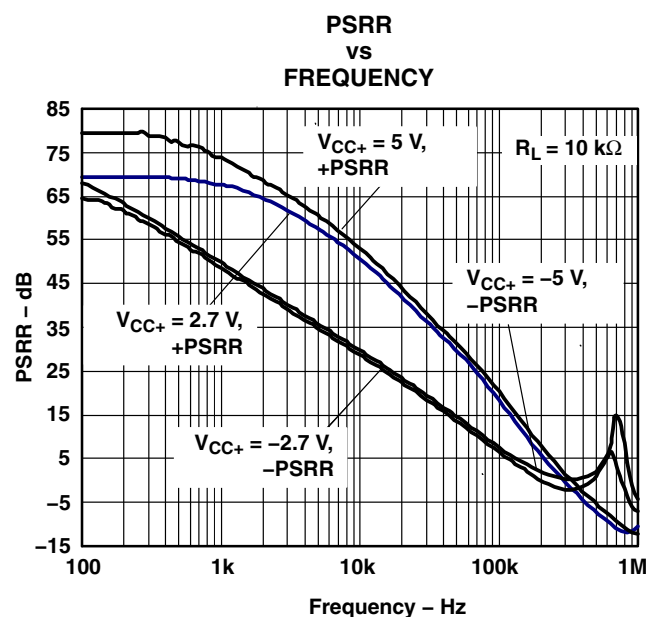


Figure 11

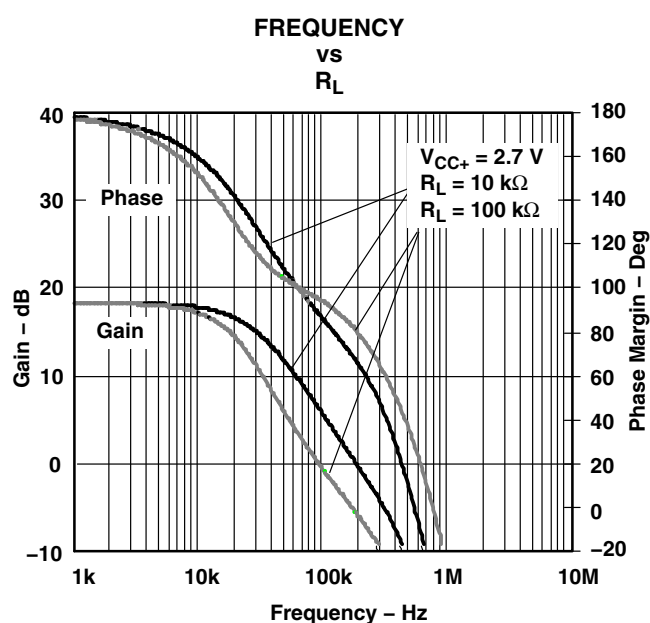


Figure 12

**LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD
GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT
OPERATIONAL AMPLIFIERS**

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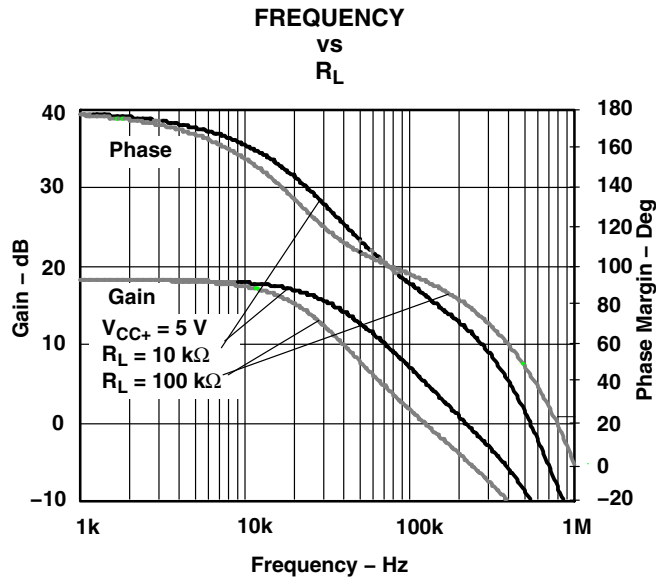


Figure 13

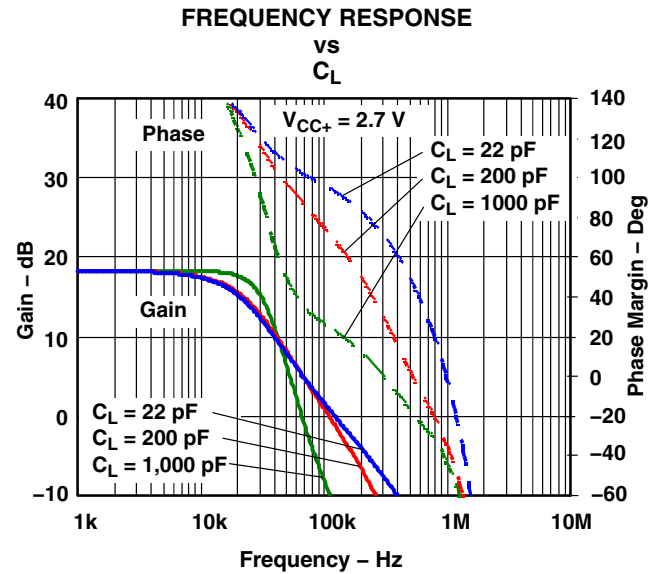


Figure 14

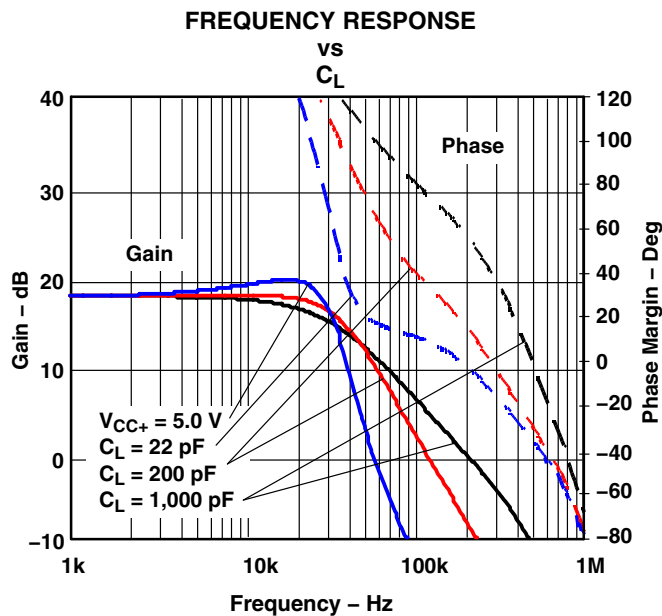


Figure 15

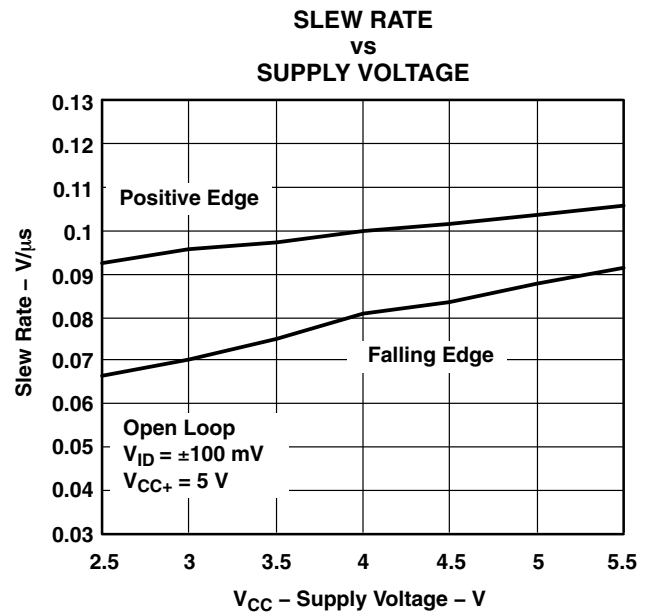


Figure 16

LPV321 SINGLE, LPV358 DUAL, LPV324 QUAD GENERAL-PURPOSE, LOW-VOLTAGE, LOW-POWER, RAIL-TO-RAIL OUTPUT OPERATIONAL AMPLIFIERS

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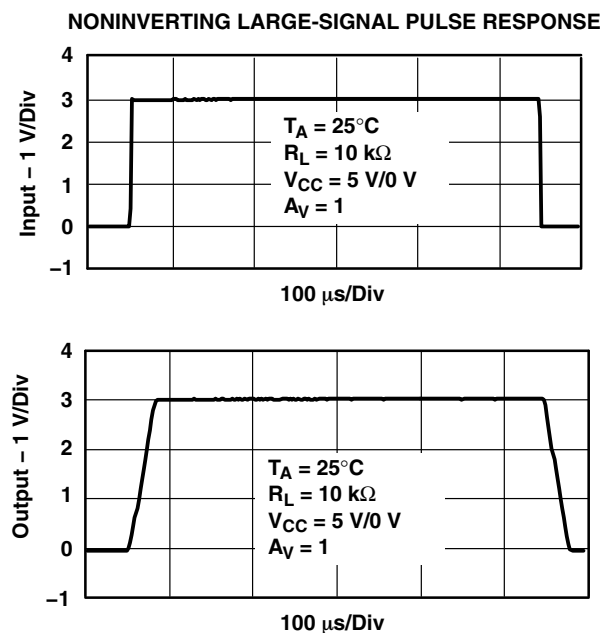


Figure 17

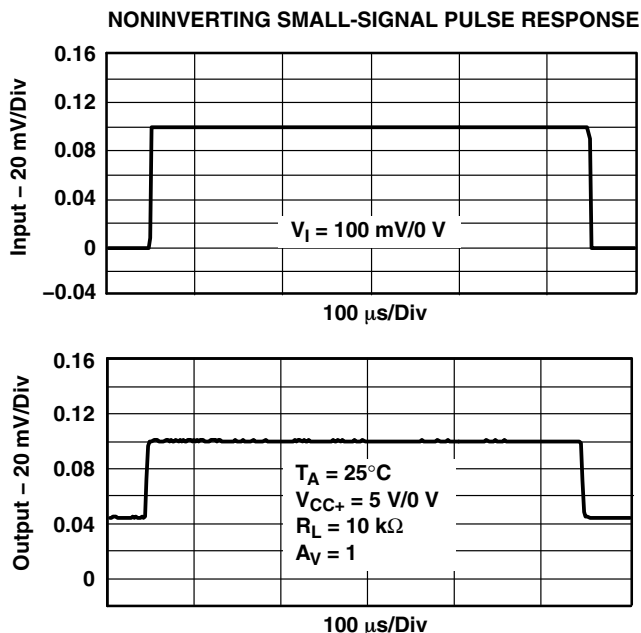


Figure 18

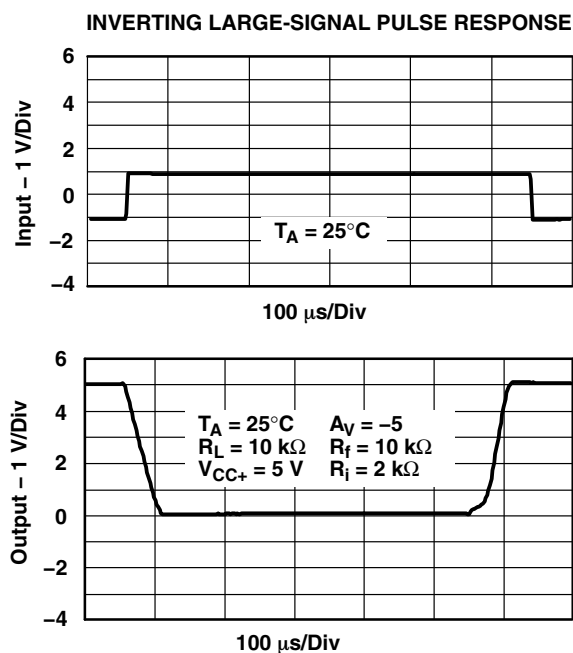


Figure 19

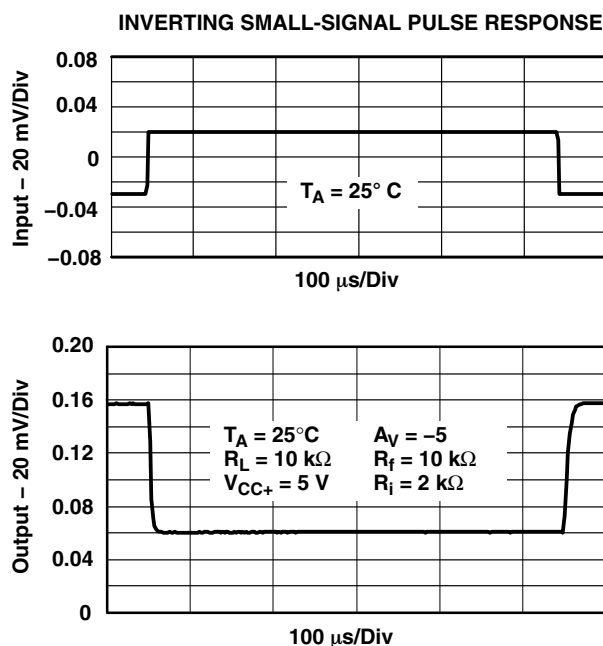


Figure 20



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LPV321DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV321IDCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LPV324DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324ID	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IDRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324IPWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PWG4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV324PWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LPV324PWRG4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DDURE4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDDUR	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDDURE4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDDURG4	ACTIVE	VSSOP	DDU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LPV358IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LPV358IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

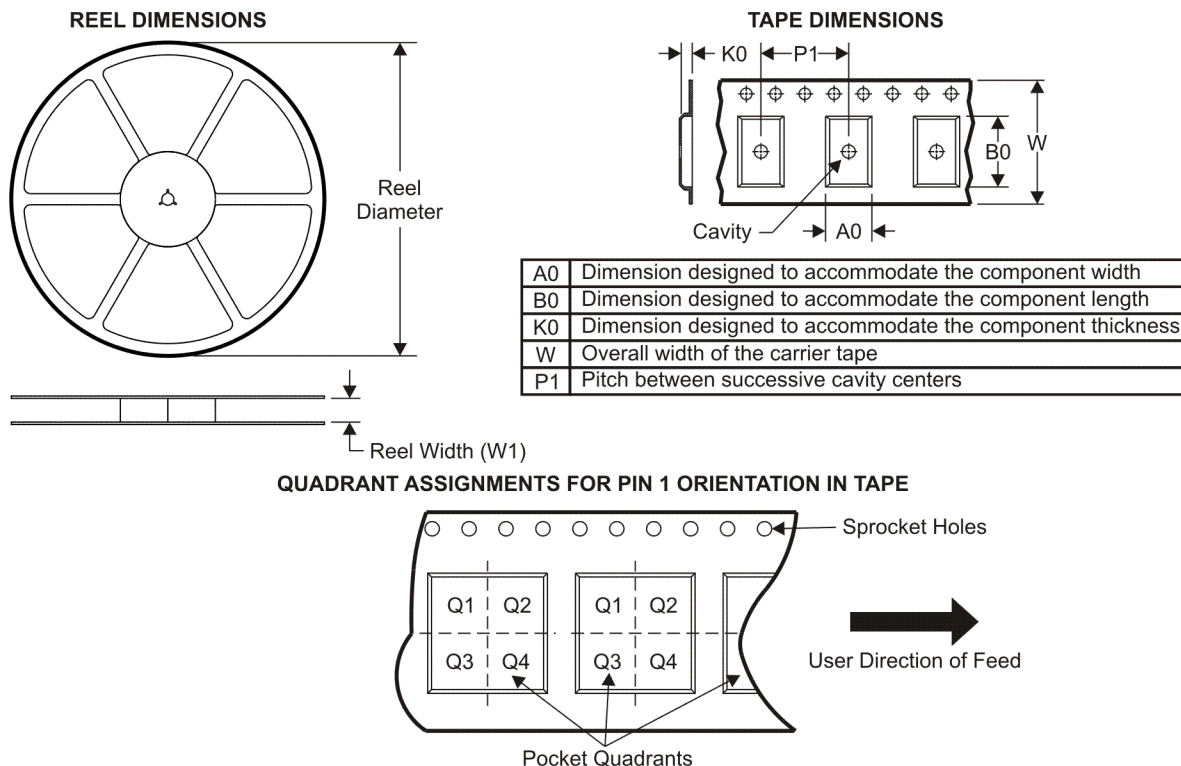
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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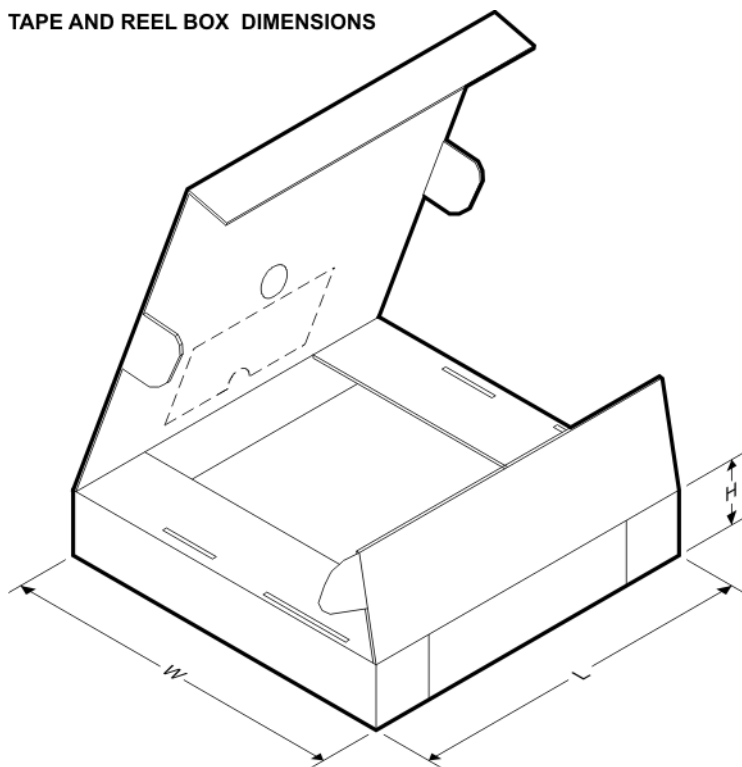
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LPV321DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LPV321DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LPV321IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
LPV321IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
LPV324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LPV324IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LPV324IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LPV324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LPV358DDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LPV358DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LPV358IDDUR	VSSOP	DDU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
LPV358IDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LPV358IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

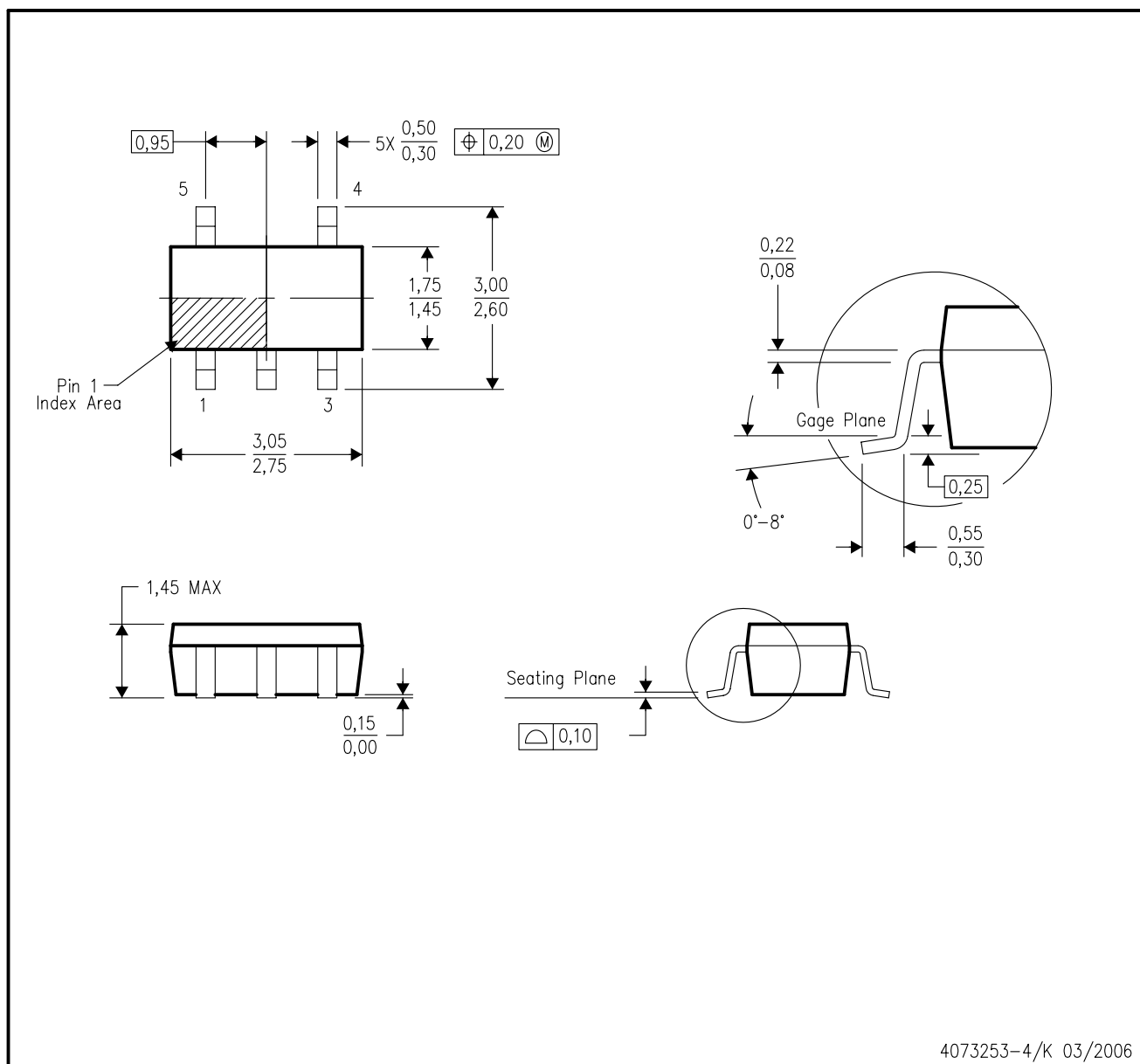


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LPV321DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LPV321DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LPV321IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
LPV321IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
LPV324DR	SOIC	D	14	2500	346.0	346.0	33.0
LPV324IDR	SOIC	D	14	2500	346.0	346.0	33.0
LPV324IPWR	TSSOP	PW	14	2000	346.0	346.0	29.0
LPV324PWR	TSSOP	PW	14	2000	346.0	346.0	29.0
LPV358DDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LPV358DGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
LPV358DR	SOIC	D	8	2500	340.5	338.1	20.6
LPV358IDUR	VSSOP	DDU	8	3000	202.0	201.0	28.0
LPV358IDGKR	MSOP	DGK	8	2500	358.0	335.0	35.0
LPV358IDR	SOIC	D	8	2500	340.5	338.1	20.6

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

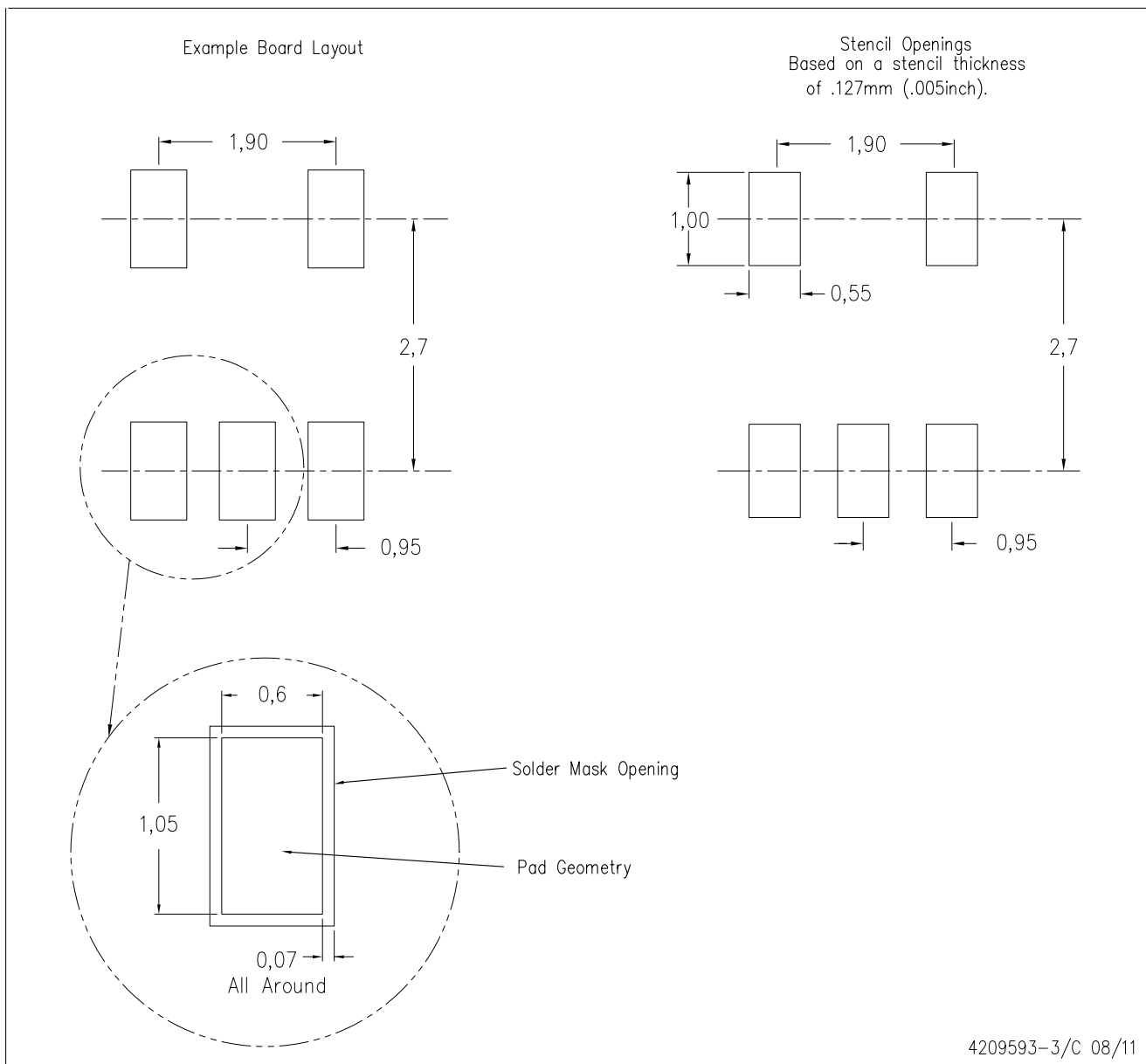


4073253-4/K 03/2006

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

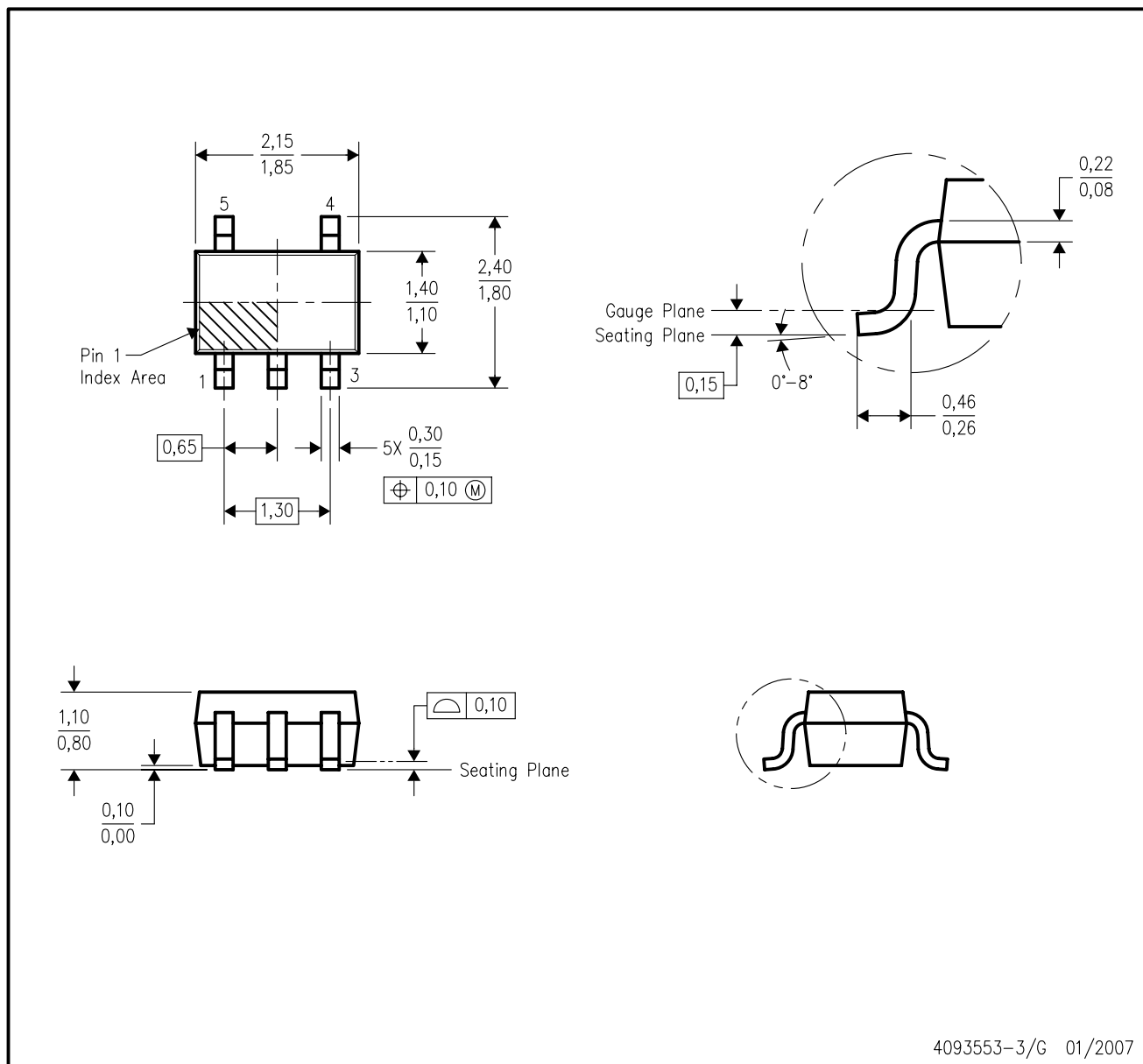
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE

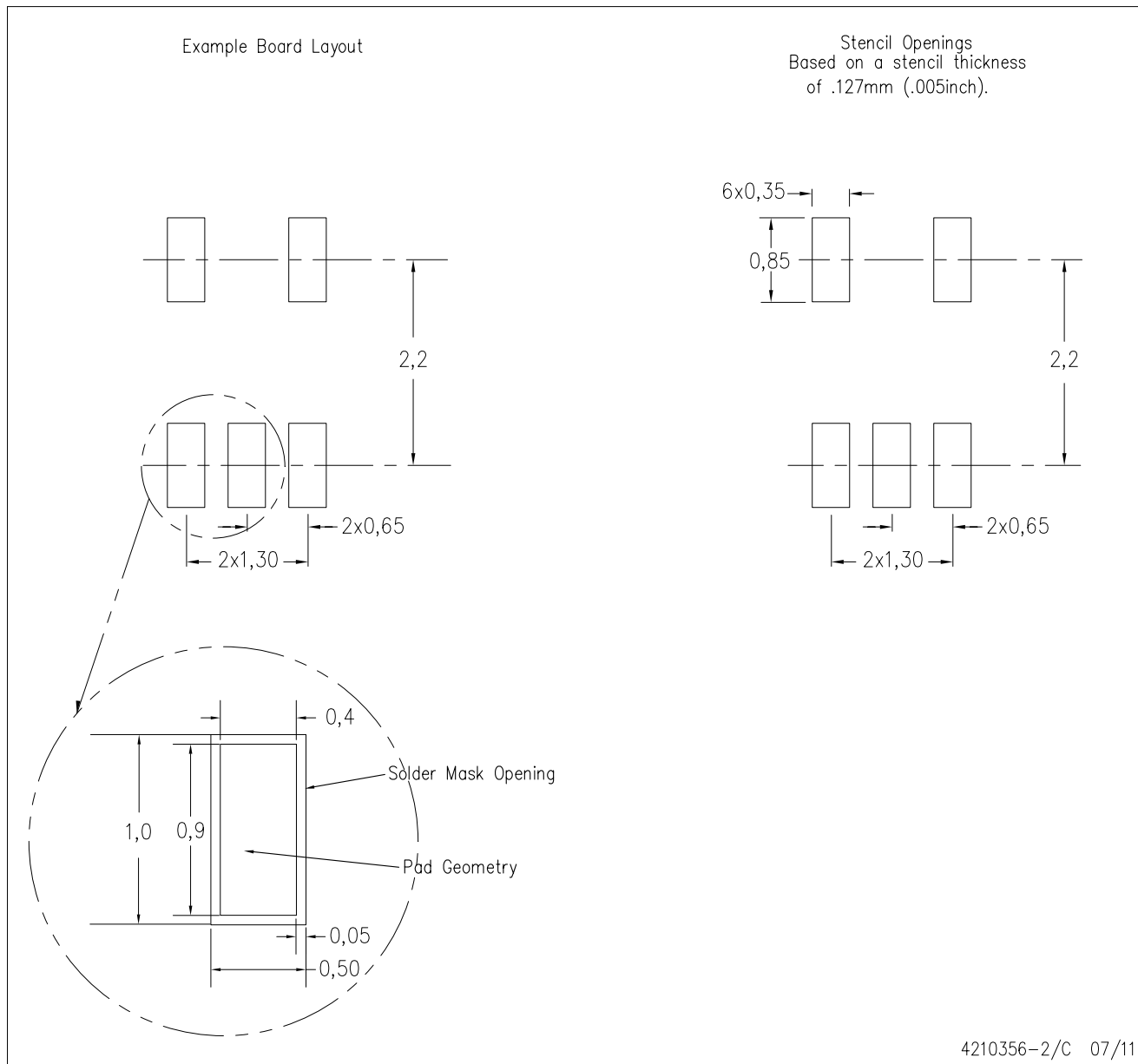


4093553-3/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

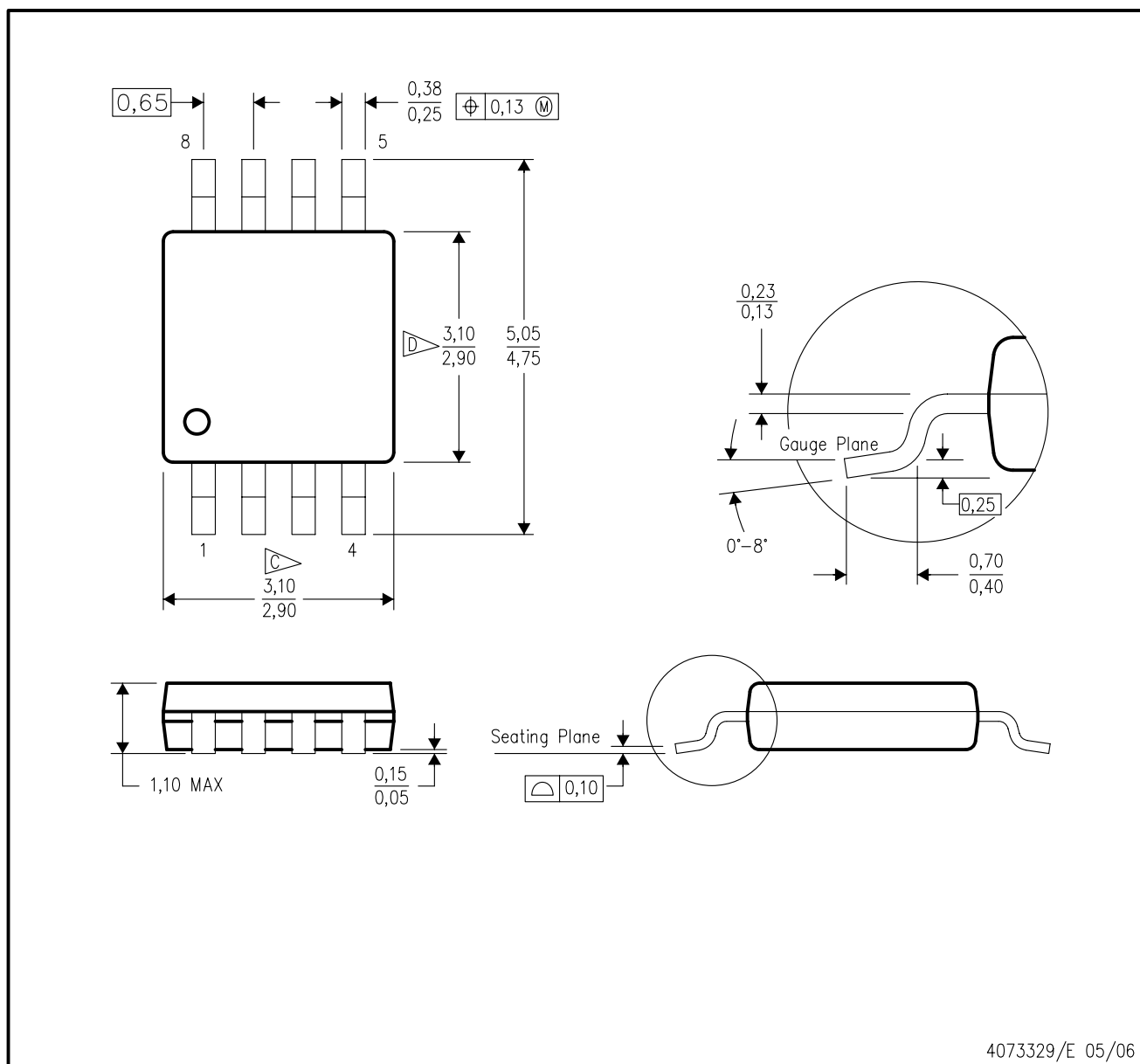
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

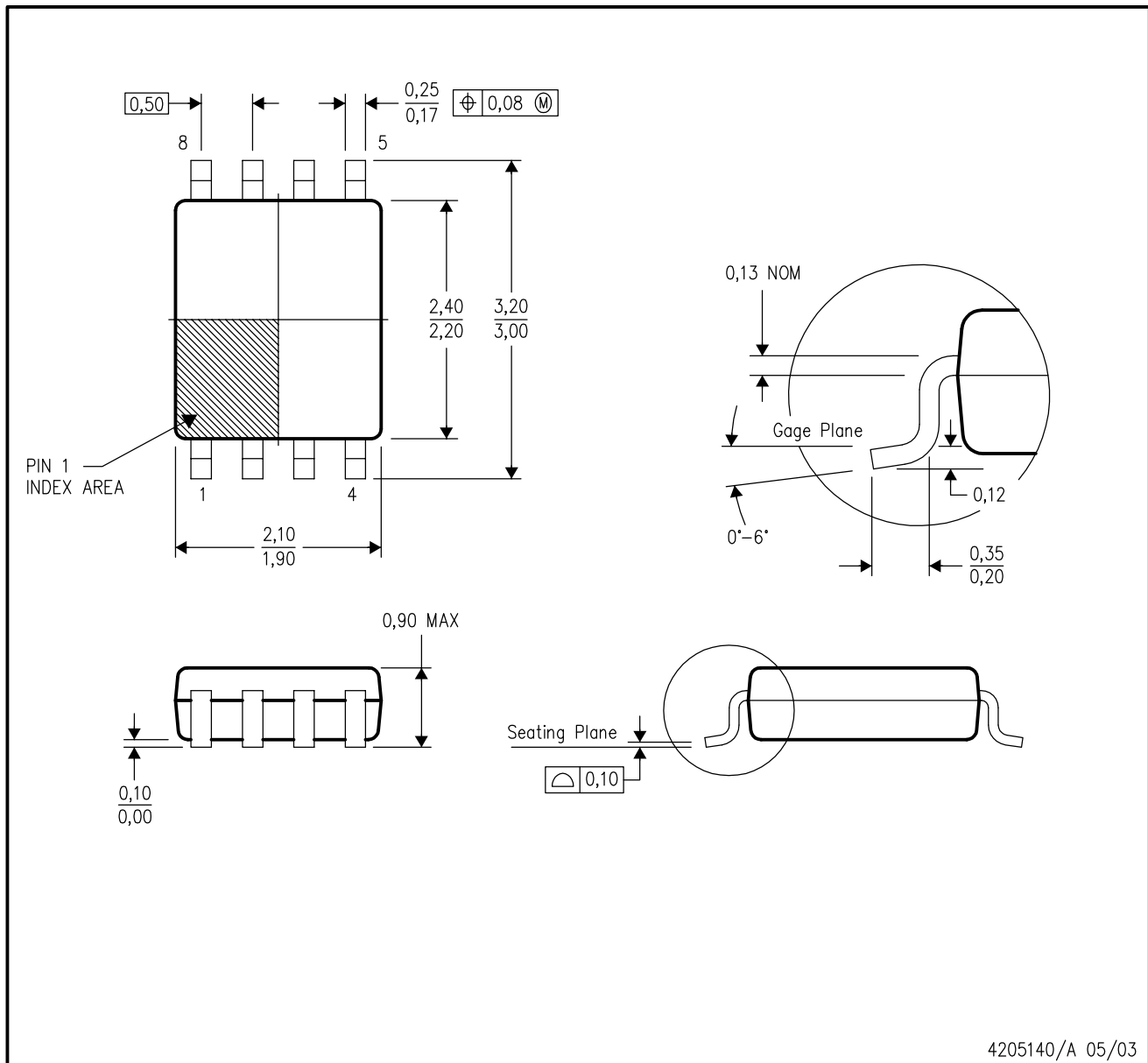


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DDU (R-PDSO-G8)

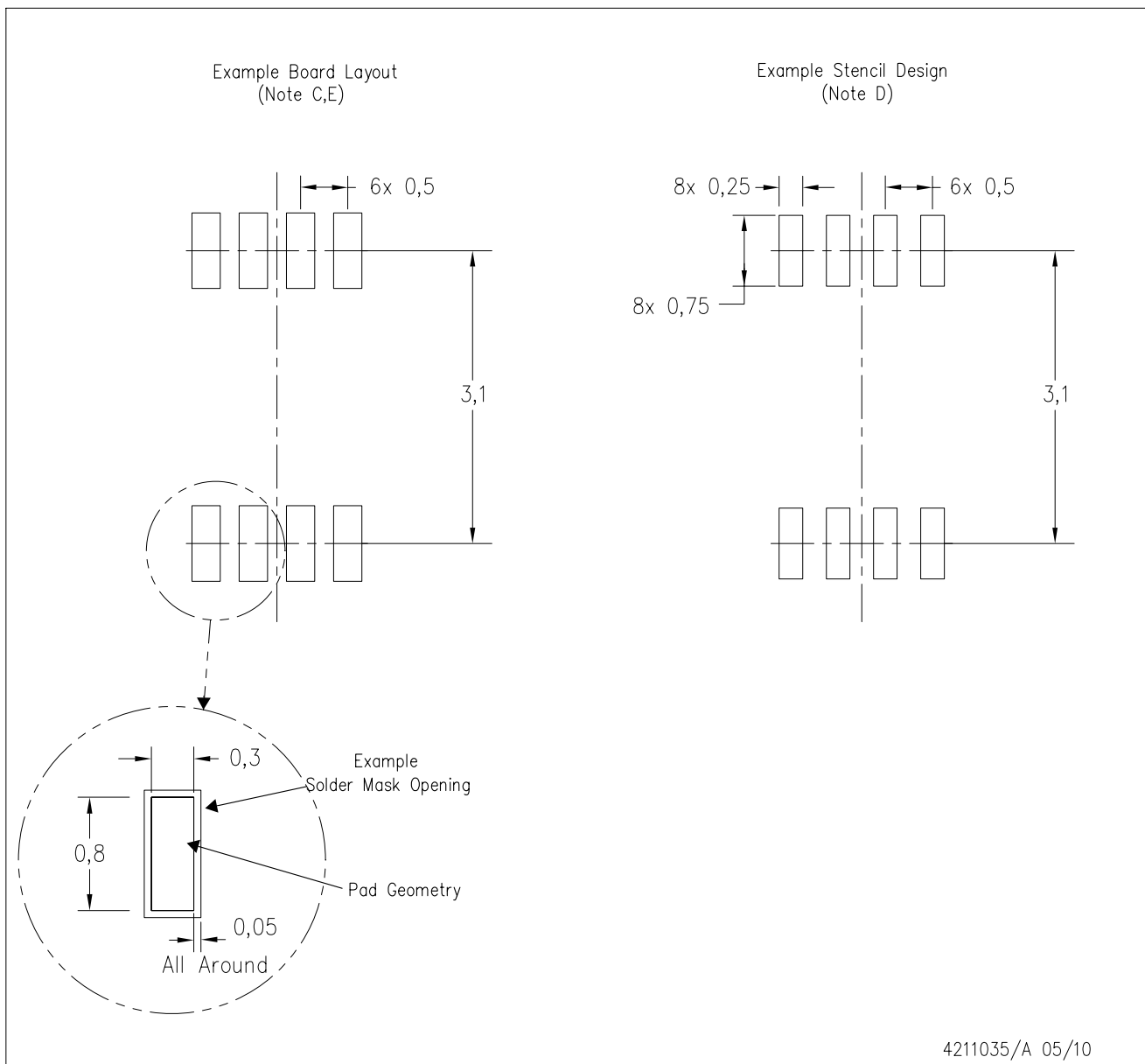
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation CA.

DDU (S-PDSO-G8)

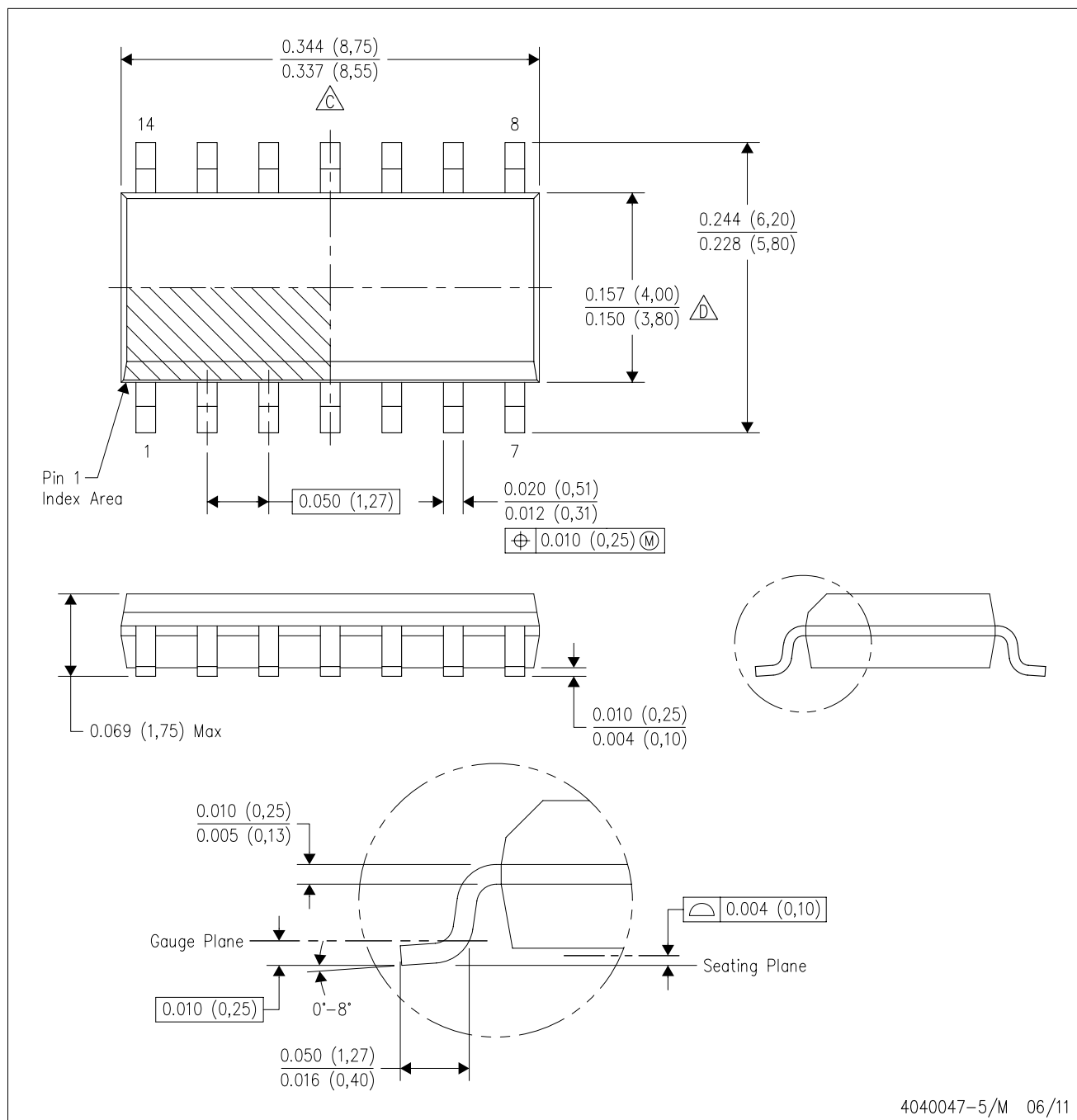
PLASTIC SMALL OUTLINE PACKAGE (DIE UP)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

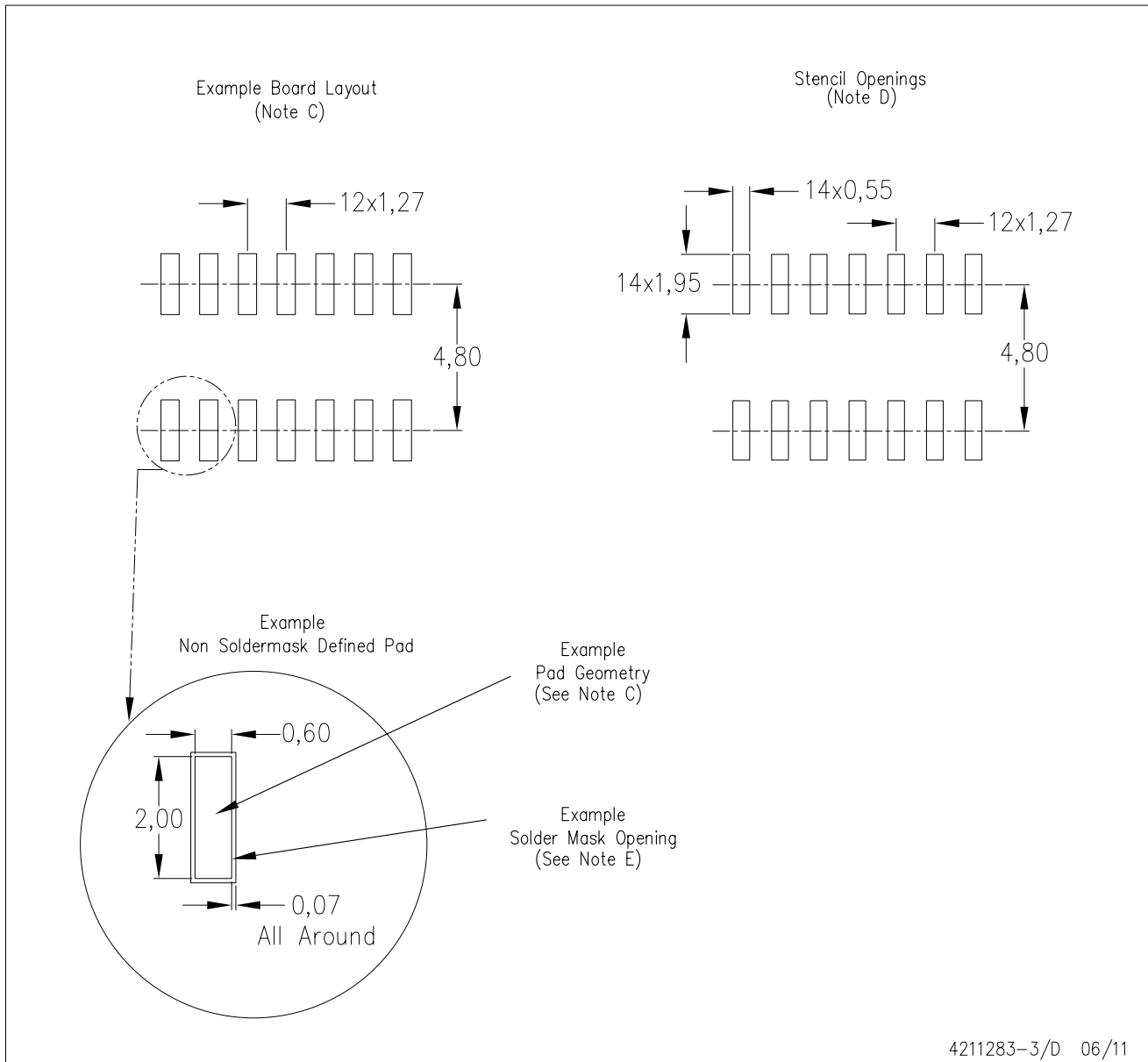


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

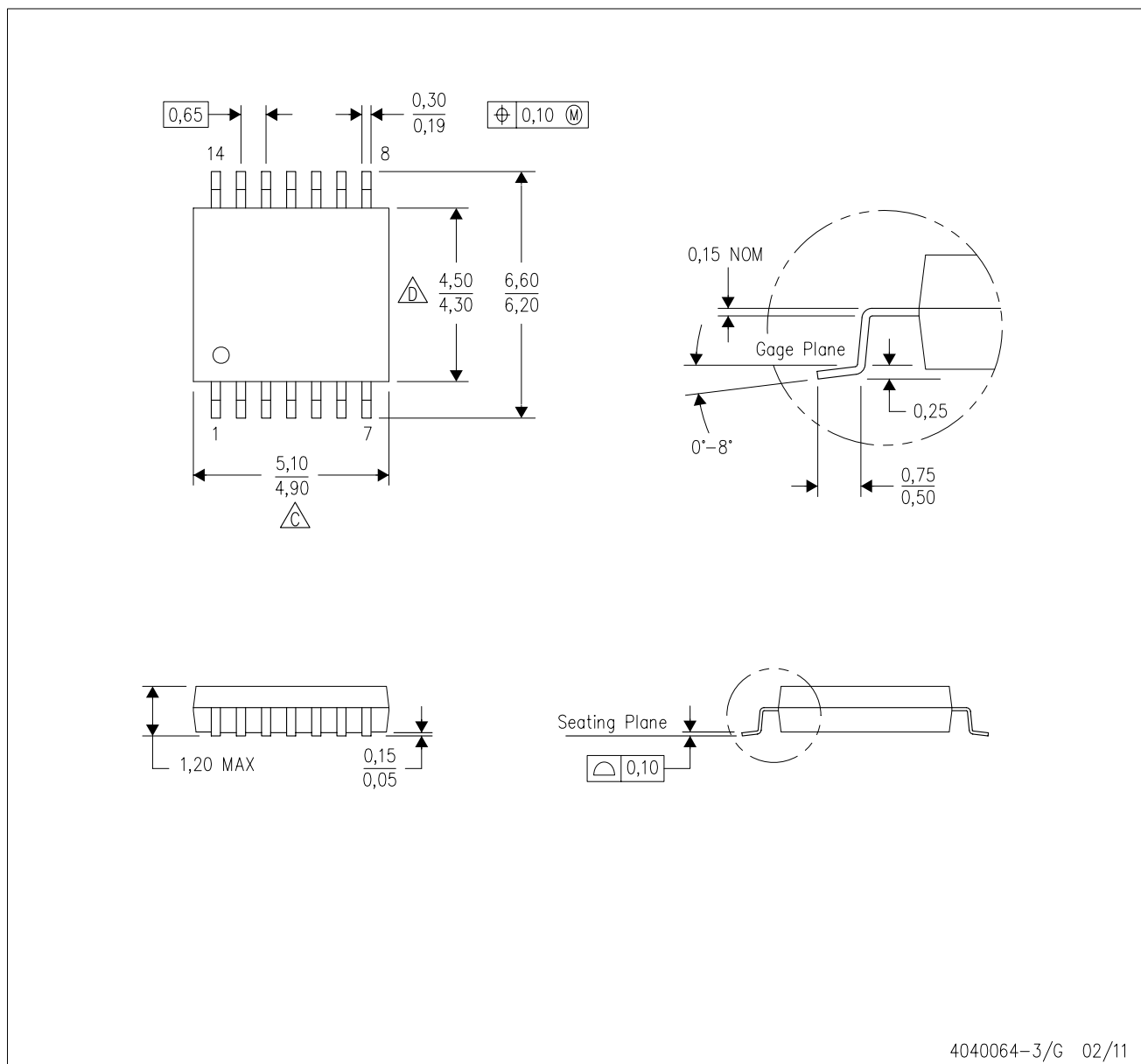
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

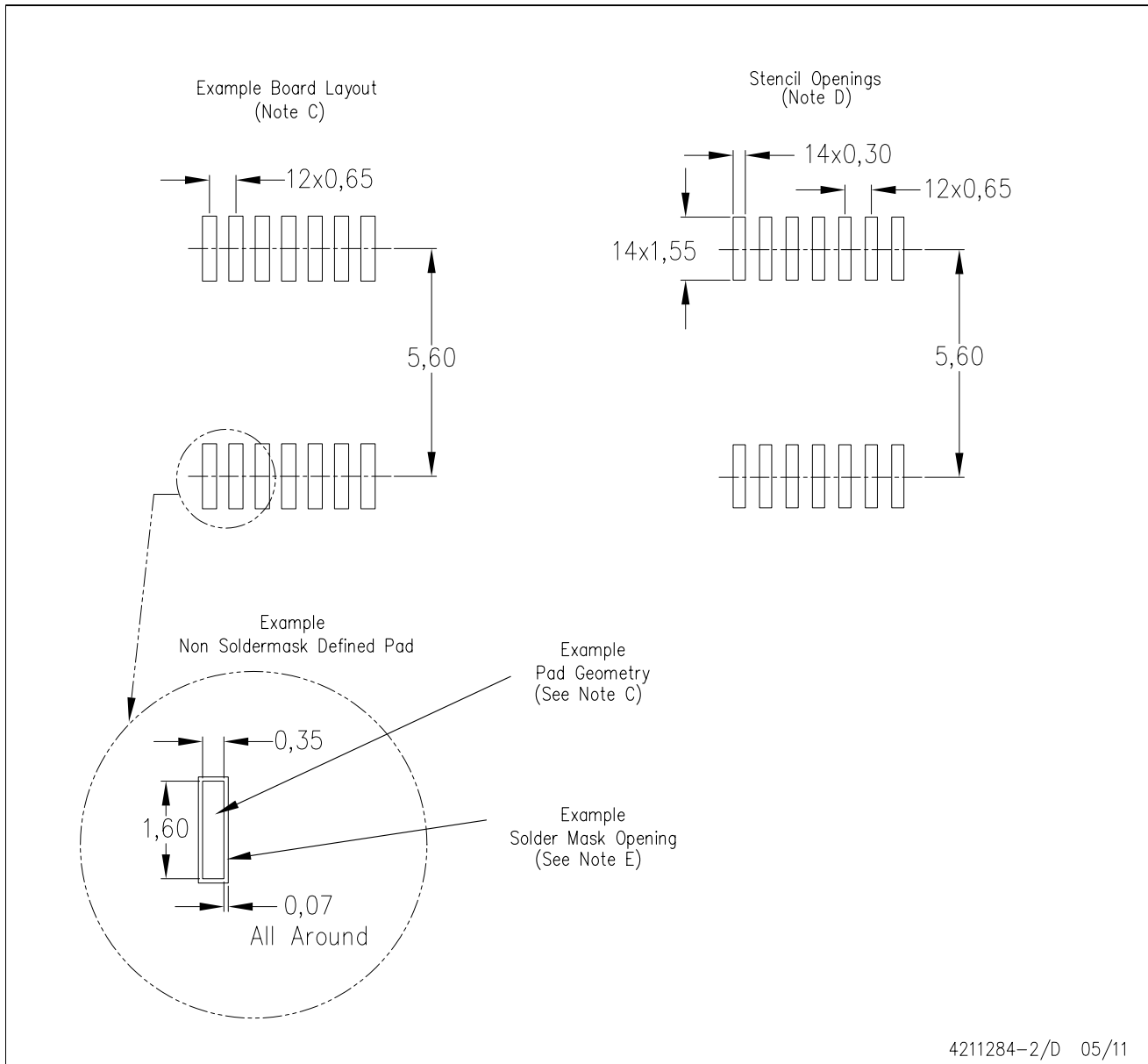
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

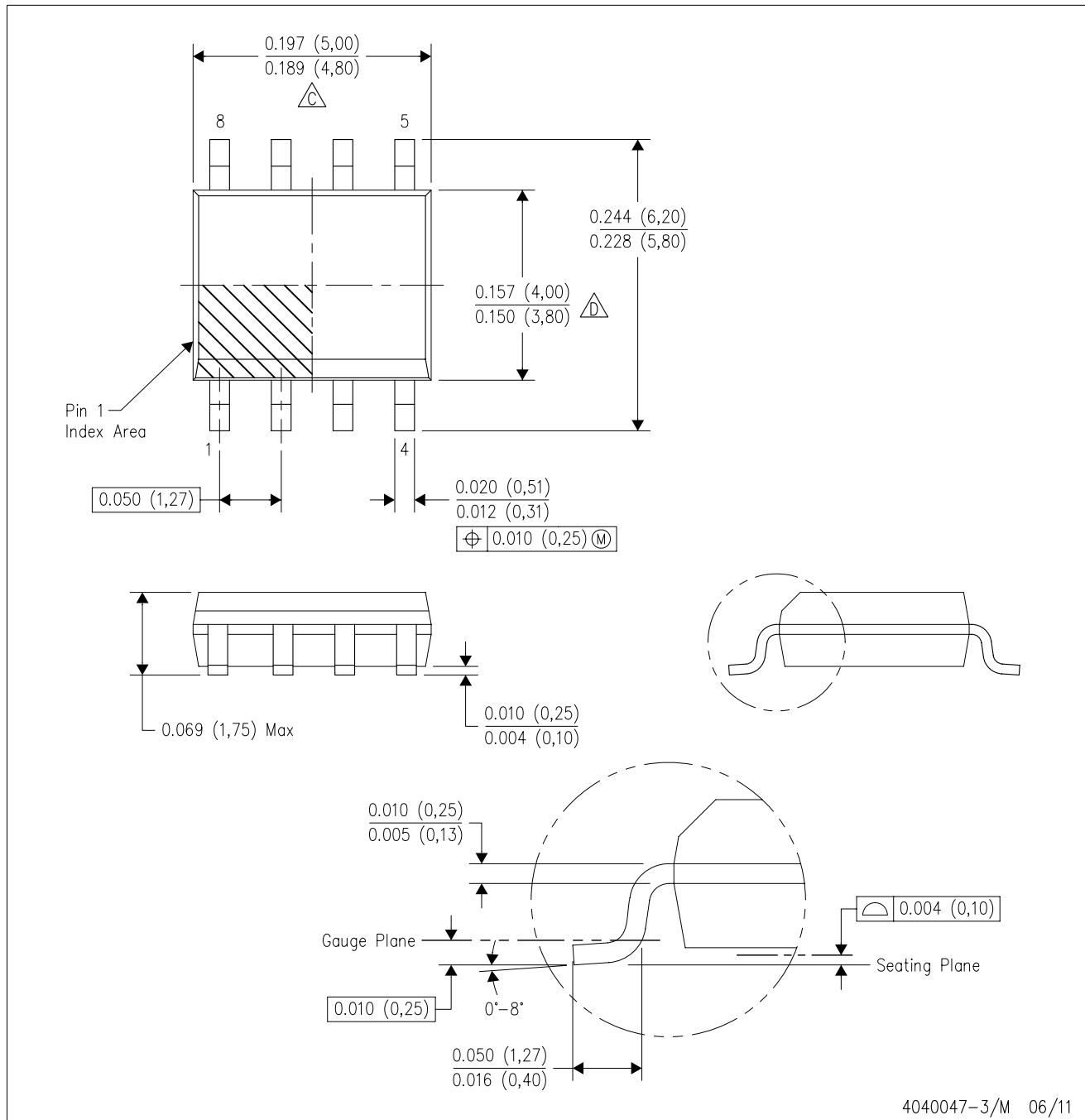
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

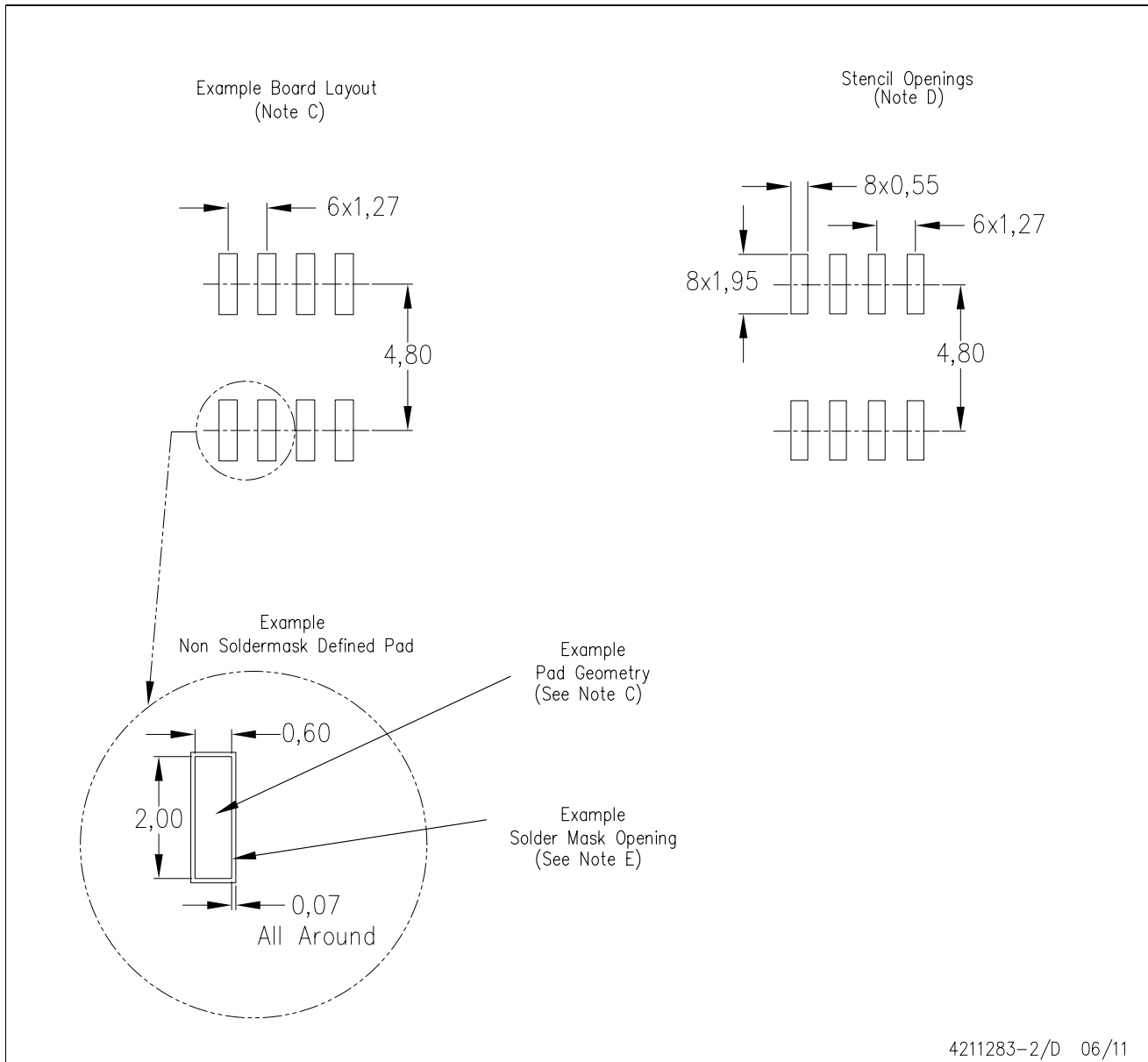
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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