

#### LP358, LP2904 ULTRA-LOW-POWER DUAL OPERATIONAL AMPLIFIERS

10UT [

1IN- 🛮 2

1IN+ **∏** 3

GND ∏ 4

D OR DGK PACKAGE

(TOP VIEW)

8 Vcc

7 🛮 20UT

□ 2IN+

6 ¶ 2IN−

SLOS475-AUGUST 2005

#### **FEATURES**

- Low Supply Current . . . 85 μA Typ
- Low Offset Voltage . . . 2 mV Typ
- Low Input Bias Current . . . 2 nA Typ
- Input Common Mode to GND
- Wide Supply Voltage . . . 3 V < V<sub>CC</sub> < 32 V
- Pin Compatible With LM358

#### **APPLICATIONS**

- LCD Displays
- Portable Instrumentation
- Sensor/Metering Equipment
- Consumer Electronics (MP3 Players, Toys)
- Power Supplies

#### **DESCRIPTION/ORDERING INFORMATION**

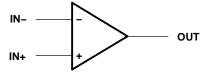
The LP358 and LP2904 are dual low-power operational amplifiers especially suited for battery-operated applications. Good input specifications and wide supply-voltage range still are achieved, despite the ultra-low supply current. Single-supply operation is achieved with an input common-mode range that includes GND.

The LP358 and LP2904 are ideal in applications where wide supply voltage and low power are more important than speed and bandwidth. These applications include portable instrumentation, LCD displays, consumer electronics (MP3 players, toys, etc.), and power supplies.

#### ORDERING INFORMATION

T <sub>A</sub>	PACK	AGE <sup>(1)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC - D	Tube of 75	LP358D	LP358
	3010 - 0	Reel of 2500	LP358DR	LF330
0°C to 70°C		Tube of 100	LP358DGK	
	VSSOP – DGK	Reel of 250	LP358DGKT	PREVIEW
		Reel of 2500	LP358DGKR	
	SOIC - D	Tube of 75	LP2904D	PREVIEW
		Reel of 2500	LP2904DR	PREVIEW
-40°C to 85°C		Tube of 100	LP2904DGK	
	VSSOP - DGK	Reel of 250	LP2904DGKT	PREVIEW
		Reel of 2500	LP2904DGKR	

#### **SYMBOL (EACH AMPLIFIER)**



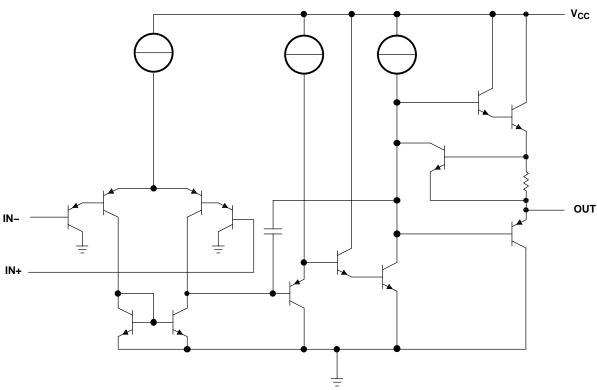
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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## SCHEMATIC (EACH AMPLIFIER)



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range (2)		±16 or 32	V	
$V_{ID}$	Differential input voltage (3)		±32	V	
$V_{I}$	Input voltage (either input)	-0.3	32	V	
	Duration of output short circuit (one amplifier) to ground		Unlimited		
0	Deckers thermal impedance (5) (6)	D package		97	°C/W
$\theta_{JA}$	Package thermal impedance (5) (6)	DGK package		172	°C/VV
TJ	Operating virtual junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values (except differential voltages and V<sub>CC</sub> specified for the measurement of I<sub>OS</sub>) are with respect to the network GND.
- (3) Differential voltages are at IN+, with respect to IN-.
- 4) Short circuits from outputs to V<sub>CC</sub> can cause excessive heating and eventual destruction.
- (5) Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

#### **ESD Protection**

TEST CONDITIONS	TYP	UNIT
Human-Body Model	±2	kV



SLOS475-AUGUST 2005

#### **Electrical Characteristics**

 $\rm T_A$  = 25°C,  $\rm V_{CC}$  = 5 V,  $\rm V_{IC}$  = V $_{CC}/2,$   $\rm R_L$  = 100 k $\Omega$  to GND (unless otherwise noted)

	DADAMETED	TEST CONDITIONS(1)	T (2)	L	P358		L	P2904		UNIT
	PARAMETER	TEST CONDITIONS <sup>(1)</sup>	T <sub>A</sub> <sup>(2)</sup>	MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	UNII
V	Innut offeet valtage		25°C		2	4		2	4	m)/
$V_{IO}$	Input offset voltage		Full range			9			10	mV
_	Input bigg gurrent		25°C		2	10		2	20	nA
I <sub>IB</sub>	Input bias current		Full range			20			40	ΠA
-	Innut offeet ourrent		25°C		0.2	2		0.5	4	nA
I <sub>IO</sub>	Input offset current		Full range			4			8	ΠA
۸	Large-signal	$R_L = 10 \text{ k}\Omega \text{ to GND},$	25°C	50	100		40	70		V/mV
$A_V$	voltage gain	V <sub>CC</sub> = 30 V	Full range	40			30			V/IIIV
CMRR	Common-mode	V <sub>CC</sub> = 30 V,	25°C	80	90		80	90		dB
CIVIKK	rejection ratio	$V_{IC} = 0 \text{ V to } V_{CC} - 1.5 \text{ V}$	Full range	75			75			uБ
le.	Power-supply	V 5 V to 20 V	25°C	80	90		80	90		\/
k <sub>VSR</sub>	rejection ratio	$V_{CC} = 5 \text{ V to } 30 \text{ V}$	Full range	75			75			V
_	0	R₁ = ∞	25°C		85	150		85	150	μΑ
I <sub>CC</sub>	Supply current	KL = ∞	Full range			250			275	μΑ
V	,, Output voltage	$I_L = 0.35 \text{ mA to GND},$	25°C	3.4	3.6		3.4	3.6		V
V <sub>OH</sub>	swing (high)	$V_{IC} = 0 \text{ V}$	Full range	V <sub>CC</sub> – 1.9			V <sub>CC</sub> - 1.9			V
V	Output voltage	$I_L = 0.35 \text{ mA from } V_{CC}$	25°C	0.82	0.7		0.82	0.7		V
$V_{OL}$	swing (low)	$V_{IC} = 0 V$	Full range	1			1			V
	Output source	V <sub>O</sub> = 3 V, V <sub>ID</sub> = 1 V	25°C	7	10		7	10		- mA
I <sub>O</sub>	current	$V_O = 3 V$ , $V_{ID} = 1 V$	Full range	4			4			
		V 45V V 4V	25°C	4	5		4	5		
	Output sink surrent	$V_{O} = 1.5 \text{ V}, V_{ID} = -1 \text{ V}$	Full range	3			3			A
I <sub>O</sub>	Output sink current	$V_{O} = 1.5 \text{ V}, V_{ID} = -1 \text{ V},$	25°C	2	4		2	4		mA
		$V_{IC} = 0 V$	Full range	1			1			
	Outrout about to CND	V 4.V	25°C		20	35		20	35	A
los,gnd	Output short to GND	$V_{ID} = 1 V$	Full range			40			40	mA
I Outmant also at 1 a 34	Output short to V	V <sub>ID</sub> = -1 V	25°C		15	30		15	30	m۸
l <sub>os,vcc</sub>	Output short to V <sub>CC</sub>	V <sub>ID</sub> = -1 V	Full range			45			45	mA
$\alpha V_{IO}$	Input offset voltage drift		25°C		10			10		μV/°C
$\alpha I_{IO}$	Input offset current drift		25°C		10			10		pA/°C

<sup>(1)</sup> For full-range temperature limits: V<sub>CC</sub> = 3 V to 32 V, V<sub>ICR</sub> = 0 V to V<sub>CC</sub> - 1.5 V (unless otherwise noted)
(2) Full range is 0°C to 70°C for LP358 and -40°C to 85°C for LP2904.
(3) All typical values are at T<sub>A</sub> = 25°C.

### **Operating Conditions**

 $V_{CC} = \pm 15 \text{ V}, T_A = 25^{\circ}\text{C}$ 

	TYP	UNIT	
GBW	Gain bandwidth product	100	kHz
SR	Slew rate	50	V/ms

#### PACKAGE OPTION ADDENDUM

com 23-Apr-2007

#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
LP2904D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2904DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2904DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2904DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP2904DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP358D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP358DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP358DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP358DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP358DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LP358DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## **PACKAGE OPTION ADDENDUM**



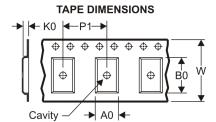
23-Apr-2007

to Customer on an annual basis.



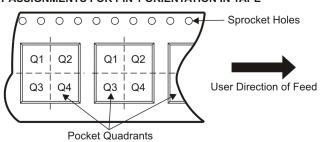
#### TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

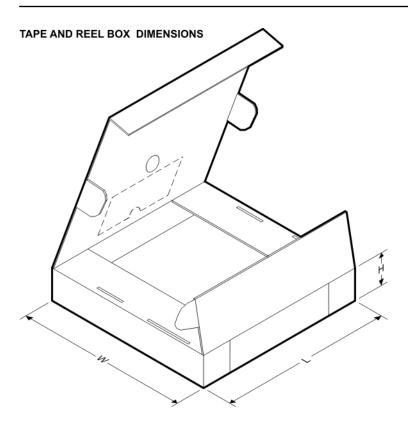


\*All dimensions are nominal

	Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	LP2904DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ſ	LP358DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

## PACKAGE MATERIALS INFORMATION

19-Mar-2008

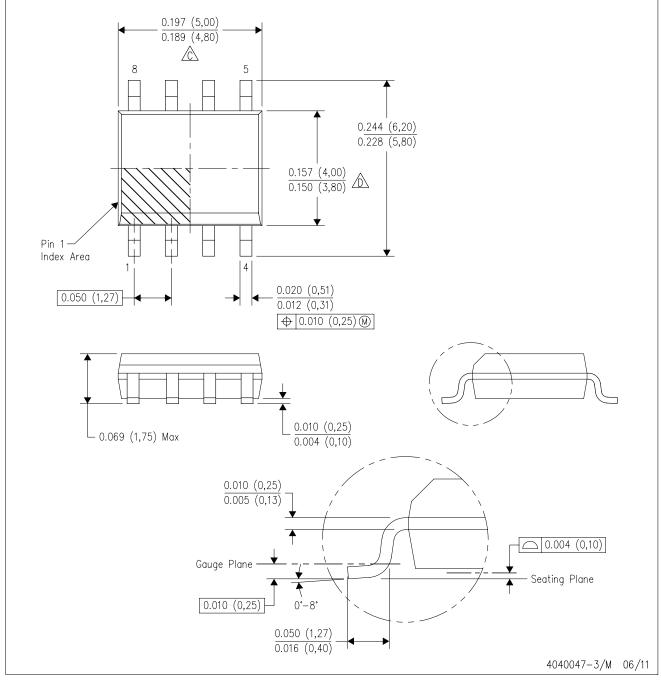


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2904DR	SOIC	D	8	2500	340.5	338.1	20.6
LP358DR	SOIC	D	8	2500	340.5	338.1	20.6

# D (R-PDSO-G8)

### PLASTIC SMALL OUTLINE



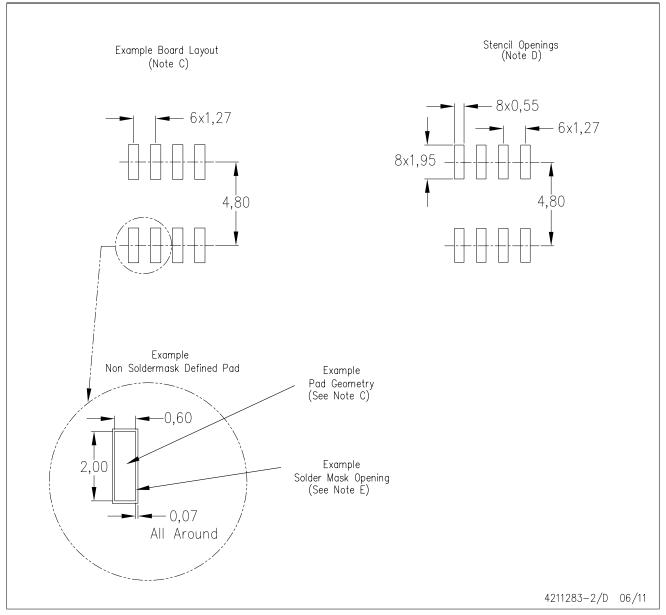
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.



# D (R-PDSO-G8)

## PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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