# SoundPlus™ High-Performance, Bipolar-Input AUDIO OPERATIONAL AMPLIFIERS

**Check for Samples: OPA1611 OPA1612**

## FEATURES

- **SUPERIOR SOUND QUALITY**
- **ULTRALOW NOISE: 1.1nV/√Hz at 1kHz**
- **ULTRALOW DISTORTION: 0.000015% AT 1kHz**
- **HIGH SLEW RATE: 27V/µs**
- **WIDE BANDWIDTH: 40MHz (G = +1)**
- **HIGH OPEN-LOOP GAIN: 130dB**
- **UNITY GAIN STABLE**
- **LOW QUIESCENT CURRENT: 3.6mA (Single), 7.2mA (Dual)**
- **RAIL-TO-RAIL OUTPUT**
- **WIDE SUPPLY RANGE: ±2.25V to ±18V**
- **SINGLE AND DUAL VERSIONS AVAILABLE**

## APPLICATIONS

- **PROFESSIONAL AUDIO EQUIPMENT**
- **MICROPHONE PREAMPLIFIERS**
- **ANALOG AND DIGITAL MIXING CONSOLES**
- **BROADCAST STUDIO EQUIPMENT**
- **AUDIO TEST AND MEASUREMENT**
- **HIGH-END A/V RECEIVERS**

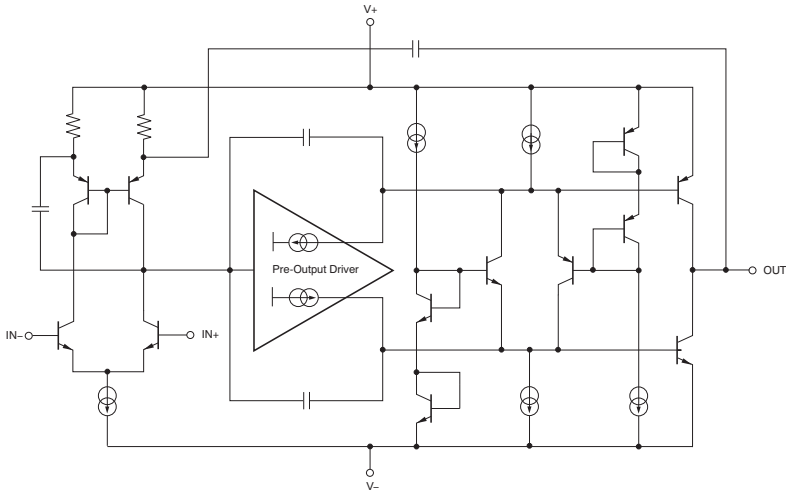
## DESCRIPTION

The OPA1611 (single) and OPA1612 (dual) bipolar-input operational amplifiers achieve very low 1.1nV/√Hz noise density with an ultralow distortion of 0.000015% at 1kHz. The OPA1611 and OPA1612 offer rail-to-rail output swing to within 600mV with a 2kΩ load, which increases headroom and maximizes dynamic range. These devices also have a high output drive capability of ±30mA.

These devices operate over a very wide supply range of ±2.25V to ±18V, on only 3.6mA of supply current per channel. The OPA1611 and OPA1612 op amps are unity-gain stable and provide excellent dynamic behavior over a wide range of load conditions.

The dual version features completely independent circuitry for lowest crosstalk and freedom from interactions between channels, even when overdriven or overloaded.

Both the OPA1611 and OPA1612 are available in SO-8 packages and are specified from –40°C to +85°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

| | | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage | $V_S$ = (V+) – (V–) | 40 | V |
| Input Voltage | | (V–) – 0.5 to (V+) + 0.5 | V |
| Input Current (All pins except power-supply pins) | | ±10 | mA |
| Output Short-Circuit(2) | | Continuous | |
| Operating Temperature | ($T_A$) | –55 to +125 | °C |
| Storage Temperature | ($T_A$) | –65 to +150 | °C |
| Junction Temperature | ($T_J$) | 200 | °C |
| ESD Ratings | Human Body Model (HBM) | 3000 | V |
| | Charged Device Model (CDM) | 1000 | V |
| | Machine Model (MM) | 200 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Short-circuit to $V_S$/2 (ground in symmetrical dual supply setups), one amplifier per package.

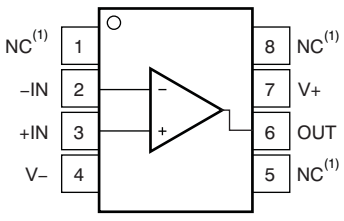
## PACKAGE INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING |
|---|---|---|---|
| OPA1611 | SO-8 | D | TI OPA 1611A |
| OPA1612 | SO-8 | D | TI OPA 1612A |

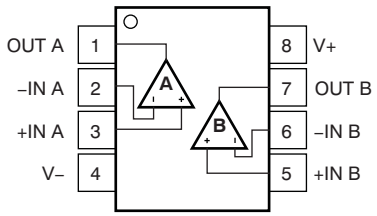
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

## PIN CONFIGURATIONS

**D PACKAGE**
**OPA1611, SO-8**
**(TOP VIEW)**




**D PACKAGE**
**OPA1612, SO-8**
**(TOP VIEW)**




(1) NC denotes no internal connection. Pin can be left floating or connected to any voltage between (V–) and (V+).

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±2.25V to ±18V

At $T_A$ = +25°C and $R_L$ = 2kΩ, unless otherwise noted. $V_{CM}$ = $V_{OUT}$ = midsupply, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to +85°C.

| PARAMETER | | CONDITIONS | OPA1611AI, OPA1612AI | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **AUDIO PERFORMANCE** | | | | | | |
| Total Harmonic Distortion + Noise | THD+N | G = +1, f = 1kHz, $V_O$ = 3$V_{RMS}$ | | 0.000015 | | % |
| | | | | –136 | | dB |
| Intermodulation Distortion | IMD | G = +1, $V_O$ = 3$V_{RMS}$ | | | | |
| | | SMPTE/DIN Two-Tone, 4:1 (60Hz and 7kHz) | | 0.000015 | | % |
| | | | | –136 | | dB |
| | | DIM 30 (3kHz square wave and 15kHz sine wave) | | 0.000012 | | % |
| | | | | –138 | | dB |
| | | CCIF Twin-Tone (19kHz and 20kHz) | | 0.000008 | | % |
| | | | | –142 | | dB |
| **FREQUENCY RESPONSE** | | | | | | |
| Gain-Bandwidth Product | GBW | G = 100 | | 80 | | MHz |
| | | G = 1 | | 40 | | MHz |
| Slew Rate | SR | G = –1 | | 27 | | V/µs |
| Full Power Bandwidth(1) | | $V_O$ = 1$V_{PP}$ | | 4 | | MHz |
| Overload Recovery Time | | G = –10 | | 500 | | ns |
| Channel Separation (Dual) | | f = 1kHz | | –130 | | dB |
| **NOISE** | | | | | | |
| Input Voltage Noise | | f = 20Hz to 20kHz | | 1.2 | | $\mu V_{PP}$ |
| Input Voltage Noise Density | $e_n$ | f = 10Hz | | 2 | | nV/√Hz |
| | | f = 100Hz | | 1.5 | | nV/√Hz |
| | | f = 1kHz | | 1.1 | | nV/√Hz |
| Input Current Noise Density | $I_n$ | f = 10Hz | | 3 | | pA/√Hz |
| | | f = 1kHz | | 1.7 | | pA/√Hz |
| **OFFSET VOLTAGE** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_S$ = ±15V | | ±100 | ±500 | µV |
| **over Temperature(2)** | **$dV_{OS}/dT$** | | | **1** | **4** | **µV/°C** |
| vs Power Supply | PSRR | $V_S$ = ±2.25V to ±18V | | 0.1 | 1 | µV/V |
| **INPUT BIAS CURRENT** | | | | | | |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0V | | ±60 | ±250 | nA |
| **over Temperature(2)** | | | | | **350** | **nA** |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 0V | | ±25 | ±175 | nA |
| **INPUT VOLTAGE RANGE** | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | (V–) + 2 | | (V+) – 2 | V |
| Common-Mode Rejection Ratio | CMRR | (V–) + 2V ≤ $V_{CM}$ ≤ (V+) – 2V | 110 | 120 | | dB |
| **INPUT IMPEDANCE** | | | | | | |
| Differential | | | | 20k \|\| 8 | | Ω \|\| pF |
| Common-Mode | | | | $10^9$ \|\| 2 | | Ω \|\| pF |

(1) Full-power bandwidth = SR/(2π × $V_{PP}$), where SR = slew rate.
(2) Specified by design and characterization.

## ELECTRICAL CHARACTERISTICS: $V_S$ = ±2.25V to ±18V (continued)

At $T_A$ = +25°C and $R_L$ = 2kΩ, unless otherwise noted. $V_{CM}$ = $V_{OUT}$ = midsupply, unless otherwise noted.
**Boldface** limits apply over the specified temperature range, $T_A$ = –40°C to +85°C.

| PARAMETER | | CONDITIONS | OPA1611AI, OPA1612AI | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **OPEN-LOOP GAIN** | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | (V–) + 0.2V ≤ $V_O$ ≤ (V+) – 0.2V, $R_L$ = 10kΩ | 114 | 130 | | dB |
| | $A_{OL}$ | (V–) + 0.6V ≤ $V_O$ ≤ (V+) – 0.6V, $R_L$ = 2kΩ | 110 | 114 | | dB |
| **OUTPUT** | | | | | | |
| Voltage Output | $V_{OUT}$ | $R_L$ = 10kΩ, $A_{OL}$ ≥ 114dB | (V–) + 0.2 | | (V+) – 0.2 | V |
| | | $R_L$ = 2kΩ, $A_{OL}$ ≥ 110dB | (V–) + 0.6 | | (V+) – 0.6 | V |
| Output Current | $I_{OUT}$ | | See Figure 27 | | | mA |
| Open-Loop Output Impedance | $Z_O$ | | See Figure 28 | | | Ω |
| Short-Circuit Current | $I_{SC}$ | | | +55/–62 | | mA |
| Capacitive Load Drive | $C_{LOAD}$ | | See Typical Characteristics | | | pF |
| **POWER SUPPLY** | | | | | | |
| Specified Voltage | $V_S$ | | ±2.25 | | ±18 | V |
| Quiescent Current (per channel) | $I_Q$ | $I_{OUT}$ = 0A | | 3.6 | 4.5 | mA |
| **over Temperature**[3] | | | | | **5.5** | **mA** |
| **TEMPERATURE RANGE** | | | | | | |
| Specified Range | | | –40 | | +85 | °C |
| Operating Range | | | –55 | | +125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | | | | |
| SO-8 | | | | 150 | | °C/W |

(3) Specified by design and characterization.

## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

**INPUT VOLTAGE NOISE DENSITY AND INPUT CURRENT NOISE DENSITY vs FREQUENCY**

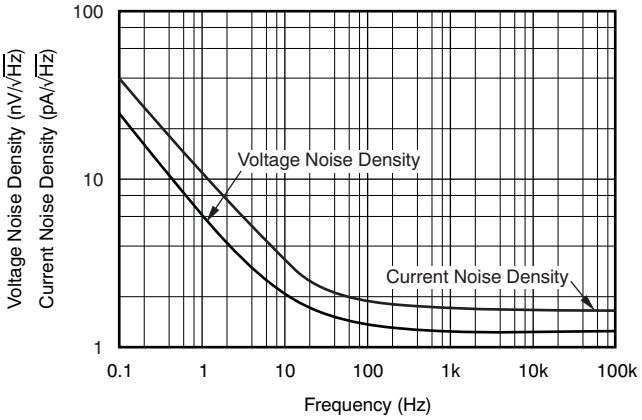



**Figure 1.**

**0.1Hz TO 10Hz NOISE**

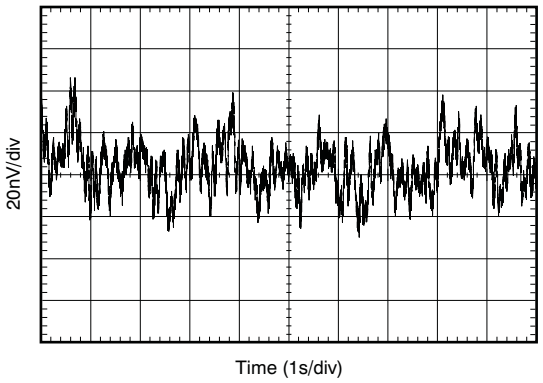



**Figure 2.**

**VOLTAGE NOISE vs SOURCE RESISTANCE**

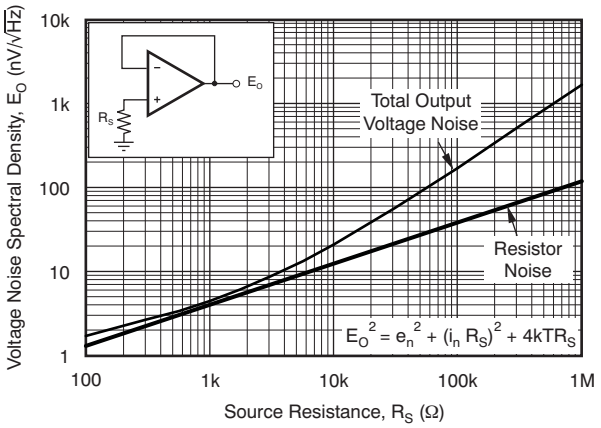



**Figure 3.**

**MAXIMUM OUTPUT VOLTAGE vs FREQUENCY**

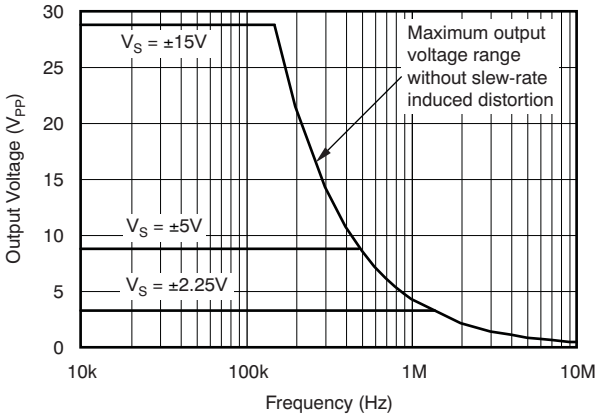



**Figure 4.**

**GAIN AND PHASE vs FREQUENCY**

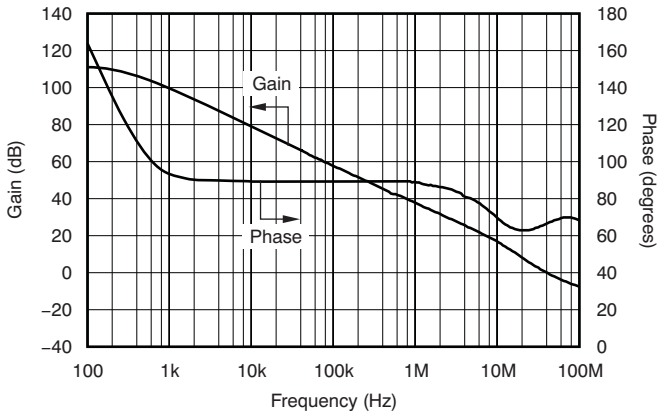



**Figure 5.**

**CLOSED-LOOP GAIN vs FREQUENCY**

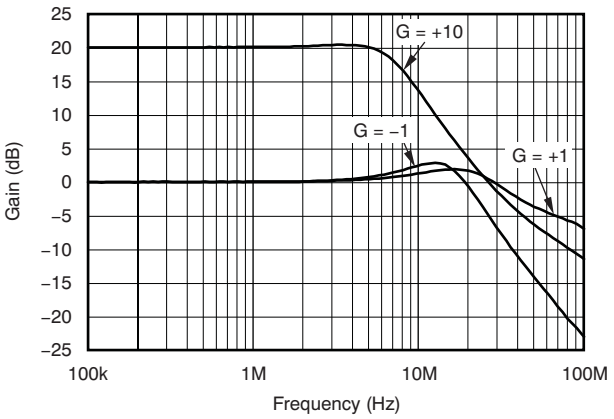



**Figure 6.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

**THD+N RATIO vs FREQUENCY**

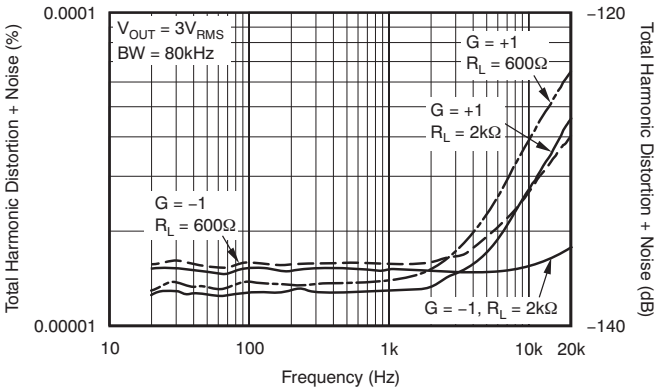



**Figure 7.**

**THD+N RATIO vs FREQUENCY**

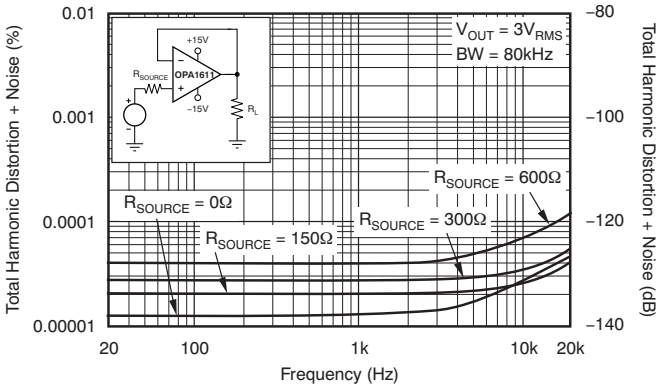



**Figure 8.**

**THD+N RATIO vs FREQUENCY**

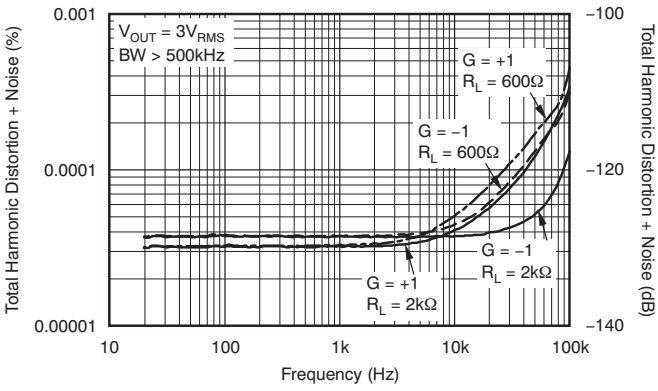



**Figure 9.**

**THD+N RATIO vs FREQUENCY**

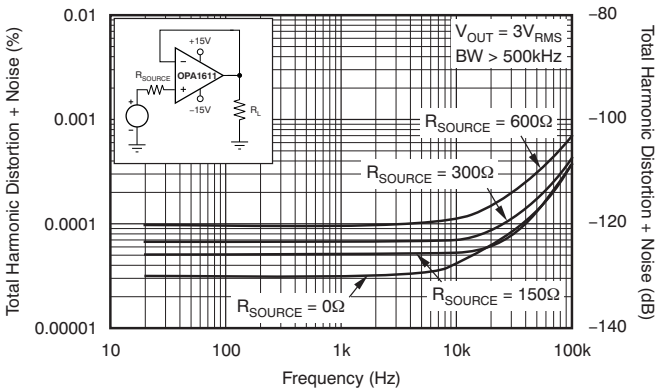



**Figure 10.**

**THD+N RATIO vs OUTPUT AMPLITUDE**

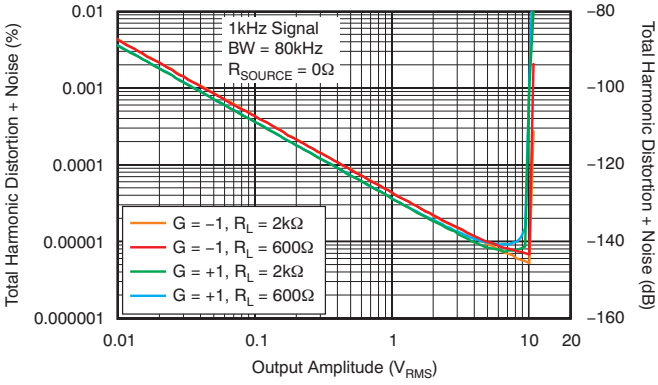



**Figure 11.**

**INTERMODULATION DISTORTION vs OUTPUT AMPLITUDE**

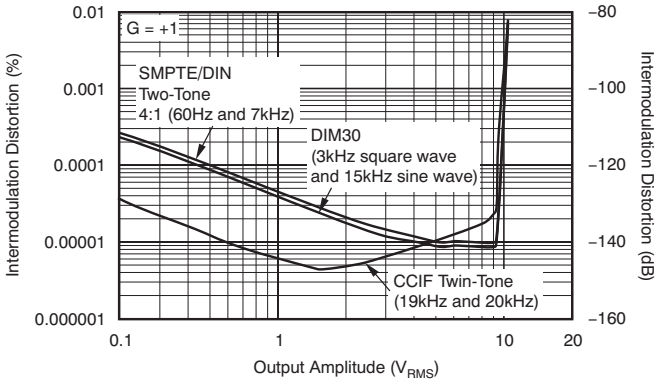



**Figure 12.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

**CHANNEL SEPARATION vs FREQUENCY**

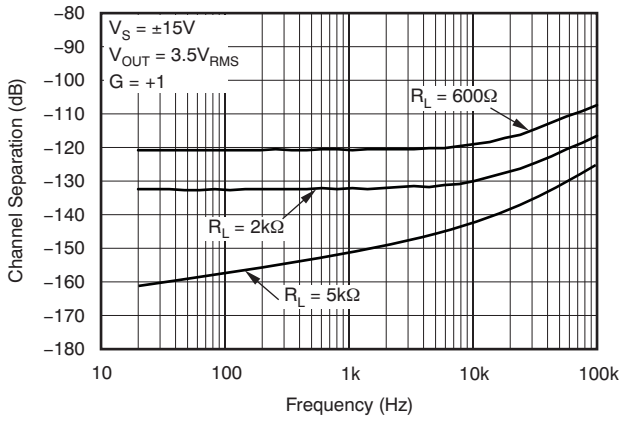



**Figure 13.**

**CMRR AND PSRR vs FREQUENCY (Referred to Input)**

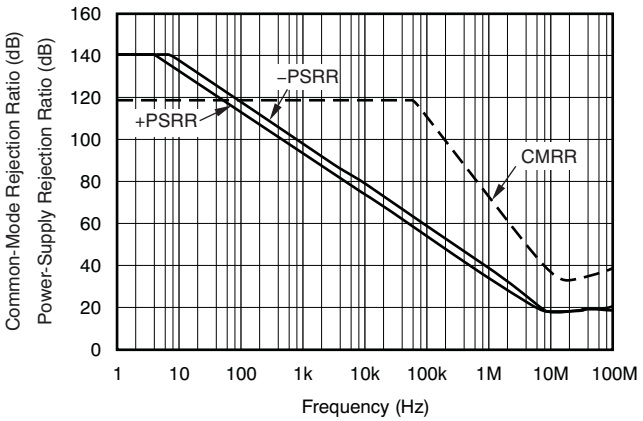



**Figure 14.**

**SMALL-SIGNAL STEP RESPONSE (100mV)**

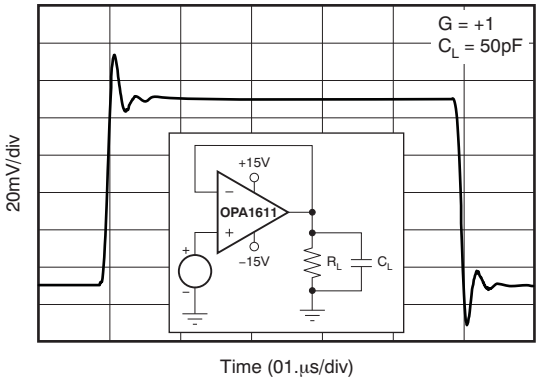



**Figure 15.**

**SMALL-SIGNAL STEP RESPONSE (100mV)**

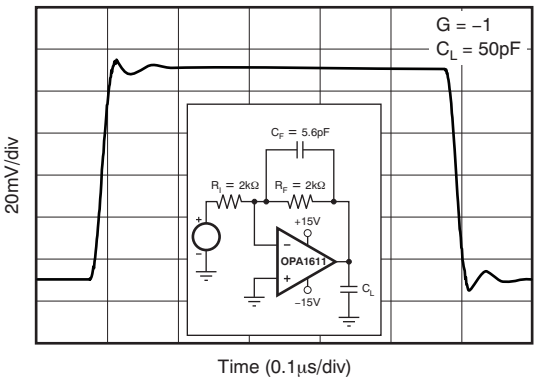



**Figure 16.**

**LARGE-SIGNAL STEP RESPONSE**

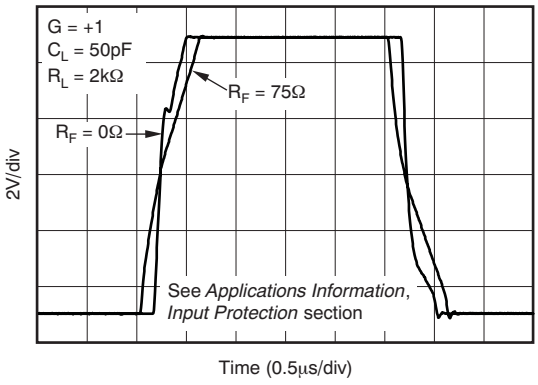



**Figure 17.**

**LARGE-SIGNAL STEP RESPONSE**

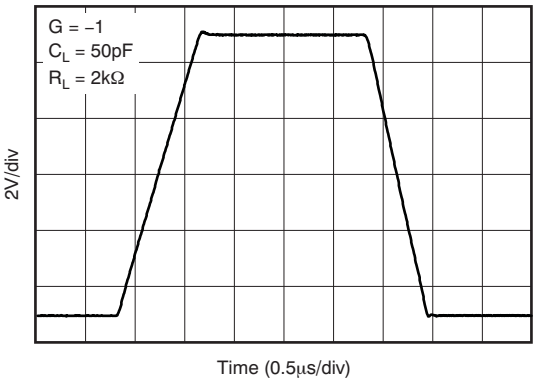



**Figure 18.**

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

**SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)**

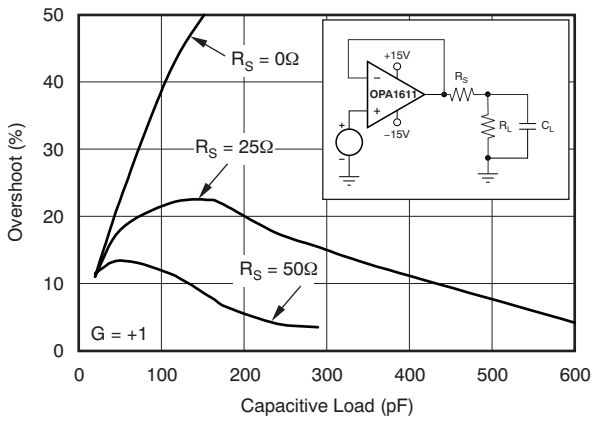



Figure 19.

**SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)**

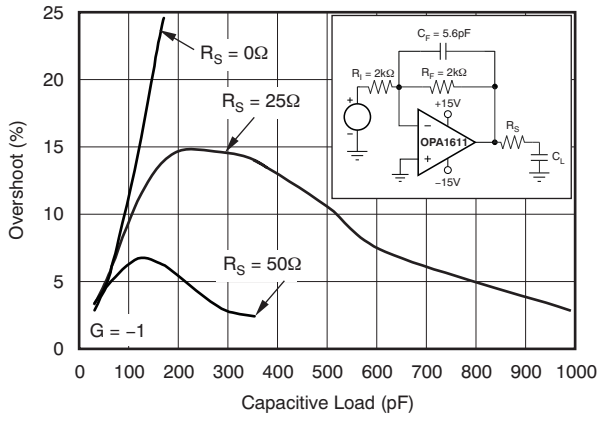



Figure 20.

**OPEN-LOOP GAIN vs TEMPERATURE**

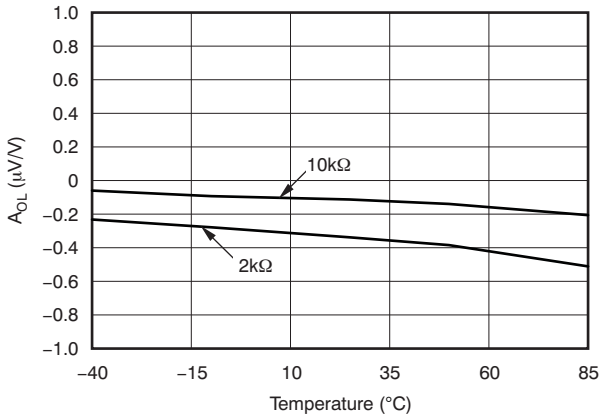



Figure 21.

**$I_B$ AND $I_{OS}$ vs TEMPERATURE**

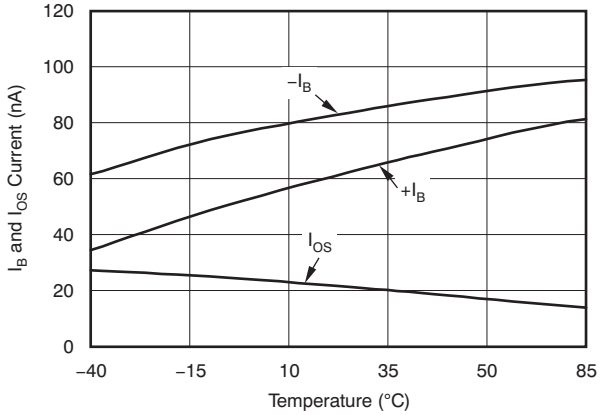



Figure 22.

**$I_B$ AND $I_{OS}$ vs COMMON-MODE VOLTAGE**

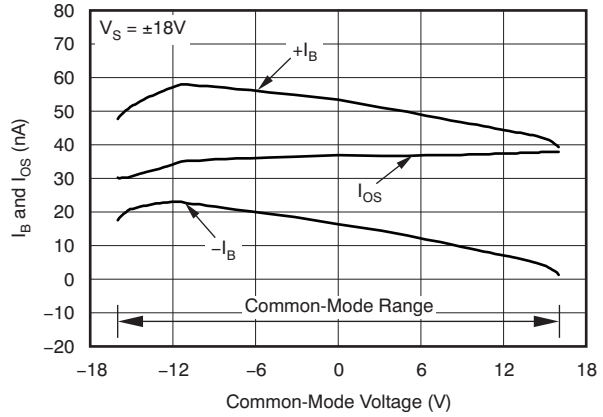



Figure 23.

**QUIESCENT CURRENT vs TEMPERATURE**

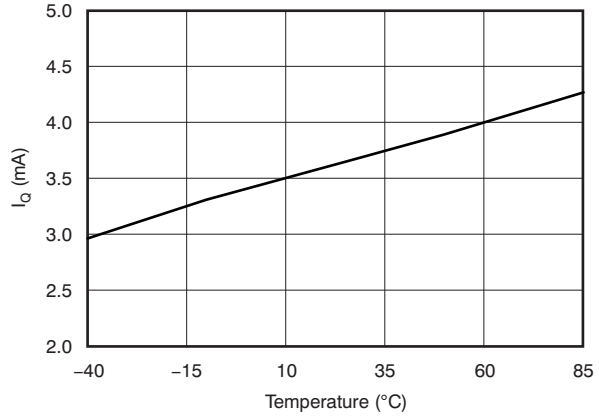



Figure 24.

## TYPICAL CHARACTERISTICS (continued)

At $T_A$ = +25°C, $V_S$ = ±15V, and $R_L$ = 2kΩ, unless otherwise noted.

**QUIESCENT CURRENT vs SUPPLY VOLTAGE**

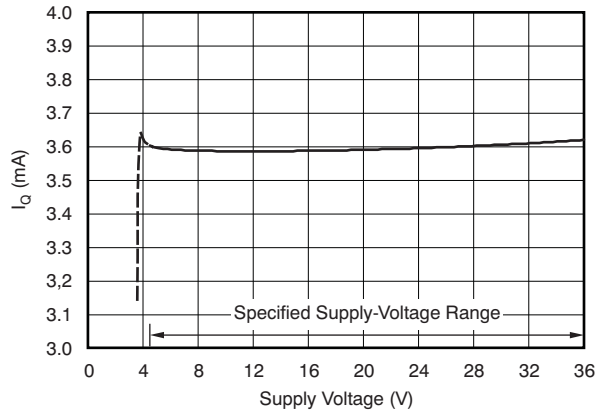



**Figure 25.**

**SHORT-CIRCUIT CURRENT vs TEMPERATURE**

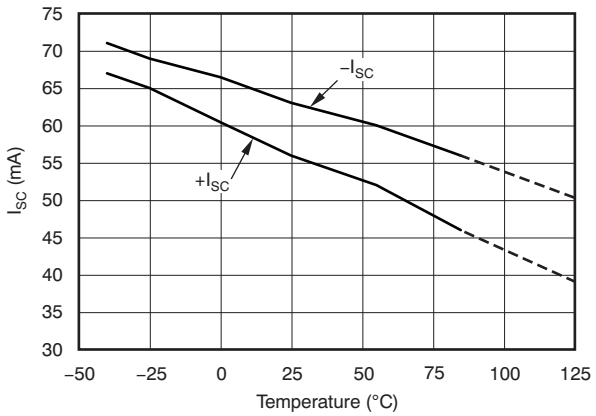



**Figure 26.**

**OUTPUT VOLTAGE vs OUTPUT CURRENT**

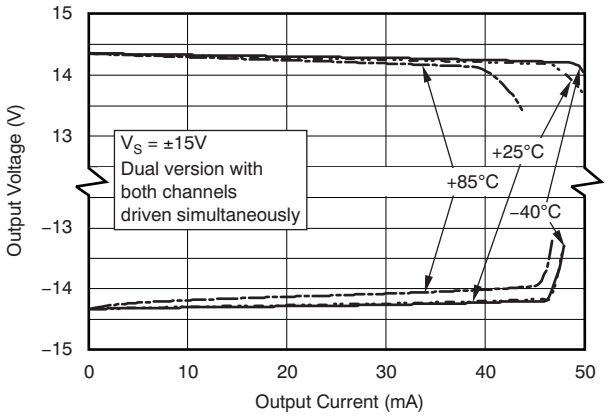



**Figure 27.**

**OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY**

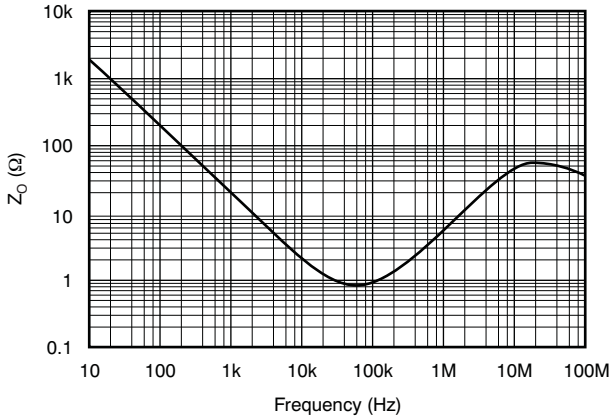



**Figure 28.**

## APPLICATION INFORMATION

The OPA1611 and OPA1612 are unity-gain stable, precision op amps with very low noise; these devices are also free from output phase reversal. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device power-supply pins. In most cases, 0.1µF capacitors are adequate. Figure 29 shows a simplified internal schematic of the OPA1611.

### OPERATING VOLTAGE

The OPA161x series op amps operate from ±2.25V to ±18V supplies while maintaining excellent performance. The OPA161x series can operate with as little as +4.5V between the supplies and with up to +36V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA161x series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25V with the negative supply at –5V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of $T_A$ = –40°C to +85°C. Parameters that vary with operating voltage or temperature are shown in the Typical Characteristics.

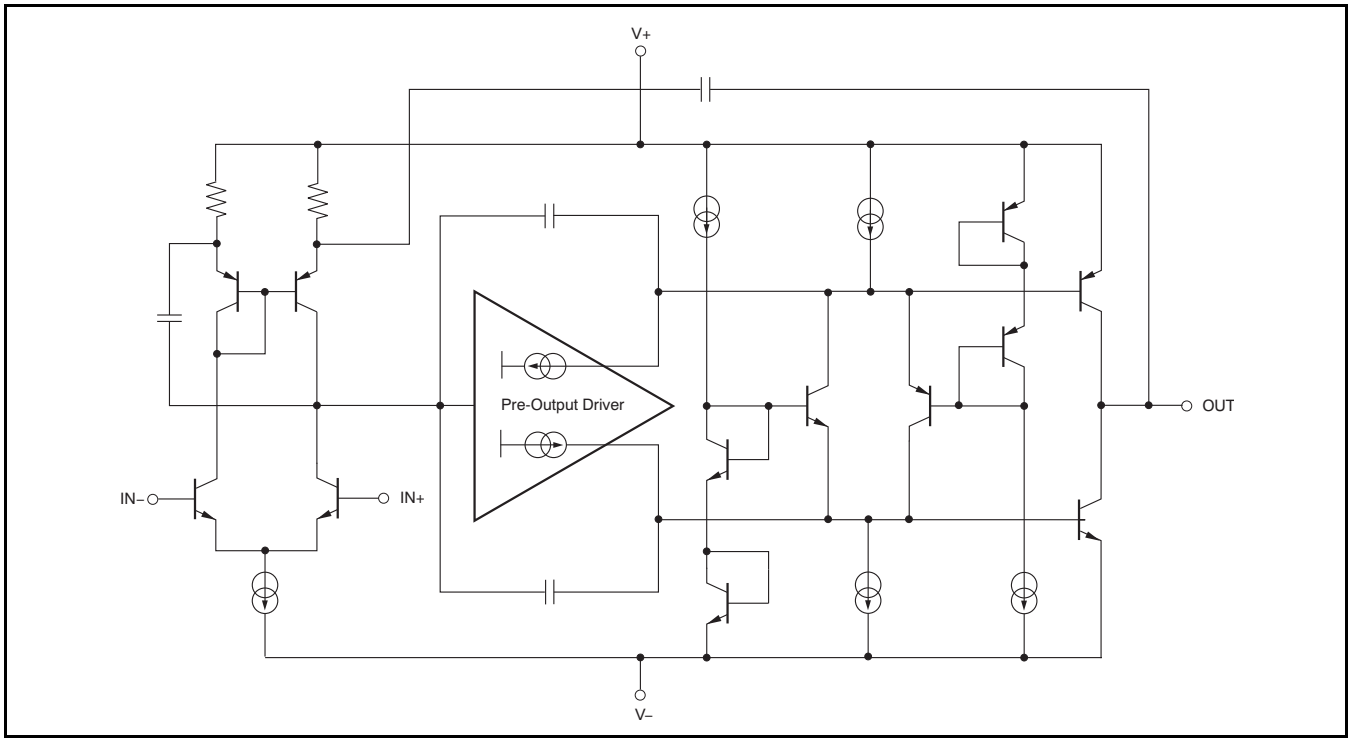



**Figure 29. OPA1611 Simplified Schematic**

## INPUT PROTECTION

The input terminals of the OPA1611 and the OPA1612 are protected from excessive differential voltage with back-to-back diodes, as Figure 30 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 17 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor ($R_I$) and/or a feedback resistor ($R_F$) can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA1611 and is examined in the following *Noise Performance* section. Figure 30 shows an example configuration when both current-limiting input and feedback resistors are used.

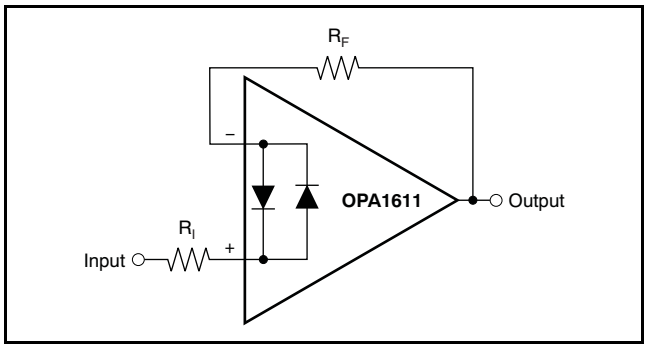



**Figure 30. Pulsed Operation**

## NOISE PERFORMANCE

Figure 31 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA1611 (GBW = 40MHz, G = +1) is shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the OPA161x series op amps makes them a good choice for use in applications where the source impedance is less than 1kΩ.

The equation in Figure 31 shows the calculation of the total circuit noise, with these parameters:

- $e_n$ = Voltage noise
- $I_n$ = Current noise
- $R_S$ = Source impedance
- k = Boltzmann's constant = $1.38 \times 10^{-23}$ J/K
- T = Temperature in degrees Kelvin (K)

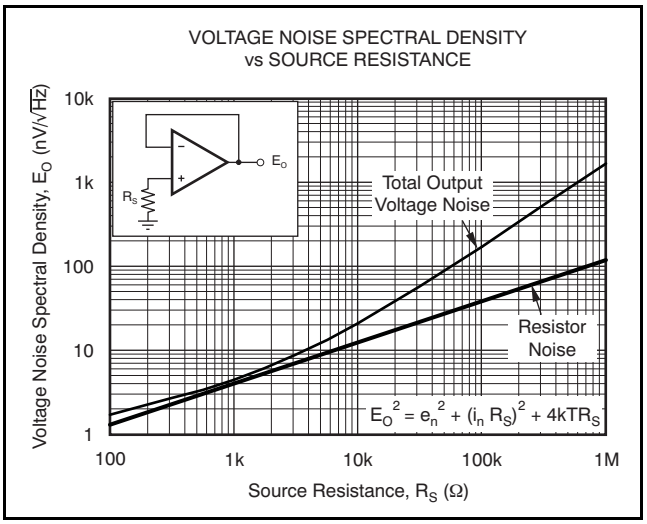



**Figure 31. Noise Performance of the OPA1611 in Unity-Gain Buffer Configuration**

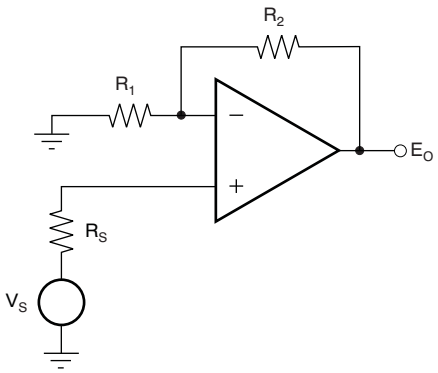
## BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 31 plots this function. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 32 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

**Noise in Noninverting Gain Configuration**




Noise at the output:

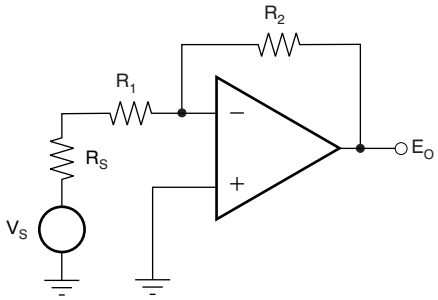
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2 \left(1 + \frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(1 + \frac{R_2}{R_1}\right)$ = thermal noise of $R_S$

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1}\right)$ = thermal noise of $R_1$

$e_2 = \sqrt{4kTR_2}$ = thermal noise of $R_2$

**Noise in Inverting Gain Configuration**




Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of $R_S$

$e_1 = \sqrt{4kTR_1} \times \left(\frac{R_2}{R_1 + R_S}\right)$ = thermal noise of $R_1$

$e_2 = \sqrt{4kTR_2}$ = thermal noise of $R_2$

For the OPA161x series op amps at 1kHz, $e_n = 1.1nV/\sqrt{Hz}$ and $i_n = 1.7pA/\sqrt{Hz}$.

**Figure 32. Noise Calculation in Gain Configurations**

## TOTAL HARMONIC DISTORTION MEASUREMENTS

The OPA161x series op amps have excellent distortion characteristics. THD + Noise is below 0.00008% (G = +1, $V_O$ = 3$V_{RMS}$, BW = 80kHz) throughout the audio frequency range, 20Hz to 20kHz, with a 2kΩ load (see Figure 7 for characteristic performance).

The distortion produced by OPA1611 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 33 shows) can be used to extend the measurement capabilities.

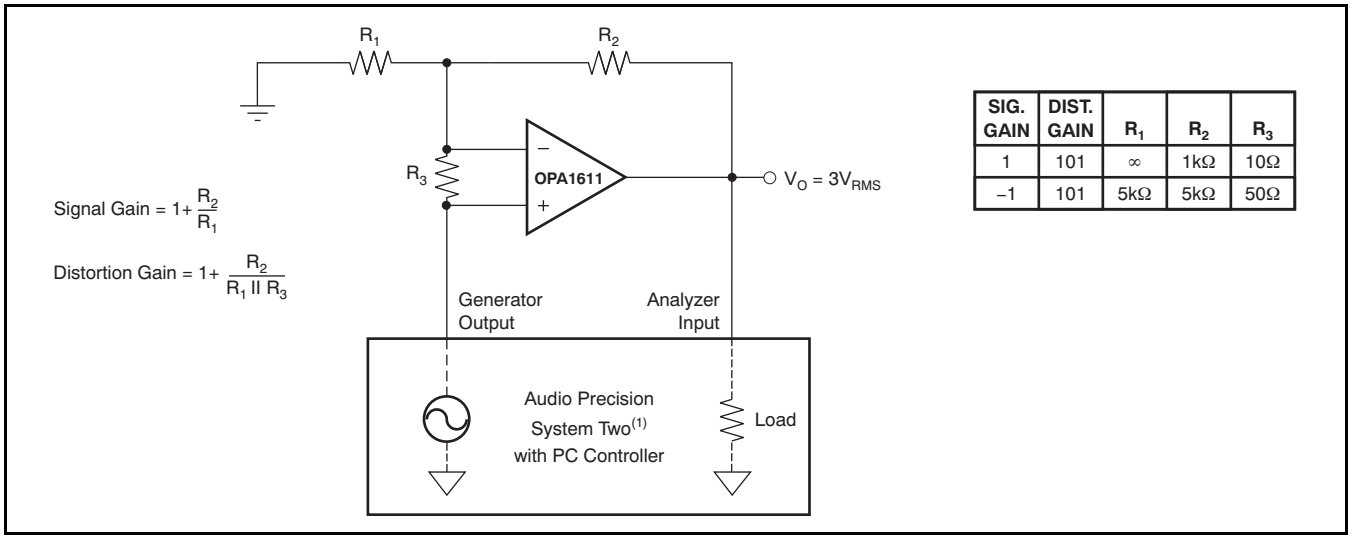
Op amp distortion can be considered an internal error source that can be referred to the input. Figure 33 shows a circuit that causes the op amp distortion to be 101 times (or approximately 40dB) greater than that normally produced by the op amp. The addition of $R_3$ to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without $R_3$. The value of $R_3$ should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

## CAPACITIVE LOADS

The dynamic characteristics of the OPA1611 and OPA1612 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor ($R_S$ equal to 50Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. Figure 19 and Figure 20 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of $R_S$. Also, refer to Applications Bulletin AB-028 (literature number SBOA015, available for download from the TI web site) for details of analysis techniques and application circuits.




| SIG. GAIN | DIST. GAIN | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|---|
| 1 | 101 | ∞ | 1kΩ | 10Ω |
| –1 | 101 | 5kΩ | 5kΩ | 50Ω |

(1) For measurement bandwidth, see Figure 7 through Figure 12.

**Figure 33. Distortion Test Circuit**

## POWER DISSIPATION

OPA1611 and OPA1612 series op amps are capable of driving 2kΩ loads with a power-supply voltage up to ±18V. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA1611 and OPA1612 series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

## ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 34 illustrates the ESD circuits contained in the OPA161x series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA161x but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

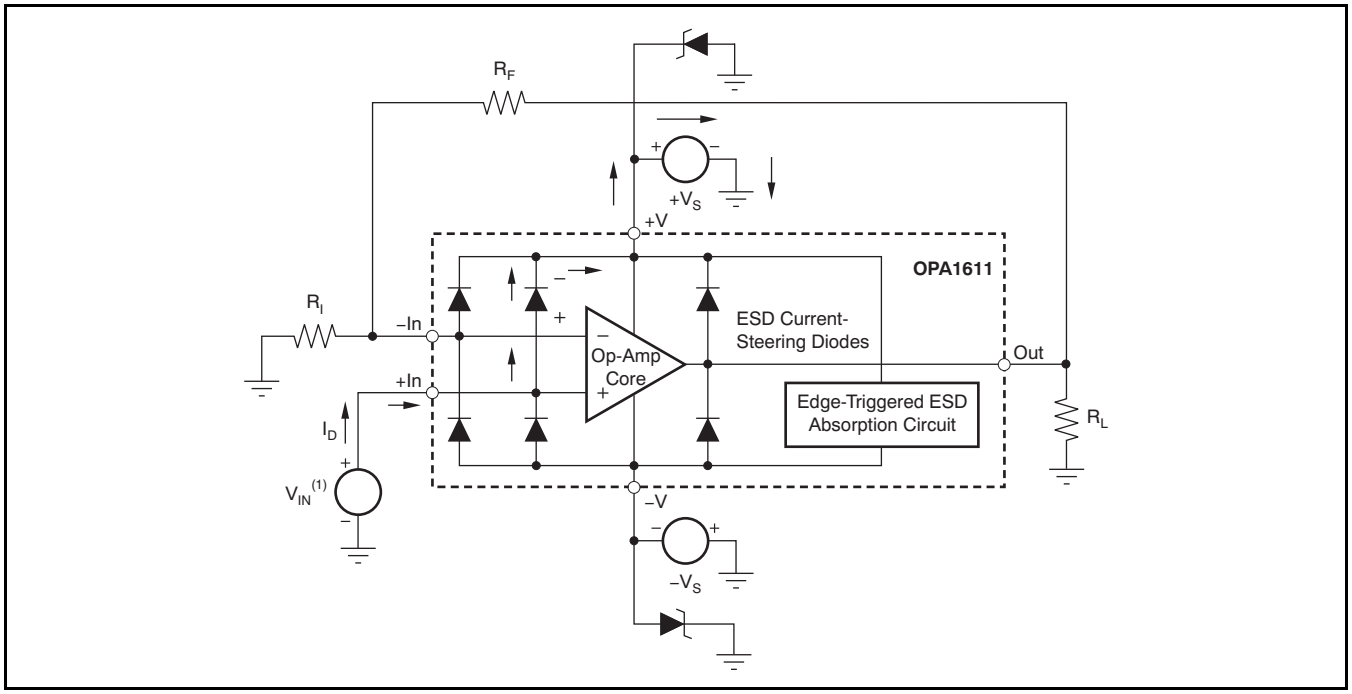
When the operational amplifier connects into a circuit such as the one Figure 34 shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 34 depicts a specific example where the input voltage, $V_{IN}$, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher $V_{IN}$. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, $V_{IN}$ may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $-V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $-V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 34. The zener voltage must be selected such that the diode does not turn on during normal operation. However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.




(1) $V_{IN} = +V_S + 500mV$.

**Figure 34. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application**

## APPLICATION CIRCUIT

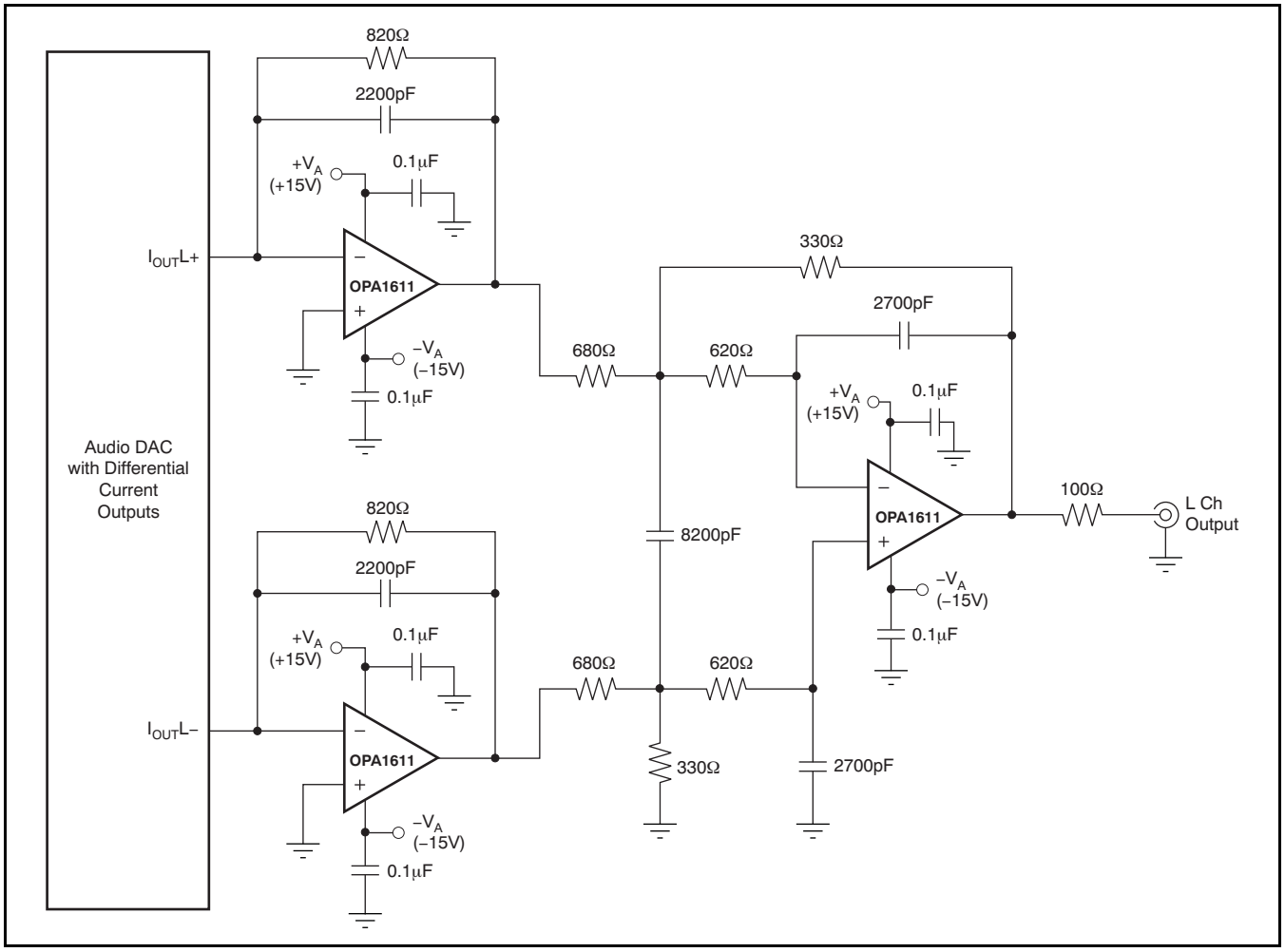



**Figure 35. Audio DAC Post Filter (I/V Converter and Low-Pass Filter)**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| OPA1611AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA1611AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA1612AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| OPA1612AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

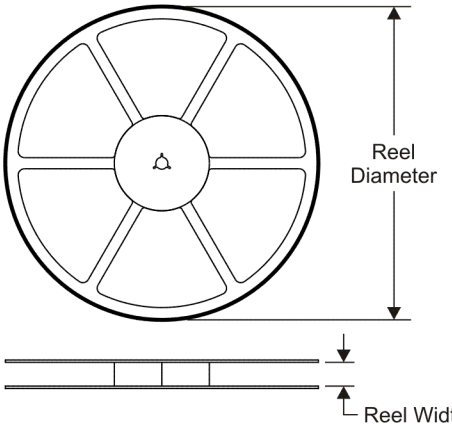
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

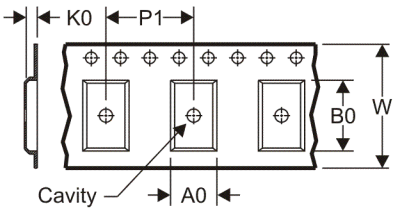
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

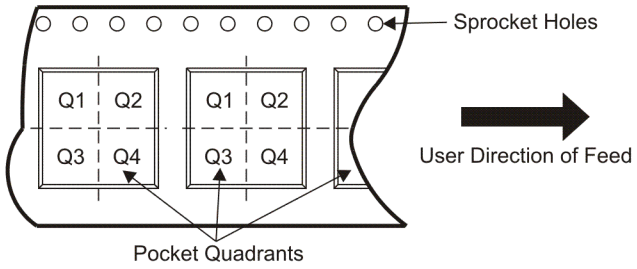



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

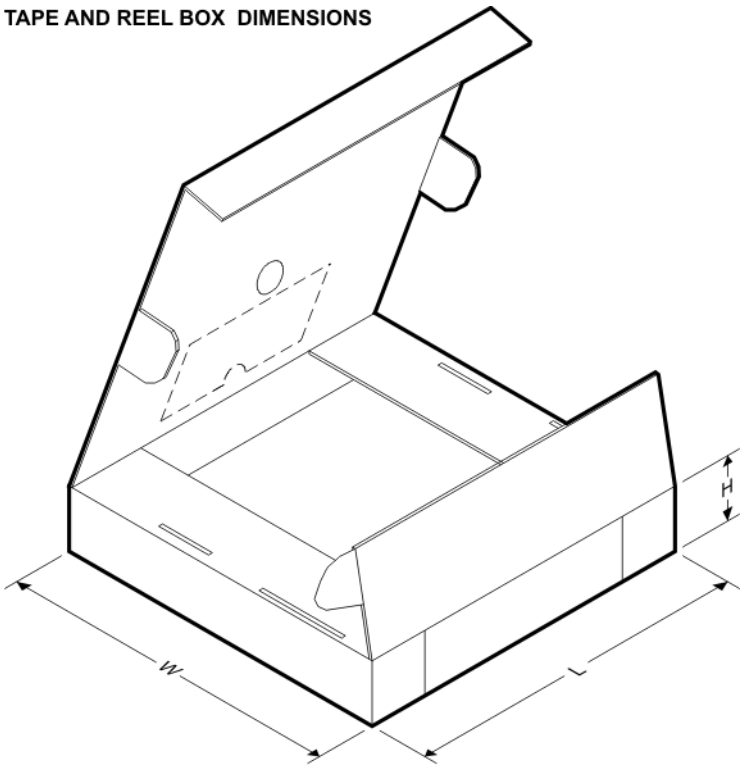
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA1611AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA1612AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

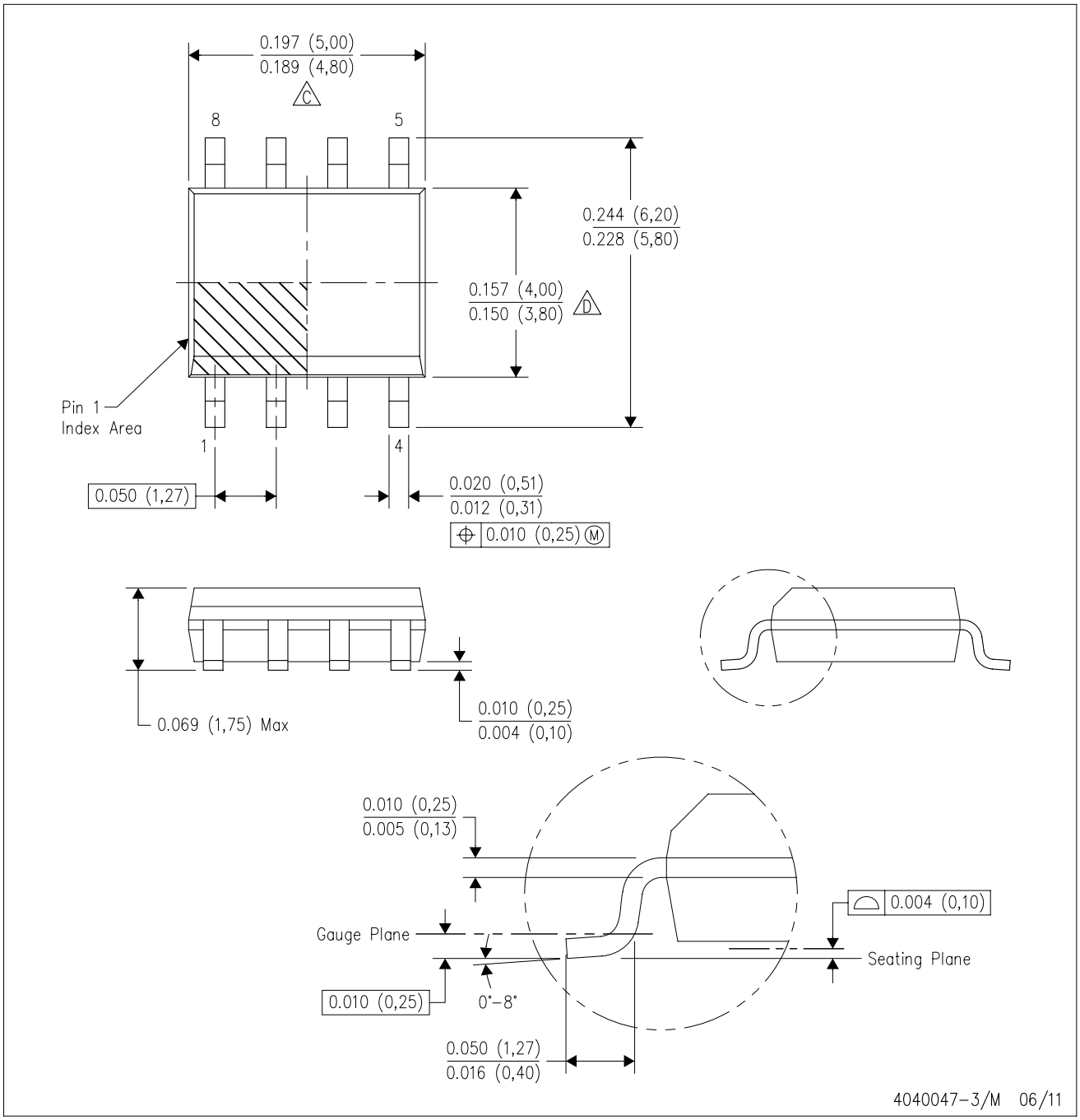
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

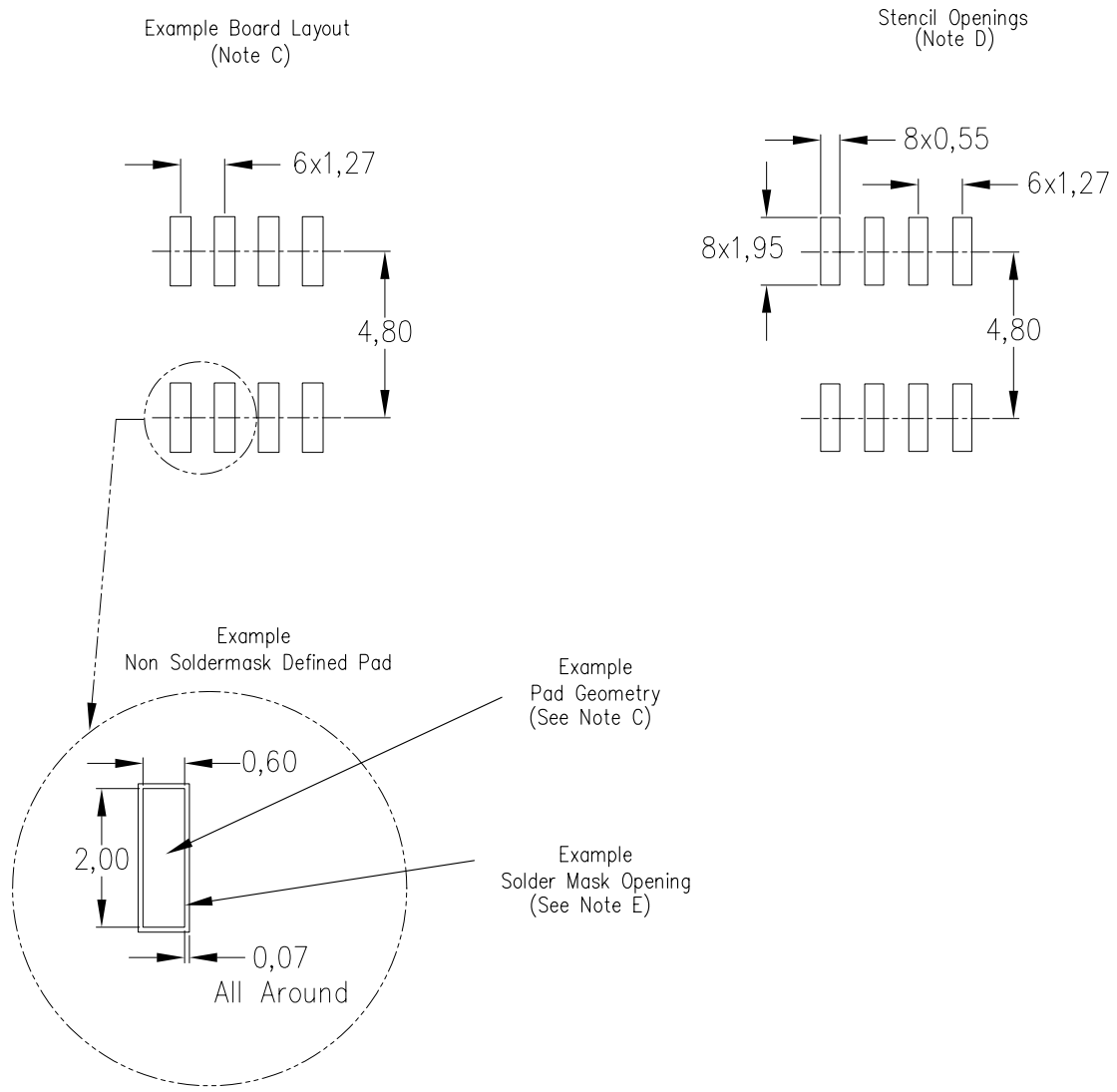
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA1611AIDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |
| OPA1612AIDR | SOIC | D | 8 | 2500 | 346.0 | 346.0 | 29.0 |

D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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