具有停机模式的 20MHz、低噪声、1.8V、RRI/O、CMOS 运算放大器

查询样品: OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S

特性

- 增益带宽： **20MHz**
- 低噪声： **8.5nV/√Hz** （在 **1kHz** 频率条件下）
- 转换速率： **10V/μs**
- 低 **THD + N： 0.0005%**
- 轨至轨输入输出 **(I/O)**
- 失调电压： **2mV** （最大值）
- 电源电压： **1.8V** 至 **5.5V**
- 电源电流： 每通道 **1.5mA**
  - 停机模式： 每个通道的静态电流为 **0.1μA**
- 具有稳定的单位增益
- 小外形封装：
  - **SOT23, DFN, MSOP, TSSOP**

应用

- 传感器信号调节
- 消费类音频
- 多极点有源滤波器
- 控制环路放大器
- 通信
- 安全
- 扫描仪

说明

OPA322 系列包含具有低噪声和轨至轨输入/输出的单通道、双通道和四通道 CMOS 运算放大器，专为低功耗、单电源应用而优化。 1.8V 至 5.5V 的宽电源范围以及每通道仅 1.5mA 的低静态电流，使得这些器件非常适合于功耗敏感型应用。

由于兼具超低的噪声（在 1kHz 频率下为 8.5nV/√Hz）、高的增益带宽 (20MHz) 和高转换速率 (10V/μs)，因而使得 OPA322 系列成为众多应用的理想选择，包括信号调节及需要高增益的传感器放大。另外，OPA322 系列还拥有很低的 THD + N，因此同样极为适合于消费类音频应用，尤其是单电源系统。

OPAy322S 型号的器件具有一种停机模式，该模式允许将放大器从正常操作状态切换至待机状态 （待机电流通常小于 0.1μA）。

OPA322 （单通道版本） 采用 SOT23-5 和 SOT23-6 封装，而 OPA2322 （双通道版本） 则可提供 MSOP-8、MSOP-10、SO-8 和 DFN-8 封装。 四通道版本 OPA4322 采用 TSSOP-14 和 TSSOP-16 封装。所有器件版本的规定工作温度范围均为 —40℃ 至 +125℃

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA322(2)	SOT23-5	DBV	RAD
OPA322S(2)	SOT23-6	DBV	RAF
OPA2322(2)	SO-8	D	O2322A
OPA2322	MSOP-8	DGK	OOZI
	DFN-8	DRG	OPCI
OPA2322S(2)	MSOP-10	DGS	OPBI
OPA4322(2)	TSSOP-14	PW	OPA4322
OPA4322S(2)	TSSOP-16	PW	OPA4322S

(1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet, or visit the device product folder at www.ti.com.
(2) Product preview device.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S	UNIT
Supply voltage, V_S = (V+) – (V–)		6	V
Signal input pins	Voltage(2)	(V–) – 0.5 to (V+) + 0.5	V
	Current(2)	±10	mA
Output short-circuit current(3)		Continuous	mA
Operating temperature, T_A		–40 to +150	°C
Storage temperature, T_{stg}		–65 to +150	°C
Junction temperature, T_J		+150	°C
ESD ratings	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V, or ±0.9 V to ±2.75 V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2, and $\overline{SHDN\_x}$ = V_S+, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input offset voltage	V_{OS}			0.5	2	mV
vs Temperature	**dV_{OS}/dT**	**V_S = +5.5 V**		**1.8**	**6**	**µV/°C**
vs Power supply	PSR	V_S = +1.8 V to +5.5 V		10	50	µV/V
Over temperature		**V_S = +1.8 V to +5.5 V**		**20**	**65**	**µV/V**
Channel separation		At 1 kHz		130		dB
INPUT VOLTAGE						
Common-mode voltage range	V_{CM}		(V–) – 0.1		(V+) + 0.1	V
Common-mode rejection ratio	CMRR	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	90	100		dB
Over temperature			**90**			**dB**
INPUT BIAS CURRENT						
Input bias current	I_B			±0.2	±10	pA
Over temperature		**T_A = –40°C to +85°C**			**±50**	**pA**
		T_A = –40°C to +125°C			**±400**	**pA**
Input offset current	I_{OS}			±0.2	±10	pA
Over temperature		**T_A = –40°C to +85°C**			**±50**	**pA**
		T_A = –40°C to +125°C			**±400**	**pA**
NOISE						
Input voltage noise		f = 0.1 Hz to 10 Hz		2.8		μV_{PP}
Input voltage noise density	e_n	f = 1 kHz		8.5		nV/√Hz
		f = 10 kHz		7		nV/√Hz
Input current noise density	i_n	f = 1 kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
Differential				5		pF
Common-mode				4		pF
OPEN-LOOP GAIN						
Open-loop voltage gain	A_{OL}	0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ	100	120		dB
		0.1 V < V_O < (V+) – 0.1 V, R_L = 10 kΩ	**94**			**dB**
Phase margin	PM	G = 1 V/V, V_S = 5 V, C_L = 50 pF		47		Degrees
FREQUENCY RESPONSE		**V_S = 5.0 V, C_L = 50 pF**				
Gain bandwidth product	GBP	Unity gain		20		MHz
Slew rate	SR	G = +1		10		V/µs
Settling time	t_S	To 0.1%, 2-V step, G = +1		0.25		µs
		To 0.01%, 2-V step, G = +1		0.32		µs
Overload recovery time		V_{IN} × G > V_S		100		ns
Total harmonic distortion + noise(1)	THD+N	V_O = 4 V_{PP}, G = +1, f = 10 kHz, R_L = 10 kΩ		0.0005		%
		V_O = 2 V_{PP}, G = +1, f = 10 kHz, R_L = 600 Ω		0.0011		%

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

ELECTRICAL CHARACTERISTICS: V_S = +1.8 V to +5.5 V, or ±0.9 V to ±2.75 V (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, V_{OUT} = V_S/2, and $\overline{SHDN\_x}$ = V_S+, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA322, OPA322S, OPA2322, OPA2322S, OPA4322, OPA4322S			UNIT
			MIN	TYP	MAX	
OUTPUT						
Voltage output swing from both rails	V_O	R_L = 10 kΩ		10	20	mV
Over temperature		**R_L = 10 kΩ**			**30**	**mV**
Short-circuit current	I_{SC}	V_S = 5.5 V		±65		mA
Capacitive load drive	C_L		See Typical Characteristics			
Open-loop output resistance	R_O	I_O = 0 mA, f = 1 MHz		90		Ω
POWER SUPPLY						
Specified voltage range	V_S		1.8		5.5	V
Quiescent current per amplifier	I_Q	I_O = 0 mA, V_S = +5.5 V				
OPA322, OPA322S				1.6	1.8	mA
Over temperature					**TBD**	**mA**
OPA2322, OPA2322S				1.5	1.75	mA
Over temperature					**1.85**	**mA**
OPA4322, OPA4322S				1.45	1.65	mA
Over temperature					**TBD**	**mA**
Power-on time		V_{S+} = 0 V to 5 V, to 90% I_Q level		28		µs
SHUTDOWN(2)		V_S = 1.8 V to 5.5 V				
Quiescent current, per amplifier	I_{QSD}	All amplifiers disabled, $\overline{SHDN}$ = $V_{S–}$		0.1	1	µA
OPA2322S only		$\overline{SHDN\_A}$ = $V_{S–}$, $\overline{SHDN\_B}$ = V_{S+}		1.6		mA
		$\overline{SHDN\_A}$ = V_{S+}, $\overline{SHDN\_B}$ = $V_{S–}$		1.6		mA
High voltage (enabled)	V_{IH}	Amplifier enabled	0.7 × V_{S+}		5.5	V
Low voltage (disabled)	V_{IL}	Amplifier disabled			0.3 × V_{S+}	V
Amplifier enable time(3)	t_{ON}	G = 1, V_{OUT} = 0.9 × V_S/2, full shutdown(4)		20		µs
Amplifier enable time,(3) OPA2322S only	t_{ON}	Partial shutdown(4)		6		µs
Amplifier disable time(3)	t_{OFF}	G = 1, V_{OUT} = 0.1 × V_S/2		3		µs
$\overline{SHDN}$ pin input bias current (per pin)		V_{IH} = 5.0 V		0.13		µA
		V_{IL} = 0 V		0.04		µA
TEMPERATURE						
Specified range			–40		+125	°C
Operating range			–40		+150	°C

(2) Ensured by design and characterization; not production tested.
(3) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(4) Full shutdown refers to the dual OPA2322S having both channels A and B disabled ($\overline{SHDN\_A}$ = $\overline{SHDN\_B}$ = $V_{S–}$) and the quad OPA4322S having all channels A to D disabled ($\overline{SHDN\_A/B}$ = $\overline{SHDN\_C/D}$ = $V_{S–}$). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in this mode, the internal biasing and oscillator remain operational and the enable time is shorter.

THERMAL INFORMATION

THERMAL METRIC(1)		OPA322	OPA322S	UNITS
		DBV	DBV	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	219.3	TBD	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	107.5	TBD	
θ_{JB}	Junction-to-board thermal resistance	57.5	TBD	
ψ_{JT}	Junction-to-top characterization parameter	7.4	TBD	
ψ_{JB}	Junction-to-board characterization parameter	56.9	TBD	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	TBD	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

THERMAL INFORMATION

THERMAL METRIC(1)		OPA2322			OPA2322S	UNITS
		D	DRG	DGK	DGS	
		8 PINS	8 PINS	8 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	122.6	50.6	174.8	TBD	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	67.1	54.9	43.9	TBD	
θ_{JB}	Junction-to-board thermal resistance	64.0	25.2	95.0	TBD	
ψ_{JT}	Junction-to-top characterization parameter	13.2	0.6	2.0	TBD	
ψ_{JB}	Junction-to-board characterization parameter	63.4	25.3	93.5	TBD	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	5.7	n/a	TBD	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

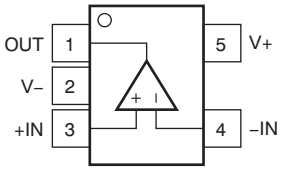
THERMAL INFORMATION

THERMAL METRIC(1)		OPA4322	OPA4322S	UNITS
		PW	PW	
		14 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	109.8	TBD	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	34.9	TBD	
θ_{JB}	Junction-to-board thermal resistance	52.5	TBD	
ψ_{JT}	Junction-to-top characterization parameter	2.2	TBD	
ψ_{JB}	Junction-to-board characterization parameter	51.8	TBD	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	TBD	

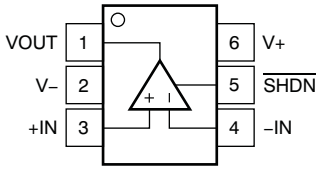
(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

PIN CONFIGURATIONS

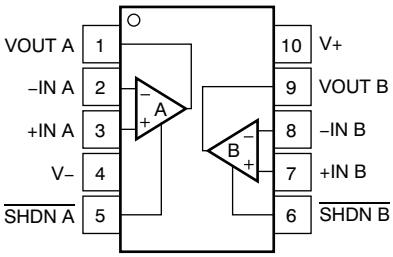
DBV PACKAGE
SOT23-5
(TOP VIEW)



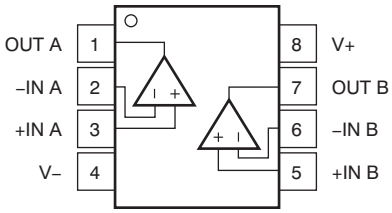
DBV PACKAGE
SOT23-6
(TOP VIEW)



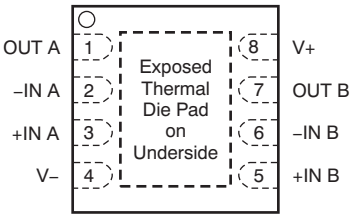
DGS PACKAGE
MSOP-10
(TOP VIEW)



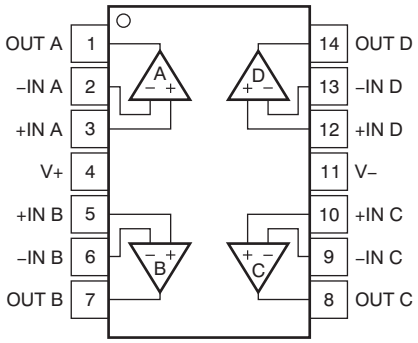
D, DGK PACKAGES
SO-8, MSOP-8
(TOP VIEW)



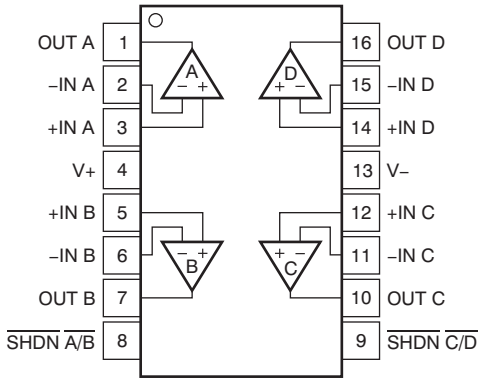
DRG PACKAGE(1)(2)
DFN-8
(TOP VIEW)



PW PACKAGE
TSSOP-14
(TOP VIEW)



PW PACKAGE
TSSOP-16
(TOP VIEW)



(1) Connect thermal pad to V–.
(2) Pad size: 2mm × 1.2mm.

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

OPEN-LOOP GAIN/PHASE vs FREQUENCY

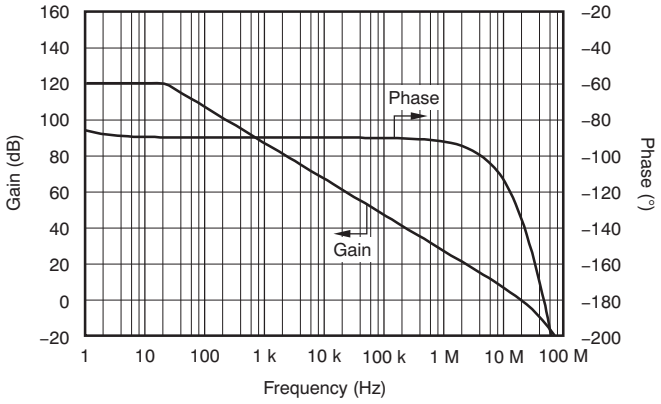


Figure 1.

OPEN-LOOP GAIN vs TEMPERATURE

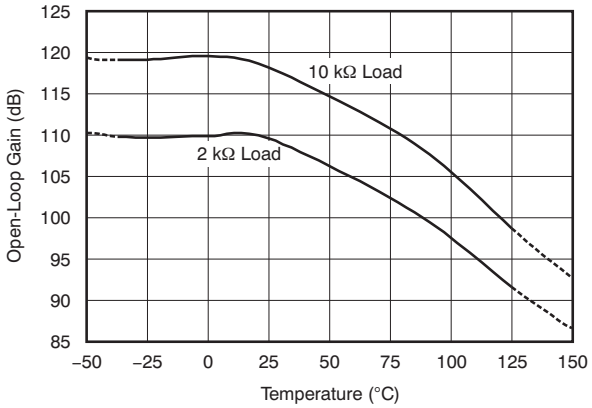


Figure 2.

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

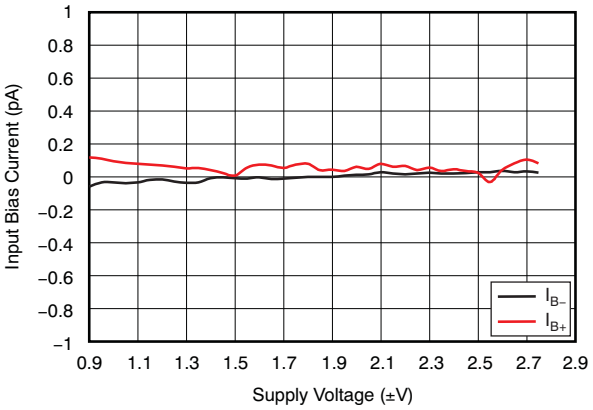


Figure 3.

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

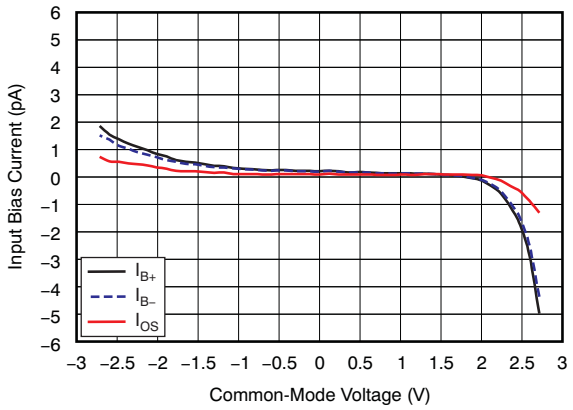


Figure 4.

INPUT BIAS CURRENT vs TEMPERATURE

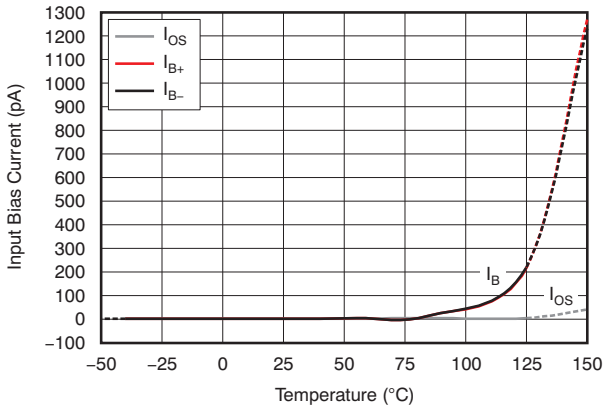


Figure 5.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

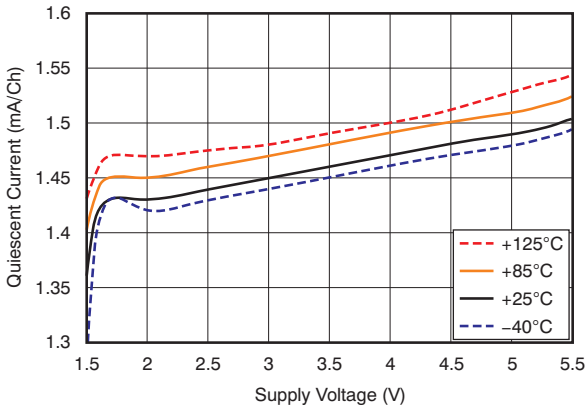


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION HISTOGRAM

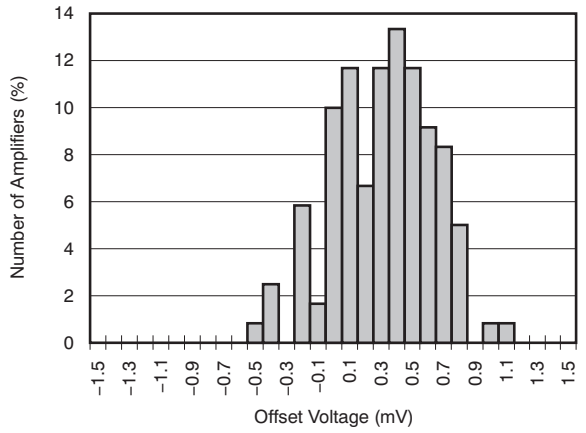


Figure 7.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

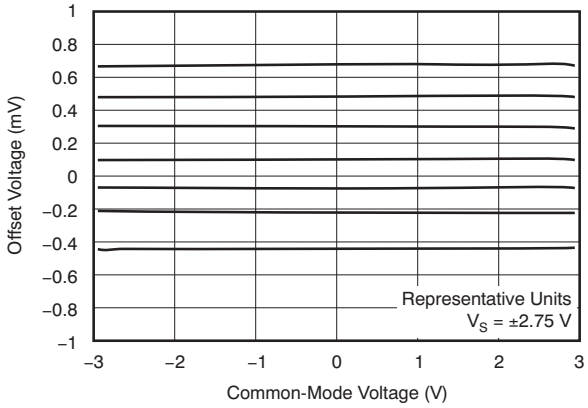


Figure 8.

INPUT VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY

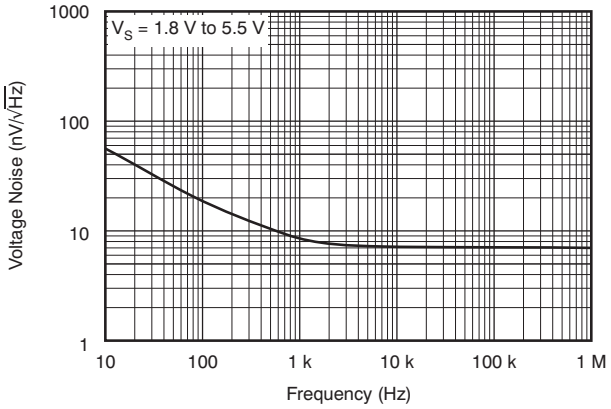


Figure 9.

0.1 Hz TO 10 Hz INPUT VOLTAGE NOISE

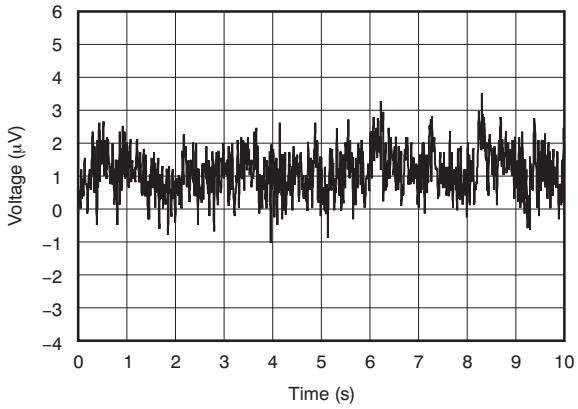


Figure 10.

CLOSED-LOOP GAIN vs FREQUENCY

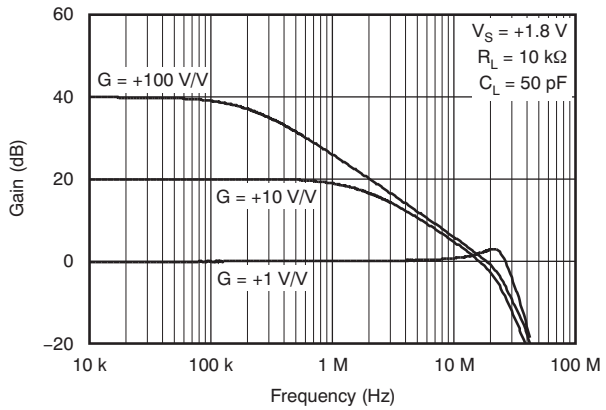


Figure 11.

CLOSED-LOOP GAIN vs FREQUENCY

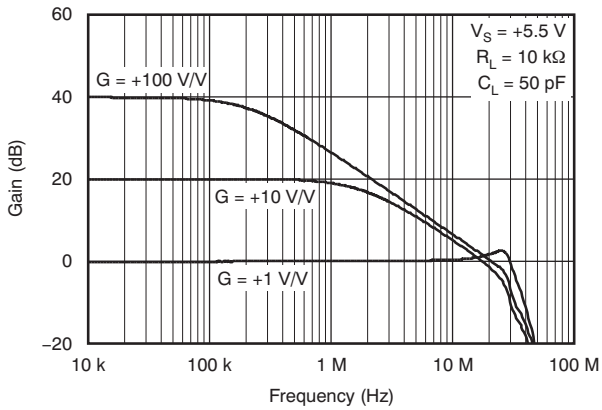


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

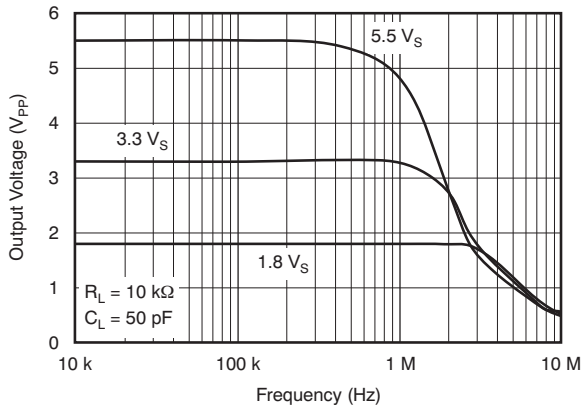


Figure 13.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

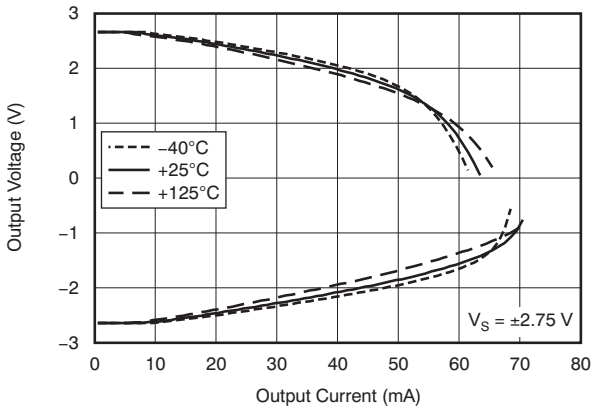


Figure 14.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

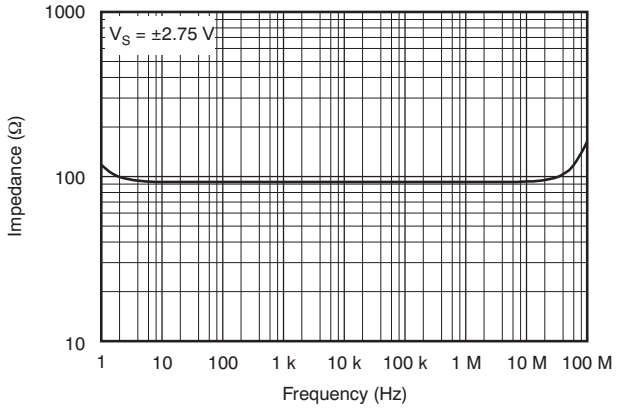


Figure 15.

SMALL-SIGNAL OVERSHOOT vs LOAD CAPACITANCE

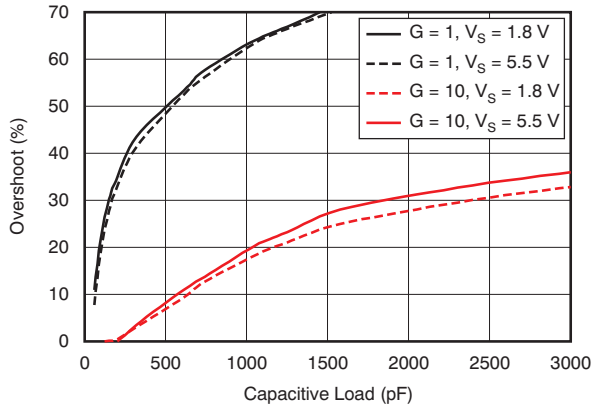


Figure 16.

THD+N vs AMPLITUDE

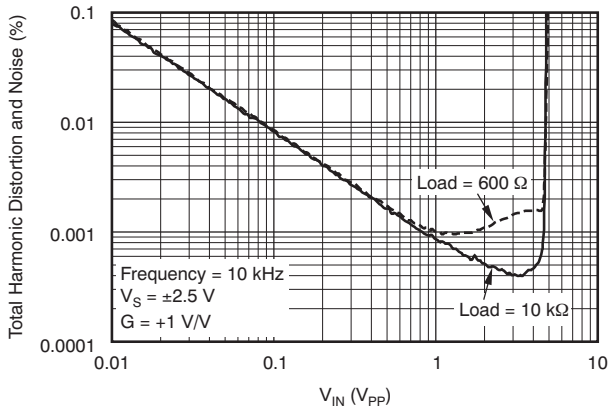


Figure 17.

THD+N vs FREQUENCY

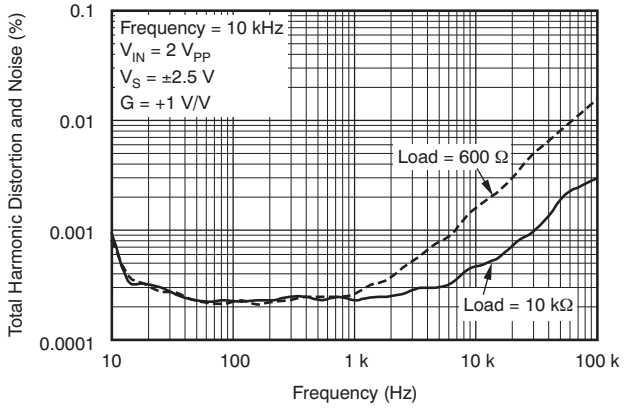


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_{CM} = V_{OUT} = mid-supply, and R_L = 10 kΩ, unless otherwise noted.

THD+N vs FREQUENCY

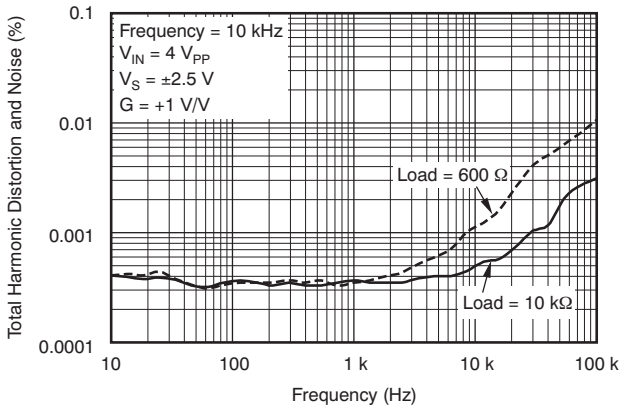


Figure 19.

CHANNEL SEPARATION vs FREQUENCY (for Dual)

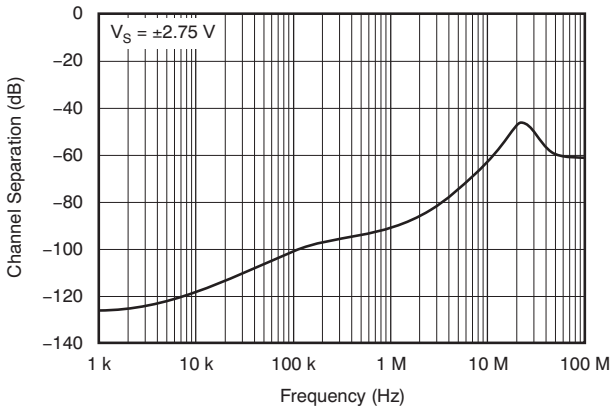


Figure 20.

SLEW RATE vs SUPPLY VOLTAGE

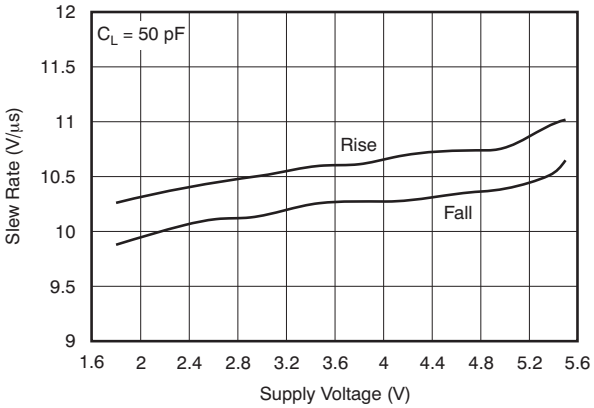


Figure 21.

SMALL-SIGNAL STEP RESPONSE

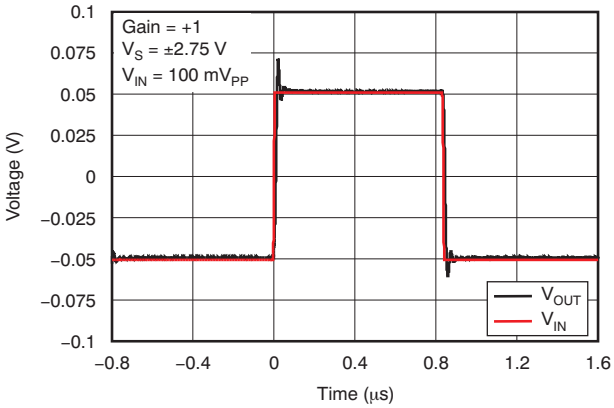


Figure 22.

SMALL-SIGNAL STEP RESPONSE

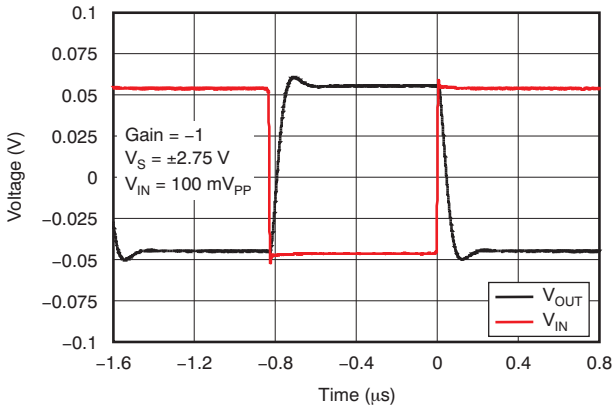


Figure 23.

LARGE-SIGNAL STEP RESPONSE vs TIME

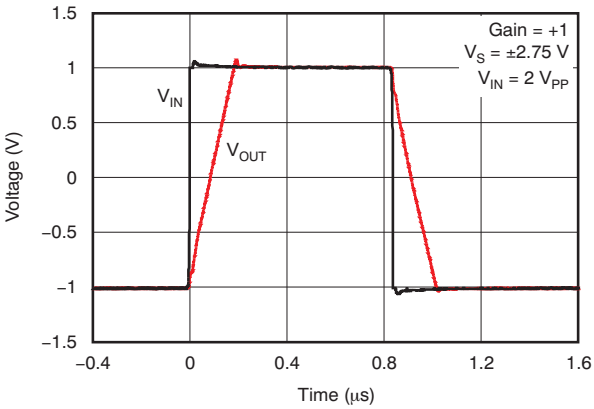


Figure 24.

APPLICATION INFORMATION

OPERATING VOLTAGE

The OPA322 series op amps are unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split-supply voltage (±0.9 V to ±2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 µF to 0.1 µF). These amplifiers are fully specified from +1.8 V to +5.5 V and over the extended temperature range of –40°C to +125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

INPUT AND ESD PROTECTION

The OPA322 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings table. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 25 shows how a series input resistor (R_S) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

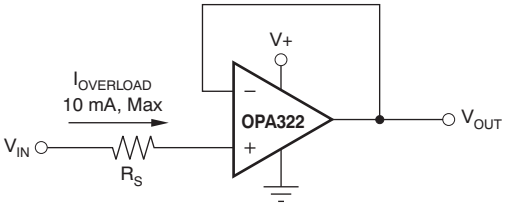


Figure 25. Input Current Protection

PHASE REVERSAL

The OPA322 op amps are designed to be immune to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. Figure 26 shows the input voltage exceeding the supply voltage without any phase reversal.

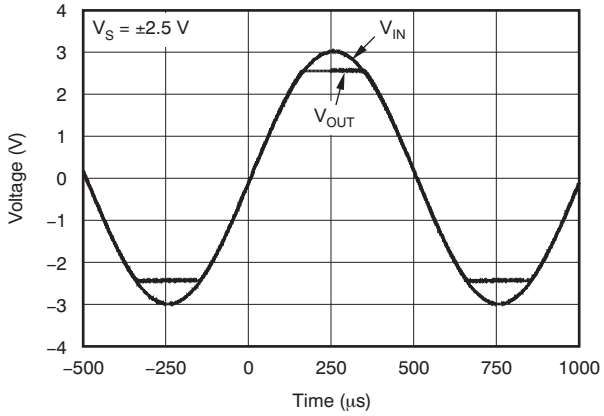
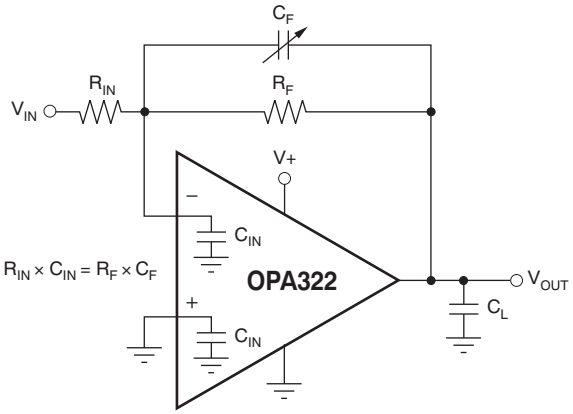


Figure 26. No Phase Reversal

FEEDBACK CAPACITOR IMPROVES RESPONSE

For optimum settling time and stability with high-impedance feedback networks, it may be necessary to add a feedback capacitor across the feedback resistor, R_F, as shown in Figure 27. This capacitor compensates for the zero created by the feedback network impedance and the OPA322 input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.



NOTE: Where C_{IN} is equal to the OPA322 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 27. Feedback Capacitor Improves Dynamic Performance

It is suggested that a variable capacitor be used for the feedback capacitor because input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 27, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA322 (typically 9 pF) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$R_{IN} \times C_{IN} = R_F \times C_F$

Where:

C_{IN} is equal to the OPA322 input capacitance (sum of differential and common-mode) plus the layout capacitance.

The capacitor value can be adjusted until optimum performance is obtained.

EMI SUSCEPTIBILITY AND INPUT FILTERING

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the device, the dc offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA322 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 580 MHz (–3 dB), with a roll-off of 20 dB per decade.

OUTPUT IMPEDANCE

The open-loop output impedance of the OPA322 common-source output stage is approximately 90 Ω. When the op amp is connected with feedback, this value is reduced significantly by the loop gain. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPA322 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This characteristic, in turn, prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA322 has excellent capacitive load drive capability for an op amp with its bandwidth.

CAPACITIVE LOAD AND STABILITY

The OPA322 is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA322 can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (+1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA322 remains stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors (C_L > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 29. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor (R_S), typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 28.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider, however, may be insignificant. For instance, with a load resistance, R_L = 10 kΩ and R_S = 20 Ω, the gain error is only about 0.2%. However, when R_L is decreased to 600 Ω, which the OPA322 is able to drive, the error increases to 7.5%.

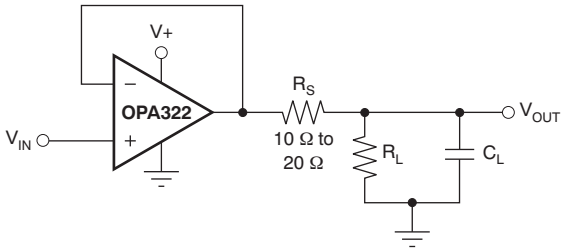


Figure 28. Improving Capacitive Load Drive

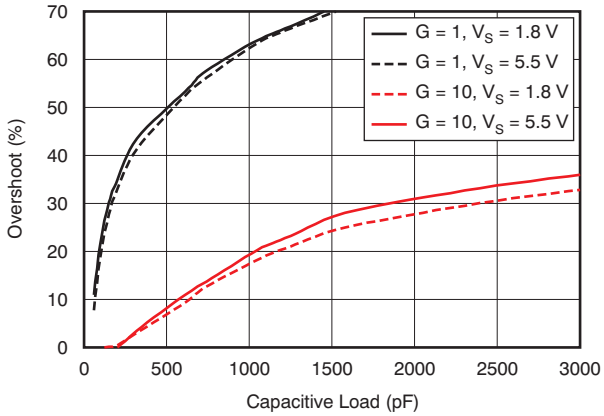


Figure 29. Small-Signal Overshoot versus Capacitive Load (100-mV_{PP} output step)

OVERLOAD RECOVERY TIME

Overload recovery time is the time required for the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 30 and Figure 31 show the positive and negative overload recovery times of the OPA322, respectively. In both cases, the time elapsed before the OPA322 comes out of saturation is less than 100 µs. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

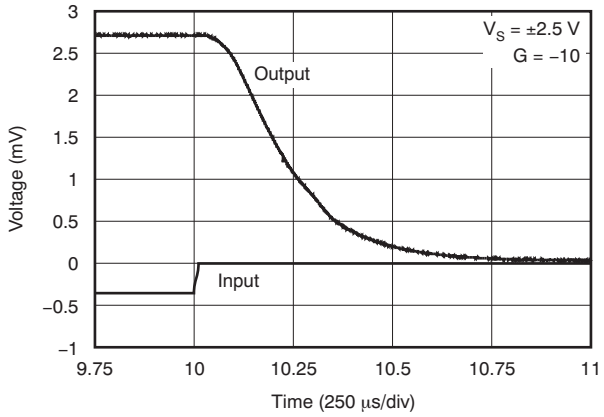


Figure 30. Positive Recovery Time

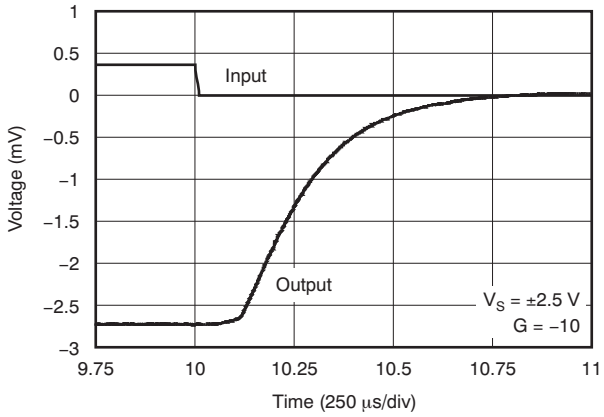


Figure 31. Negative Recovery Time

GENERAL LAYOUT GUIDELINES

The OPA322 is a wideband amplifier. To realize the full operational performance of the device, good high-frequency printed circuit board (PCB) layout practices are required. The bypass capacitors must be connected between each supply pin and ground as close to the device as possible. The bypass capacitor traces should be designed for minimum inductance.

LEADLESS DFN PACKAGE

The OPA2322 uses the DFN style package (also known as SON), which is a QFN with contacts on only two sides of the package bottom. This leadless package maximizes PCB space and offers enhanced thermal and electrical characteristics through an exposed pad. One of the primary advantages of the DFN package is its low height (0.8 mm).

DFN packages are physically small, and have a smaller routing area. Additionally, they offer improved thermal performance, reduced electrical parasitics, and a pinout scheme that is consistent with other commonly-used packages (such as SO and MSOP). Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can easily be mounted using standard PCB assembly techniques. See the application reports, *QFN/SON PCB Attachment* (SLUA271) and *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com. **The exposed leadframe die pad on the bottom of the DFN package should be connected to the most negative potential (V–).** The dimension of the exposed thermal die pad is 2mm × 1.2mm and is centered.

APPLICATION EXAMPLES

ACTIVE FILTER

The OPA322 is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 32 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications that require predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of these options:

1. adding an inverting amplifier;
2. adding an additional second-order MFB stage; or
3. using a noninverting filter topology, such as the Sallen-Key (shown in Figure 33).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

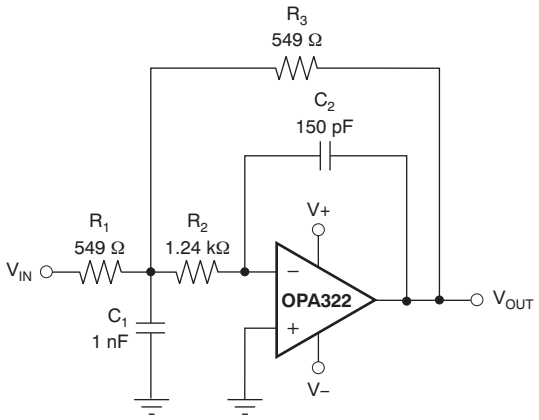


Figure 32. Second-Order Butterworth 500-kHz Low-Pass Filter

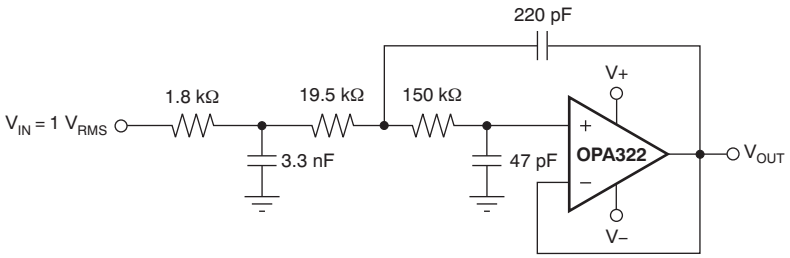


Figure 33. OPA322 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
OPA2322AID	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	
OPA2322AIDGKR	PREVIEW	MSOP	DGK	8	2500	TBD	Call TI	Call TI	
OPA2322AIDGKT	PREVIEW	MSOP	DGK	8	250	TBD	Call TI	Call TI	
OPA2322AIDR	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	
OPA2322AIDRGR	PREVIEW	SON	DRG	8	1000	TBD	Call TI	Call TI	
OPA2322AIDRGT	PREVIEW	SON	DRG	8	250	TBD	Call TI	Call TI	
OPA2322SAIDGKR	PREVIEW	MSOP	DGK	10		TBD	Call TI	Call TI	
OPA2322SAIDGKT	PREVIEW	MSOP	DGK	10		TBD	Call TI	Call TI	
OPA322AIDBVR	PREVIEW	SOT-23	DBV	5		TBD	Call TI	Call TI	
OPA322AIDBVT	PREVIEW	SOT-23	DBV	5		TBD	Call TI	Call TI	
OPA322SAIDBVR	PREVIEW	SOT-23	DBV	6		TBD	Call TI	Call TI	
OPA322SAIDBVT	PREVIEW	SOT-23	DBV	6		TBD	Call TI	Call TI	
OPA4322AIPW	PREVIEW	TSSOP	PW	14		TBD	Call TI	Call TI	
OPA4322AIPWR	PREVIEW	TSSOP	PW	14		TBD	Call TI	Call TI	
OPA4322SAIPW	PREVIEW	TSSOP	PW	16		TBD	Call TI	Call TI	
OPA4322SAIPWR	PREVIEW	TSSOP	PW	16		TBD	Call TI	Call TI	

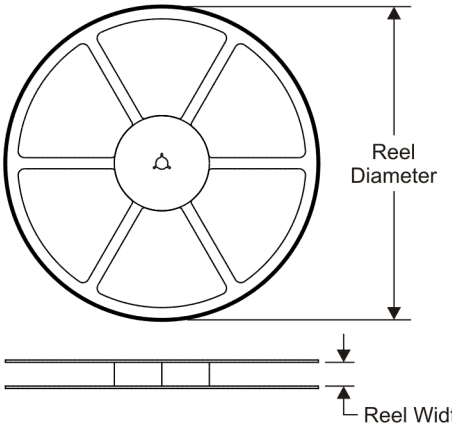
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

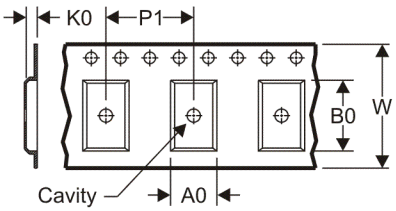
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

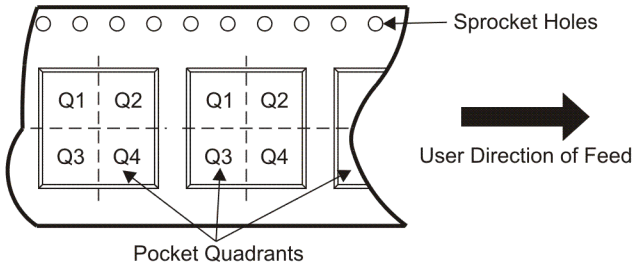


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

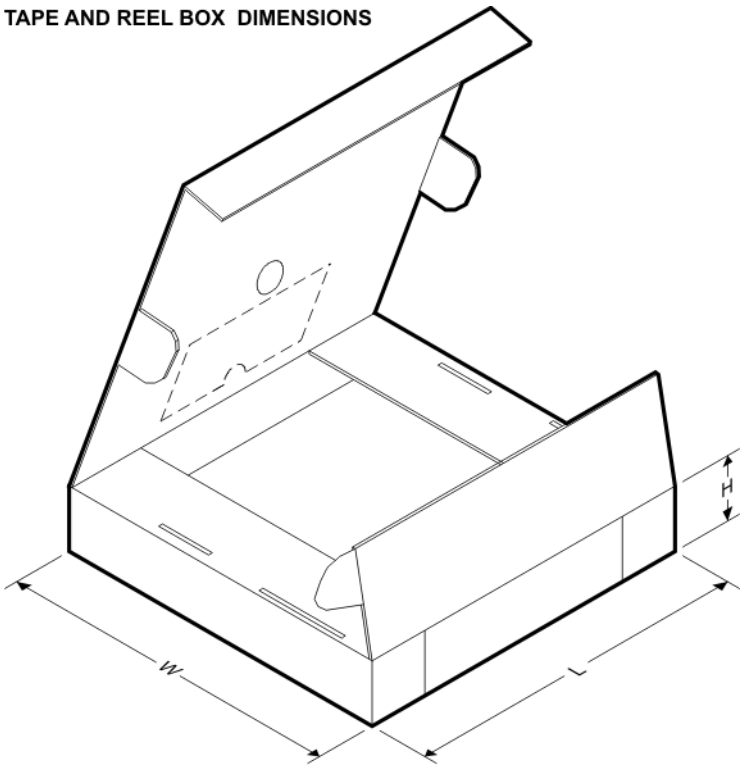
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2322AIDGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2322AIDRGR	SON	DRG	8	1000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

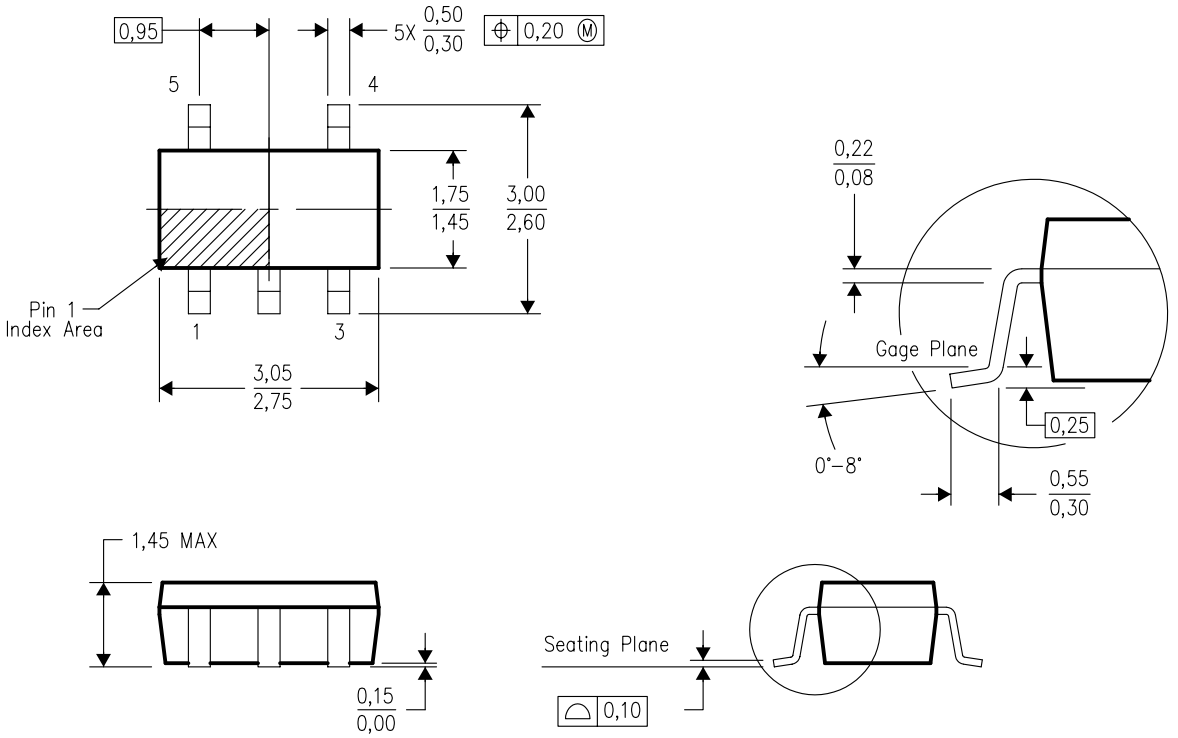
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2322AIDGKR	MSOP	DGK	8	2500	346.0	346.0	29.0
OPA2322AIDGKT	MSOP	DGK	8	250	190.5	212.7	31.8
OPA2322AIDRGR	SON	DRG	8	1000	346.0	346.0	29.0

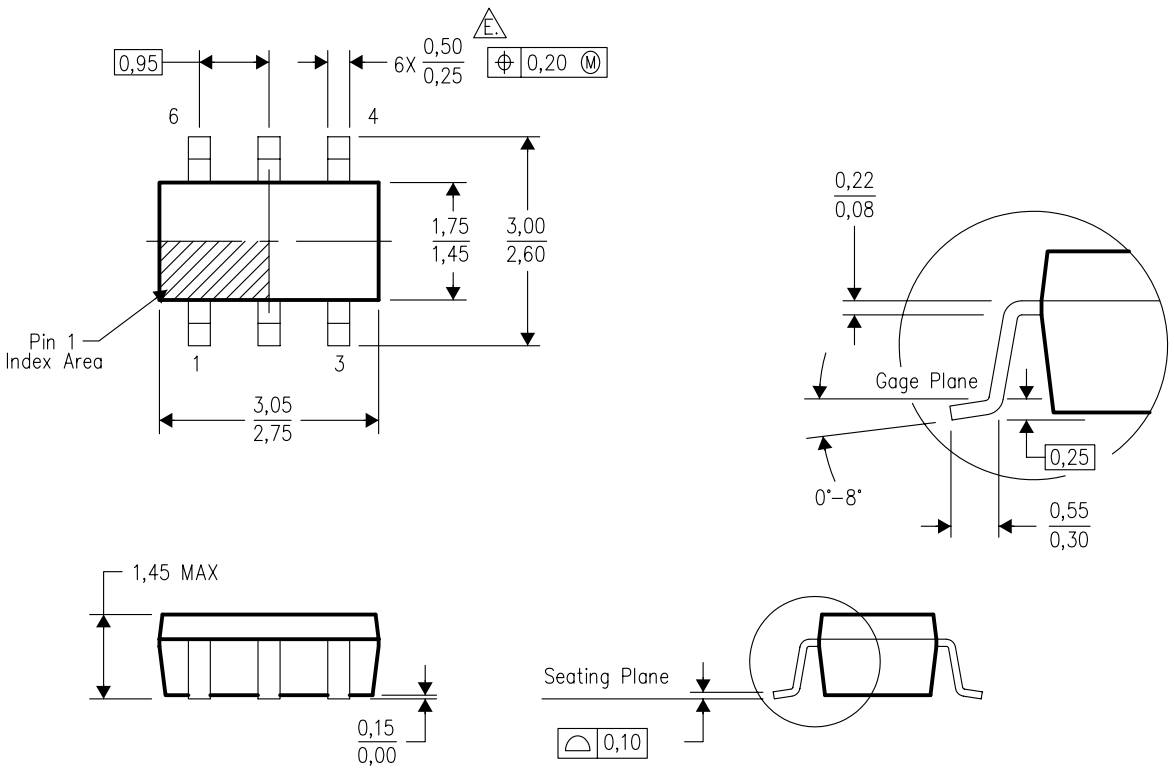
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

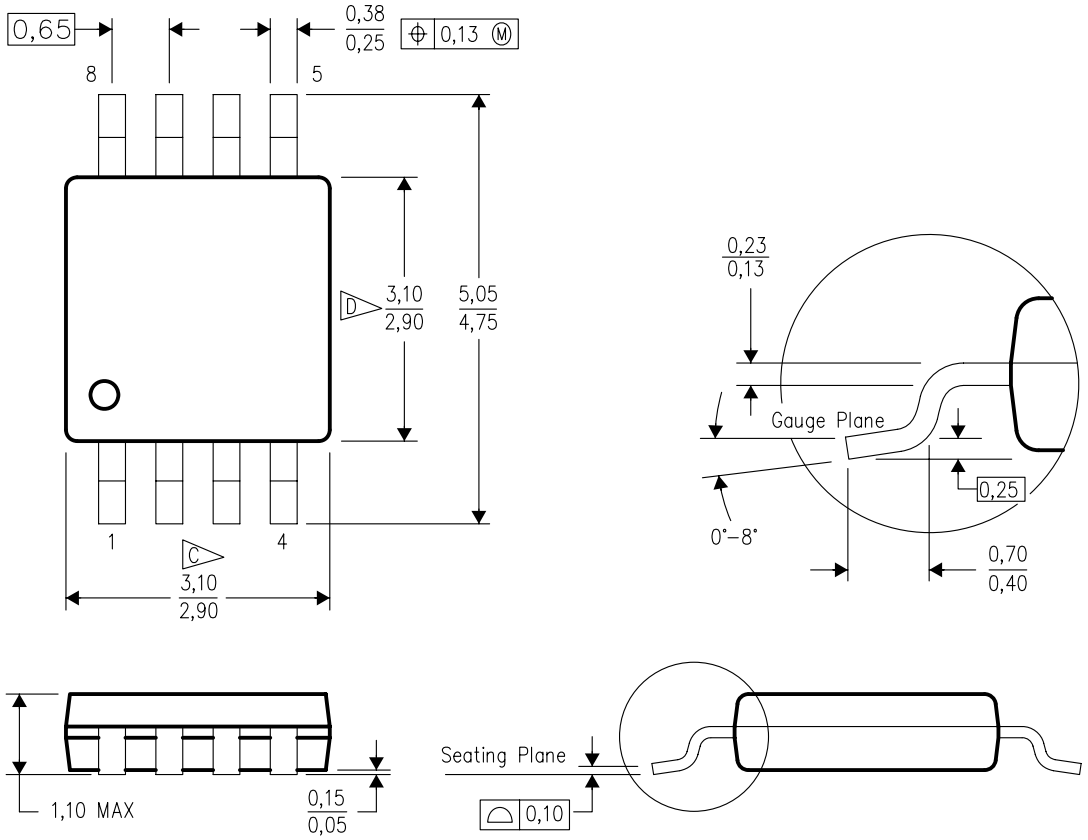
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

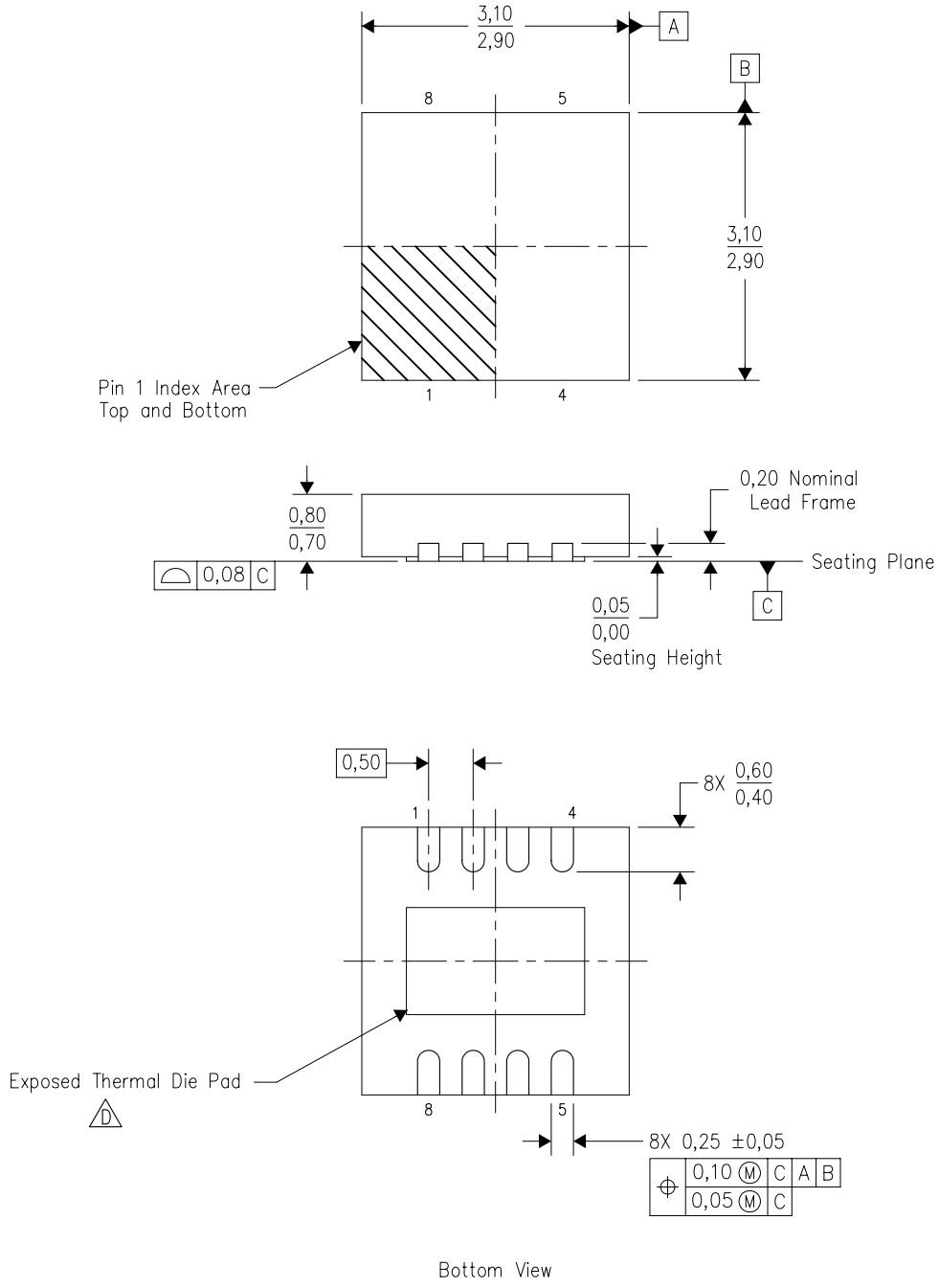
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

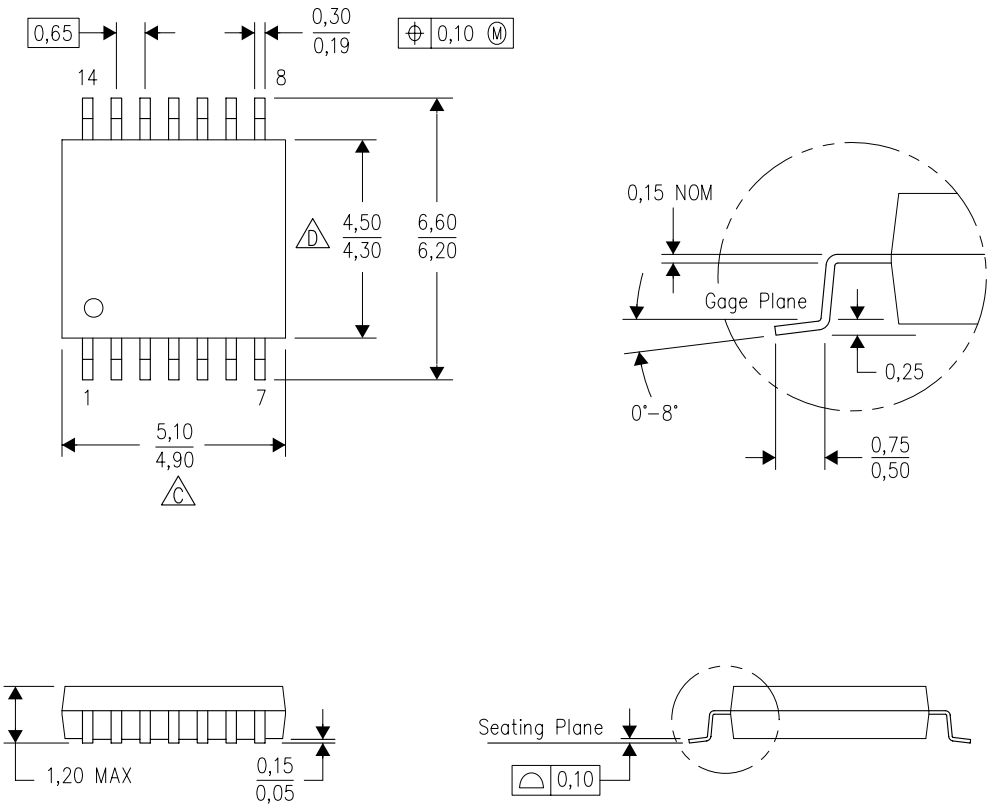
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

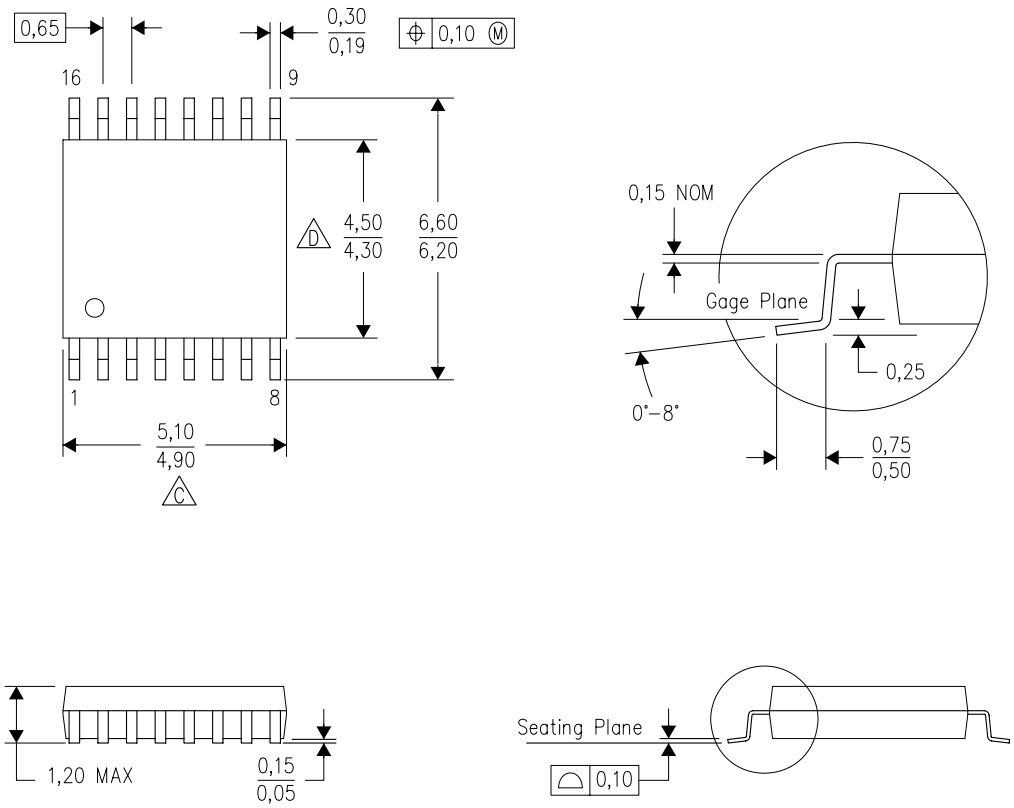
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

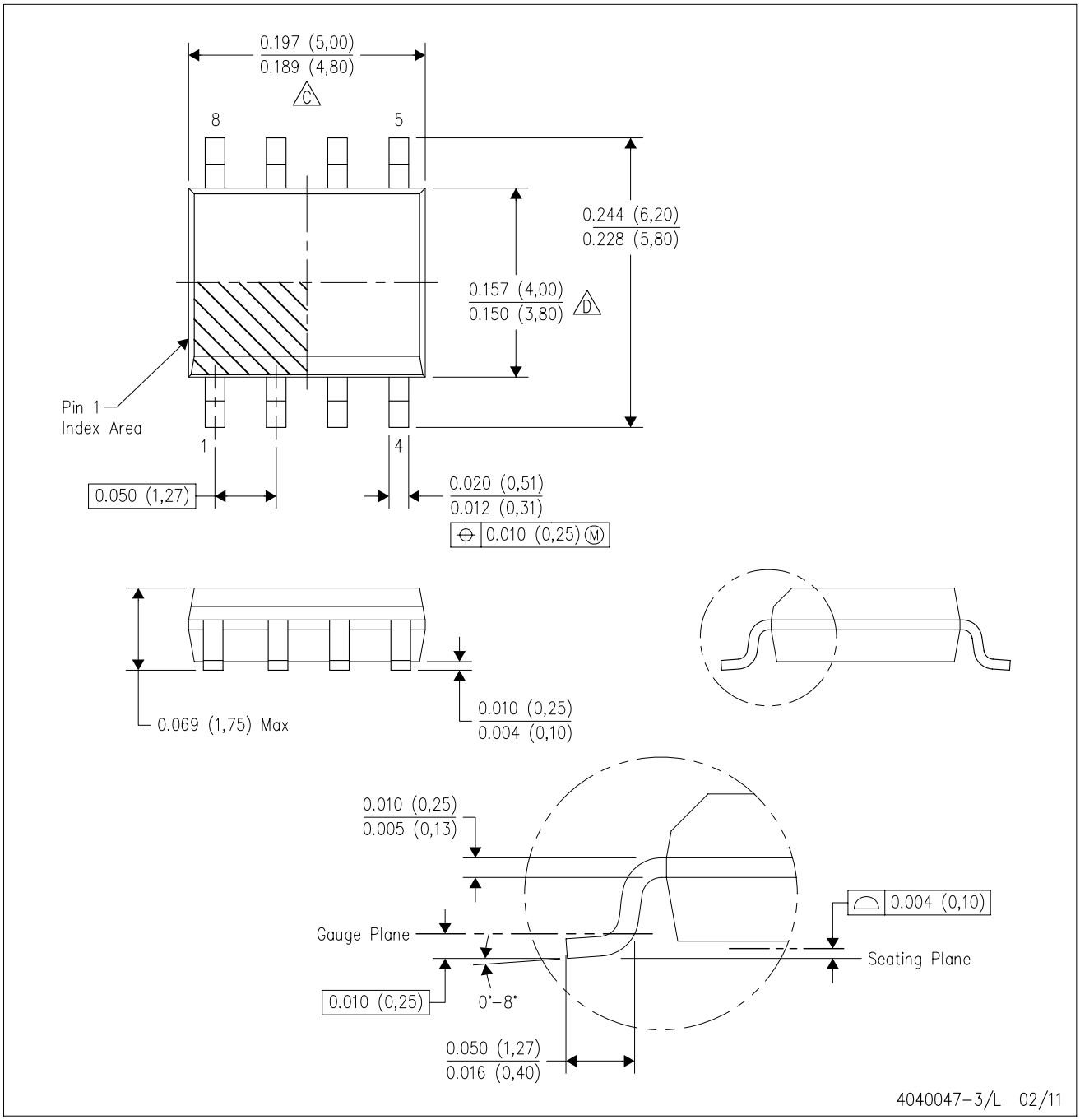
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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