超低功耗、轨至轨输出、负电源轨输入、VFB 运算放大器

查询样品: OPA835, OPA2835

特性

- 超低功耗
  - 源电压： **2.5V** 至 **5.5V**
  - 静态电流： **1mA**
  - **Power Down Mode: 0.5μA**
- 带宽： **69MHz**
- 转换速率： **160V/μs**
- 上升时间： **10ns (2V_{STEP})**
- 稳定时间： **45ns (2V_{STEP})**
- 过驱动恢复时间： **195ns**
- **SNR**： 在 **1kHz (1V_{RMS})** 时为 **0.00015% (−116.5dBc)**
- **THD**： 在 **1kHz (1V_{RMS})** 时为 **0.00003% (−130dBc)**
- **HD_2 / HD_3**： 在 **1MHz (2Vpp)** 时为 **−70dBc / −73dBc**
- 输入电压噪声： **9.3nV/√Hz (f = 100kHz)**
- 输入失调电压： **100μV** （最大值为 **500μV**）
- **CMRR: 116dB**
- 输出驱动电流： **40mA**
- **RRO**——轨至轨输出
- 输入电压范围： **−0.2V** 至 **3.9V** （**5V** 电源）
- 工作温度范围： **−40**℃ 至 **+125**℃

应用

- 低功耗信号调节
- 音频 **ADC** 输入缓冲器
- 低功耗 **SAR** 及 **ΔΣ ADC** 驱动器
- 便携式系统
- 低功耗系统
- 高密度系统

PRODUCT PREVIEW

说明

OPA835 和 OPA2835 采用业界领先的 BiCom-3x （SiGe 互补双极型）工艺制造，是单通道和双通道超低功耗、轨至轨输出、负轨输入、电压反馈运算放大器，专为在 2.5V 至 5.5V 的单电源电压范围和 ±1.25V 至 ±2.75V 的双电源电压范围内运作而设计。 这些放大器每个通道的电流消耗仅为 250μA，并具有 70MHz 的单位增益带宽，从而为轨至轨放大器设定了一个居业界领先水平的功耗一性能比。

对于将功耗作为关键性的重要指标的电池供电型便携式应用而言，OPA835 和 OPA2835 的低功耗及高频性能为设计人员提供了采用其他器件所无法获得的性能/功耗比。 再加上可将电流减小至 <1μA 的节能模式，这些器件为电池供电型应用中的高频放大器提供了一款极具吸引力的解决方案。

OPA835 和 OPA2835 提供了下列封装选项：

- OPA835 单通道器件： SOT23-6 (DBV)，和具有集成型增益电阻器的 10 引脚 RUN。
- OPA2835 双通道器件： SOIC-8 (D)、MSOP-10 (DGS) 和 10 引脚 RUN。

OPA835 RUN 封装选项包括断电 (<1μA) 和集成型增益设定电阻器，以在印刷电路板上占用尽可能小的面积（≈2mm x 2mm）。 通过在 PCB 上增设电路走线，可以实现 +1、−1、+2、−3、+4、−4、+5、−7、+8 和若干其他非整数值的增益以及衰减。 片上电阻器的阻值被精确地修整至 1% 绝对值容差以内，因而可使用外部电阻器以实现更大的灵活性。

该器件针对 −40℃ 至 125℃ 扩展工业温度范围内的运作进行了特性分析。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)

PRODUCT	CHANNEL COUNT	PACKAGE – LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA835	1	SOT23-6	DBV	–40°C to 125°C	QUM	OPA835IDBVT	TAPE and REEL, 250
OPA835	1	SOT23-6	DBV	–40°C to 125°C	QUM	OPA835IDBVR	TAPE and REEL, 3000
OPA835	1	RUN-10	RUN	–40°C to 125°C	TBD	OPA835IRUNT	TAPE and REEL, 250
OPA835	1	RUN-10	RUN	–40°C to 125°C	TBD	OPA835IRUNR	TAPE and REEL, 2500
OPA2835	2	SOIC-8	D	–40°C to 125°C	TBD	OPA2835IDT	TAPE and REEL, 250
OPA2835	2	SOIC-8	D	–40°C to 125°C	TBD	OPA2835IDR	TAPE and REEL, 2500
OPA2835	2	MSOP-10	D	–40°C to 125°C	TBD	OPA2835IDGST	TAPE and REEL, 250
OPA2835	2	MSOP-10	D	–40°C to 125°C	TBD	OPA2835IDGSR	TAPE and REEL, 2500
OPA2835	2	RUN-10	RUN	–40°C to 125°C	TBD	OPA2835IRUNT	TAPE and REEL, 250
OPA2835	2	RUN-10	RUN	–40°C to 125°C	TBD	OPA2835IRUNR	TAPE and REEL, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS

		UNITS
$V_{S–}$ to V_{S+}	Supply voltage	5.5
V_I	Input voltage	$\pm V_S$
V_{ID}	Differential input voltage	1 V
I_i	Continuous input current	20 mA
I_O	Continuous output current	100 mA
	Continuous power dissipation	See Thermal Characteristics Specification
T_J	Maximum junction temperature	150°C
T_A	Operating free-air temperature range	–40°C to 125°C
T_{stg}	Storage temperature range	–65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C
ESD ratings	HBM	2 kV
	CDM	1 kV
	MM	200 V

THERMAL INFORMATION

THERMAL METRIC(1)		OPA835 SOT23-6 (DBV) 6 PINS	OPA835 RUN-10 10 PINS	OPA2835 SOIC-8 (D) 8 PINS	OPA2835 MSOP-10 (DGS) 10 PINS	OPA2835 RUN-10 (DGS) 10 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	194					°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	129.2					
θ_{JB}	Junction-to-board thermal resistance	39.4					
ψ_{JT}	Junction-to-top characterization parameter	25.6					
ψ_{JB}	Junction-to-board characterization parameter	38.9					
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a					

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

SPECIFICATIONS: V_S = 2.7 V

Test conditions unless otherwise noted: V_{S+} = +2.7V, V_{S-} = 0V, V_{OUT} = 1V_{PP}, R_F = 0Ω, R_L = 1kΩ, G = 1V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 50 mV_{PP}, G = 1		69		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 1		51			
	V_{OUT} = 100 mV_{PP}, G = 2		27			
	V_{OUT} = 100 mV_{PP}, G = 5		7.2			
	V_{OUT} = 100 mV_{PP}, G = 10		3			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		30		MHz	C
Large-signal bandwidth	V_{OUT} = 1 V_{PP}, G = 1		24		MHz	C
Bandwidth for 0.1dB flatness	V_{OUT} = 1 V_{PP}, G = 2		4		MHz	C
Slew rate, Rise/Fall	V_{OUT} = 1V_{STEP}, G = 2		110/130		V/µs	C
Rise/Fall time			9.5/9		ns	C
Settling time to 1%, Rise/Fall			35/30		ns	C
Settling time to 0.1%, Rise/Fall			60/65		ns	C
Settling time to 0.01%, Rise/Fall			120/90		ns	C
Overshoot/Undershoot			0.5/0.2		%	C
2nd Order Harmonic Distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5V		-133		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5V		-110			
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5V		-73			C
3rd Order Harmonic Distortion	f = 10 kHz, V_{IN_CM} = mid-supply – 0.5V		-137		dBc	C
	f = 100 kHz, V_{IN_CM} = mid-supply – 0.5V		-125			
	f = 1 MHz, V_{IN_CM} = mid-supply – 0.5V		-78			C
2nd Order Intermodulation Distortion	f = 1 MHz, 200 kHz Tone Spacing, V_{OUT} Envelope = 1V_{PP}, V_{IN_CM} = mid-supply – 0.5V		-75		dBc	C
3rd Order Intermodulation Distortion			-81		dBc	C
Input voltage noise	f = 100 KHz		9.3		nV/√Hz	C
Voltage Noise 1/f corner frequency			650		Hz	C
Input current noise	f = 1 MHz		0.45		pA/√Hz	C
Current Noise 1/f corner frequency			TBD		Hz	C
Overdrive recovery time, Over/Under	Overdrive = 0.5 V		140/125		ns	C
Closed-loop output impedance	f = 100 kHz		0.028		Ω	C
Channel to channel crosstalk (OPA2836)	f = 10 kHz		TBD		dB	C

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.

PRODUCT PREVIEW

SPECIFICATIONS: V_{S+} = 2.7 V

Test conditions unless otherwise noted: V_{S+} = +2.7V, V_{S-} = 0V, V_{OUT} = 1V_{PP}, R_F = 0Ω, R_L = 1kΩ, G = 1V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
DC PERFORMAN CE						
Open-loop voltage gain (A_{OL})		100	120		dB	A
Input referred offset voltage	T_A = 25°C		±100	±500	μV	A
	T_A = 0°C to 70°C			±880		B
	T_A = –40°C to 85°C			±1040		
	T_A = –40°C to 125°C			±1850		
Input offset voltage drift(2)	T_A = 0°C to 70°C		±1.4	±8.5	μV/°C	B
	T_A = –40°C to 85°C		±1.5	±9		
	T_A = –40°C to 125°C		±2.25	±13.5		
Input bias current	T_A = 25°C	50	200	400	nA	A
	T_A = 0°C to 70°C	47		410		B
	T_A = –40°C to 85°C	45		425		
	T_A = –40°C to 125°C	45		530		
Input bias current drift	T_A = 0°C to 70°C		±0.25	±1.4	nA/°C	B
	T_A = –40°C to 85°C		±0.175	±1.05		
	T_A = –40°C to 125°C		±0.185	±1.1		
Input offset current	T_A = 25°C		±13	±100	nA	A
	T_A = 0°C to 70°C		±13	±100		B
	T_A = –40°C to 85°C		±13	±100		
	T_A = –40°C to 125°C		±13	±100		
Input offset current drift(2)	T_A = 0°C to 70°C		±0.205	±1.230	nA/°C	B
	T_A = –40°C to 85°C		±0.155	±0.940		
	T_A = –40°C to 125°C		±0.155	±0.940		
INPUT						
Common-mode input range low	T_A = 25°C		V_{S-} – 0.2	V_{S-}	V	A
	T_A = –40°C to 125°C		V_{S-} – 0.2	V_{S-}	V	B
Common-mode input range high	T_A = 25°C	V_{S+} – 1.2	V_{S+}– 1.1		V	A
	T_A = –40°C to 125°C	V_{S+} – 1.2	V_{S+} – 1.1		V	B
Common-mode rejection ratio		91	110		dB	A
Input impedance common mode			200||1.2		kΩ || pF	C
Input impedance differential mode			200||1		kΩ || pF	C
OUTPUT						
Linear output voltage low	T_A = 25°C, G = 5		V_{S-} + 0.15	V_{S-} + 0.2	V	A
	T_A = –40°C to 125°C, G = 5		V_{S-} + 0.15	V_{S-} + 0.2	V	B
Linear output voltage high	T_A = 25°C, G = 5	V_{S+} – 0.25	V_{S+} – 0.2		V	A
	T_A = –40°C to 125°C, G = 5	V_{S+} – 0.25	V_{S+} – 0.2		V	B
Output saturation voltage, High / Low	T_A = 25°C, G = 5		45/13		mV	C
Linear output current drive	T_A = 25°C	±25	±35		mA	A
	T_A = –40°C to 125°C	±20				B
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current	T_A = 25°C	205	245	340	μA	A
	T_A = –40°C to 125°C	135		345	μA	B
Power supply rejection (±PSRR)		91	105		dB	A

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

PRODUCT PREVIEW

SPECIFICATIONS: V_{S+} = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = +2.7V, V_{S-} = 0V, V_{OUT} = 1V_{PP}, R_F = 0Ω, R_L = 1kΩ, G = 1V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
POWER DOWN (PIN MUST BE DRIVEN)						
Enable voltage threshold	Specified "on" above V_{S-}+ 2.1 V		V_{S-}+ 1.4	V_{S-}+ 2.1	V	A
Disable voltage threshold	Specified "off" below V_{S-}+ 0.7 V	V_{S-}+ 0.7	V_{S-}+ 1.4		V	A
Powerdown pin bias current			20	500	nA	A
Powerdown quiescent current			0.5	1.5	µA	A
Turn-on time delay	Time from PD = high to V_{OUT} = 90% of final value		250		ns	C
Turn-off time delay	Time from PD = low to V_{OUT} = 10% of original value		50		ns	C

PRODUCT PREVIEW

SPECIFICATIONS: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = +5V, V_{S-} = 0V, V_{OUT} = 2V_{PP}, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
AC PERFORMANCE						
Small-signal bandwidth	V_{OUT} = 50 mV_{PP}, G = 1		69		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 1		56			
	V_{OUT} = 100 mV_{PP}, G = 2		27			
	V_{OUT} = 100 mV_{PP}, G = 5		7.4			
	V_{OUT} = 100 mV_{PP}, G = 10		3.1			
Gain-bandwidth product	V_{OUT} = 100 mV_{PP}, G = 10		31		MHz	C
Large-signal bandwidth	V_{OUT} = 2 V_{PP}, G = 1		31		MHz	C
Bandwidth for 0.1dB flatness	V_{OUT} = 2 V_{PP}, G=2		14.5		MHz	C
Slew rate, Rise/Fall	V_{OUT} = 2V Step, G=2		160/260		V/µs	C
Rise/Fall time			10/7		ns	C
Settling time to 1%, Rise/Fall			45/45			C
Settling time to 0.1%, Rise/Fall			50/55			C
Settling time to 0.01%, Rise/Fall			82/85			C
Overshoot/Undershoot			2.5/1.5		%	C
2nd Order Harmonic Distortion	f = 10 kHz		–135		dBc	C
	f = 100 kHz		–105			C
	f = 1 MHz		-70			C
3rd Order Harmonic Distortion	f = 10 kHz		–139		dBc	C
	f = 100 kHz		–122			C
	f = 1 MHz		-73			C
2nd Order Intermodulation Distortion	f = 1 MHz, 200 kHz Tone Spacing, V_{OUT} Envelope = 2V_{PP}		–70		dBc	C
3rd Order Intermodulation Distortion			–83		dBc	C
Signal to Noise Ratio, SNR	f = 1kHz, V_{OUT} = 1 V_{RMS}, 22kHz bandwidth		0.00015		%	C
			-116.4		dBc	
Total Harmonic Distortion, THD	f = 1kHz, V_{OUT} = 1 V_{RMS}		0.00003		%	C
			-130		dBc	C
Input voltage noise	f = 100 KHz		9.3		nV/√Hz	C
Voltage Noise 1/f corner frequency			650		Hz	C
Input current noise	f = 1 MHz		0.45		pA/√Hz	C
Current Noise 1/f corner frequency			TBD		Hz	C
Overdrive recovery time, Over/Under	Overdrive = 0.5 V		195/135		ns	C
Closed-loop output impedance	f = 100 kHz		0.028		Ω	C
Channel to channel crosstalk (OPA2835)	f = 10 kHz		TBD		dB	C

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.

PRODUCT PREVIEW

SPECIFICATIONS: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = +5V, V_{S-} = 0V, V_O = $2V_{PP}$, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
DC PERFORMANCE						
Open-loop voltage gain (A_{OL})		100	120		dB	A
Input referred offset voltage	T_A = 25°C		±100	±500	μV	A
	T_A = 0°C to 70°C			±880		B
	T_A = –40°C to 85°C			±1040		
	T_A = –40°C to 125°C			±1850		
Input offset voltage drift(2)	T_A = 0°C to 70°C		±1.4	±8.5	μV/°C	B
	T_A = –40°C to 85°C		±1.5	±9		
	T_A = –40°C to 125°C		±2.25	±13.5		
Input bias current	T_A = 25°C	50	200	400	nA	A
	T_A = 0°C to 70°C	47		410		B
	T_A = –40°C to 85°C	45		425		
	T_A = –40°C to 125°C	45		530		
Input bias current drift	T_A = 0°C to 70°C		±0.25	±1.4	nA/°C	B
	T_A = –40°C to 85°C		±0.175	±1.05		
	T_A = –40°C to 125°C		±0.185	±1.1		
Input offset current	T_A = 25°C		±13	±100	nA	A
	T_A = 0°C to 70°C		±13	±100		B
	T_A = –40°C to 85°C		±13	±100		
	T_A = –40°C to 125°C		±13	±100		
Input offset current drift(2)	T_A = 0°C to 70°C		±0.205	±1.23	nA/°C	B
	T_A = –40°C to 85°C		±0.155	±0.94		
	T_A = –40°C to 125°C		±0.155	±0.94		
INPUT						
Common-mode input range low	T_A = 25°C		V_{S-} – 0.2	V_{S-}	V	A
	T_A = –40°C to 125°C		V_{S-} – 0.1	V_{S-}	V	B
Common-mode input range high	T_A = 25°C	V_{S+} – 1.2	V_{S+} – 1.1		V	A
	T_A = –40°C to 125°C	V_{S+} – 1.2	V_{S+} – 1.1		V	B
Common-mode rejection ratio		94	113		dB	A
Input impedance common mode			200||1.2		kΩ || pF	C
Input impedance differential mode			200||1		kΩ || pF	C
OUTPUT						
Linear output voltage low	T_A = 25°C, G = 5		V_{S-} + 0.15	V_{S-} + 0.2	V	A
	T_A = –40°C to 125°C, G = 5		V_{S-} + 0.15	V_{S-} + 0.2	V	B
Linear output voltage high	T_A = 25°C, G = 5	V_{S+} – 0.25	V_{S+} – 0.2		V	A
	T_A = –40°C to 125°C, G = 5	V_{S+} – 0.25	V_{S+} – 0.2		V	B
Output saturation voltage, High / Low	T_A = 25°C, G = 5		70/25		mV	C
Linear output current drive	T_A = 25°C	±30	±40		mA	A
	T_A = –40°C to 125°C	±25				B
POWER SUPPLY						
Specified operating voltage		2.5		5.5	V	B
Quiescent operating current	T_A = 25°C	215	250	350	μA	A
	T_A = –40°C to 125°C	150		365	μA	B
Power supply rejection (±PSRR)		93	110		dB	A

(1) Test levels (all values set by characterization and simulation): **(A)** 100% tested at 25°C; over temperature limits by characterization and simulation. **(B)** Not tested in production; limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Input Offset Voltage Drift, Input Bias Current Drift, and Input Offset Current Drift are average values calculated by taking data at the end points, computing the difference, and dividing by the temperature range.

PRODUCT PREVIEW

SPECIFICATIONS: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = +5V, V_{S-} = 0V, V_O = $2V_{PP}$, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply. T_A = 25°C. Unless otherwise noted.

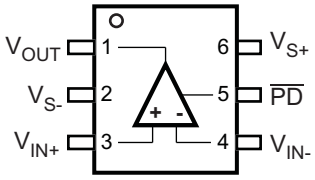
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	TEST LEVEL(1)
POWER DOWN (PIN MUST BE DRIVEN)						
Enable voltage threshold	Specified "on" above 2.1 V		V_{S-} + 1.4	V_{S-} + 2.1	V	A
Disable voltage threshold	Specified "off" below 0.7 V	V_{S-} + 0.7	V_{S-} + 1.4		V	A
Powerdown pin bias current			20	500	nA	A
Powerdown quiescent current			0.6	2	µA	A
Turn-on time delay	Time from PD = high to V_{OUT} = 90% of final value		200		ns	C
Turn-off time delay	Time from PD = low to V_{OUT} = 10% of original value		60		ns	C

PRODUCT PREVIEW

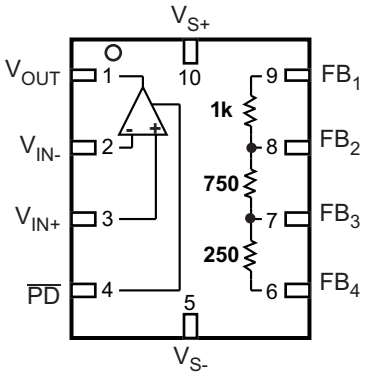
DEVICE INFORMATION

PIN CONFIGURATIONS

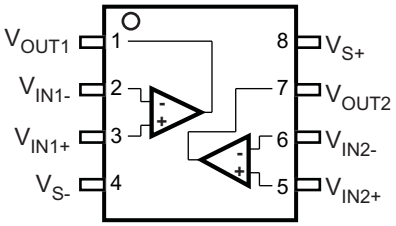
OPA835 (TOP VIEW)
SOT23-6 (DBV)



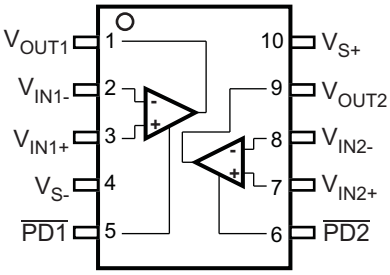
OPA835 (TOP VIEW)
RUN-10



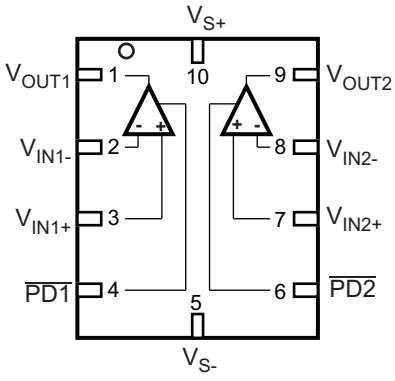
OPA2835 (TOP VIEW)
SOIC-8 (D)



OPA2835 (TOP VIEW)
MSOP-10 (DGS)



OPA2835 (TOP VIEW)
RUN-10



PRODUCT PREVIEW

PIN FUNCTIONS

PIN		DESCRIPTION
NUMBER	NAME	
OPA835 DBV PACKAGE		
1	V_{OUT}	Amplifier output
2	V_{S-}	Negative power supply input
3	V_{IN+}	Amplifier non-inverting input
4	V_{IN-}	Amplifier inverting input
5	PD	Amplifier Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
6	V_{S+}	Positive power supply input
OPA835 RUN PACKAGE		
1	V_{OUT}	Amplifier output
2	V_{IN-}	Amplifier inverting input
3	V_{IN+}	Amplifier non-inverting input
4	PD	Amplifier Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
5	V_{S-}	Negative power supply input
6	FB_4	Connection to bottom of 250 Ω internal gain setting resistors
7	FB_3	Connection to junction of 750 and 250 Ω internal gain setting resistors
8	FB_2	Connection to junction of 1k and 750 Ω internal gain setting resistors
9	FB_1	Connection to top of 1kΩ internal gain setting resistors
10	V_{S+}	Positive power supply input
OPA2835 D PACKAGE		
1	V_{OUT1}	Amplifier 1 output
2	V_{IN1-}	Amplifier 1 inverting input
3	V_{IN1+}	Amplifier 1 non-inverting input
4	V_{S-}	Negative power supply input
5	V_{IN2+}	Amplifier 2 non-inverting input
6	V_{IN2-}	Amplifier 2 inverting input
7	V_{OUT2}	Amplifier 2 output
8	V_{S+}	Positive power supply input
OPA2835 DSG PACKAGE		
1	V_{OUT1}	Amplifier 1 output
2	V_{IN1-}	Amplifier 1 inverting input
3	V_{IN1+}	Amplifier 1 non-inverting input
4	V_{S-}	Negative power supply input
5	PD1	Amplifier 1 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
6	PD2	Amplifier 2 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
7	V_{IN2+}	Amplifier 2 non-inverting input
8	V_{IN2-}	Amplifier 2 inverting input
9	V_{OUT2}	Amplifier 2 output
10	V_{S+}	Positive power supply input
OPA2835 RUN PACKAGE		
1	V_{OUT1}	Amplifier 1 output
2	V_{IN1-}	Amplifier 1 inverting input
3	V_{IN1+}	Amplifier 1 non-inverting input
4	PD1	Amplifier 1 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
5	V_{S-}	Negative power supply input
6	PD2	Amplifier 2 Power Down, low = low power mode, high = normal operation **(PIN MUST BE DRIVEN)**
7	V_{IN2+}	Amplifier 2 non-inverting input

PRODUCT PREVIEW

PIN FUNCTIONS (continued)

PIN		DESCRIPTION
NUMBER	NAME	
8	V_{IN2-}	Amplifier 2 inverting input
9	V_{OUT2}	Amplifier 2 output
10	V_{S+}	Positive power supply input

PRODUCT PREVIEW

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V

Test conditions unless otherwise noted: V_{S+} = +2.7V, V_{S-} = 0V, V_{OUT} = 1Vpp, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply unless otherwise noted. T_A = 25°C.

SMALL SIGNAL FREQUENCY RESPONSE

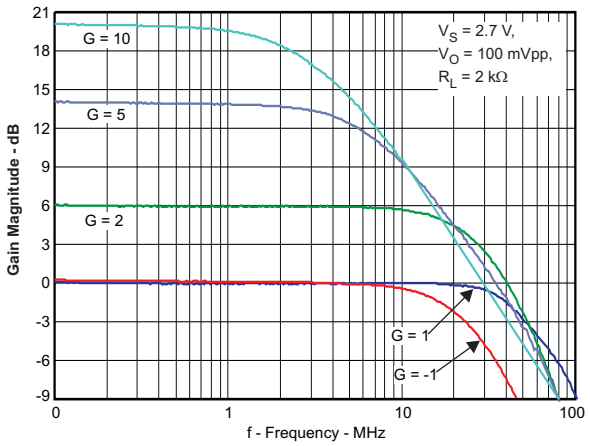


Figure 1.

LARGE SIGNAL FREQUENCY RESPONSE

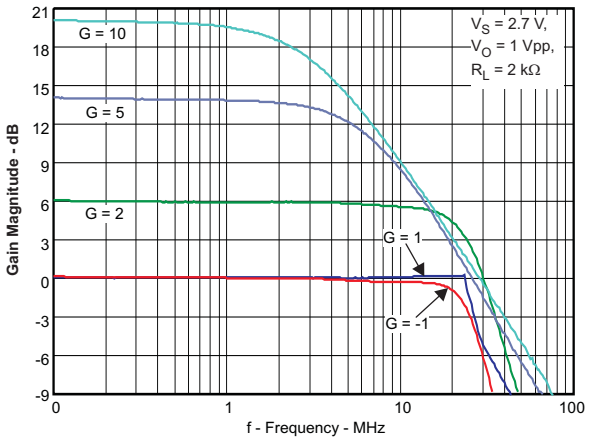


Figure 2.

FREQUENCY RESPONSE WITH CAPACITIVE LOAD

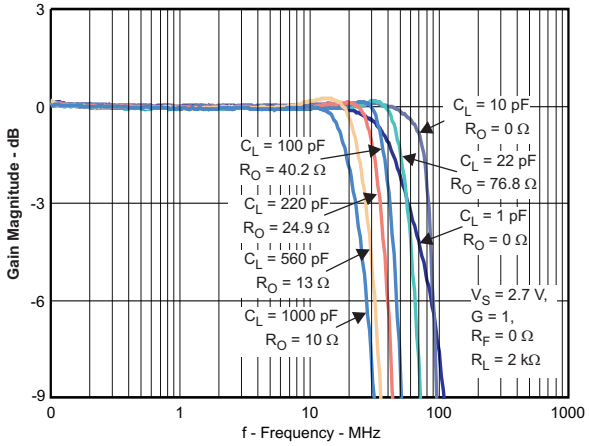


Figure 3.

SERIES OUTPUT RESISTOR vs CAPACITIVE LOAD

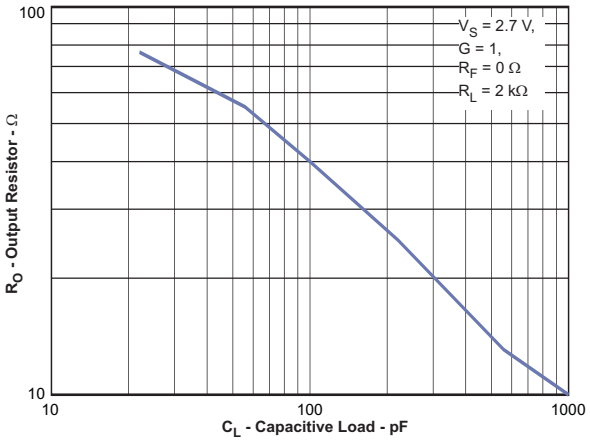


Figure 4.

PRODUCT PREVIEW

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = +2.7V, V_{S-} = 0V, V_{OUT} = 1Vpp, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply unless otherwise noted. T_A = 25°C.

NONINVERTING PULSE RESPONSE

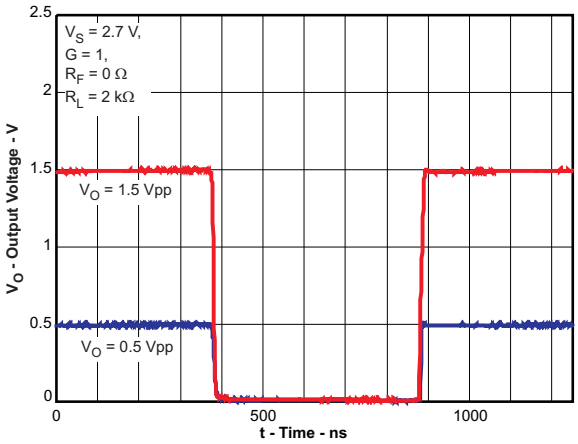


Figure 5.

INVERTING PULSE RESPONSE

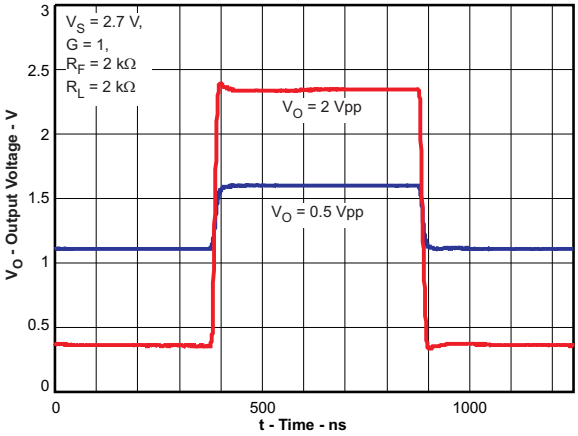


Figure 6.

OUTPUT OVERDRIVE RECOVERY

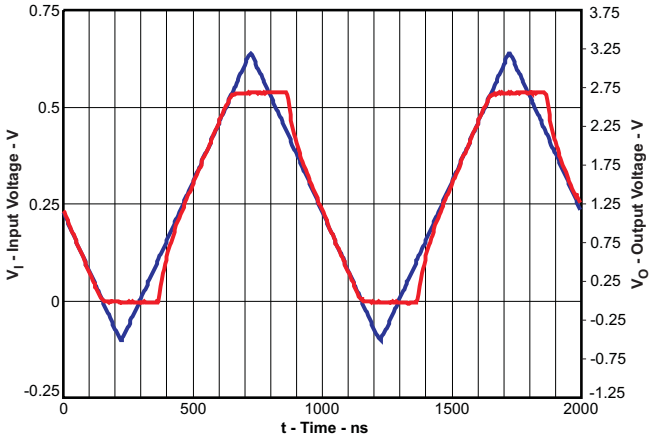


Figure 7.

SLEW RATE vs OUTPUT VOLTAGE STEP

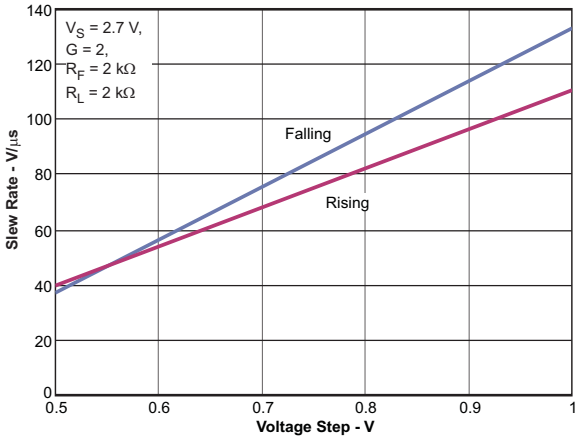


Figure 8.

PRODUCT PREVIEW

TYPICAL PERFORMANCE GRAPHS: V_S = 2.7 V (continued)

Test conditions unless otherwise noted: V_{S+} = +2.7V, V_{S-} = 0V, V_{OUT} = 1Vpp, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply unless otherwise noted. T_A = 25°C.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

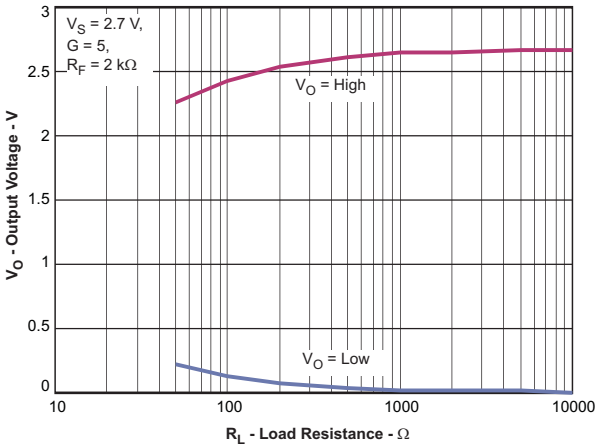


Figure 9.

OUTPUT SATURATION VOLTAGE vs LOAD CURRENT

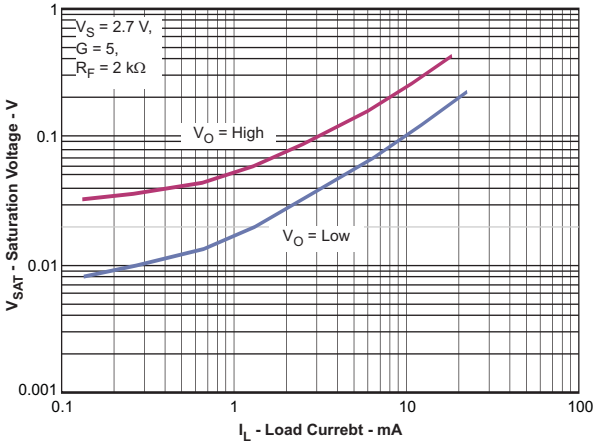


Figure 10.

OUTPUT IMPEDANCE vs FREQUENCY

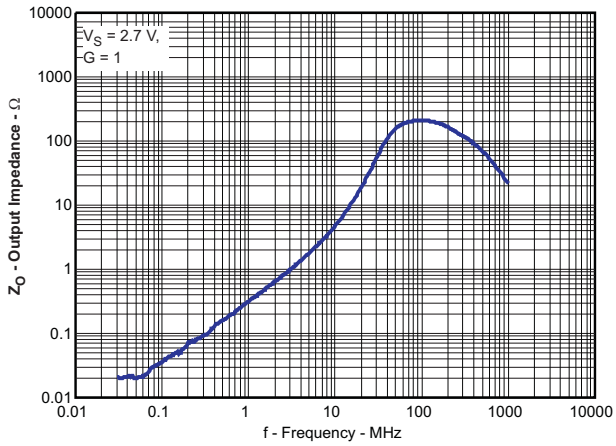


Figure 11.

POWER DOWN RESPONSE

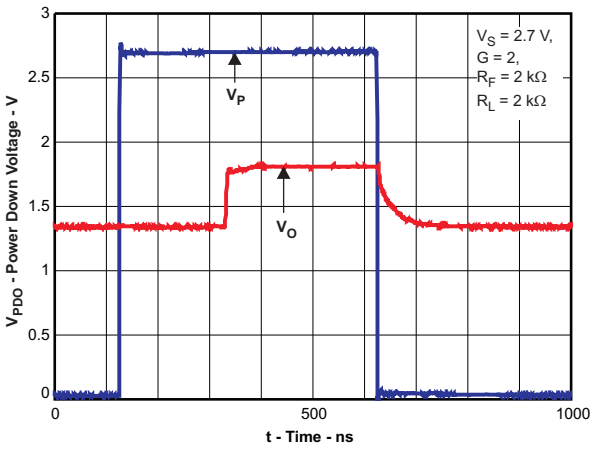


Figure 12.

PRODUCT PREVIEW

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V

Test conditions unless otherwise noted: V_{S+} = +5V, V_{S-} = 0V, V_{OUT} = 2Vpp, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply unless otherwise noted. T_A = 25°C.

SMALL SIGNAL FREQUENCY RESPONSE

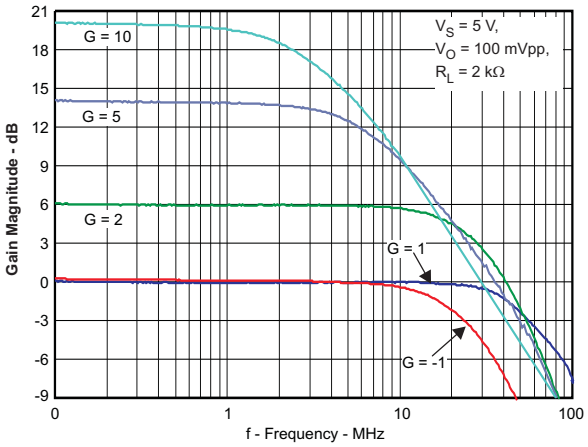


Figure 13.

LARGE SIGNAL FREQUENCY RESPONSE

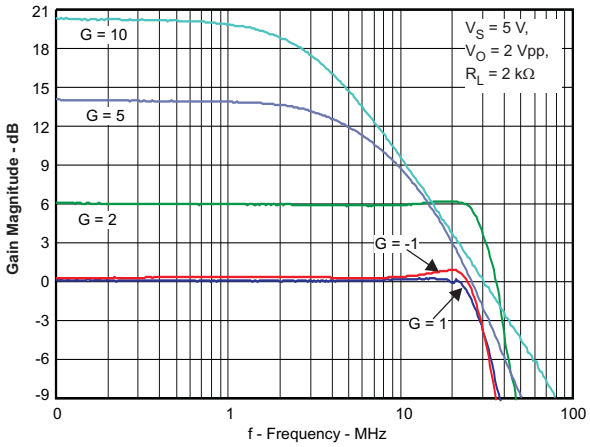


Figure 14.

FREQUENCY RESPONSE WITH CAPACITIVE LOAD

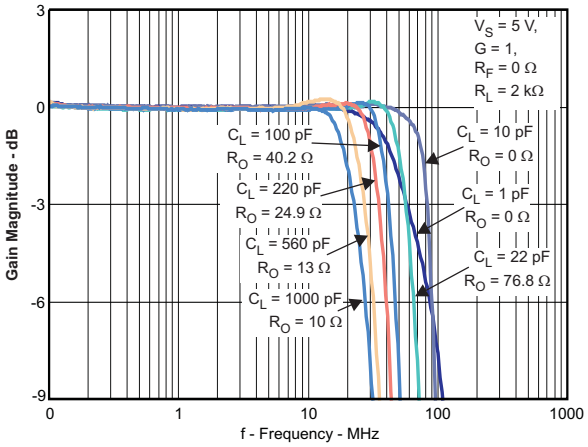


Figure 15.

SERIES OUTPUT RESISTOR vs CAPACITIVE LOAD

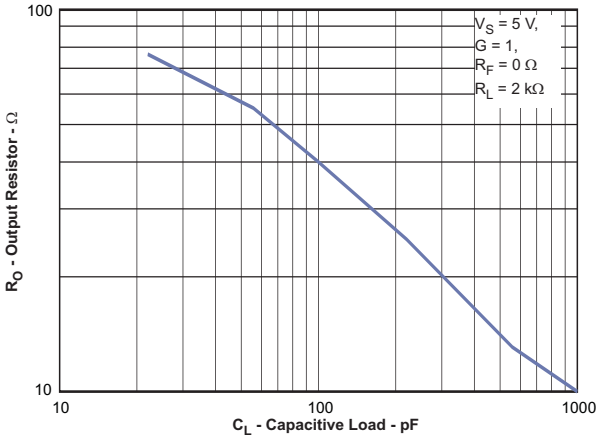


Figure 16.

PRODUCT PREVIEW

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = +5V, V_{S-} = 0V, V_{OUT} = 2Vpp, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply unless otherwise noted. T_A = 25°C.

NONINVERTING PULSE RESPONSE

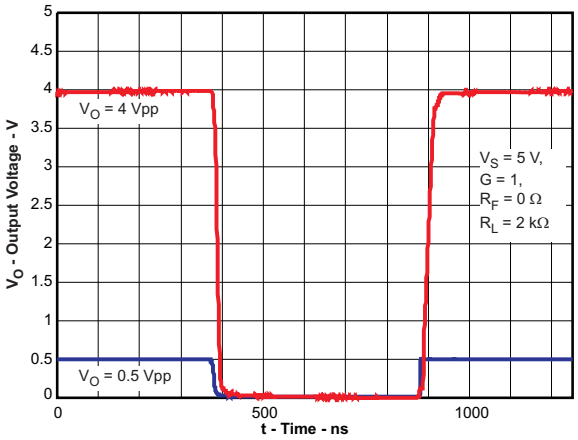


Figure 17.

INVERTING PULSE RESPONSE

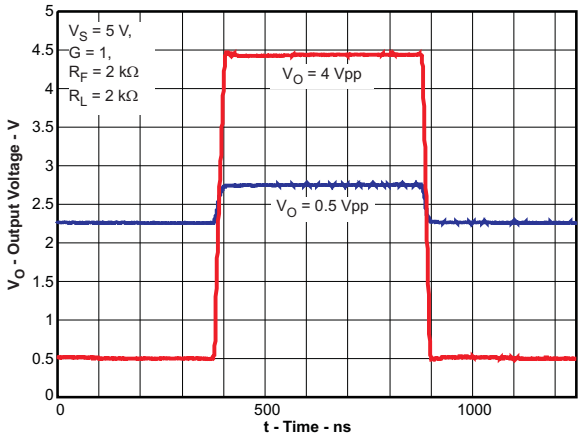


Figure 18.

OUTPUT OVERDRIVE RECOVERY

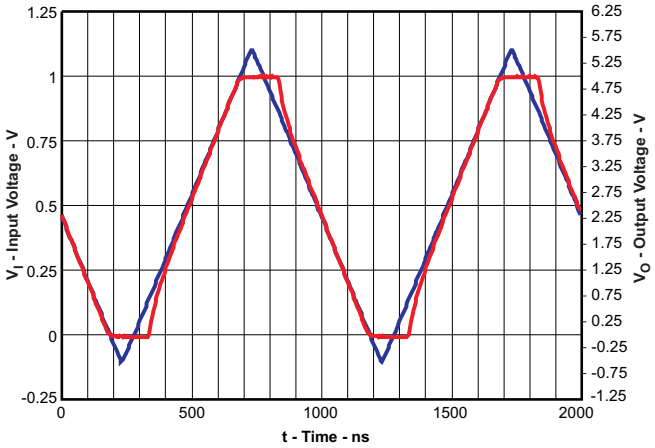


Figure 19.

SLEW RATE vs OUTPUT VOLTAGE STEP

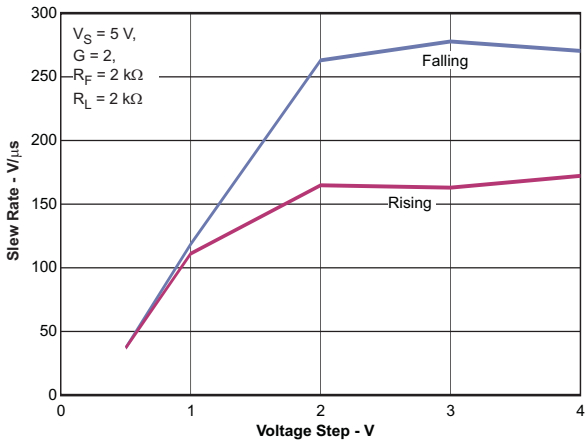


Figure 20.

PRODUCT PREVIEW

TYPICAL PERFORMANCE GRAPHS: V_S = 5 V (continued)

Test conditions unless otherwise noted: V_{S+} = +5V, V_{S-} = 0V, V_{OUT} = 2Vpp, R_F = 0Ω, R_L = 2kΩ, G = 1V/V, Input and Output Referenced to mid-supply unless otherwise noted. T_A = 25°C.

OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

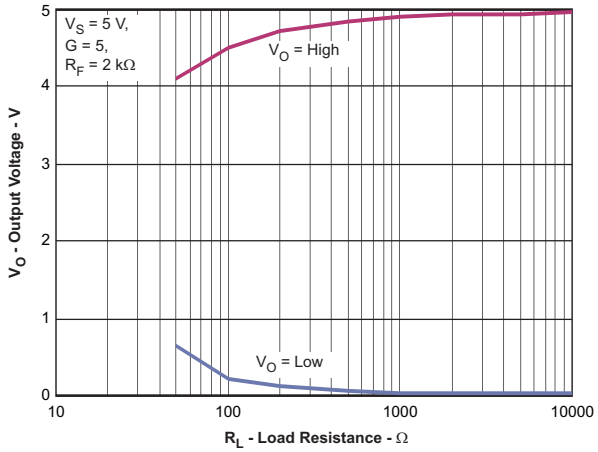


Figure 21.

OUTPUT SATURATION VOLTAGE vs LOAD CURRENT

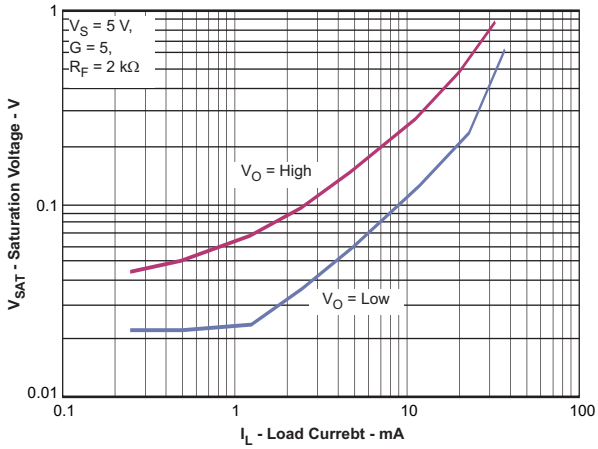


Figure 22.

OUTPUT IMPEDANCE vs FREQUENCY

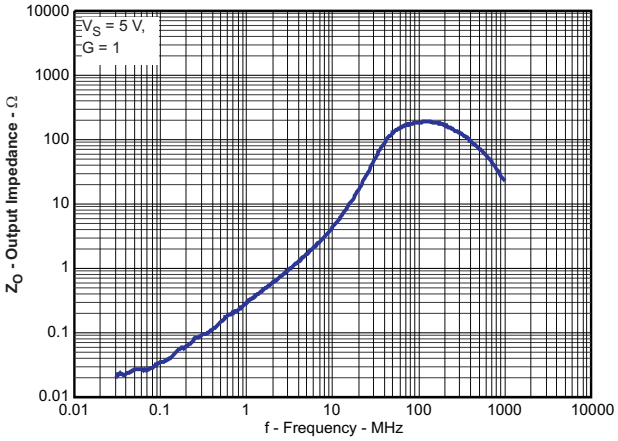


Figure 23.

POWER DOWN RESPONSE

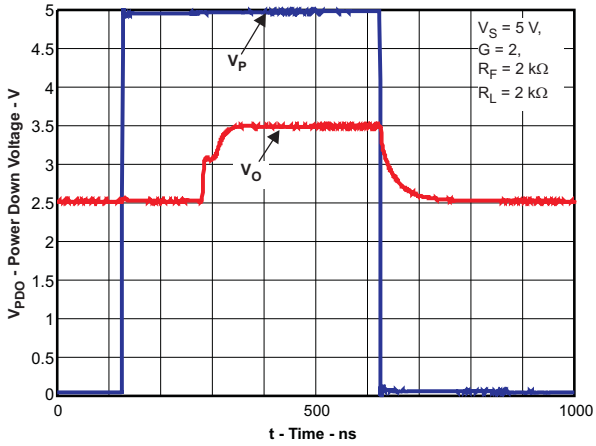


Figure 24.

PRODUCT PREVIEW

APPLICATION INFORMATION

Power down must be driven or tied high or low (maximum resistor value 100k) for proper operation and cannot be left floating.

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