

SMJ320C31, SMJ320LC31, SMQ320LC31 DIGITAL SIGNAL PROCESSORS

SGUS026G – APRIL 1998 – REVISED SEPTEMBER 2006

- Processed to MIL-PRF-38535 (QML)
- Operating Temperature Ranges:
 - Military (M) –55°C to 125°C
 - Special (S) –55°C to 105°C
- SMD Approval
- High-Performance Floating-Point Digital Signal Processor (DSP):
 - SMJ320C31-60 (5 V)
 - 33-ns Instruction Cycle Time
 - 330 Million Operations Per Second (MOPS), 60 Million Floating-Point Operations Per Second (MFLOPS), 30 Million Instructions Per Second (MIPS)
 - SMJ320C31-50 (5 V)
 - 40-ns Instruction Cycle Time
 - 275 MOPS, 50 MFLOPS, 25 MIPS
 - SMJ320C31-40 (5 V)
 - 50-ns Instruction Cycle Time
 - 220 MOPS, 40 MFLOPS, 20 MIPS
 - SMJ320LC31-40 (3.3 V)
 - 50-ns Instruction Cycle Time
 - 220 MOPS, 40 MFLOPS, 20 MIPS
 - SMQ320LC31-40 (3.3 V)
 - 50-ns Instruction Cycle Time
 - 220 MOPS, 40 MFLOPS, 20 MIPS
- 32-Bit High-Performance CPU
- 16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations
- 32-Bit Instruction and Data Words, 24-Bit Addresses
- Two 1K Word × 32-Bit Single-Cycle Dual-Access On-Chip RAM Blocks
- Boot-Program Loader
- 64-Word × 32-Bit Instruction Cache
- Eight Extended-Precision Registers
- Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)
- Two Low-Power Modes
- On-Chip Memory-Mapped Peripherals:
 - One Serial Port Supporting 8-/16-/24-/32-Bit Transfers
 - Two 32-Bit Timers
 - One-Channel Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation
- Fabricated Using Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI)
- Two- and Three-Operand Instructions
- 40/32-Bit Floating-Point/Integer Multiplier and Arithmetic Logic Unit (ALU)
- Parallel ALU and Multiplier Execution in a Single Cycle
- Block-Repeat Capability
- Zero-Overhead Loops With Single-Cycle Branches
- Conditional Calls and Returns
- Interlocked Instructions for Multiprocessing Support
- Bus-Control Registers Configure Strobe-Control Wait-State Generation
- Validated Ada Compiler
- Integer, Floating-Point, and Logical Operations
- 32-Bit Barrel Shifter
- One 32-Bit Data Bus (24-Bit Address)
- Packaging
 - 132-Lead Ceramic Quad Flatpack With Nonconductive Tie-Bar (HFG Suffix)
 - 141-Pin Ceramic Staggered Pin Grid-Array Package (GFA Suffix)
 - 132-Lead TAB Frame
 - 132-Lead Plastic Quad Flatpack (PQ Suffix)

description

The SMJ320C31, SMJ320LC31, and SMQ320LC31 digital signal processors (DSPs) are 32-bit, floating-point processors manufactured in 0.6- μ m triple-level-metal CMOS technology. The devices are part of the SMJ320C3x generation of DSPs from Texas Instruments.



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 **TEXAS
INSTRUMENTS**

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description (continued)

The SMJ320C3x internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 60 MFLOPS. The SMJ320C3x optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.

The SMJ320C3x can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are results of these features.

General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure. The SMJ320C3x supports a wide variety of system applications from host processor to dedicated coprocessor.

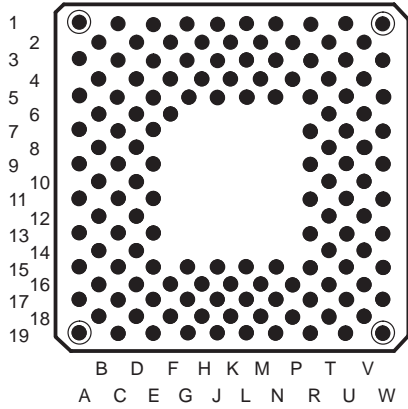
High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

For additional information when designing for cold temperature operation, please see Texas Instruments application report *320C3x, 320C4x and 320MCM42x Power-up Sensitivity at Cold Temperature*, literature number SGUA001.

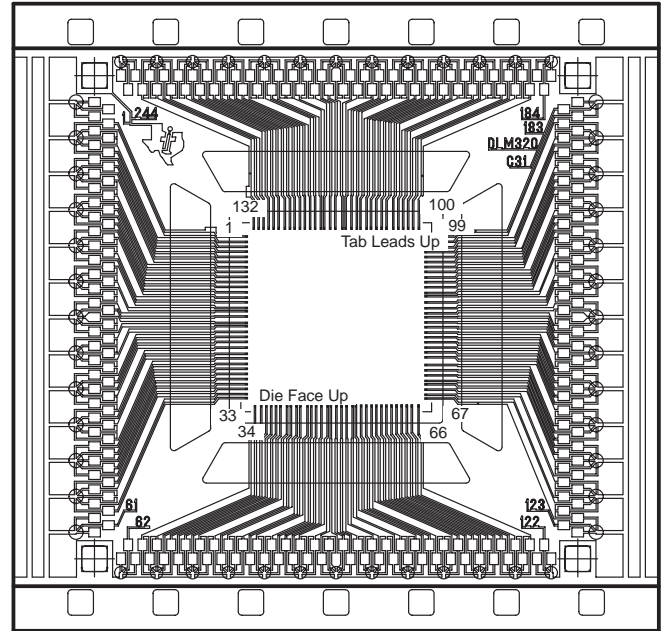
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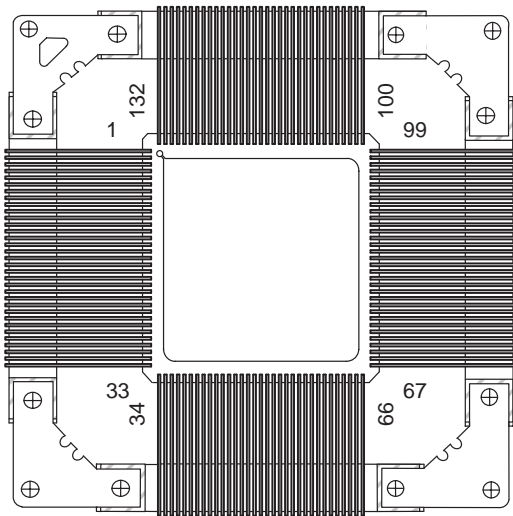
**141-PIN GFA STAGGERED GRID ARRAY
PACKAGE
(BOTTOM VIEW)**



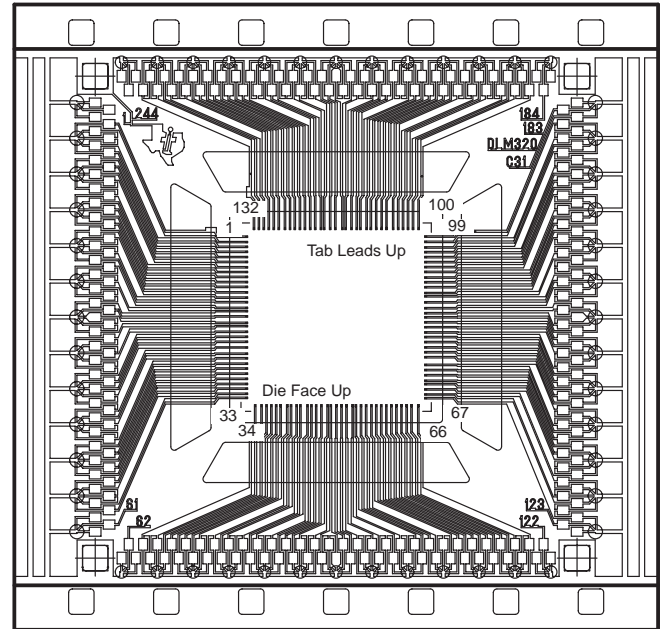
**TA PACKAGE
(TOP VIEW)**



**132-PIN HFG QUAD FLATPACK
(TOP VIEW)**



**TB PACKAGE
(TOP VIEW)**



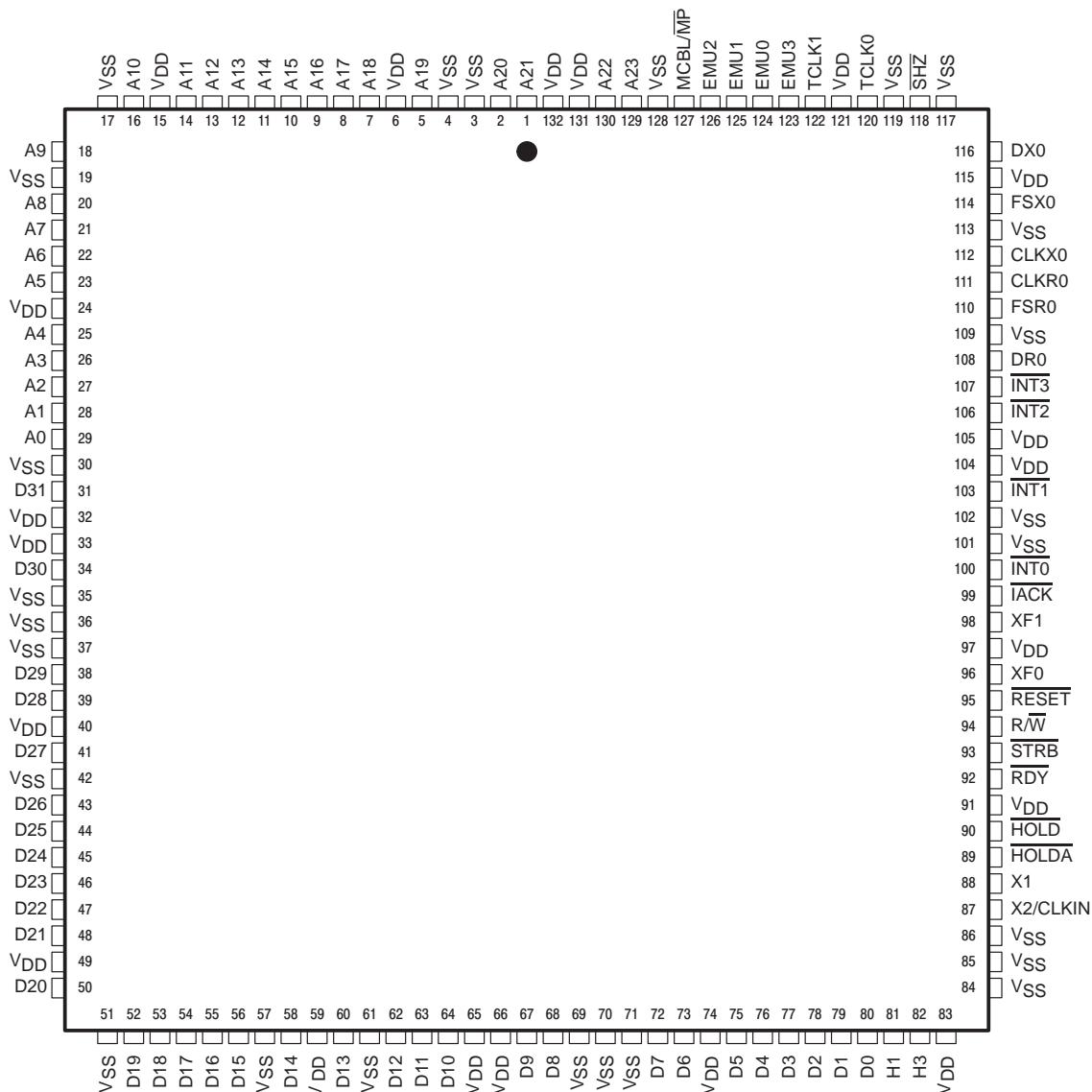
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SMQ320LC31 pinout (top view)

The SMQ320LC31 device is also packaged in a 132-pin plastic quad flatpack (PQ Suffix). The full part numbers are SMQ320LC31PQM40 and 5962-9760601NXB.

PQ PACKAGE (TOP VIEW)



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Terminal Assignments

PIN				PIN			
NUMBER			NAME	NUMBER			NAME
PQ PKG	HFG PKG	GFA PKG		PQ PKG	HFG PKG	GFA PKG	
29	12	L1	A0	64	47	W9	D10
28	11	K2	A1	63	46	U9	D11
27	10	J1	A2	62	45	V8	D12
26	9	J3	A3	60	43	W7	D13
25	8	G1	A4	58	41	U7	D14
23	6	F2	A5	56	39	V6	D15
22	5	E1	A6	55	38	W5	D16
21	4	E3	A7	54	37	U5	D17
20	3	D2	A8	53	36	V4	D18
18	1	C1	A9	52	35	W3	D19
16	131	C3	A10	50	33	U3	D20
14	129	B2	A11	48	31	V2	D21
13	128	A1	A12	47	30	W1	D22
12	127	C5	A13	46	29	R3	D23
11	126	B4	A14	45	28	T2	D24
10	125	A3	A15	44	27	U1	D25
9	124	C7	A16	43	26	N3	D26
8	123	B6	A17	41	24	P2	D27
7	122	C9	A18	39	22	R1	D28
5	120	B8	A19	38	21	L3	D29
2	117	A7	A20	34	17	M2	D30
1	116	A9	A21	31	14	N1	D31
130	113	B10	A22	108	91	C19	DR0
129	112	A11	A23	116	99	C17	DX0
111	94	E17	CLKR0	124	107	B14	EMU0
112	95	A19	CLKX0	125	108	A13	EMU1
80	63	W19	D0	126	109	B12	EMU2
79	62	V16	D1	123	106	A15	EMU3
78	61	W17	D2	110	93	D18	FSR0
77	60	U13	D3	114	97	B18	FSX0
76	59	V14	D4	81	73	P18	HOLD
75	58	W15	D5	82	72	R19	HOLDA
73	56	U11	D6	90	64	V18	H1
72	55	V12	D7	89	65	U17	H3
68	51	W11	D8	99	82	H18	IACK
67	50	V10	D9	100	83	J17	INT0

† CVSS, VSSL, and IVSS are on the same plane.

‡ AVDD, DVDD, CVDD, and PVDD are on the same plane.

§ VSUBS connects to die metallization. Tie this pin to clean ground.

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Terminal Assignments (Continued)

PIN				PIN			
NUMBER			NAME	NUMBER			NAME
PQ PKG	HFG PKG	GFA PKG		PQ PKG	HFG PKG	GFA PKG	
103	86	E19	$\overline{\text{INT1}}$	30	18	P4	VSSL [†]
106	89	F18	$\overline{\text{INT2}}$	35	19	T10	VSSL [†]
107	90	G17	$\overline{\text{INT3}}$	36	20	K4	DVSS
127	110	C11	MCBL/ $\overline{\text{MP}}$	37	25	T4	IVSS [†]
92	77	L19	$\overline{\text{R/W}}$	42	34	G3	DVSS
95	75	N17	$\overline{\text{RDY}}$	51	40	K16	CVSS [†]
94	78	K18	$\overline{\text{RESET}}$	57	44	T8	IVSS [†]
118	101	A17	$\overline{\text{SHZ}}$	61	52	T12	DVSS
93	76	M18	$\overline{\text{STRB}}$	69	53	R11	VSSL [†]
120	103	B16	TCLK0	70	54	J15	VSSL [†]
	105	C15	TCLK1	71	67	W13	DVSS
	121	G5	AVDD [‡]	84	68	D10	CVSS [†]
6	130	E7	AVDD [‡]	85	69	D16	IVSS [†]
15	7	E5	AVDD [‡]	86	84	T16	DVSS
24	15	N5	VDDL	101	85	D12	VSSL [†]
32	16	R5	VDDL	102	92	F16	CVSS [†]
33	23	H4	DVDD [‡]	109	96	H16	IVSS [†]
40	32	J5	DVDD [‡]	113	100	D14	VSUBS [§]
49	42	T14	DVDD [‡]	117	102	U15	DVSS
59	48	R7	VDDL	119	111	C13	CVSS [†]
65	49	R9	VDDL	128	71	T18	X1
66	57	R13	DVDD [‡]	88	70	U19	X2/CLKIN
74	66	R15	DVDD [‡]	87	79	J19	XF0
83	74	P16	CVDD [‡]	96	81	G19	XF1
91	80	N15	CVDD [‡]	98		F6	No Connect
97	87	G15	VDDL			D4	DVSS
104	88	E15	VDDL			N19	DVSS
105	98	L15	PVDD [‡]			R17	DVSS
115	104	E9	PVDD [‡]			L17	DVSS
121	114	E13	VDDL			M16	DVSS
131	115	E11	VDDL			D6	DVSS
132	118	L5	VSSL [†]			A5	DVSS
3	119	H2	DVSS			D8	DVSS
4	132	M4	CVSS [†]				
17	2	F4	DVSS				
19	13	T6	CVSS [†]				

[†] CVSS, VSSL, and IVSS are on the same plane.

[‡] AVDD, DVDD, CVDD, and PVDD are on the same plane.

[§] VSUBS connects to die metallization. Tie this pin to clean ground.

Terminal Functions

TERMINAL NAME	QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡
PRIMARY-BUS INTERFACE				
D31–D0	32	I/O/Z	32-bit data port	S H R
A23–A0	24	O/Z	24-bit address port	S H R
R/ \overline{W}	1	O/Z	Read/write. $\overline{R/W}$ is high when a read is performed and low when a write is performed over the parallel interface.	S H R
\overline{STRB}	1	O/Z	External-access strobe	S H
\overline{RDY}	1	I	Ready. \overline{RDY} indicates that the external device is prepared for a transaction completion.	
\overline{HOLD}	1	I	Hold. When \overline{HOLD} is a logic low, any ongoing transaction is completed. A23–A0, D31–D0, \overline{STRB} , and R/ \overline{W} are placed in the high-impedance state and all transactions over the primary-bus interface are held until \overline{HOLD} becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set.	
\overline{HOLDA}	1	O/Z	Hold acknowledge. \overline{HOLDA} is generated in response to a logic low on \overline{HOLD} . \overline{HOLDA} indicates that A23–A0, D31–D0, \overline{STRB} , and R/ \overline{W} are in the high-impedance state and that all transactions over the bus are held. \overline{HOLDA} is high in response to a logic high of \overline{HOLD} or the NOHOLD bit of the primary-bus-control register is set.	S
CONTROL SIGNALS				
\overline{RESET}	1	I	Reset. When \overline{RESET} is a logic low, the device is in the reset condition. When \overline{RESET} becomes a logic high, execution begins from the location specified by the reset vector.	
$\overline{INT3}$ – $\overline{INT0}$	4	I	External interrupts	
\overline{IACK}	1	O/Z	Interrupt acknowledge. \overline{IACK} is generated by the IACK instruction. \overline{IACK} can be used to indicate the beginning or the end of an interrupt-service routine.	S
MCBL/ \overline{MP}	1	I	Microcomputer boot-loader/microprocessor mode-select	
\overline{SHZ}	1	I	Shutdown high impedance. When active, \overline{SHZ} shuts down the device and places all pins in the high-impedance state. \overline{SHZ} is used for board-level testing to ensure that no dual-drive conditions occur. CAUTION: A low on \overline{SHZ} corrupts the device memory and register contents. Reset the device with \overline{SHZ} high to restore it to a known operating condition.	
XF1, XF0	2	I/O/Z	External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction.	S R
SERIAL PORT 0 SIGNALS				
CLKR0	1	I/O/Z	Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver.	S R
CLKX0	1	I/O/Z	Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter.	S R
DR0	1	I/O/Z	Data-receive. Serial port 0 receives serial data on DR0.	S R
DX0	1	I/O/Z	Data-transmit output. Serial port 0 transmits serial data on DX0.	S R
FSR0	1	I/O/Z	Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0.	S R
FSX0	1	I/O/Z	Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0.	S R
TIMER SIGNALS				
TCLK0	1	I/O/Z	Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0.	S
TCLK1	1	I/O/Z	Timer clock 1. As an input, TCLK0 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1.	S

† I = input, O = output, Z = high-impedance state

‡ S = \overline{SHZ} active, H = \overline{HOLD} active, R = \overline{RESET} active

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Terminal Functions (Continued)

TERMINAL NAME	QTY	TYPE†	DESCRIPTION	CONDITIONS WHEN SIGNAL IS Z TYPE‡
SUPPLY AND OSCILLATOR SIGNALS				
H1	1	O/Z	External H1 clock. H1 has a period equal to twice CLKIN.	S
H3	1	O/Z	External H3 clock. H3 has a period equal to twice CLKIN.	S
V _{DD}	20	I	5-V supply for 'C31 devices and 3.3-V supply for 'LC31 devices. All must be connected to a common supply plane.§	
V _{SS}	25	I	Ground. All grounds must be connected to a common ground plane.	
X1	1	O	Output from the internal-crystal oscillator. If a crystal is not used, X1 should be left unconnected.	
X2/CLKIN	1	I	Internal-oscillator input from a crystal or a clock	
RESERVED¶				
EMU2-EMU0	3	I	Reserved for emulation. Use pullup resistors to V _{DD}	
EMU3	1	O/Z	Reserved for emulation	S

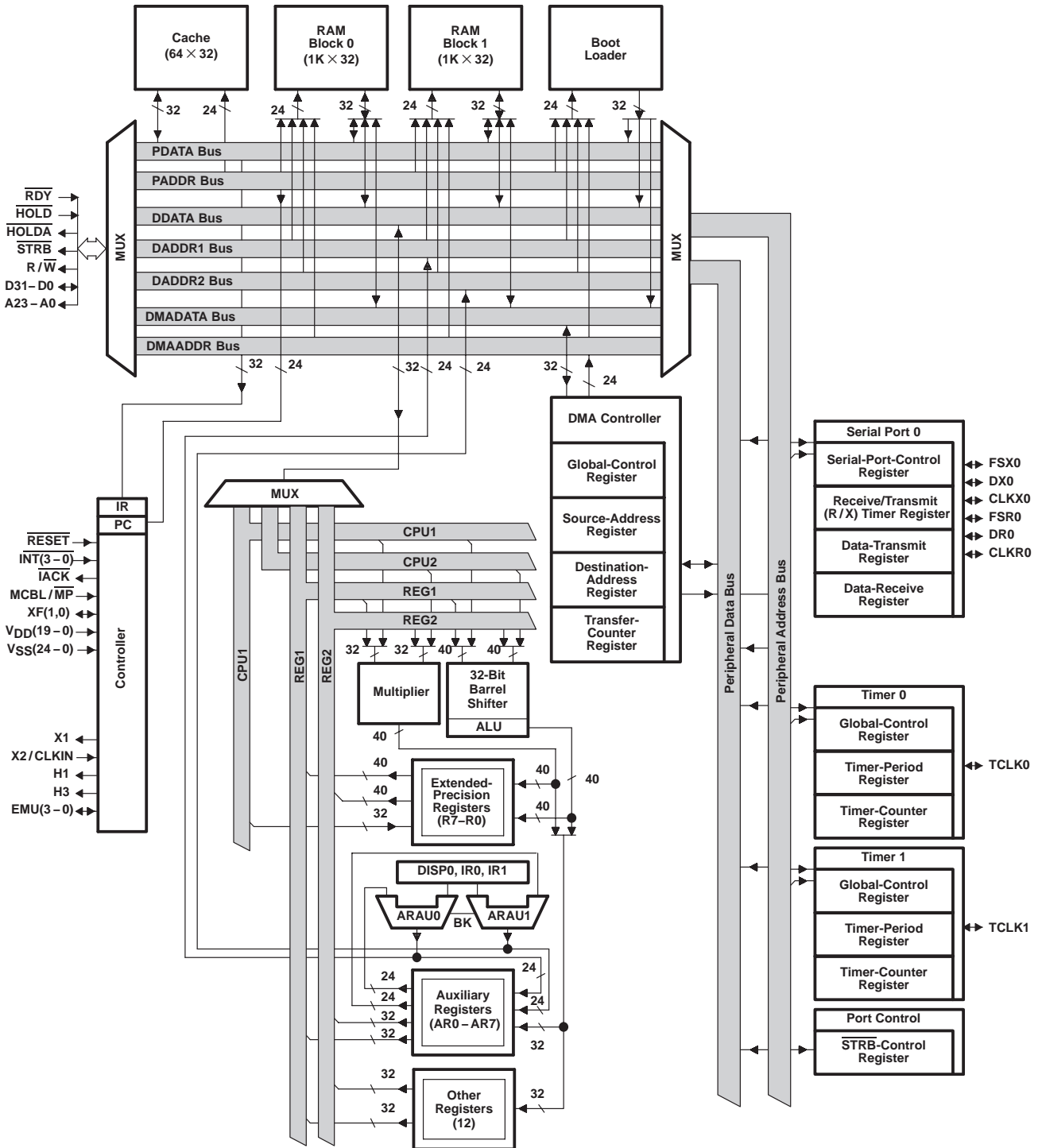
† I = input, O = output, Z = high-impedance state

‡ S = SHZ active, H = HOLD active, R = RESET active

§ Recommended decoupling capacitor value is 0.1 μF.

¶ Follow the connections specified for the reserved pins. Use 18-kΩ – 22-kΩ pullup resistors for best results. All V_{DD} supply pins must be connected to a common supply plane, and all ground pins must be connected to a common ground plane.

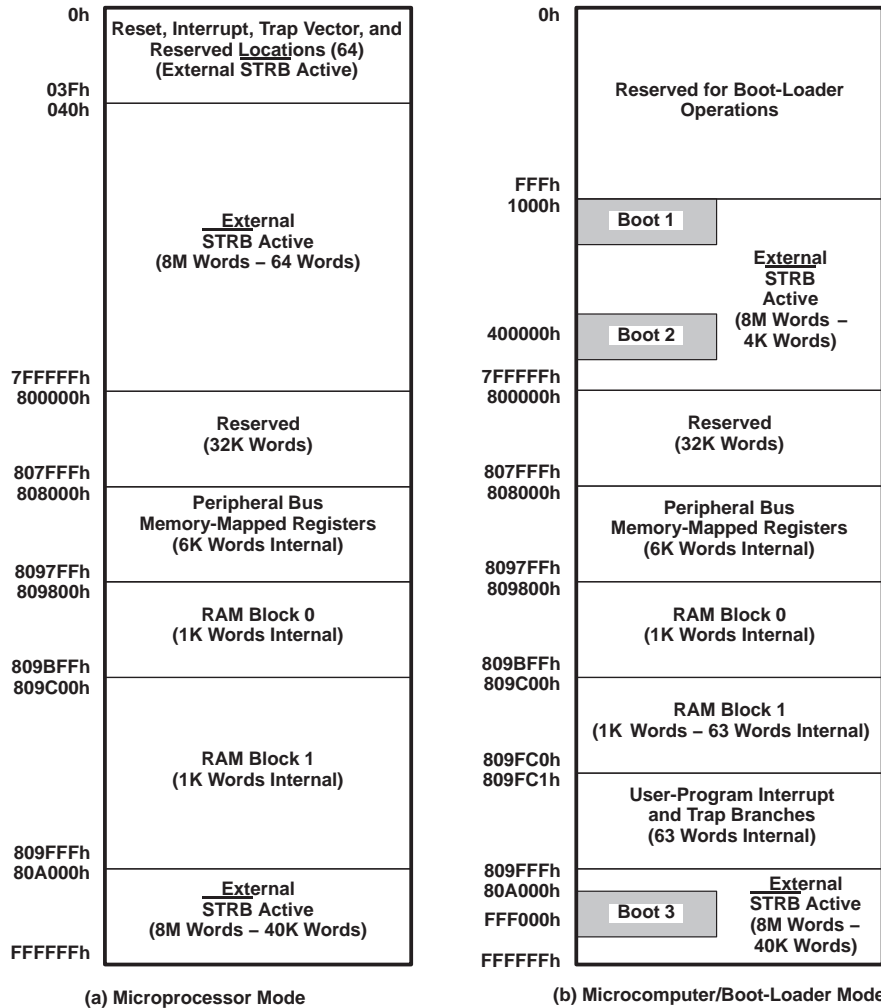
functional block diagram



SMJ320C31, SMJ320LC31, SMQ320LC31 DIGITAL SIGNAL PROCESSORS

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memory map†



† Figure 1 depicts the memory map for the SMJ320C31. See the *TMS320C3x Users Guide* (literature number SPRU031) for a detailed description of this memory mapping.

Figure 1. SMJ320C31 Memory Map

memory map (continued)

00h	Reset
01h	INT0
02h	INT1
03h	INT2
04h	INT3
05h	XINT0
06h	RINT0
07h	Reserved
08h	
09h	TINT0
0Ah	TINT1
0Bh	DINT
0Ch	Reserved
1Fh	
20h	TRAP 0
	•
	•
	•
3Bh	TRAP 27
3Ch	Reserved
3Fh	

(a) Microprocessor Mode

809FC1h	INT0
809FC2h	INT1
809FC3h	INT2
809FC4h	INT3
809FC5h	XINT0
809FC6h	RINT0
809FC7h	Reserved
809FC8h	
809FC9h	TINT0
809FCAh	TINT1
809FCBh	DINT
809FCCh	Reserved
809FDFh	
809FE0h	TRAP 0
	•
	•
	•
809FFBh	TRAP 27
809FFCh	Reserved
809FFFh	

(b) Microcomputer/Boot-Loader Mode

Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

SMJ320C31, SMJ320LC31, SMQ320LC31 DIGITAL SIGNAL PROCESSORS

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memory map (continued)

808000h	DMA Global Control
808004h	DMA Source Address
808006h	DMA Destination Address
808008h	DMA Transfer Counter
808020h	Timer 0 Global Control
808024h	Timer 0 Counter
808028h	Timer 0 Period Register
808030h	Timer 1 Global Control
808034h	Timer 1 Counter
808038h	Timer 1 Period Register
808040h	Serial Global Control
808042h	FSX/DX/CLKX Serial Port Control
808043h	FSR/DR/CLKR Serial Port Control
808044h	Serial R/X Timer Control
808045h	Serial R/X Timer Counter
808046h	Serial R/X Timer Period Register
808048h	Data-Transmit
80804Ch	Data-Receive
808064h	Primary-Bus Control

†Shading denotes reserved address locations

Figure 3. Peripheral Bus Memory-Mapped Registers†

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absolute maximum ratings over specified temperature range (unless otherwise noted)†

	'C31	'LC31
Supply voltage, V_{DD} (see Note 1)	–0.3 V to 7 V	–0.3 V to 5 V
Input voltage, V_I	–0.3 V to 7 V	–0.3 V to 5 V
Output voltage, V_O	–0.3 V to 7 V	–0.3 V to 5 V
Continuous power dissipation (worst case) (see Note 2)	1.7 W (for SMJ320C31-33)	850 mW (for SMJ320LC31-33)
Operating case temperature, T_C	–55°C to 125°C	–55°C to 125°C
Storage temperature, T_{stg}	–65°C to 150°C	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS} .

2. Actual operating power is less. This value was obtained under specially produced worst-case test conditions for the TMS320C31-33 and the TMS320LC31-33, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and extension buses at the maximum rate possible. See normal (I_{CC}) current specification in the electrical characteristics table and also read *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

recommended operating conditions (see Note 3)

		'C31			'LC31			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{DD}	Supply voltage (DV_{DD} , etc.)	4.75	5	5.25	3.13	3.3	3.47	V
V_{SS}	Supply voltage (CV_{SS} , etc.)	0			0			V
V_{IH}	High-level input voltage (except \overline{RESET})	2.1	$V_{DD} + 0.3^*$		1.8	$V_{DD} + 0.3^*$		V
	High-level input voltage (\overline{RESET})	2.2	$V_{DD} + 0.3^*$		2.2	$V_{DD} + 0.3^*$		V
V_{IL}	Low-level input voltage	–0.3*	0.8		–0.3*	0.6		V
I_{OH}	High-level output current	–300			–300			μA
I_{OL}	Low-level output current	2			2			mA
T_C	Operating case temperature	'320C31-40	–55	125	–55	125		°C
		'320C31-50	–55	125				
		'320C31-60	–55	105				
		'320LC31-40						
V_{TH}	High-level input voltage for CLKIN	3.0	$V_{DD} + 0.3^*$		2.5	$V_{DD} + 0.3^*$		V

* This parameter is not production tested.

NOTE 3: All voltage values are with respect to V_{SS} . All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.

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electrical characteristics over recommended ranges of supply voltage (unless otherwise noted)
(see Note 3)†

PARAMETER	TEST CONDITIONS	'C31			'LC31			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V _{OH} High-level output voltage	V _{DD} = MIN, I _{OH} = MAX	2.4	3		2			V
V _{OL} Low-level output voltage	V _{DD} = MIN, I _{OH} = MAX		0.3	0.6			0.4	V
I _Z High-impedance current	V _{DD} = MAX	- 20		+ 20	- 20		+ 20	μA
I _I Input current	V _I = V _{SS} to V _{DD}	- 10		+ 10	- 10		+ 10	μA
I _{IP} Input current (with internal pullup)	Inputs with internal pullups§	- 600		20	- 600		10	μA
I _{CC} Supply current¶#	T _A = 25°C, V _{DD} = MAX	f _x = 40 MHz	'C31-40 'LC31-40	160	400	150	300	mA
		f _x = 50 MHz	'C31-50	200	425			
		f _x = 60 MHz	'C31-60	225	475			
I _{DD} Supply current	Standby, IDLE2 Clocks shut off			50		20		μA
C _i Input capacitance	All inputs except CLKIN			15*		15*		pF
	CLKIN			25		25		
C _O Output capacitance				20*		20*		pF

† All input and output voltage levels are TTL compatible.

‡ For 'C31, all typical values are at V_{DD} = 5 V, T_A = 25°C. For 'LC31, all typical values are at V_{DD} = 3.3 V, T_A = 25°C.

§ Pins with internal pullup devices: INT3–INT0, MCBL/MP.

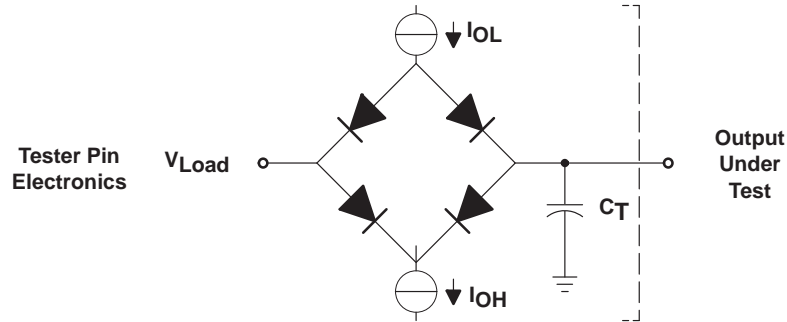
¶ Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to both primary and expansion buses at the maximum rate possible. See *Calculation of TMS320C30 Power Dissipation Application Report* (literature number SPRA020).

f_x is the input clock frequency.

* This parameter is not production tested.

NOTE 3: All voltage values are with respect to V_{SS}. All input and output voltage levels are TTL-compatible. CLKIN can be driven by a CMOS clock.

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Where: I_{OL} = 2 mA (all outputs)
 I_{OH} = 300 μ A (all outputs)
 V_{LOAD} = Selected to emulate 50- Ω termination (typical value = 1.54 V).
 C_T = 80-pF typical load-circuit capacitance

Figure 4. SMJ320C31 Test Load Circuit

signal transition levels for 'C31 (see Figure 5 and Figure 6)

TTL-level outputs are driven to a minimum logic-high level of 2.4 V and to a maximum logic-low level of 0.6 V. Output transition times are specified as follows:

- For a high-to-low transition on a TTL-compatible output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

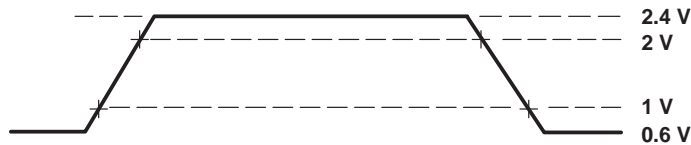


Figure 5. TTL-Level Outputs

Transition times for TTL-compatible inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 2.1 V and the level at which the input is said to be low is 0.8 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.8 V and the level at which the input is said to be high is 2.1 V.

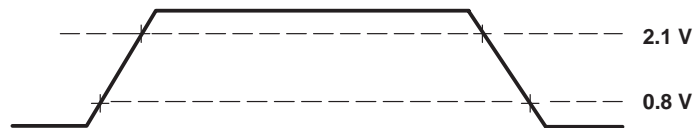
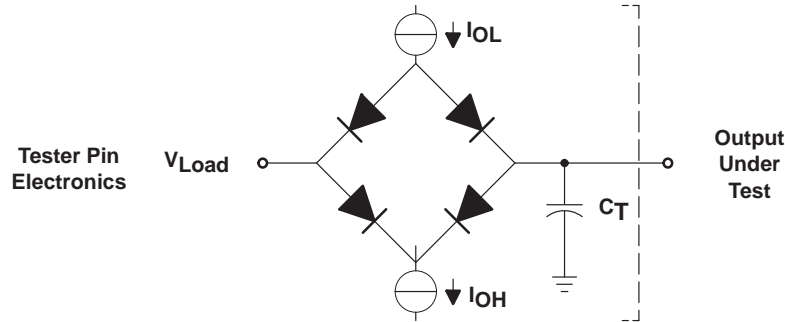


Figure 6. TTL-Level Inputs

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Where: I_{OL} = 2 mA (all outputs)
 I_{OH} = 300 μ A (all outputs)
 V_{LOAD} = 2.15 V
 C_T = 80-pF typical load-circuit capacitance

Figure 7. SMJ320LC31 Test Load Circuit

signal transition levels for 'LC31 (see Figure 8 and Figure 9)

Outputs are driven to a minimum logic-high level of 2 V and to a maximum logic-low level of 0.4 V. Output transition times are specified as follows:

- For a high-to-low transition on an output signal, the level at which the output is said to be no longer high is 2 V and the level at which the output is said to be low is 1 V.
- For a low-to-high transition, the level at which the output is said to be no longer low is 1 V and the level at which the output is said to be high is 2 V.

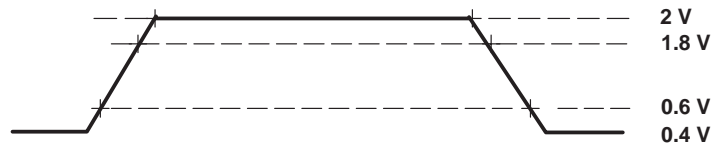


Figure 8. 'LC31 Output Levels

Transition times for inputs are specified as follows:

- For a high-to-low transition on an input signal, the level at which the input is said to be no longer high is 1.8 V and the level at which the input is said to be low is 0.6 V.
- For a low-to-high transition on an input signal, the level at which the input is said to be no longer low is 0.6 V and the level at which the input is said to be high is 1.8 V.

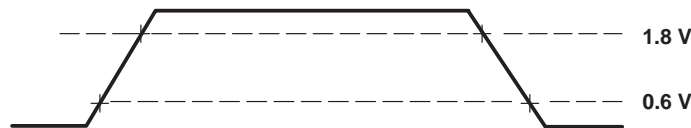


Figure 9. 'LC31 Input Levels

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100-A. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

A	A23–A0	H	H1 and H3
ASYNCH	Asynchronous reset signals	HOLD	$\overline{\text{HOLD}}$
C	CLKX0	HOLDA	$\overline{\text{HOLDA}}$
CI	CLKIN	IACK	$\overline{\text{IACK}}$
CLKR	CLKR0	INT	$\overline{\text{INT3}}-\overline{\text{INT0}}$
CONTROL	Control signals	RDY	$\overline{\text{RDY}}$
D	D31–D0	RW	$\overline{\text{R/W}}$
DR	DR	RESET	$\overline{\text{RESET}}$
DX	DX	S	$\overline{\text{STRB}}$
FS	FSX/R	SCK	CLKX/R
FSX	FSX0	SHZ	$\overline{\text{SHZ}}$
FSR	FSR0	TCLK	TCLK0, TCLK1, or TCLKx
GPI	General-purpose input	XF	XF0, XF1, or XFx
GPIO	General-purpose input/output; peripheral pin	XFIO	XFx switching from input to output
GPO	General-purpose output		

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timing

Timing specifications apply to the SMJ320C31 and SMJ320LC31.

X2/CLKIN, H1, and H3 timing

The following table defines the timing parameters for the X2/CLKIN, H1, and H3 interface signals.

timing parameters for X2/CLKIN, H1, H3 (see Figure 10, Figure 11, Figure 12, and Figure 13)

NO.			'C31-40 'LC31-40		'C31-50		'C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
1	$t_f(\text{Cl})$	Fall time, CLKIN		5*		5*		4*	ns
2	$t_w(\text{ClL})$	Pulse duration, CLKIN low $t_c(\text{Cl}) = \text{min}$	9		7		6		ns
3	$t_w(\text{ClH})$	Pulse duration, CLKIN high $t_c(\text{Cl}) = \text{min}$	9		7		6		ns
4	$t_r(\text{Cl})$	Rise time, CLKIN		5*		5*		4*	ns
5	$t_c(\text{Cl})$	Cycle time, CLKIN	25	303	20	303	16.67	303	ns
6	$t_f(\text{H})$	Fall time, H1 and H3		3		3		3	ns
7	$t_w(\text{HL})$	Pulse duration, H1 and H3 low	P-5†		P-5†		P-4†		ns
8	$t_w(\text{HH})$	Pulse duration, H1 and H3 high	P-6†		P-6†		P-5†		ns
9	$t_r(\text{H})$	Rise time, H1 and H3		3		3		3	ns
10	$t_d(\text{HL-HH})$	Delay time. from H1 low to H3 high or from H3 low to H1 high	0	4	0	4	0	4	ns
11	$t_c(\text{H})$	Cycle time, H1 and H3	50	606	40	606	33.3	606	ns

† P = $t_c(\text{Cl})$

* This parameter is not production tested.

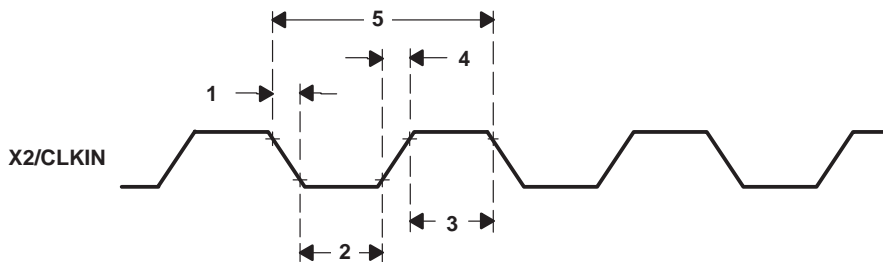


Figure 10. Timing for X2/CLKIN

X2/CLKIN, H1, and H3 timing (continued)

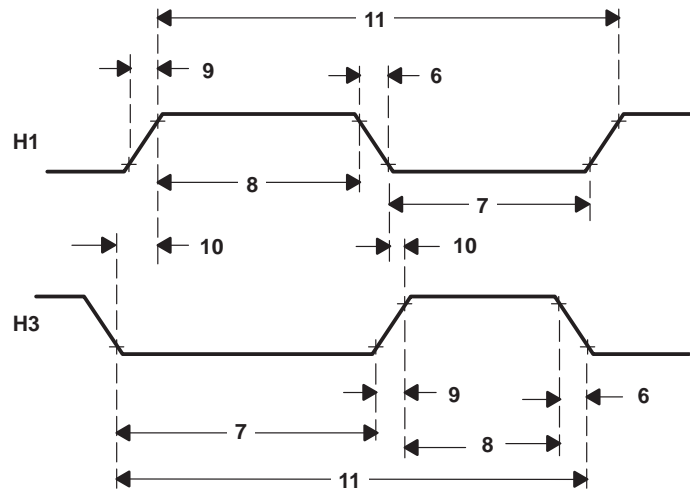


Figure 11. Timing for H1 and H3

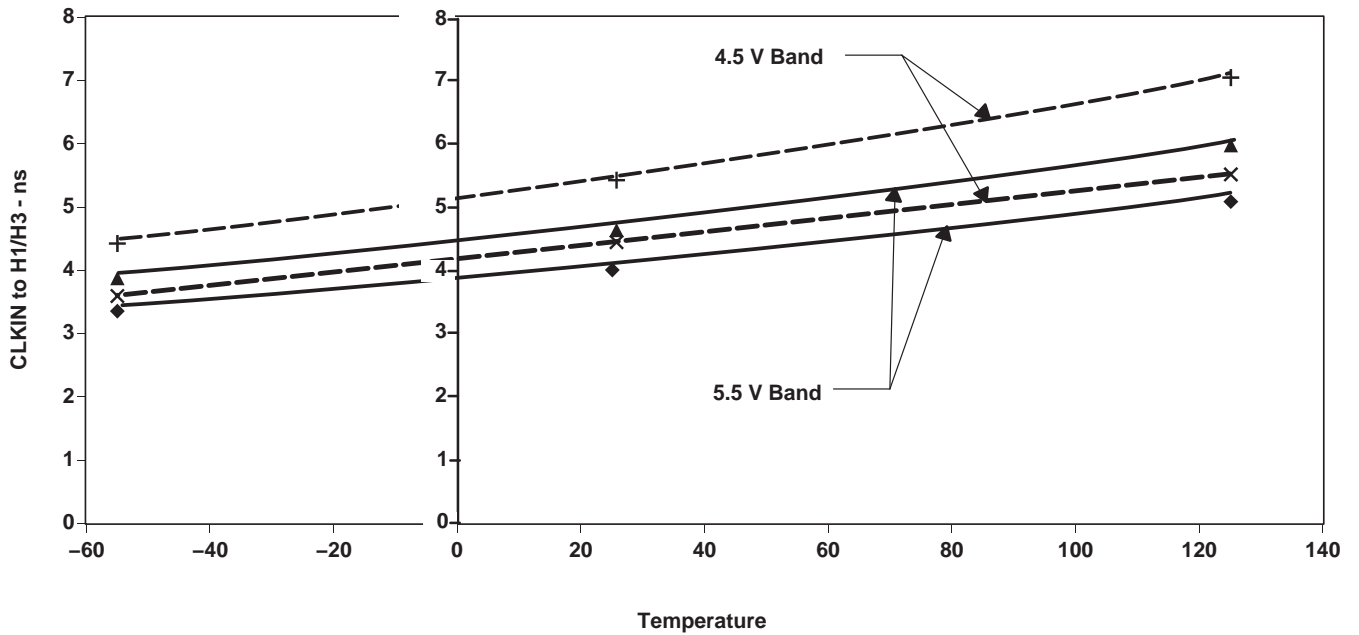


Figure 12. SMJ320C31 CLKIN to H1/H3 as a Function of Temperature (Typical)

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X2/CLKIN, H1, and H3 timing (continued)

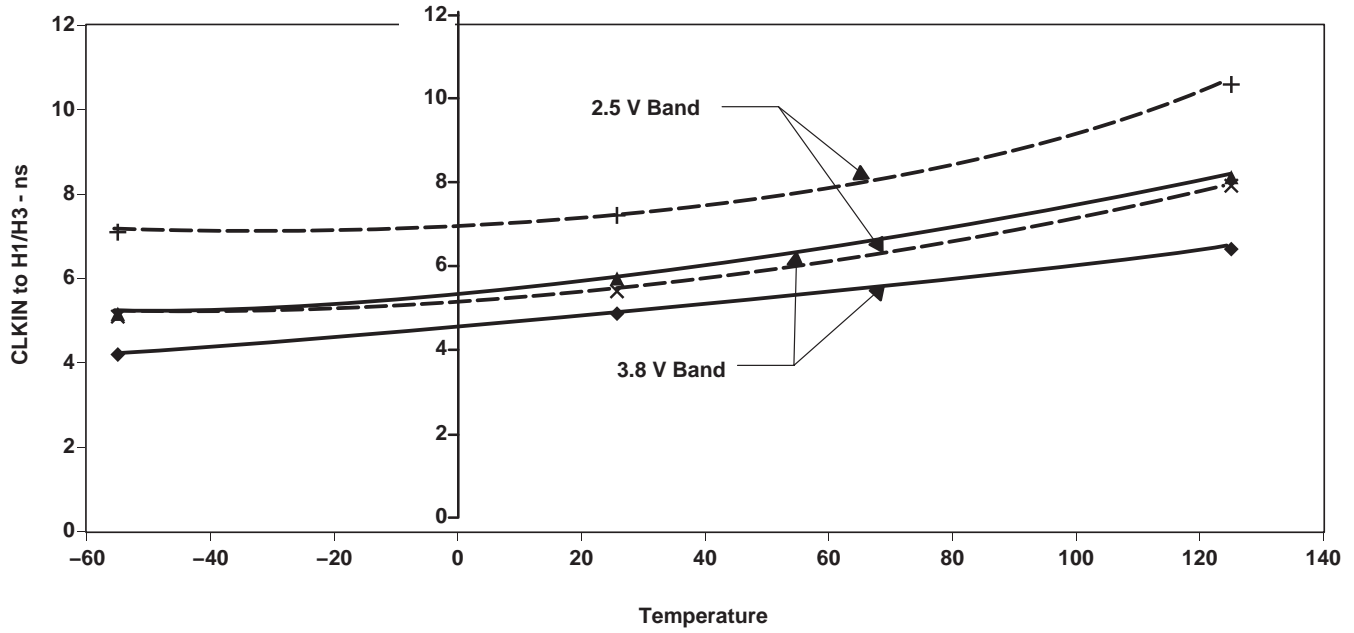


Figure 13. SMJ320LC31 CLKIN to H1/H3 as a Function of Temperature (Typical)

memory read/write timing

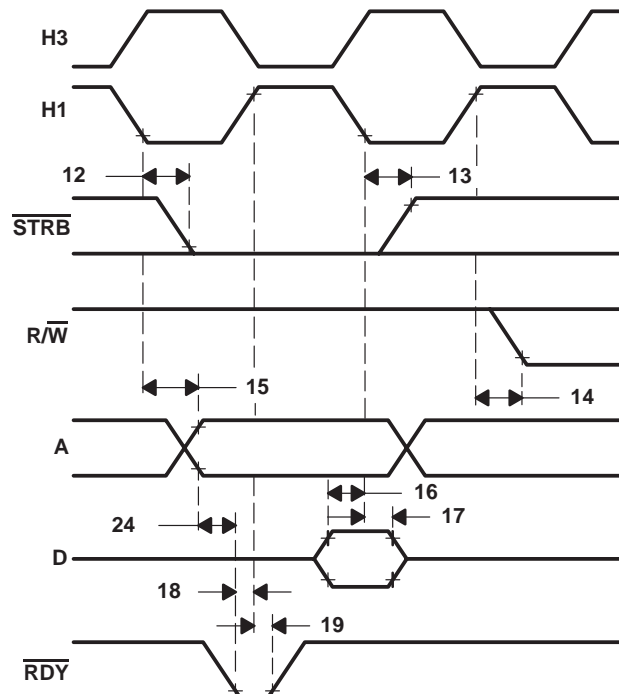
The following table defines memory read/write timing parameters for $\overline{\text{STRB}}$.

timing parameters for memory ($\overline{\text{STRB}} = 0$) read/write (see Figure 14 and Figure 15)†

NO.			'C31-40 'LC31-40		'C31-50		'C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
12	$t_{d(H1L-SL)}$	Delay time, H1 low to $\overline{\text{STRB}}$ low	0*	6	0*	5	0*	5	ns
13	$t_{d(H1L-SH)}$	Delay time, H1 low to $\overline{\text{STRB}}$ high	0*	6	0*	5	0*	5	ns
14	$t_{d(H1H-RWL)R}$	Delay time, H1 high to R/W low (read)	0*	9	0*	7	0*	6	ns
15	$t_{d(H1L-A)}$	Delay time, H1 low to A valid	0*	10	0*	10	0*	8	ns
16	$t_{su(D-H1L)R}$	Setup time, D before H1 low (read)	14		10		9		ns
17	$t_h(H1L-D)R$	Hold time, D after H1 low (read)	0		0		0		ns
18	$t_{su}(\overline{\text{RDY}}-H1H)$	Setup time, $\overline{\text{RDY}}$ before H1 high	8		6		5		ns
19	$t_h(H1H-\overline{\text{RDY}})$	Hold time, $\overline{\text{RDY}}$ after H1 high	0		0		0		ns
20	$t_{d(H1H-RWH)W}$	Delay time, H1 high to R/W high (write)		9		7		6	ns
21	$t_v(H1L-D)W$	Valid time, D after H1 low (write)		17		14		12	ns
22	$t_h(H1H-D)W$	Hold time, D after H1 high (write)	0		0		0		ns
23	$t_{d(H1H-A)W}$	Delay time, H1 high to A valid on back-to-back write cycles (write)		15		14		10	ns
24	$t_{d(A-\overline{\text{RDY}})$	Delay time, $\overline{\text{RDY}}$ from A valid		7*		6*		6*	ns

† See Figure 16 for address bus timing variation with load capacitance greater than typical load-circuit capacitance ($C_T = 80$ pF).

* This parameter is not production tested.



NOTE A: $\overline{\text{STRB}}$ remains low during back-to-back read operations.

Figure 14. Timing for Memory ($\overline{\text{STRB}} = 0$) Read

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memory read/write timing (continued)

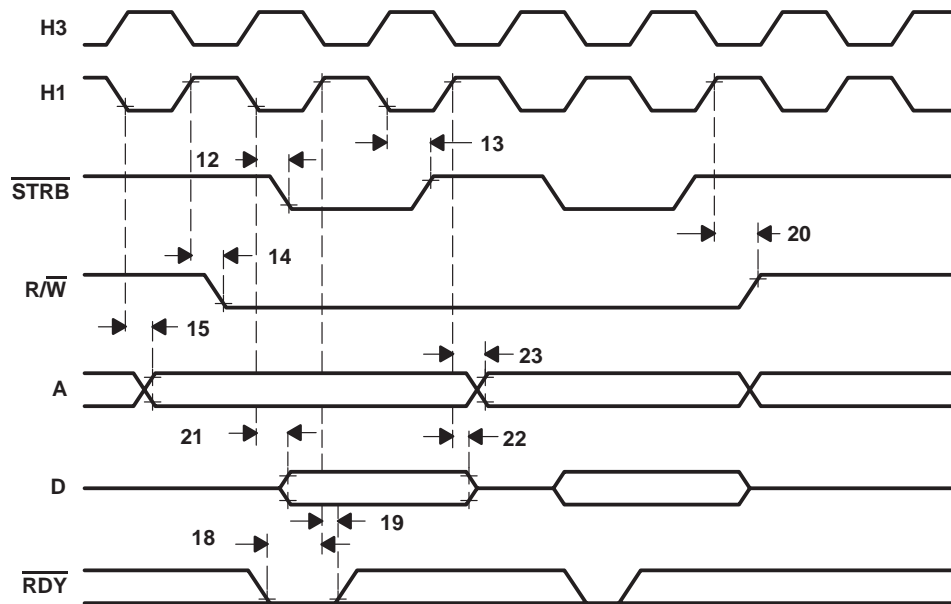
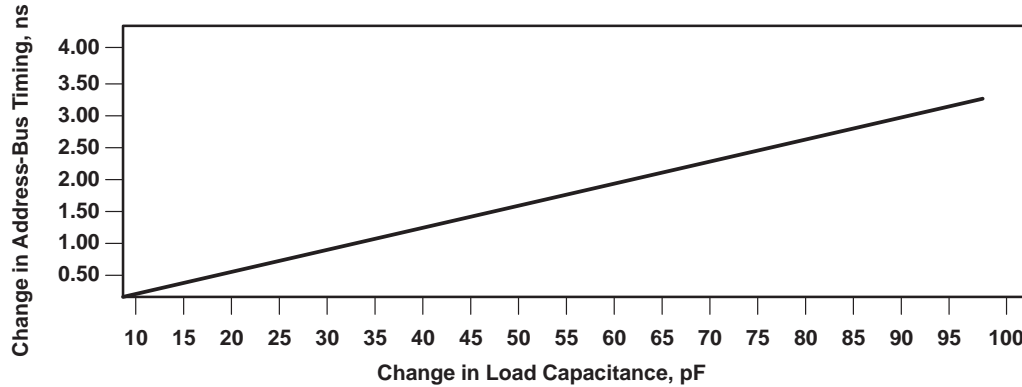


Figure 15. Timing for Memory ($\overline{\text{STRB}} = 0$) Write

Address-Bus Timing Variation Load Capacitance



NOTE A: 30 pF/ns slope

Figure 16. Address-Bus Timing Variation With Load Capacitance (see Note A)

XF0 and XF1 timing when executing LDFI or LDII

The following table defines the timing parameters for XF0 and XF1 during execution of LDFI or LDII.

timing for XF0 and XF1 when executing LDFI or LDII for SMJ320C31 (see Figure 17)

NO.			'C31-40		'LC31-40		'C31-50		'C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
25	$t_{d(H3H-XF0L)}$	Delay time, H3 high to XF0 low		13		13		12		11	ns
26	$t_{su(XF1-H1L)}$	Setup time, XF1 before H1 low	9		10		8		8		ns
27	$t_h(H1L-XF1)$	Hold time, XF1 after H1 low	0		0		0		0		ns

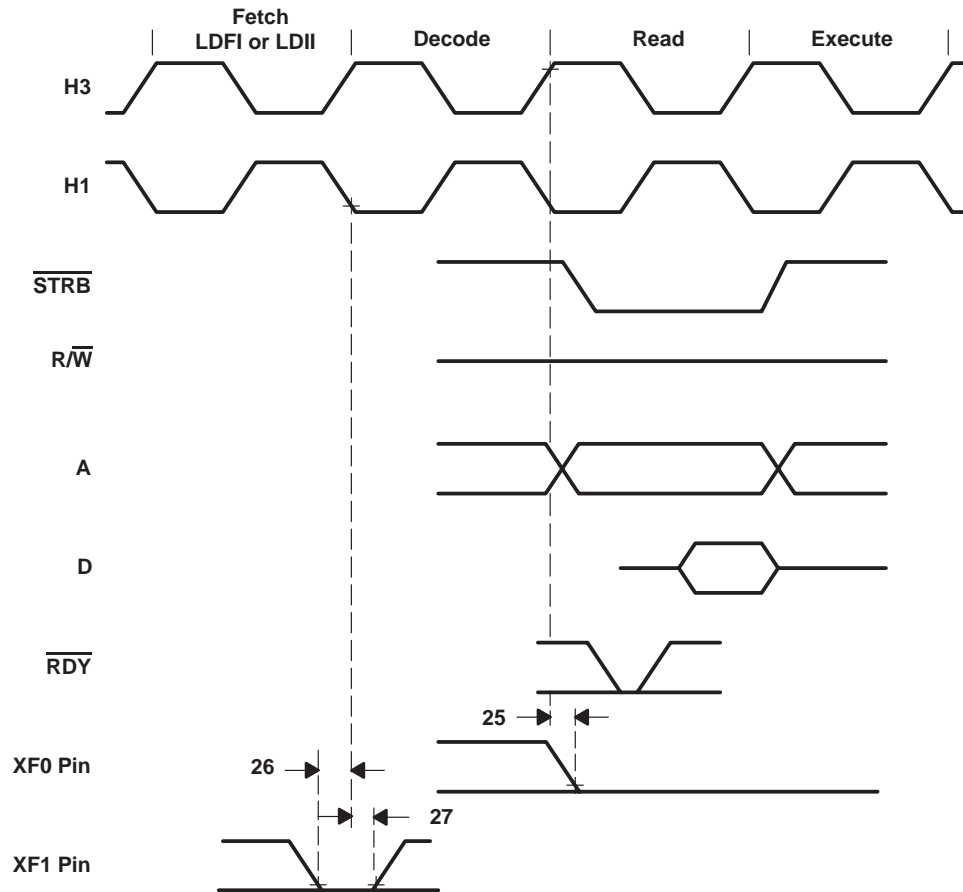


Figure 17. Timing for XF0 and XF1 When Executing LDFI or LDII

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XF0 timing when executing STFI and STII†

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII.

timing for XF0 when executing STFI or STII (see Figure 18)

NO.		'C31-40 'LC31-40	'C31-50	'C31-60	UNIT
		MIN MAX	MIN MAX	MIN MAX	
28	$t_d(H3H-XF0H)$ Delay time, H3 high to XF0 high	13	12	11	ns

† XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

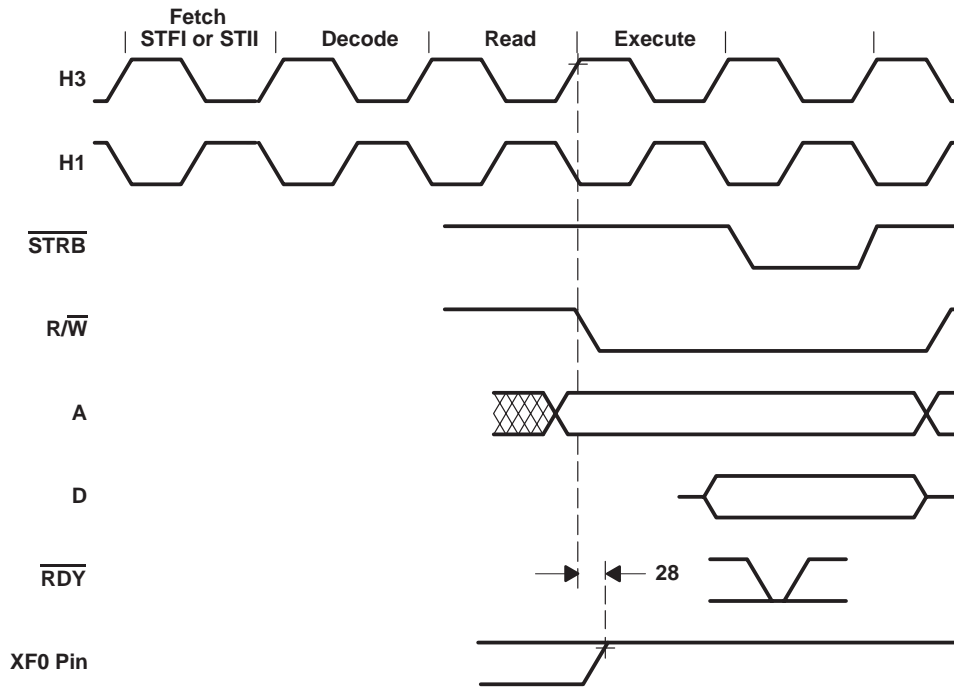


Figure 18. Timing for XF0 When Executing an STFI or STII

XF0 and XF1 timing when executing SIGI

The following table defines the timing parameters for the XF0 and XF1 pins during execution of SIGI.

timing for XF0 and XF1 when executing SIGI for SMJ320C31 (see Figure 19)

NO.		'C31-40		'LC31-40		'C31-50		'C31-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
29	$t_{d(H3H-XF0L)}$ Delay time, H3 high to XF0 low		13		13		12		11	ns
30	$t_{d(H3H-XF0H)}$ Delay time, H3 high to XF0 high		13		13		12		11	ns
31	$t_{su}(XF1-H1L)$ Setup time, XF1 before H1 low	9		10		8		8		ns
32	$t_h(H1L-XF1)$ Hold time, XF1 after H1 low	0		0		0		0		ns

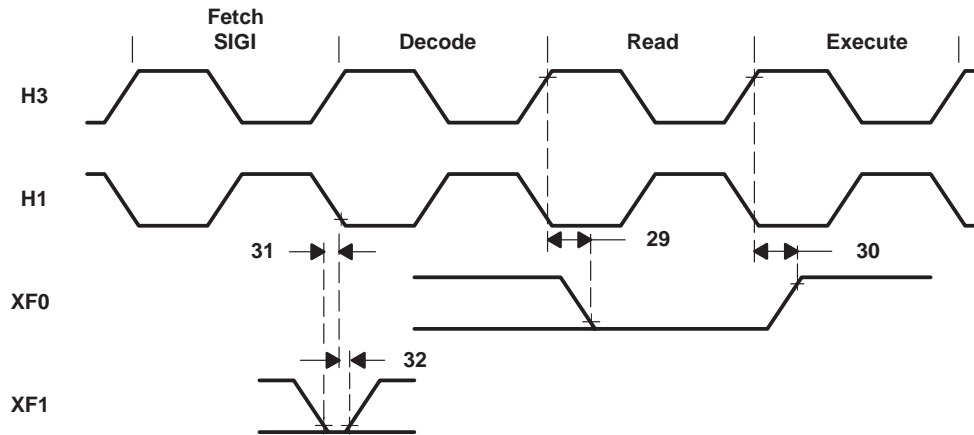


Figure 19. Timing for XF0 and XF1 When Executing SIGI

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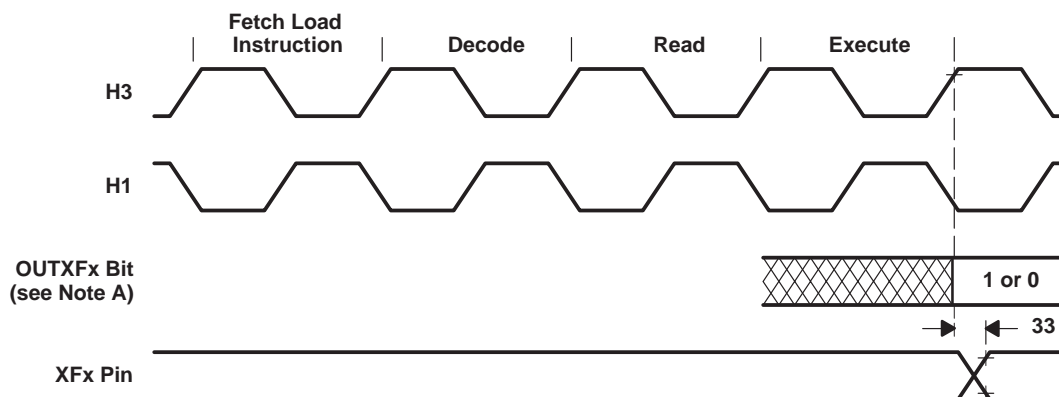
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loading when XF is configured as an output

The following table defines the timing parameter for loading the XF register when the XFx pin is configured as an output.

timing for loading the XF register when configured as an output pin (see Figure 20)

NO.		'C31-40 'LC31-40	'C31-50	'C31-60	UNIT
		MIN MAX	MIN MAX	MIN MAX	
33	$t_{v(H3H-XF)}$ Valid time, H3 high to XFx	13	12	11	ns



NOTE A: OUTXFx represents either bit 2 or 6 of the IOF register.

Figure 20. Timing for Loading XF Register When Configured as an Output Pin

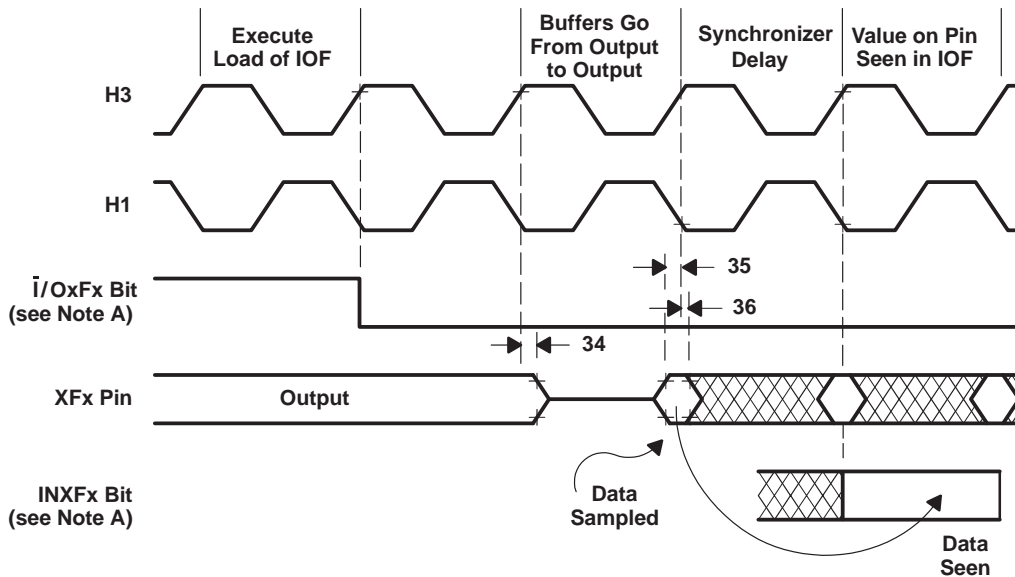
changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin.

timing of XFx changing from output to input mode for SMJ320C31 (see Figure 21)

NO.		'C31-40		'LC31-40		'C31-50		'C31-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
34	$t_{h(H3H-XF)}$ Hold time, XFx after H3 high	13*		13*		12*		11*		ns
35	$t_{su(XF-H1L)}$ Setup time, XFx before H1 low	9		10		8		8		ns
36	$t_{h(H1L-XF)}$ Hold time, XFx after H1 low	0		0		0		0		ns

* This parameter is not production tested.



NOTE A: $\bar{I}/OxFx$ represents either bit 1 or bit 5 of the IOF register, and $INxFx$ represents either bit 3 or bit 7 of the IOF register.

Figure 21. Timing for Change of XFx From Output to Input Mode

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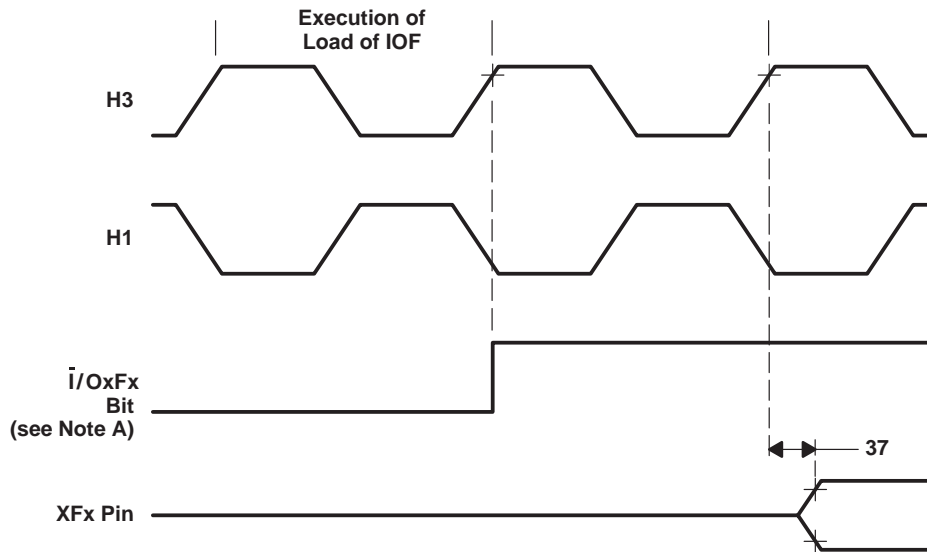
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changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin.

timing for XFx changing from input to output mode (see Figure 22)

NO.		'C31-40 'LC31-40		'C31-50		'C31-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
37	$t_d(H3H-XFIO)$ Delay time, H3 high to XFx switching from input to output		17		17		16	ns



NOTE A: $\bar{I}/OxFx$ represents either bit 1 or bit 5 of the IOF register.

Figure 22. Timing for Change of XFx From Input to Output Mode

reset timing

\overline{RESET} is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 23 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

Resetting the device initializes the primary- and expansion-bus control registers to seven software wait states and therefore results in slow external accesses until these registers are initialized.

\overline{HOLD} is an asynchronous input and can be asserted during reset.

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RESET timing (see Figure 23)

NO.		'C31-40		'LC31-40		'C31-50		'C31-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
38	$t_{su}(\text{RESET-CIL})$ Setup time, $\overline{\text{RESET}}$ before CLKIN low	10	$P\ddagger^*$	10	$P\ddagger^*$	10	$P\ddagger^*$	7	$P\ddagger^*$	ns
39	$t_d(\text{CLKINH-H1H})$ Delay time, CLKIN high to H1 high (see Note 4)	2	14	2	14	2	10	2	10	ns
40	$t_d(\text{CLKINH-H1L})$ Delay time, CLKIN high to H1 low (see Note 4)	2	14	2	14	2	10	2	10	ns
41	$t_{su}(\text{RESETH-H1L})$ Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles	9		9		7		6		ns
42	$t_d(\text{CLKINH-H3L})$ Delay time, CLKIN high to H3 low (see Note 4)	2	14	2	14	2	10	2	10	ns
43	$t_d(\text{CLKINH-H3H})$ Delay time, CLKIN high to H3 high (see Note 4)	2	14	2	14	2	10	2	10	ns
44	$t_{dis}(\text{H1H-DZ})$ Disable time, H1 high to D (high impedance)		15*		13*		12*		11*	ns
45	$t_{dis}(\text{H3H-AZ})$ Disable time, H3 high to A (high impedance)		9*		9*		8*		7*	ns
46	$t_d(\text{H3H-CONTROLH})$ Delay time, H3 high to control signals high		9*		9*		8*		7*	ns
47	$t_d(\text{H1H-RWH})$ Delay time, H1 high to $\overline{R/W}$ high		9*		9*		8*		7*	ns
48	$t_d(\text{H1H-IACKH})$ Delay time, H1 high to $\overline{\text{IACK}}$ high		9*		9*		8*		7*	ns
49	$t_{dis}(\text{RESETL-ASYNCH})$ Disable time, $\overline{\text{RESET}}$ low to asynchronous reset signals disabled (high impedance)		21*		21*		17*		14*	ns

$\ddagger P = t_c(\text{Cl})$

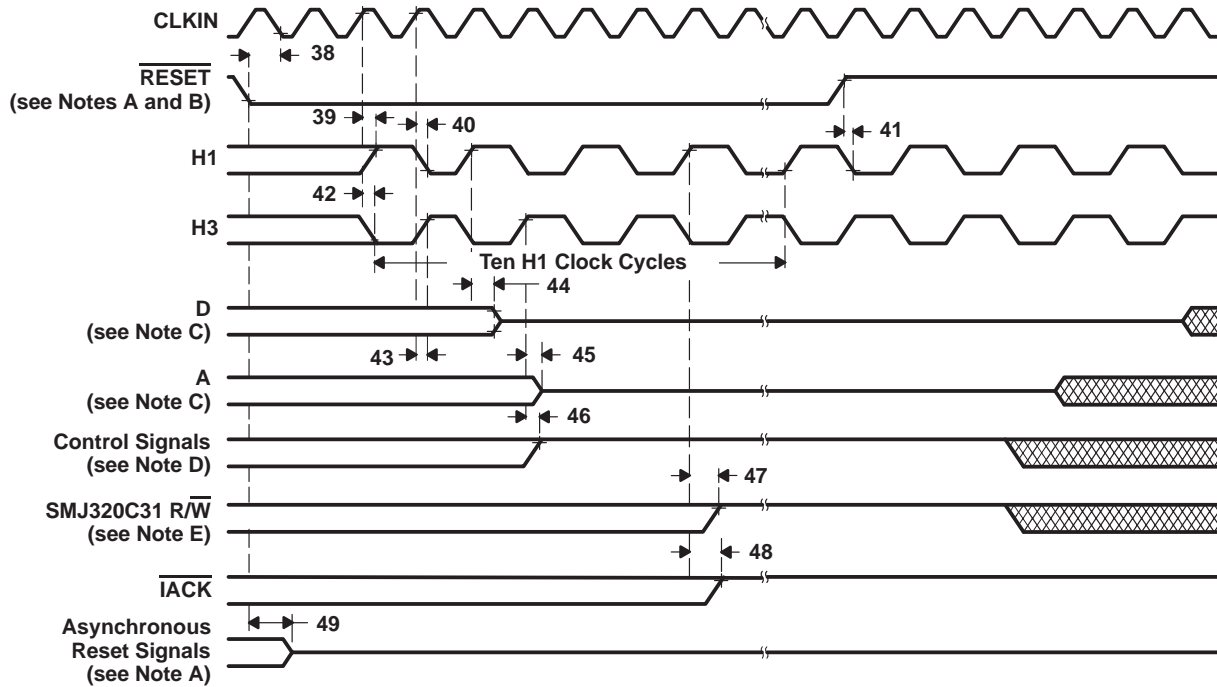
* This parameter is not production tested.

NOTE 4: See Figure 12 and Figure 13 for typical temperature dependence.

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RESET timing (continued)



- NOTES:
- Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
 - $\overline{\text{RESET}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
 - In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
 - Control signals include STRB.
 - The R/W outputs are placed in a high-impedance state during reset and can be provided with a resistive pullup, nominally 18–22 k Ω , if undesirable spurious writes are caused when these outputs go low.

Figure 23. Timing for $\overline{\text{RESET}}$

interrupt response timing

The following table defines the timing parameters for the $\overline{\text{INT}}$ signals.

timing for $\overline{\text{INT3}}\text{--}\overline{\text{INT0}}$ response (see Figure 24)

NO.			'C31-40		'LC31-40		'C31-50		'C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
50	$t_{\text{su}}(\overline{\text{INT}}\text{-H1L})$	Setup time, $\overline{\text{INT3}}\text{--}\overline{\text{INT0}}$ before H1 low	13		15		11		8		ns
51	$t_{\text{w}}(\overline{\text{INT}})$	Pulse duration, interrupt to ensure only one interrupt	P	$2P^{\dagger*}$	P	$2P^{\dagger*}$	P	$2P^{\dagger*}$	P	$2P^{\dagger*}$	ns

$\dagger P = t_{\text{c}}(\text{H})$

* This parameter is not production tested.

The interrupt ($\overline{\text{INT}}$) pins are asynchronous inputs that can be asserted at any time during a clock cycle. The SMJ320C3x interrupts are level-sensitive, not edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt on a given input, an interrupt pulse must be set up and held to:

- A minimum of one H1 falling edge
- No more than two H1 falling edges

The SMJ320C3x can accept an interrupt from the same source every two H1 clock cycles.

If the specified timings are met, the exact sequence shown in Figure 24 occurs; otherwise, an additional delay of one clock cycle is possible.

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timing parameters for $\overline{\text{INT3}}\text{--}\overline{\text{INT0}}$ response (continued)

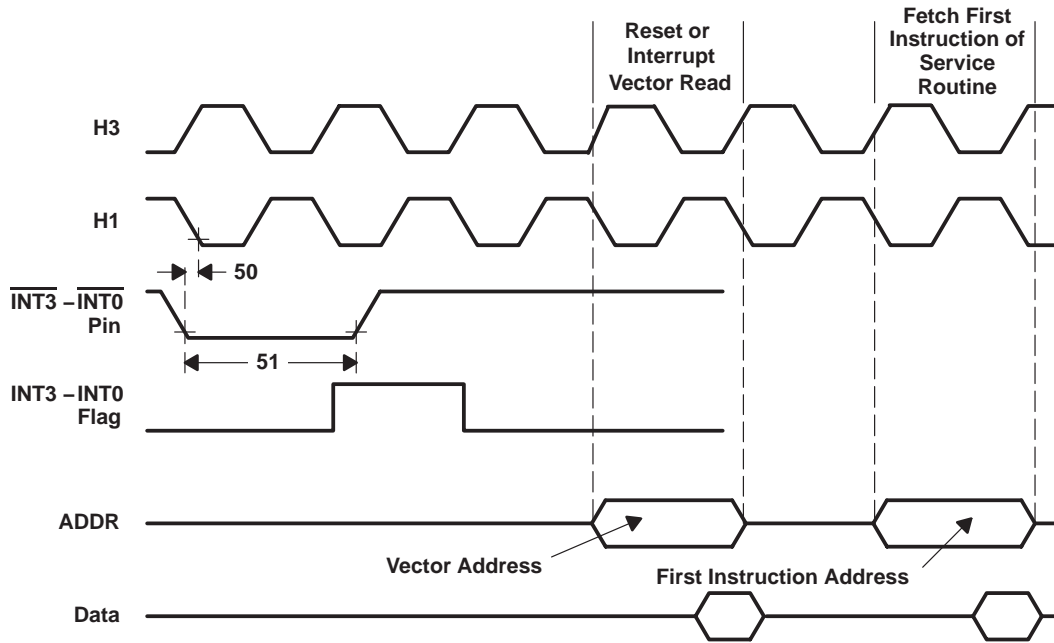


Figure 24. Timing for $\overline{\text{INT3}}\text{--}\overline{\text{INT0}}$ Response

interrupt-acknowledge timing

The $\overline{\text{IACK}}$ output goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction.

timing for $\overline{\text{IACK}}$ (see Note 5 and Figure 25)

NO.		'C31-40 'LC31-40		'C31-50		'C31-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
52	$t_{d(H1H-IACKL)}$ Delay time, H1 high to $\overline{\text{IACK}}$ low		9		7		6	ns
53	$t_{d(H1H-IACKH)}$ Delay time, H1 high to $\overline{\text{IACK}}$ high		9		7		6	ns

NOTE 5: $\overline{\text{IACK}}$ goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction. Because of pipeline conflicts, $\overline{\text{IACK}}$ remains low for one cycle even if the decode phase of the IACK instruction is extended.

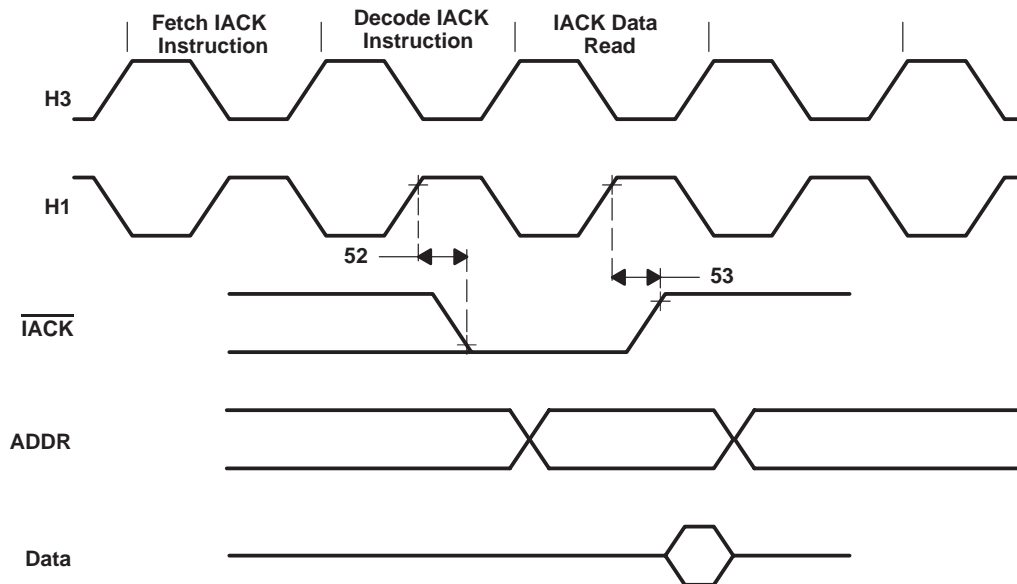


Figure 25. Timing for $\overline{\text{IACK}}$

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serial-port timing for SMJ320C31-40 and SMJ320LC31-40 (see Figure 26 and Figure 27)

NO.			'C31-40 'LC31-40		UNIT
			MIN	MAX	
54	t _d (H1H-SCK)	Delay time, H1 high to internal CLKX/R		13	ns
55	t _c (SCK)	Cycle time, CLKX/R	CLKX/R ext	t _c (H)x2.6	ns
			CLKX/R int	t _c (H)x2 t _c (H)x2 ³²	
56	t _w (SCK)	Pulse duration, CLKX/R high/low	CLKX/R ext	t _c (H)+10	ns
			CLKX/R int	[t _c (SCK)/2]-5 [t _c (SCK)/2]+5	
57	t _r (SCK)	Rise time, CLKX/R		7	ns
58	t _f (SCK)	Fall time, CLKX/R		7	ns
59	t _d (C-DX)	Delay time, CLKX to DX valid	CLKX ext	30	ns
			CLKX int	17	
60	t _{su} (DR-CLKRL)	Setup time, DR before CLKR low	CLKR ext	9	ns
			CLKR int	21	
61	t _h (CLKRL-DR)	Hold time, DR from CLKR low	CLKR ext	9	ns
			CLKR int	0	
62	t _d (C-FSX)	Delay time, CLKX to internal FSX high/low	CLKX ext	27	ns
			CLKX int	15	
63	t _{su} (FSR-CLKRL)	Setup time, FSR before CLKR low	CLKR ext	9	ns
			CLKR int	9	
64	t _h (SCKL-FS)	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	9	ns
			CLKX/R int	0	
65	t _{su} (FSX-C)	Setup time, external FSX before CLKX	CLKX ext	-[t _c (H)-8]* [t _c (SCK)/2]-10*	ns
			CLKX int	[t _c (H)-21]* t _c (SCK)/2*	
66	t _d (CH-DX)V	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext	30*	ns
			CLKX int	18*	
67	t _d (FSX-DX)V	Delay time, FSX to first DX bit, CLKX precedes FSX		30*	ns
68	t _d (CH-DXZ)	Delay time, CLKX high to DX high impedance following last data bit		17*	ns

* This parameter is not production tested.

SMJ320C31, SMJ320LC31, SMQ320LC31 DIGITAL SIGNAL PROCESSORS

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serial-port timing for SMJ320C31-50 (see Figure 26 and Figure 27)

NO.			'C31-50		UNIT
			MIN	MAX	
54	$t_d(H1H-SCK)$	Delay time, H1 high to internal CLKX/R		10	ns
55	$t_c(SCK)$	Cycle time, CLKX/R	CLKX/R ext	$t_c(H) \times 2.6$	ns
			CLKX/R int	$t_c(H) \times 2$ $t_c(H) \times 2^{32}$	
56	$t_w(SCK)$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_c(H) + 10$	ns
			CLKX/R int	$[t_c(SCK)/2] - 5$ $[t_c(SCK)/2] + 5$	
57	$t_r(SCK)$	Rise time, CLKX/R		6	ns
58	$t_f(SCK)$	Fall time, CLKX/R		6	ns
59	$t_d(C-DX)$	Delay time, CLKX to DX valid	CLKX ext	24	ns
			CLKX int	16	
60	$t_{su}(DR-CLKRL)$	Setup time, DR before CLKR low	CLKR ext	9	ns
			CLKR int	17	
61	$t_h(CLKRL-DR)$	Hold time, DR from CLKR low	CLKR ext	7	ns
			CLKR int	0	
62	$t_d(C-FSX)$	Delay time, CLKX to internal FSX high/low	CLKX ext	22	ns
			CLKX int	15	
63	$t_{su}(FSR-CLKRL)$	Setup time, FSR before CLKR low	CLKR ext	7	ns
			CLKR int	7	
64	$t_h(SCKL-FS)$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	7	ns
			CLKX/R int	0	
65	$t_{su}(FSX-C)$	Setup time, external FSX before CLKX	CLKX ext	$-[t_c(H) - 8]^*$ $[t_c(SCK)/2] - 10^*$	ns
			CLKX int	$-[t_c(H) - 21]^*$ $t_c(SCK)/2^*$	
66	$t_d(CH-DX)V$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext	24*	ns
			CLKX int	14*	
67	$t_d(FSX-DX)V$	Delay time, FSX to first DX bit, CLKX precedes FSX		24*	ns
68	$t_d(CH-DXZ)$	Delay time, CLKX high to DX high impedance following last data bit		14*	ns

* This parameter is not production tested.

SMJ320C31, SMJ320LC31, SMQ320LC31 DIGITAL SIGNAL PROCESSORS

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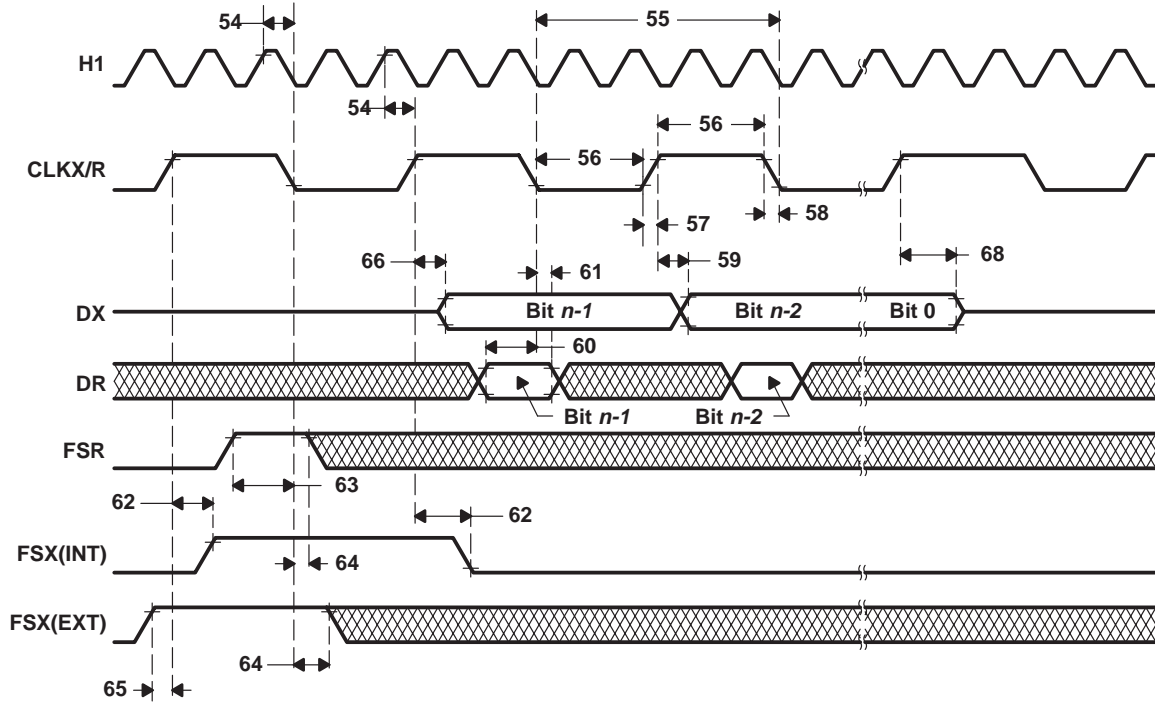
serial-port timing for SMJ320C31-60 (see Figure 26 and Figure 27)

NO.			'C31-60		UNIT
			MIN	MAX	
54	$t_d(H1H-SCK)$	Delay time, H1 high to internal CLKX/R		8	ns
55	$t_c(SCK)$	Cycle time, CLKX/R	CLKX/R ext	$t_c(H) \times 2.6$	ns
			CLKX/R int	$t_c(H) \times 2$ $t_c(H) \times 2^{32}$	
56	$t_w(SCK)$	Pulse duration, CLKX/R high/low	CLKX/R ext	$t_c(H) + 10$	ns
			CLKX/R int	$[t_c(SCK)/2] - 5$ $[t_c(SCK)/2] + 5$	
57	$t_r(SCK)$	Rise time, CLKX/R		5	ns
58	$t_f(SCK)$	Fall time, CLKX/R		5	ns
59	$t_d(C-DX)$	Delay time, CLKX to DX valid	CLKX ext	20	ns
			CLKX int	15	
60	$t_{su}(DR-CLKRL)$	Setup time, DR before CLKR low	CLKR ext	8	ns
			CLKR int	15	
61	$t_h(CLKRL-DR)$	Hold time, DR from CLKR low	CLKR ext	6	ns
			CLKR int	0	
62	$t_d(C-FSX)$	Delay time, CLKX to internal FSX high/low	CLKX ext	20	ns
			CLKX int	14	
63	$t_{su}(FSR-CLKRL)$	Setup time, FSR before CLKR low	CLKR ext	6	ns
			CLKR int	6	
64	$t_h(SCKL-FS)$	Hold time, FSX/R input from CLKX/R low	CLKX/R ext	6	ns
			CLKX/R int	0	
65	$t_{su}(FSX-C)$	Setup time, external FSX before CLKX	CLKX ext	$-[t_c(H) - 8]^*$ $[t_c(SCK)/2] - 10^*$	ns
			CLKX int	$-[t_c(H) - 21]^*$ $t_c(SCK)/2^*$	
66	$t_d(CH-DX)V$	Delay time, CLKX to first DX bit, FSX precedes CLKX high	CLKX ext	20*	ns
			CLKX int	12*	
67	$t_d(FSX-DX)V$	Delay time, FSX to first DX bit, CLKX precedes FSX		20*	ns
68	$t_d(CH-DXZ)$	Delay time, CLKX high to DX high impedance following last data bit		12*	ns

* This parameter is not production tested.

data-rate timing modes

Unless otherwise indicated, the data-rate timings shown in Figure 26 and Figure 27 are valid for all serial-port modes, including handshake. For a functional description of serial-port operation, see subsection 8.2.12 of the *TMS320C3x User's Guide* (literature number SPRU031).



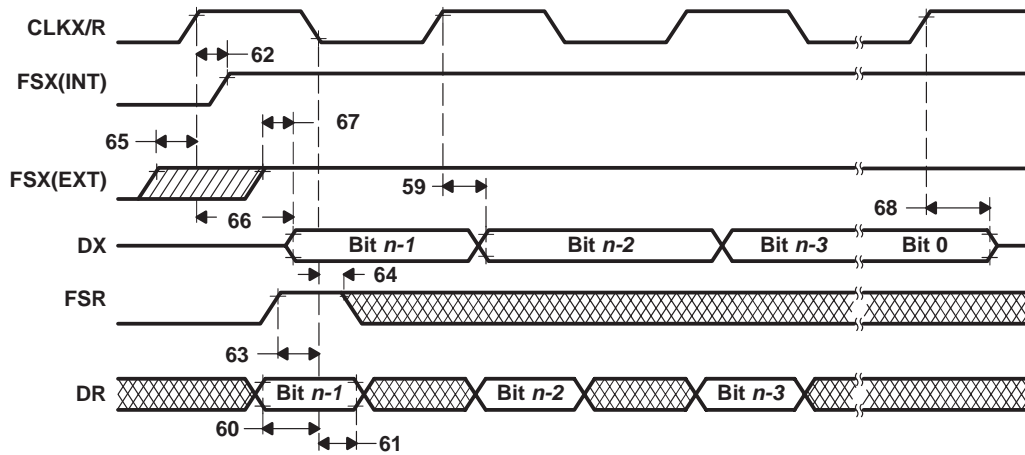
- NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

Figure 26. Timing for Fixed Data-Rate Mode

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data-rate timing modes (continued)



- NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
 B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
 C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 27. Timing for Variable Data-Rate Mode

HOLD timing

$\overline{\text{HOLD}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 27 occurs; otherwise, an additional delay of one clock cycle is possible.

The NOHOLD bit of the primary-bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue until a second write is encountered.

timing for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (see Figure 28)

NO.		'C31-40		'LC31-40		'C31-50		'C31-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
69	$t_{su}(\overline{\text{HOLD}}\text{-H1L})$ Setup time, $\overline{\text{HOLD}}$ before H1 low	13		13		10		8		ns
70	$t_v(\text{H1L}\text{-}\overline{\text{HOLDA}})$ Valid time, $\overline{\text{HOLDA}}$ after H1 low	0†	9	0*	9	0*	7	0*	6	ns
71	$t_w(\overline{\text{HOLD}})^\dagger$ Pulse duration, $\overline{\text{HOLD}}$ low	$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		$2t_{c(H)}$		ns
72	$t_w(\overline{\text{HOLDA}})$ Pulse duration, $\overline{\text{HOLDA}}$ low	$t_{cH}\text{-}5^*$		$t_{cH}\text{-}5^*$		$t_{cH}\text{-}5^*$		$t_{cH}\text{-}5^*$		ns
73	$t_d(\text{H1L}\text{-SH})\text{H}$ Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$	0*	9	0*	9	0*	7	0*	6	ns
74	$t_{dis}(\text{H1L}\text{-S})$ Disable time, H1 low to $\overline{\text{STRB}}$ to the high-impedance state	0*	9*	0*	9*	0*	7*	0*	7*	ns
75	$t_{en}(\text{H1L}\text{-S})$ Enable time, H1 low to $\overline{\text{STRB}}$ enabled (active)	0*	9	0*	9	0*	7	0*	6	ns
76	$t_{dis}(\text{H1L}\text{-RW})$ Disable time, H1 low to $\overline{\text{R}/\overline{\text{W}}}$ to the high-impedance state	0*	9*	0*	9*	0*	8*	0*	7*	ns
77	$t_{en}(\text{H1L}\text{-RW})$ Enable time, H1 low to $\overline{\text{R}/\overline{\text{W}}}$ enabled (active)	0*	9	0*	9	0*	7	0*	6	ns
78	$t_{dis}(\text{H1L}\text{-A})$ Disable time, H1 low to address to the high-impedance state	0*	9*	0*	10*	0*	8*	0*	7*	ns
79	$t_{en}(\text{H1L}\text{-A})$ Enable time, H1 low to address enabled (valid)	0*	13	0*	13	0*	10	0*	11?	ns
80	$t_{dis}(\text{H1H}\text{-D})$ Disable time, H1 high to data to the high-impedance state	0*	12*	0*	9*	0*	10*	0*	7*	ns

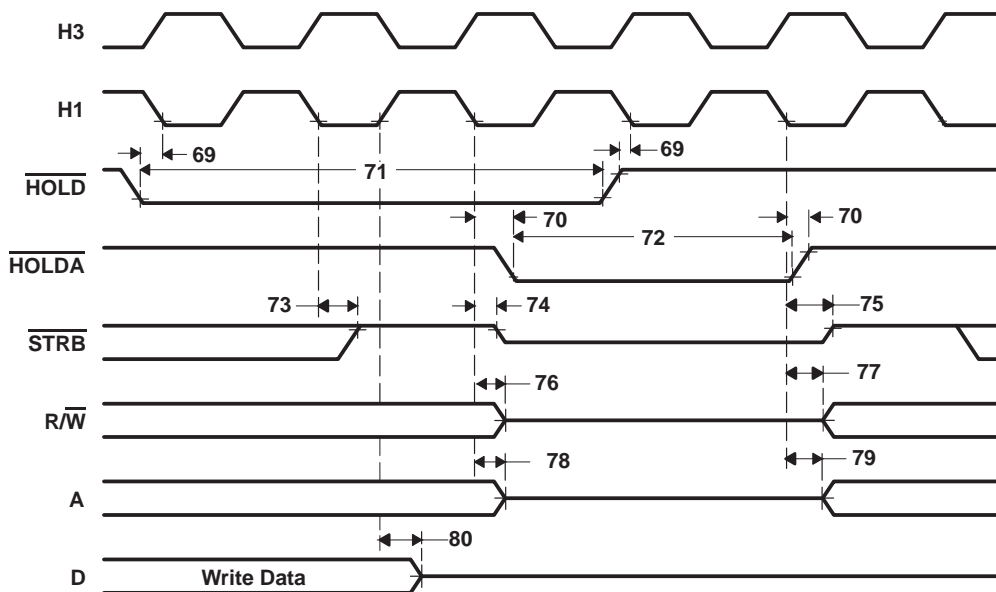
† $\overline{\text{HOLD}}$ is an asynchronous input and can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 28 occurs; otherwise, an additional delay of one clock cycle is possible.

* This parameter is not production tested.

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HOLD timing (continued)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 28. Timing for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$

general-purpose I/O timing

Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The contents of the internal control registers associated with each peripheral define the modes for these pins.

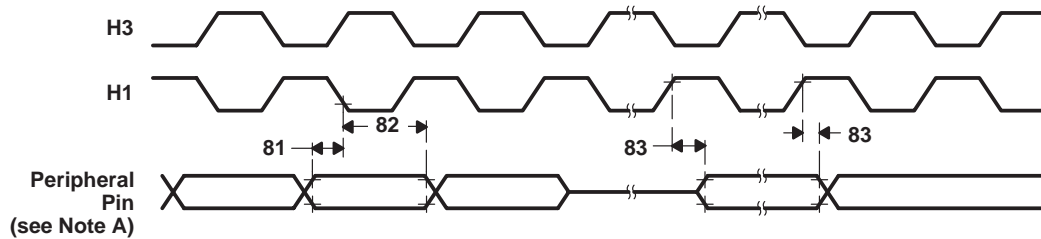
peripheral pin I/O timing

The table, timing parameters for peripheral pin general-purpose I/O, defines peripheral pin general-purpose I/O timing parameters.

timing requirements for peripheral pin general-purpose I/O (see Note 6 and Figure 29)

NO.			'C31-33		'C31-40 'LC31-40		'C31-50		'C31-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
81	$t_{su}(GPIO-H1L)$	Setup time, general-purpose input before H1 low	12		10		9		8		ns
82	$t_h(H1L-GPIO)$	Hold time, general-purpose input after H1 low	0		0		0		0		ns
83	$t_d(H1H-GPIO)$	Delay time, general-purpose output after H1 high		15		13		10		8	ns

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 29. Timing for Peripheral Pin General-Purpose I/O

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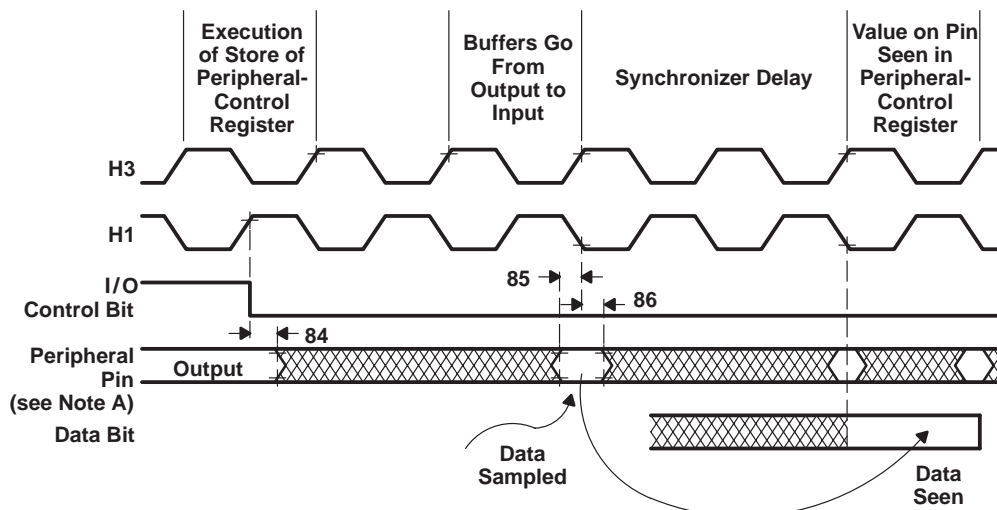
changing the peripheral pin I/O modes

The following tables show the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and vice versa.

timing requirements for peripheral pin changing from general-purpose output to input mode (see Note 6 and Figure 30)

NO.		'C31-40	'C31-50	'C31-60	UNIT
		'LC31-40	MIN MAX	MIN MAX	
84	$t_{h(H1H)}$ Hold time, peripheral pin after H1 high	13	10	8	ns
85	$t_{su(GPIO-H1L)}$ Setup time, peripheral pin before H1 low	9	9	8	ns
86	$t_{h(H1L-GPIO)}$ Hold time, peripheral pin after H1 low	0	0	0	ns

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



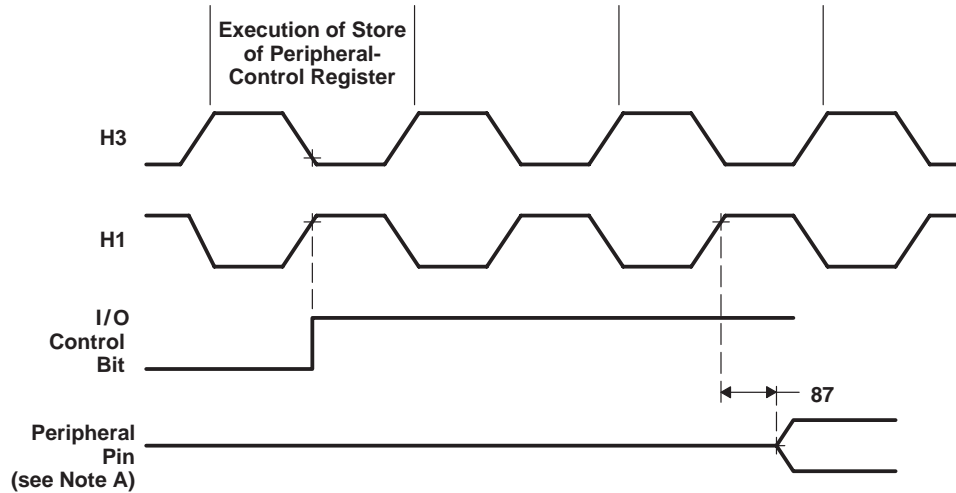
NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 30. Timing for Change of Peripheral Pin From General-Purpose Output to Input Mode

timing for peripheral pin changing from general-purpose input to output mode (see Note 6 and Figure 31)

NO.		'C31-40 'LC31-40		'C31-50		'C31-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
87	$t_d(H1H-GPIO)$ Delay time, H1 high to peripheral pin switching from input to output		13		10		8	ns

NOTE 6: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 31. Timing for Change of Peripheral Pin From General-Purpose Input to Output Mode

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timer pin timing

Valid logic-level periods and polarity are specified by the contents of the internal control registers.

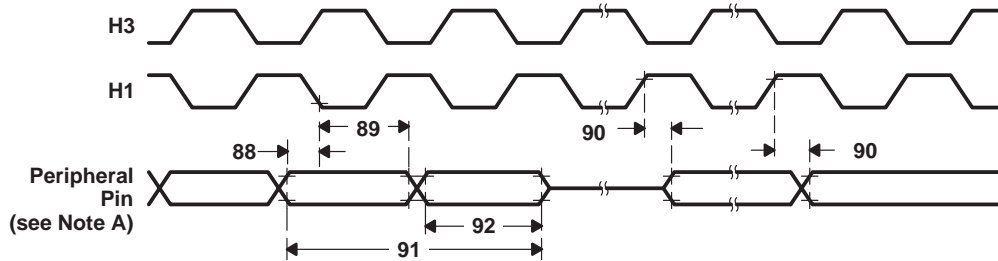
The following tables define the timing requirements for the timer pin.

timing for timer pin (see Figure 32 and Note 7)

NO.			'C31-40, 'LC31-40 'C31-50		'C31-60		UNIT
			MIN	MAX	MIN	MAX	
88	$t_{su}(TCLK-H1L)$	Setup time, TCLK external before H1 low	10		6		ns
89	$t_h(H1L-TCLK)$	Hold time, TCLK external after H1 low	0		0		ns
90	$t_d(H1H-TCLK)$	Delay time, H1 high to TCLK internal valid		9		8	ns
91	$t_c(TCLK)$	Cycle time, TCLK	TCLK ext	$t_c(H) \times 2.6$		$t_c(H) \times 2.6$	ns
			TCLK int	$t_c(H) \times 2$	$t_c(H) \times 2^{32}^*$	$t_c(H) \times 2$	
92	$t_w(TCLK)$	Pulse duration, TCLK high/low	TCLK ext	$t_c(H) + 10$		$t_c(H) + 10$	ns
			TCLK int	$[t_c(TCLK)/2] - 5$	$[t_c(TCLK)/2] + 5$	$[t_c(TCLK)/2] - 5$	

NOTE 7: Numbers 88 and 89 are applicable for a synchronous input clock. Timing parameters 91 and 92 are applicable for an asynchronous input clock.

* This parameter is not production tested.



NOTE A: \overline{HOLDA} goes low in response to \overline{HOLD} going low and continues to remain low until one H1 cycle after \overline{HOLD} goes back high.

Figure 32. Timing for Timer Pin

SHZ pin timing

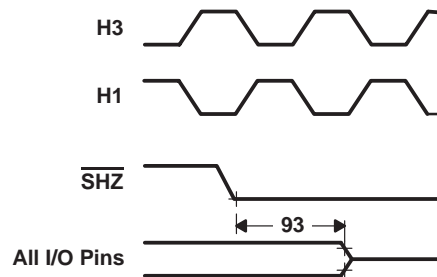
The following table defines the timing parameter for the SHZ pin.

timing parameters for SHZ (see Figure 33)

NO.		'C31 'LC31		UNIT
		MIN	MAX	
93	$t_{dis}(SHZ)$ Disable time, SHZ low to all O, I/O pins disabled (high impedance)	0*	$2P^{\dagger}$ *	ns

$^{\dagger} P = t_{c}(Cl)$

* This parameter is not production tested.



NOTE A: Enabling SHZ destroys SMJ320C3x register and memory contents. Assert SHZ = 1 and reset the SMJ320C3x to restore it to a known condition.

Figure 33. Timing for SHZ

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part order information

DEVICE	TECHNOLOGY	POWER SUPPLY	OPERATING FREQUENCY	PACKAGE TYPE	PROCESSING LEVEL
5962-9205803MXA	0.6- μ m CMOS	5 V \pm 5%	40 MHz	Ceramic 141-pin staggered PGA	DSCC SMD
SMJ320C31GFAM40	0.6- μ m CMOS	5 V \pm 5%	40 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAM40	0.6- μ m CMOS	5 V \pm 5%	40 MHz	Ceramic 141-pin staggered PGA	Std
5962-9205803MYA	0.6- μ m CMOS	5 V \pm 5%	40 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar.	DSCC SMD
SMJ320C31HFGM40	0.6- μ m CMOS	5 V \pm 5%	40 MHz	Ceramic 132-lead quad flatpack with a nonconductive tie bar	QML
SM320C31HFGM40	0.6- μ m CMOS	5 V \pm 5%	40 MHz	Ceramic 132-lead quad flatpack with a nonconductive tie bar	Std
5962-9205803Q9A	0.72- μ m CMOS	5 V \pm 5%	40 MHz	C31–40 KGD (known good die)	DSCC SMD
SMJ320C31KGD40B	0.72- μ m CMOS	5 V \pm 5%	40 MHz	C31–40 KGD (known good die)	QML
5962-9205804MXA	0.6- μ m CMOS	5 V \pm 5%	50 MHz	Ceramic 141-pin staggered PGA	DSCC SMD
SMJ320C31GFAM50	0.6- μ m CMOS	5 V \pm 5%	50 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAM50	0.6- μ m CMOS	5 V \pm 5%	50 MHz	Ceramic 141-pin staggered PGA	Std
5962-9205804MYA	0.6- μ m CMOS	5 V \pm 5%	50 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar.	DSCC SMD
SMJ320C31HFGM50	0.6- μ m CMOS	5 V \pm 5%	50 MHz	Ceramic 132-lead quad flatpack with nonconductive tie bar	QML
SM320C31HFGM50	0.6- μ m CMOS	5 V \pm 5%	50 MHz	Ceramic 132-lead quad flatpack with nonconductive tie bar	Std
5962-9205805QXA	0.6- μ m CMOS	5 V \pm 5%	60 MHz	Ceramic 141-pin staggered PGA	DSCC SMD
SMJ320C31GFAS60	0.6- μ m CMOS	5 V \pm 5%	60 MHz	Ceramic 141-pin staggered PGA	QML
SM320C31GFAS60	0.6- μ m CMOS	5 V \pm 5%	60 MHz	Ceramic 141-pin staggered PGA	Std
5962-9205805QYA	0.6- μ m CMOS	5 V \pm 5%	60 MHz	Ceramic 132-pin quad flatpack with nonconductive tie bar.	DSCC SMD
SMJ320C31HFGS60	0.6- μ m CMOS	5 V \pm 5%	60 MHz	Ceramic 132-lead quad flatpack with nonconductive tie bar	QML
SM320C31HFGS60	0.6- μ m CMOS	5 V \pm 5%	60 MHz	Ceramic 132-lead quad flatpack with nonconductive tie bar	Std
5962-9760601NXB	0.72- μ m CMOS	3.3 V \pm 5%	40 MHz	Plastic 132-lead good flatpack	DSCC SMD
SMQ320LC31PQM40	0.72- μ m CMOS	3.3 V \pm 5%	40 MHz	Plastic 132-lead good flatpack	QML
5962-9760601Q9A	0.72- μ m CMOS	3.3 V \pm 5%	40 MHz	LC31–40 KGD (known good die)	DSCC SMD
SMJ320LC31KGD40B	0.72- μ m CMOS	3.3 V \pm 5%	40 MHz	LC31–40 KGD (known good die)	QML

part order information (continued)

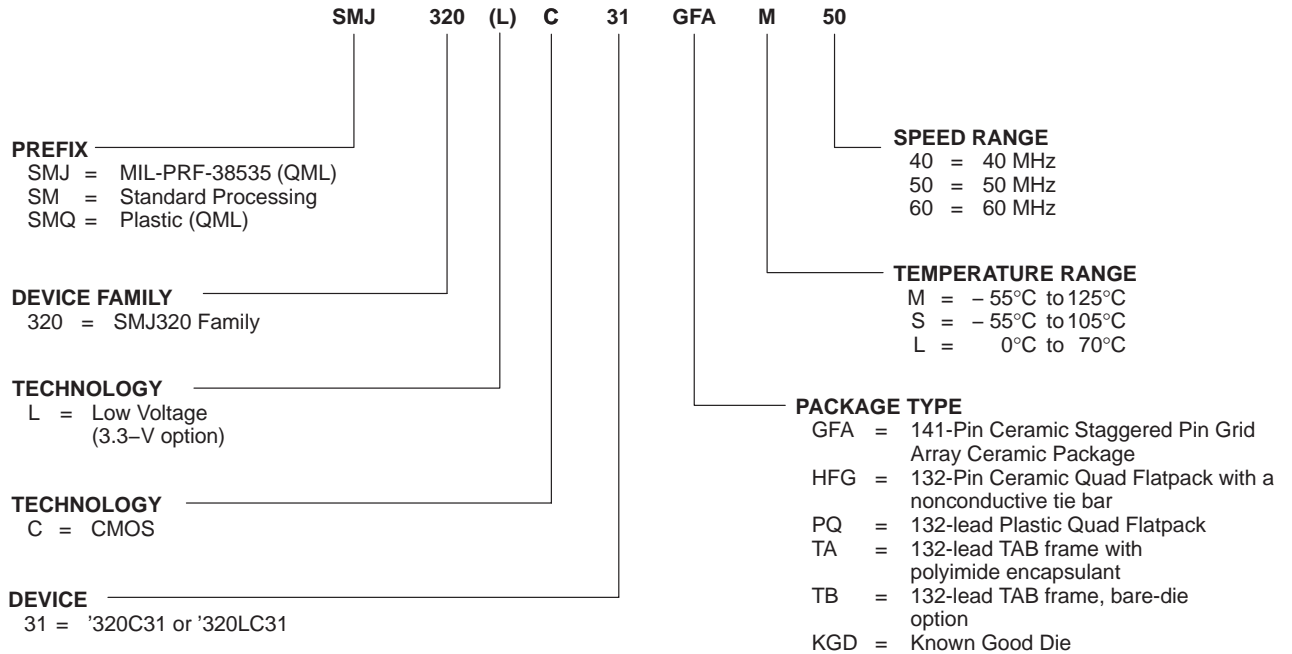


Figure 34. Device Nomenclature

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
5962-9205803MXA	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	Call TI	
5962-9205803MXC	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	N / A for Pkg Type	
5962-9205803MYA	ACTIVE	CFP	HFG	132	1	TBD	Call TI	Call TI	
5962-9205804MXA	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	Call TI	
5962-9205804MXC	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	N / A for Pkg Type	
5962-9205804MYA	ACTIVE	CFP	HFG	132	1	TBD	Call TI	Call TI	
5962-9205805QXA	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	Call TI	
5962-9205805QYA	ACTIVE	CFP	HFG	132	1	TBD	Call TI	Call TI	
5962-9760601NXB	ACTIVE	BQFP	PQ	132	1	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR	
5962-9760601Q9A	OBSOLETE	XCEPT	KGD	0		TBD	Call TI	Call TI	
SM320C31GFAM50	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	N / A for Pkg Type	
SM320C31GFAS60	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	N / A for Pkg Type	
SM320C31HFGM40	ACTIVE	CFP	HFG	132	1	TBD	Call TI	N / A for Pkg Type	
SM320C31HFGM50	ACTIVE	CFP	HFG	132	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C31GFAM40	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C31GFAM50	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C31GFAS60	ACTIVE	CPGA	GFA	141	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C31HFGM40	ACTIVE	CFP	HFG	132	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C31HFGM50	ACTIVE	CFP	HFG	132	1	TBD	Call TI	N / A for Pkg Type	
SMJ320C31HFGS60	ACTIVE	CFP	HFG	132	1	TBD	Call TI	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SM320C31, SMJ320C31 :

● Catalog: [TMS320C31](#), [TMS320C31](#)

● Military: [SMJ320C31](#)

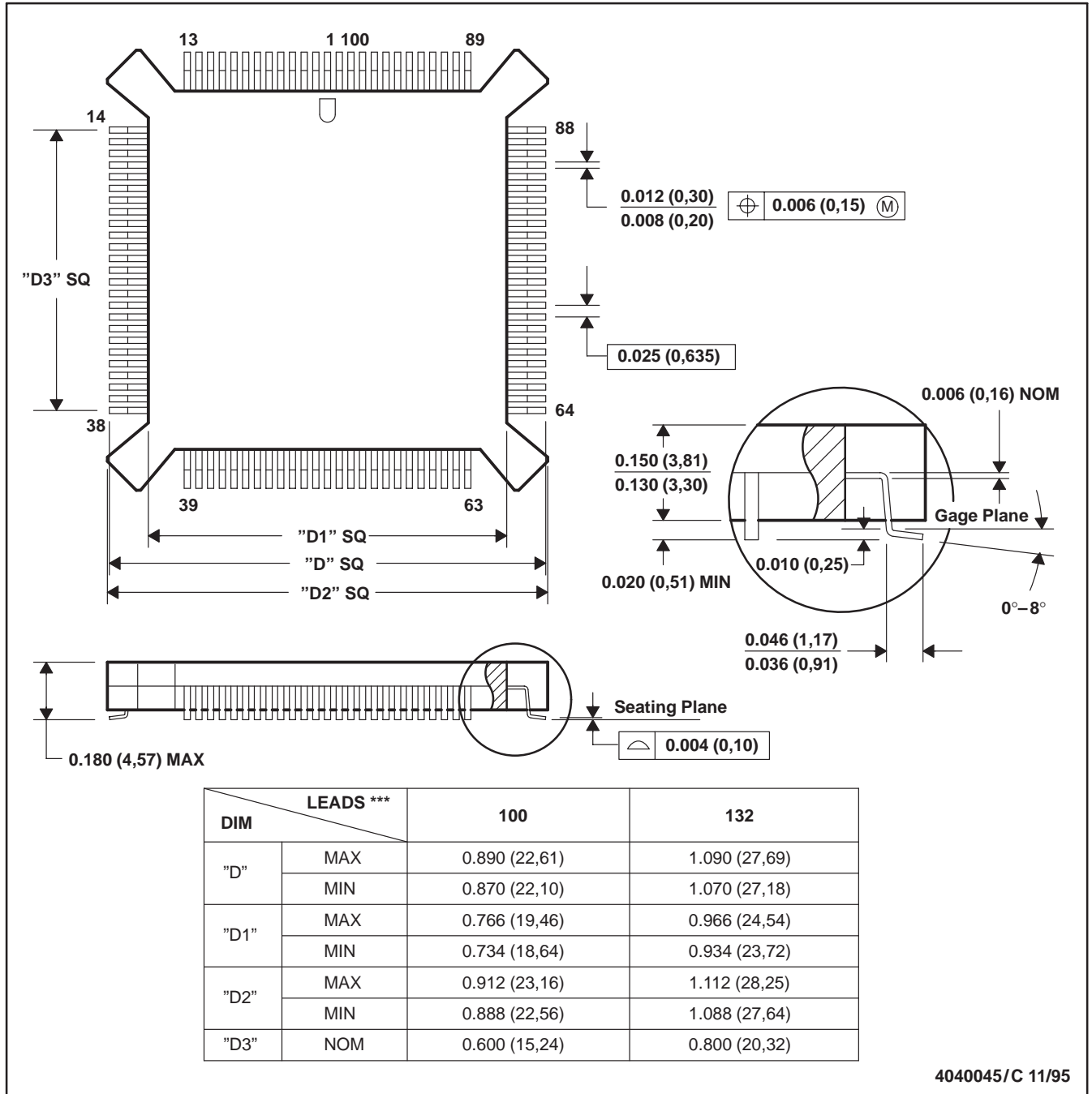
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

PQ (S-PQFP-G^{***})

PLASTIC QUAD FLATPACK

100 LEAD SHOWN

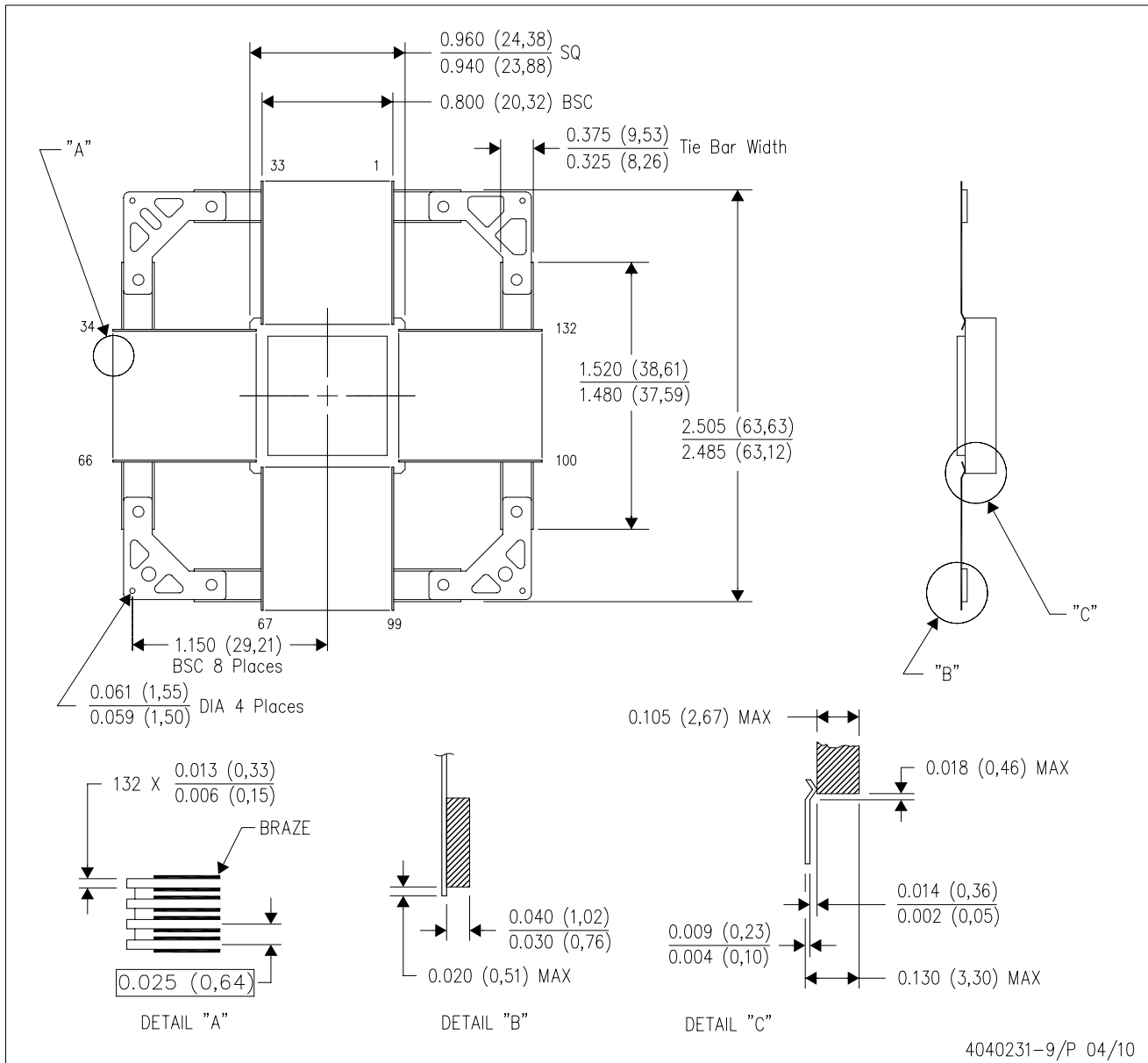


4040045/C 11/95

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MO-069

HFG (S-CQFP-F132)

CERAMIC QUAD FLATPACK WITH NCTB

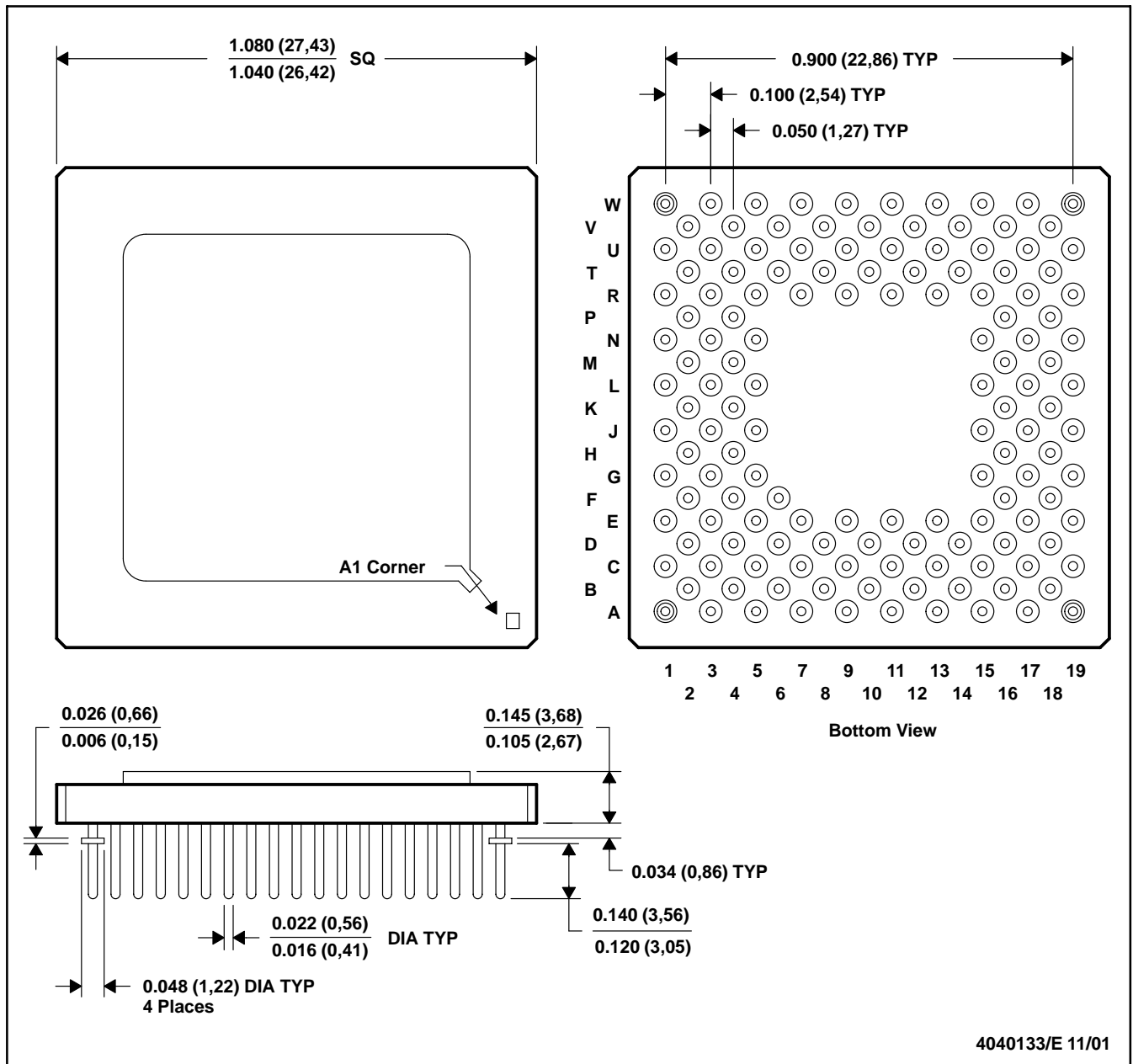


4040231-9/P 04/10

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
 - This package is hermetically sealed with a metal lid.
 - The leads are gold plated and can be solderdipped.
 - Leads not shown for clarity purposes.
 - Falls within JEDEC MO-113AC

GFA (S-CPGA-P141)

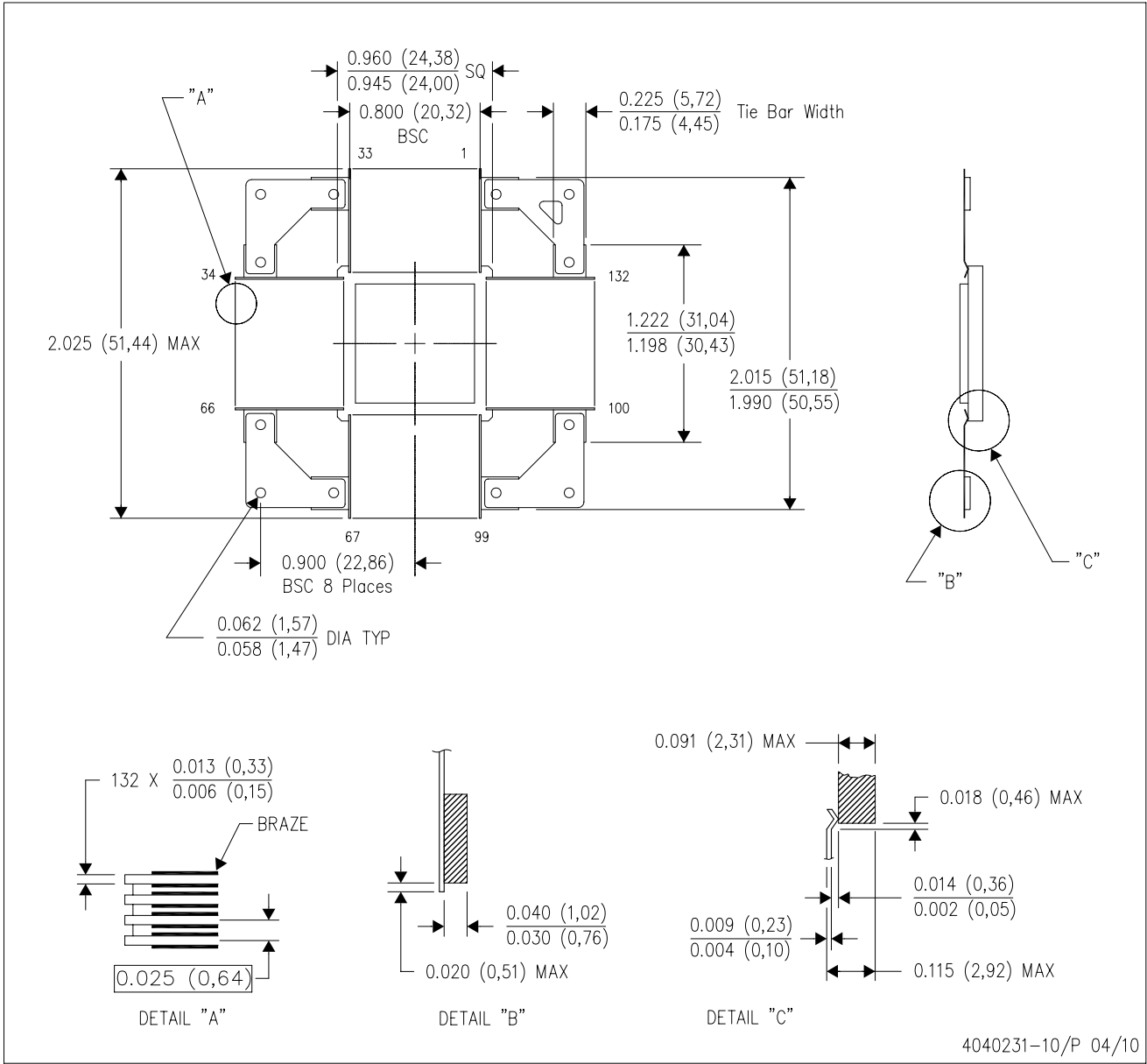
CERAMIC PIN GRID ARRAY



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Index mark can appear on top or bottom, depending on package vendor.
 - D. Pins are located within 0.010 (0,25) diameter of true position relative to each other at maximum material condition and within 0.030 (0,76) diameter relative to the edge of the ceramic.
 - E. This package can be hermetically sealed with metal lids or with ceramic lids using glass frit.
 - F. The pins can be gold-plated or solder-dipped.
 - G. Falls within JEDEC MO-128AB

HFG (S-CQFP-F132)

CERAMIC QUAD FLATPACK WITH NCTB



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
 - D. This package is hermetically sealed with a metal lid.
 - E. The leads are gold plated and can be solderdipped.
 - F. Leads not shown for clarity purposes.

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