

PROGRAMMABLE 27-BIT SERIAL-TO-PARALLEL RECEIVER

FEATURES

- **Serial Interface Technology**
- **Compatible With FlatLink™3G Such as SN65LVDS303**
- **Supports Video Interfaces up to 24-Bit RGB Data and 3 Control Bits Received Over 1 or 2 SubLVDS Differential Lines**
- **SubLVDS Differential Voltage Levels**
- **Up to 810-Mbps Data Throughput**
- **Three Operating Modes to Conserve Power**
 - Active mode QVGA: 17 mW
 - Typical Shutdown: 0.7 μW
 - Typical Standby Mode: 27 μW Typical
- **Bus-Swap Function for PCB-Layout Flexibility**
- **ESD Rating > 4 kV (HBM)**
- **Pixel Clock Range of 4 MHz–30 MHz**
- **Failsafe on all CMOS Inputs**
- **Packaged in 5-mm × 5-mm MicroStar Junior μBGA® With 0,5-mm Ball Pitch**
- **Very Low EMI Meets SAE J1752/3 'Kh'-Spec**

APPLICATIONS

- **Small Low-Emission Interface Between Graphics Controller and LCD Display**
- **Mobile Phones and Smart Phones**
- **Portable Multimedia Players**

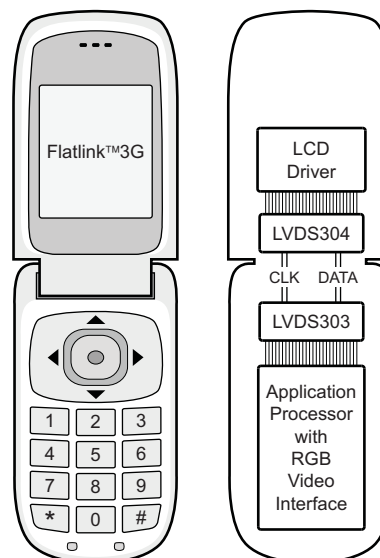
DESCRIPTION

The SN65LVDS304 receiver deserializes FlatLink™3G-compliant serial input data to 27 parallel data outputs. The SN65LVDS304 receiver contains one shift register to load 30 bits from 1 or 2 serial inputs and latches the 24 pixel bits and 3 control bits out to the parallel CMOS outputs after checking the parity bit. If the parity check confirms correct parity, the channel parity error (CPE) output remains low. If a parity error is detected, the CPE output generates a high pulse while the data output bus disregards the newly-received pixel. Instead, the last data word is held on the output bus for another clock cycle.

The serial data and clock are received via sub-low-voltage differential signalling (SubLVDS) lines. The SN65LVDS304 supports three operating power modes (shutdown, standby, and active) to conserve power.

When receiving, the PLL locks to the incoming clock CLK and generates an internal high-speed clock at the line rate of the data lines. The data is serially loaded into a shift register using the internal high-speed clock. The deserialized data is presented on the parallel output bus with a recreation of the pixel clock, PCLK, generated from the internal high-speed clock. If no input CLK signal is present, the output bus is held static with PCLK and DE held low, while all other parallel outputs are pulled high.

The parallel (CMOS) output bus offers a bus-swap feature. The SWAP control pin controls the output pin order of the output pixel data to be either R[7:0], G[7:0], B[7:0], VS, HS, DE or B[0:7], G[0:7], R[0:7], VS, HS, DE. This gives a PCB designer the flexibility to better match the bus to the LCD driver pinout or to put the receiver device on the top side or the bottom side of the PCB. The F/S control input selects between a slow CMOS bus output rise time for best EMI and power consumption and a fast CMOS output for increased speed or higher-load designs.



M0056-01



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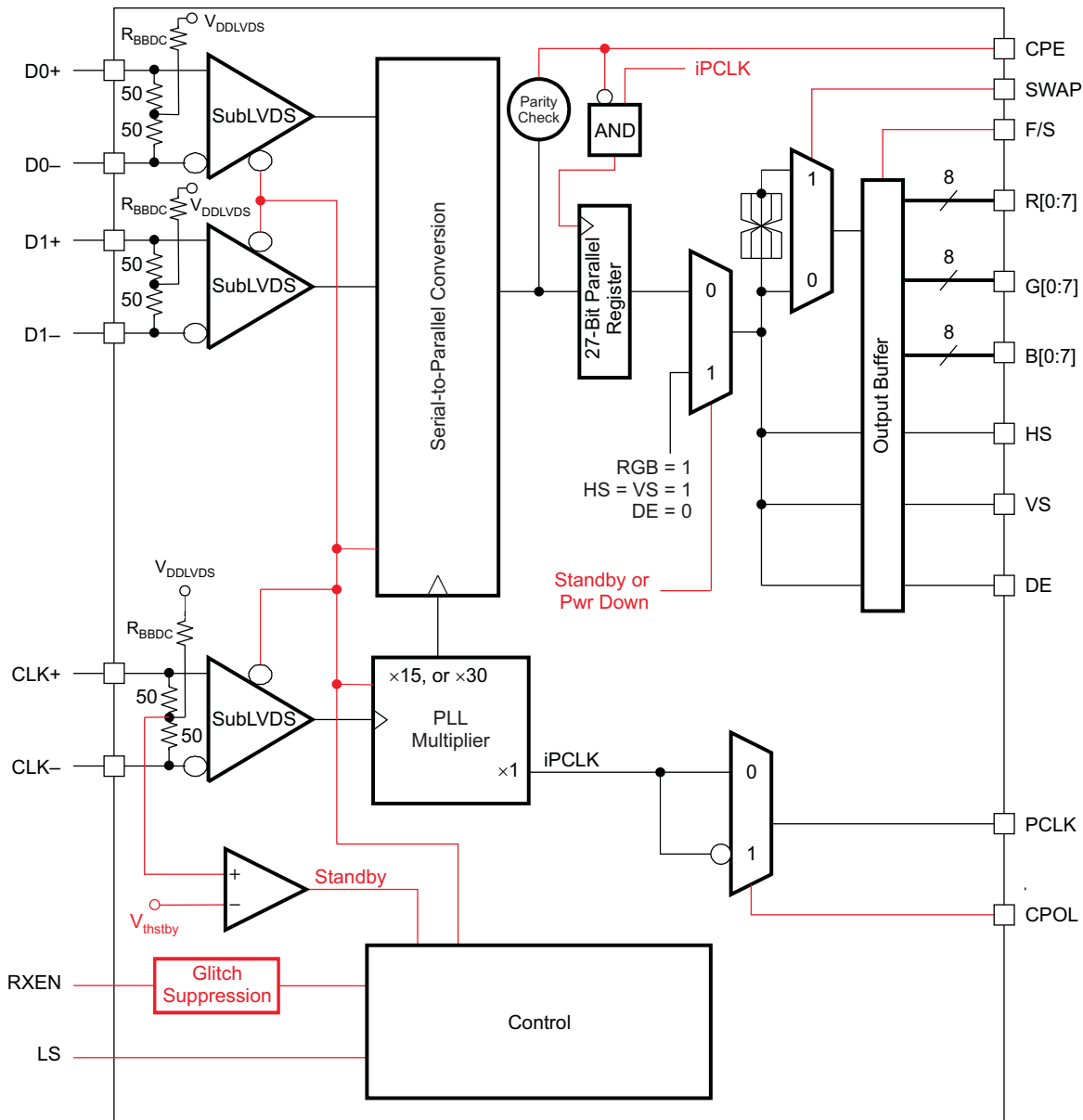


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The link select line, LS, selects whether 1 or 2 serial links are used. The RXEN input can be used to put the SN65LVDS304 in a shutdown mode. The SN65LVDS304 enters an active standby mode if the common mode voltage of the CLK input becomes shifted to V_{DDLVDs} (e.g., transmitter releases CLK output into high-impedance). This minimizes power consumption without the need of switching an external control pin. The SN65LVDS304 is characterized for operation over ambient air temperatures of -40°C to 85°C . All CMOS and SubLVDS signals are 2-V tolerant with $V_{DD} = 0\text{ V}$. This feature allows signal powerup before V_{CC} is stabilized.

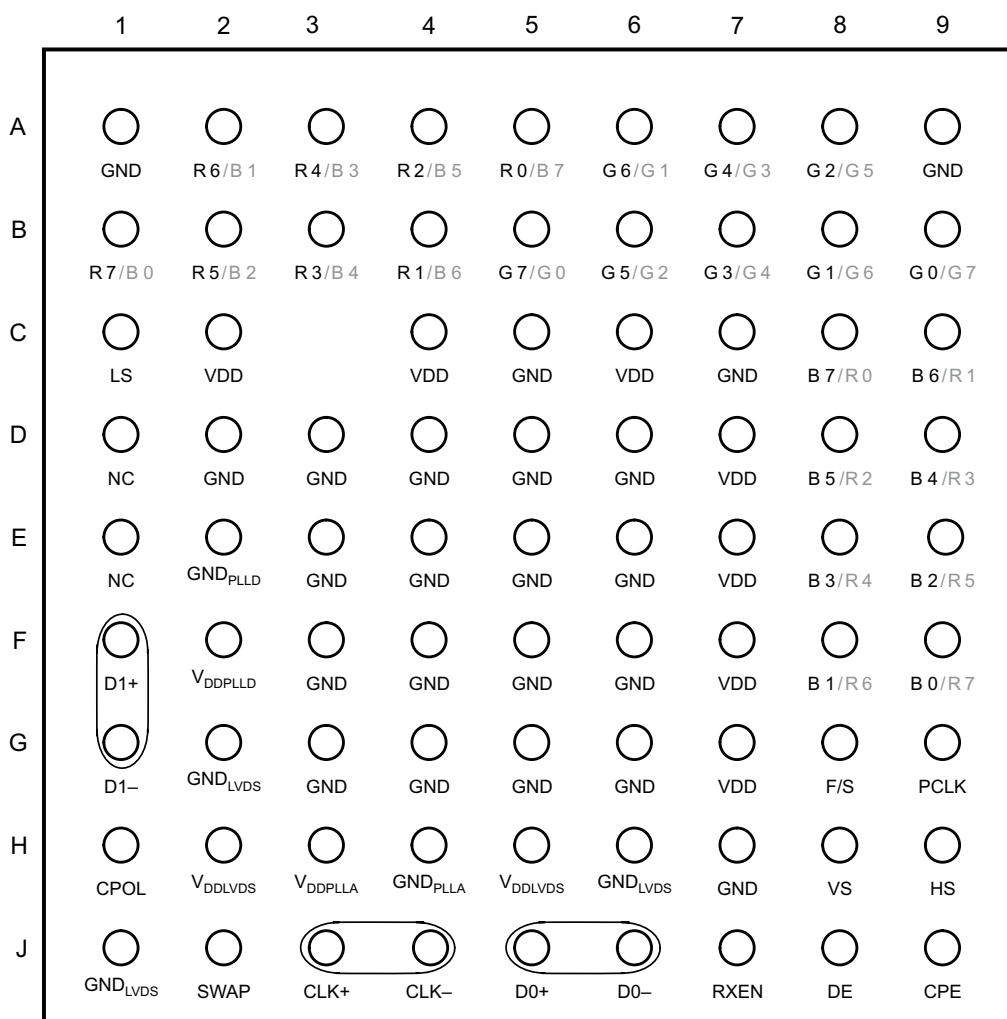
FUNCTIONAL BLOCK DIAGRAM



B0177-01

PINOUT – TOP VIEW

ZQE PACKAGE
(TOP VIEW)



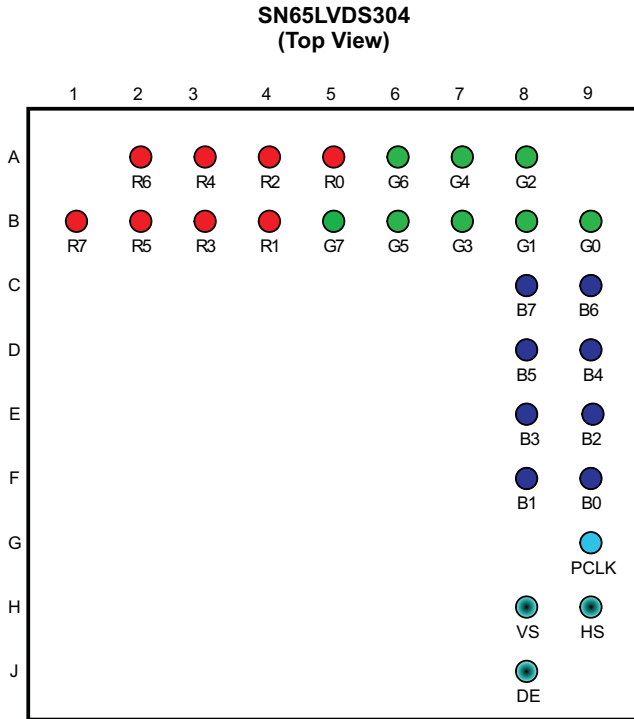
RGB Output pin assignment based on SWAP pin setting:
SWAP = 0 / SWAP = 1

P0049-01

PINOUT – TOP VIEW (continued)

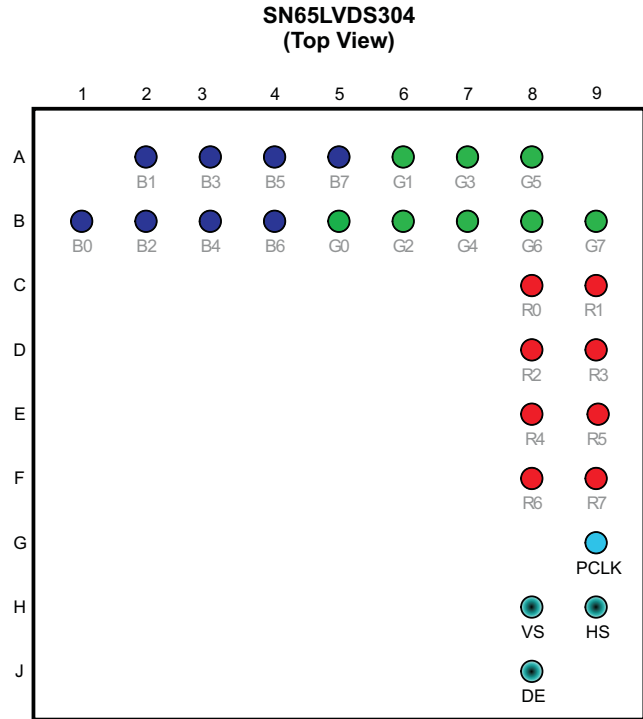
SWAP PIN FUNCTIONALITY

The SWAP pin allows the pcb designer to reverse the RGB bus, minimizing potential signal crossovers due to signal routing. The two drawings beneath show the RGB signal pin assignment based on the SWAP-pin setting.



P0049-02

Figure 1. Pinout With SWAP PIN = GND



P0049-03

Figure 2. Pinout With SWAP PIN = V_{DD}

PINOUT – TOP VIEW (continued)

Table 1. Pin Description

| PIN | SWAP | SIGNAL | PIN | SWAP | SIGNAL | PIN | SWAP | SIGNAL |
|-----|------|--------|-----|-------------|----------------------|-----|------|----------------------|
| A1 | – | GND | C1 | – | LS | F1 | – | D1+ |
| A2 | L | R6 | C2 | – | V _{DD} | F2 | – | V _{DDPLL} D |
| | H | B1 | C3 | unpopulated | | F3 | – | GND |
| A3 | L | R4 | C4 | – | V _{DD} | F4 | – | GND |
| | H | B3 | C5 | – | GND | F5 | – | GND |
| A4 | L | R2 | C6 | – | V _{DD} | F6 | – | GND |
| | H | B5 | C7 | – | GND | F7 | – | V _{DD} |
| A5 | L | R0 | C8 | L | B7 | F8 | L | B1 |
| | H | B7 | | H | R0 | | H | R6 |
| A6 | L | G6 | C9 | L | B6 | F9 | L | B0 |
| | H | G1 | | H | R1 | | H | R7 |
| A7 | L | G4 | D1 | – | NC | G1 | – | D1– |
| | H | G3 | D2 | – | GND | G2 | – | GND _{LVDS} |
| A8 | L | G2 | D3 | – | GND | G3 | – | GND |
| | H | G5 | D4 | – | GND | G4 | – | GND |
| A9 | – | GND | D5 | – | GND | G5 | – | GND |
| B1 | L | R7 | D6 | – | GND | G6 | – | GND |
| | H | B0 | D7 | – | V _{DD} | G7 | – | V _{DD} |
| B2 | L | R5 | D8 | L | B5 | G8 | – | F/S |
| | H | B2 | | H | R2 | G9 | – | PCLK |
| B3 | L | R3 | D9 | L | B4 | H1 | – | CPOL |
| | H | B4 | | H | R3 | H2 | – | V _{DDL} VDS |
| B4 | L | R1 | E1 | – | NC | H3 | – | V _{DD} PLLA |
| | H | B6 | E2 | – | GND _{PLL} D | H4 | – | GND _{PLLA} |
| B5 | L | G7 | E3 | – | GND | H5 | – | V _{DDL} VDS |
| | H | G0 | E4 | – | GND | H6 | – | GND _{LVDS} |
| B6 | L | G5 | E5 | – | GND | H7 | – | GND |
| | H | G2 | E6 | – | GND | H8 | – | VS |
| B7 | L | G3 | E7 | – | V _{DD} | H9 | – | HS |
| | H | G4 | E8 | L | B3 | J1 | – | GND _{LVDS} |
| L | G1 | H | | R4 | J2 | – | SWAP | |
| B8 | H | G6 | E9 | L | B2 | J3 | – | CLK+ |
| | L | G0 | | H | R5 | J4 | – | CLK– |
| B9 | L | G0 | | | | J5 | – | D0+ |
| | H | G7 | | | | J6 | – | D0– |
| | | | | | | J7 | – | RXEN |
| | | | | | | J8 | – | DE |
| | | | | | | J9 | – | CPE |

Table 2. TERMINAL FUNCTIONS

| NAME | I/O | DESCRIPTION |
|----------------------|--------------|---|
| D0+, D0– | SubLVDS in | SubLVDS data link (active during normal operation) |
| D1+, D1– | | SubLVDS data link (active during normal operation when LS = high, high-impedance if LS = low); input can be left open if unused. |
| CLK+, CLK– | | SubLVDS input pixel clock; polarity is fixed. |
| R0–R7 | CMOS out | Red-pixel data (8); pin assignment depends on SWAP pin setting. |
| G0–G7 | | Green-pixel data (8); pin assignment depends on SWAP pin setting. |
| B0–B7 | | Blue-pixel data (8); pin assignment depends on SWAP pin setting. |
| HS | | Horizontal sync |
| VS | | Vertical sync |
| DE | | Data enable |
| PCLK | | Output pixel clock; rising or falling clock polarity is selected by control input CPOL. |
| LS | | Link select (determines active SubLVDS data links and PLL range); see Table 3 . |
| RXEN | CMOS In | Disables the CMOS Drivers and Turns Off the PLL, putting device in shutdown mode 1 – Receiver enabled 0 – Receiver disabled (shutdown) Note: The RXEN input incorporates glitch suppression logic to avoid unwanted switching. The input must be pulled low for longer than 10 μ s continuously to force the receiver to enter shutdown. The input must be pulled high for at least 10 μ s continuously to activate the receiver. An input pulse shorter than 5 μ s is interpreted as a glitch and becomes ignored. At power up, the receiver is enabled immediately if RXEN = H and disabled if RXEN = L. |
| CPOL | | Output clock polarity selection 0 – rising edge clocking 1 – falling edge clocking |
| SWAP | | Bus swap swaps the bus pins to allow device placement on top or bottom of PCB. See pinout drawing for pin assignments. 0 – data output from R7...B0 1 – data output from B0...R7 |
| F/S | | CMOS bus rise time select 1 – fast-output rise time 0 – slow-output rise time |
| CPE | CMOS out | Channel parity error This output indicates the detection of a parity error by generating an output high-pulse for half of a PCLK clock cycle; this allows counting parity errors with a simple counter. 0 – no error high-pulse – bit error detected |
| V _{DD} | Power supply | Supply voltage |
| GND | | Supply ground |
| V _{DDL} VDS | | SubLVDS I/O supply voltage |
| GND _{LVDS} | | SubLVDS ground |
| V _{DD} PLLA | | PLL analog supply voltage |
| GND _{PLLA} | | PLL analog GND |
| V _{DD} PLLD | | PLL digital supply voltage |
| GND _{PLLD} | | PLL digital GND |

FUNCTIONAL DESCRIPTION

Deserialization Modes

The SN65LVDS304 receiver has two modes of operation controlled by link-select pin LS. Table 3 shows the deserializer modes of operation.

Table 3. Logic Table: Link Select Operating Modes

| LS | MODE OF OPERATION | | DATA LINKS STATUS |
|----|-------------------|--|-------------------|
| 0 | 1ChM | 1-channel mode (30-bit serialization rate) | D0 active |
| 1 | 2ChM | 2-channel mode (15-bit serialization rate) | D0, D1 active |

1-Channel Mode

While LS is held low, the SN65LVDS304 receives payload data over a single SubLVDS data pair, D0. The PLL locks to the SubLVDS clock input and internally multiplies the clock by a factor of 30. The internal high-speed clock is used to shift in the data payload on D0 and to deserialize 30 bits of data. Figure 3 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 30 to recreate the pixel clock, and the data payload with the pixel clock is presented on the output bus. The reserved bits and parity bit are not output. While in this mode, the PLL can lock to a clock that is in the range of 4 MHz through 15 MHz. This mode is intended for smaller video display formats that do not need the full bandwidth capabilities of the SN65LVDS304.

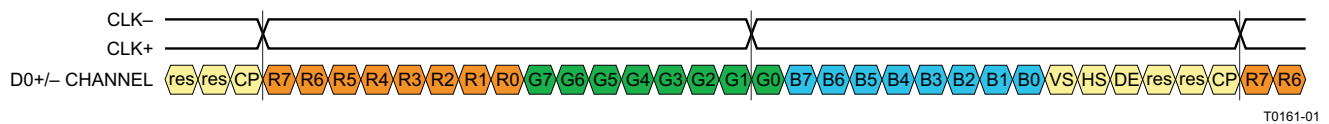


Figure 3. Data and Clock Input in 1-ChM (LS = low)

2-Channel Mode

While LS is held high, the SN65LVDS304 receives payload data over two SubLVDS data pairs, D0 and D1. The PLL locks to the SubLVDS clock input and internally multiplies the clock by a factor of 15. The internal high-speed clock is used to shift in the data payload on D0 and D1 and to deserialize 15 bits of data from each pair. Figure 4 illustrates the timing and the mapping of the data payload into the 30-bit frame. The internal high-speed clock is divided by a factor of 15 to recreate the pixel clock, and the data payload with pixel clock is presented on the output bus. The reserved bits and parity bit are not output. While in this mode, the PLL can lock to a clock that is in the range of 8 MHz through 30 MHz.

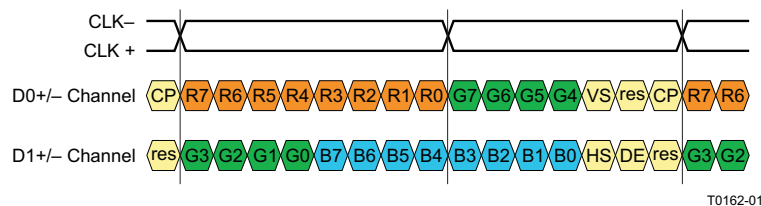


Figure 4. Data and Clock Input in 2-ChM (LS = high)

POWER-DOWN MODES

The SN65LVDS304 receiver has two power-down modes to facilitate efficient power management.

SHUTDOWN MODE

A low input signal on the RXEN pin puts the SN65LVDS304 into shutdown mode. This turns off most of the receiver circuitry including the SubLVDS receivers, PLL, and deserializers. The SubLVDS differential-input resistance remains 100 Ω, and any input signal is ignored. All outputs hold a static output pattern:

$$R[0:7] = G[0:7] = B[0:7] = VS = HS = \text{high}; DE = PCLK = \text{low}.$$

The current draw in shutdown mode is nearly zero if the SubLVDS inputs are left open or pulled high.

STANDBY MODE

The SN65LVDS304 enters the standby mode when the SN65LVDS304 is not in shutdown mode but the SubLVDS clock-input common-mode voltage is above $0.9 \times V_{DDLVDs}$. The CLK input incorporates a pullup circuit to shift the SubLVDS clock-input common-mode voltage to V_{DDLVDs} in the absence of an input signal. All circuitry except the SubLVDS clock-input standby monitor is shut down. The SN65LVDS304 also enters the standby mode when the input clock frequency on the CLK input is less than 500 kHz. The SubLVDS input resistance remains 100 Ω , and any input signal on the data inputs D0 and D1 is ignored. All outputs will hold a static output pattern:

$R[0:7] = G[0:7] = B[0:7] = VS = HS = \text{high}; DE = PCLK = \text{low}.$

The current drawn in standby mode is very low.

ACTIVE MODES

A high input signal on RXEN combined with a CLK input signal switching faster than 3 MHz and V_{ICM} smaller than 1.3 V forces the SN65LVDS304 into the active mode. Current consumption in the active mode depends on operating frequency and the number of data transitions in the data payload. CLK-input frequencies between 3 MHz and 4 MHz activate the device, but proper PLL functionality is not assured. It is not recommended to operate the SN65LVDS304 in active mode at CLK frequencies below 4 MHz.

ACQUIRE MODE (PLL Approaches Lock)

When the SN65LVDS304 is enabled and a SubLVDS clock input present, the PLL pursues lock to the input clock. While the PLL pursues lock, the output data bus holds a static output pattern:

$R[0:7] = G[0:7] = B[0:7] = VS = HS = \text{high}; DE = PCLK = \text{low}.$

For proper device operation, the pixel clock frequency must fall within the valid f_{PCLK} range specified under recommended operating conditions. If the pixel clock frequency is larger than 3 MHz but smaller than $f_{PCLK(\text{min})}$, the SN65LVDS304 PLL is enabled. Under such conditions, it is possible for the PLL to lock temporarily to the pixel clock, causing the PLL monitor to release the device into active receive mode. If this happens, the PLL may or may not be properly locked to the pixel clock input, potentially causing data errors, frequency oscillation, and PLL deadlock (loss of VCO oscillation).

RECEIVE MODE

After the PLL achieves lock the device enters the normal receive mode. The output data bus presents the deserialized data. The PCLK output pin outputs the recovered pixel clock.

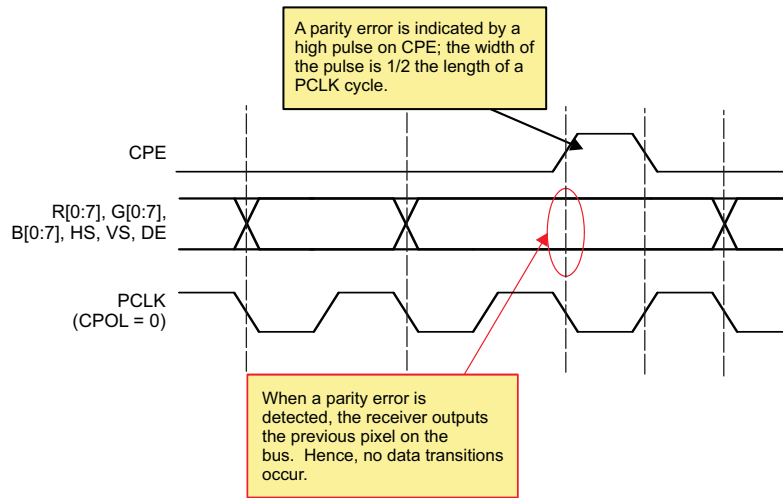
PARITY ERROR DETECTION AND HANDLING

The SN65LVDS304 receiver performs error checking on the basis of a parity bit that is transmitted across the SubLVDS interface from the transmitting device. Once the SN65LVDS304 detects the presence of the clock and the PLL has locked onto PCLK, then the parity is checked. Parity-error detection ensures detection of all single-bit errors in one pixel and 50% of all multibit errors.

The parity bit covers the 27-bit data payload consisting of 24 bits of pixel data plus VS, HS, and DE. Odd-parity bit signalling is used. The parity error is output on the CPE pin. If the sum of the 27 data bits and the parity bit result in an odd number, the receive data are assumed to be valid. The CPE output is held low. If the sum equals an even number, parity error is declared. The CPE output indicates high for half a PCLK period. The CPE output is set with the data bit transition and cleared after 1/2 the data-bit time. This allows counting every detected parity error with a simple counter connected to CPE.

If a parity error is detected, then the data on that PCLK cycle is not output. Instead, the last valid data from a previous PCLK cycle is repeated on the output bus. This is to prevent any bit error that occurs on the LVDS link from causing perturbations in VS, HS, or DE that might be visually disruptive to a display.

The reserved bits are not covered in the parity calculations.

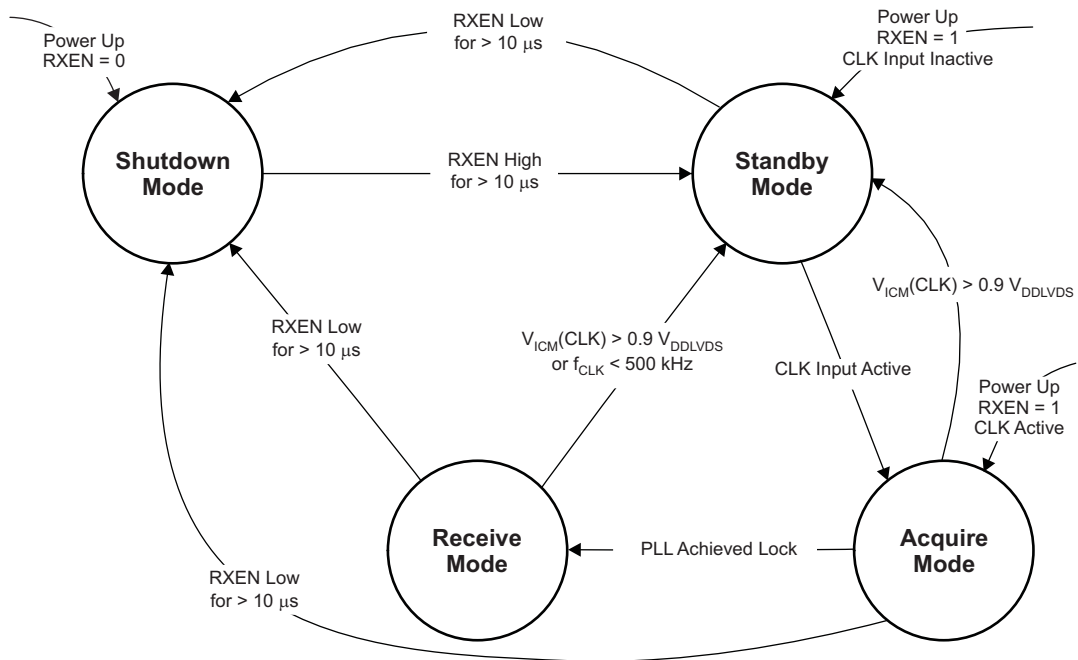


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Figure 5. Parity Error Detection

STATUS-DETECT AND OPERATING-MODES FLOW DIAGRAM

The SN65LVDS304 switches between the power saving and active modes in the following way:



F0017-01

Table 4. Status Detect and Operating Modes Descriptions

| MODE | CHARACTERISTICS | CONDITIONS |
|---------------|--|---|
| Shutdown mode | Least amount of power consumption (most circuitry turned off); all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low | RXEN is set low for longer than 10 μ s. ⁽¹⁾⁽²⁾ |
| Standby mode | Low power consumption (standby monitor circuit active; PLL is shutdown to conserve power); All outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low | RXEN is high for longer than 10 μ s and CLK inputs are common-mode, $V_{ICM(CLK)}$ is above $0.9 \times V_{DDLVDs}$, or CLK inputs are floating ⁽²⁾ |
| Acquire mode | PLL pursues lock; all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low | RXEN is high; CLK input monitor detected clock input common mode and woke up receiver from standby mode. |
| Receive mode | Data transfer (normal operation); receiver deserializes data and provides data on parallel output | RXEN is high and PLL is locked to incoming clock. |

(1) In shutdown mode, all SN65LVDS304 internal switching circuits (e.g., PLL, serializer, etc.) are turned off to minimize power consumption. The input stage of any input pin remains active.

(2) Leaving CMOS control inputs unconnected can cause random noise to toggle the input stage and potentially harm the device. All CMOS inputs must be tied to a valid logic level, V_{IL} or V_{IH} , during shutdown or standby Mode. Exceptions are the SubLVDS inputs CLK and Dx, which can be left unconnected while not in use.

Table 5. Operating Mode Transitions

| MODE TRANSITION | USE CASE | TRANSITION SPECIFICS |
|----------------------------|---|---|
| Shutdown → standby | Drive RXEN high to enable receiver. | <ol style="list-style-type: none"> 1. RXEN high > 10 μs 2. Receiver enters standby mode. <ol style="list-style-type: none"> a. R[0:7] = G[0:7] = B[0:7] = VS = HS remain high and DE = PCLK low b. Receiver activates clock input monitor. |
| Standby → acquire | Transmitter activity detected | <ol style="list-style-type: none"> 1. CLK input monitor detects clock input activity. 2. Outputs remain static. 3. PLL circuit is enabled. |
| Acquire → receive | Link is ready to receive data. | <ol style="list-style-type: none"> 1. PLL is active and approaches lock. 2. PLL achieves lock within $t_{wake-up}$. 3. Input D0 or D1 becomes active, depending on LS selection. 4. First data word is recovered. 5. Parallel output bus turns on switching from a static output pattern to output the first valid data word. |
| Receive → standby | Transmitter requested to enter standby mode by input common mode voltage $V_{ICM} > 0.9 V_{DDLVDs}$ (e.g., transmitter output clock stops or enters high-impedance state) | <ol style="list-style-type: none"> 1. Receiver disables outputs within t_{sleep}. 2. RX Input monitor detects $V_{ICM} > 0.9 V_{DDLVDs}$ within t_{sleep}. 3. R[0:7] = G[0:7] = B[0:7] = VS = HS transition to high and DE = PCLK to low on next falling PLL clock edge 4. PLL shuts down. Clock activity input monitor remains active. |
| Receive/standby → shutdown | Turn off receiver. | <ol style="list-style-type: none"> 1. RXEN pulled low for > t_{pwrdn}. 2. R[0:7] = G[0:7] = B[0:7] = VS = HS remain static high or transition to static high and DE = PCLK remain or transition to static low. 3. Most IC circuitry is shut down for least power consumption. |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | | VALUE | UNIT |
|---|--|-------------------------------|------|
| Supply voltage range, $V_{DD}^{(2)}$, V_{DDPLLA} , V_{DDPLLD} , V_{DDLVDs} | | –0.3 to 2.175 | V |
| Voltage range at any input or output terminal | When $V_{DDx} > 0$ V | –0.5 to 2.175 | V |
| | When $V_{DDx} \leq 0$ V | –0.5 to $V_{DD} + 2.175$ | |
| Electrostatic discharge | Human body model ⁽³⁾ (all pins) | ±4 | kV |
| | Charged-device model ⁽⁴⁾ (all pins) | ±1500 | V |
| | Machine model ⁽⁵⁾ (all pins) | ±200 | |
| Continuous power dissipation | | See Dissipation Ratings Table | |
| Output current, I_O | | ±5 | mA |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the GND terminals.
- (3) In accordance with JEDEC Standard 22, Test Method A114-B
- (4) In accordance with JEDEC Standard 22, Test Method C101
- (5) In accordance with JEDEC Standard 22, Test Method A115-A

DISSIPATION RATINGS

| PACKAGE | CIRCUIT BOARD MODEL | $T_A < 25^\circ\text{C}$ | DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 85^\circ\text{C}$ POWER RATING |
|---------|----------------------|--------------------------|---|---------------------------------------|
| ZQE | Low-K ⁽²⁾ | 592 mW | 7.407 mW/°C | 148 mW |

- (1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
- (2) In accordance with the low-K thermal metric definitions of EIA/JESD51-2.

DEVICE POWER DISSIPATION

| PARAMETER | TEST CONDITIONS | TYP | MAX | UNIT |
|--------------------------------|--|------|------|------|
| P_D Device power dissipation | $V_{DDx} = 1.8$ V, $T_A = 25^\circ\text{C}$, all outputs terminated with 10 pF, f_{CLK} at 4 MHz | 16.8 | | mW |
| | $V_{DDx} = 1.95$ V, $T_A = -40^\circ\text{C}$, all outputs terminated with 10 pF, f_{CLK} at 30 MHz | | 72.2 | |

RECOMMENDED OPERATING CONDITIONS⁽¹⁾

| | | | MIN | TYP | MAX | UNIT |
|--|---|---|---------------------|-----|--------------|------|
| V_{DD} V_{DDPLLA} V_{DDPLLD} V_{DDLVDs} | Supply voltages | | 1.65 | 1.8 | 1.95 | V |
| $V_{DDn(PP)}$ | Supply voltage noise magnitude | Test set-up shown in Figure 7 ; $f_{CLK} \leq 50\text{MHz}$; $f(\text{noise}) = 1\text{Hz to } 2\text{GHz}$ | | | 100 | mV |
| | | $f_{CLK} > 50\text{MHz}$; $f(\text{noise}) = 1\text{Hz to } 1\text{MHz}$ | | | 100 | |
| | | $f_{CLK} > 50\text{MHz}$; $f(\text{noise}) > 1\text{MHz}$ | | | 40 | |
| T_A | Operating free-air temperature | | -40 | | 85 | °C |
| CLK+ and CLK- | | | | | | |
| $f_{CLK\pm}$ | Input pixel clock frequency | 1-channel transmit mode, see Figure 3 | 4 | | 15 | MHz |
| | | 2-channel transmit mode, see Figure 4 | 8 | | 30 | |
| | | Standby mode ⁽²⁾ , see Figure 16 | | | 500 | kHz |
| t_{DUTCLK} | CLK input duty cycle | | 35 | | 65 | % |
| D0+, D0-, D1+, D1-, CLK+, and CLK- | | | | | | |
| $ V_{ID} $ | Magnitude of differential input voltage | $ V_{D0+} - V_{D0-} $, $ V_{D1+} - V_{D1-} $, $ V_{CLK+} - V_{CLK-} $ during normal operation | 70 | | 200 | mV |
| V_{ICM} | Input voltage common mode range | Receive or acquire mode | 0.6 | | 1.2 | V |
| | | Standby mode | 0.9 V_{DDLVDs} | | | |
| ΔV_{ICM} | Input voltage common mode variation among all SubLVDS inputs | $V_{ICM(n)} - V_{ICM(m)}$ with $n = D0, D1$, or CLK and $m = D0, D1$, or CLK | -100 | | 100 | mV |
| ΔV_{ID} | Differential input voltage amplitude variation among all SubLVDS inputs | $V_{ID(n)} - V_{ID(m)}$ with $n = D0, D1$, or CLK and $m = D0, D1$, or CLK | -10 | | 10 | % |
| $t_{r/f}$ | Input rise and fall times | RXEN at V_{DD} ; see Figure 10 | | | 800 | ps |
| $\Delta t_{r/f}$ | Input rise or fall time mismatch among all SubLVDS inputs | $t_{r(n)} - t_{r(m)}$ and $t_{f(n)} - t_{f(m)}$ with $n = D0, D1$, or CLK and $m = D0, D1$, or CLK | -100 | | 100 | ps |
| LS, CPOL, SWAP, RXEN, F/S | | | | | | |
| V_{ICMOSH} | High-level input voltage | | 0.7 V_{DD} | | V_{DD} | V |
| V_{ICMOSL} | Low-level input voltage | | 0 | | 0.3 V_{DD} | V |
| t_{inRXEN} | RXEN input pulse duration | | 10 | | | µs |
| R[7:0], G[7:0], B[7:0], VS, HS, PCLK, CPE | | | | | | |
| C_L | Output load capacitance | | | 10 | | pF |

(1) Unused single-ended inputs must be held high or low to prevent them from floating.

(2) PCLK input frequencies lower than 500 kHz force the SN65LVDS304 into standby mode. Input frequencies between 500 kHz and 3 MHz may or may not activate the SN65LVDS304. Input frequencies beyond 3 MHz activate the SN65LVDS304. Input frequencies between 500 kHz and 4 MHz are not recommended, and can cause PLL malfunction.

DEVICE ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|---------------------------------------|--|--|---------------------------|------|------|
| I _{DD} RMS supply current | 1ChM | Alternating 1010 test pattern (see Table 9); all CMOS outputs terminated with 10 pF; F/S and RXEN at V _{DD} ; V _{IH} = V _{DD} , V _{IL} = 0 V; V _{DD} = V _{DDPLL} = V _{DDPLL} = V _{DDLVD} | f _{PCLK} = 4 MHz | 9.8 | 14 | mA |
| | | | f _{PCLK} = 6 MHz | 11.7 | 15.9 | |
| | | | f _{PCLK} = 15 MHz | 19.3 | 25 | |
| | 1ChM | Typical power test pattern (see Table 7); V _{ID} = 70 mV, all CMOS outputs terminated with 10 pF; F/S and RXEN at V _{DD} ; V _{IH} = V _{DD} , V _{IL} = 0 V; V _{DD} = V _{DDPLL} = V _{DDPLL} = V _{DDLVD} | f _{PCLK} = 4 MHz | 4.7 | | mA |
| | | | f _{PCLK} = 6 MHz | 6 | | |
| | | | f _{PCLK} = 15 MHz | 13.2 | | |
| | 2ChM | Alternating 1010 test pattern (see Table 9); all CMOS outputs terminated with 10 pF; F/S and RXEN at V _{DD} ; V _{IH} = V _{DD} , V _{IL} = 0 V; V _{DD} = V _{DDPLL} = V _{DDPLL} = V _{DDLVD} | f _{PCLK} = 8 MHz | 14.3 | 19.4 | mA |
| | | | f _{PCLK} = 22 MHz | 25 | 33 | |
| | | | f _{PCLK} = 30 MHz | 26.8 | 37 | |
| | | 2ChM | Typical power test pattern (see Table 8); V _{ID} = 70 mV, all CMOS outputs terminated with 10 pF; F/S and RXEN at V _{DD} ; V _{IH} = V _{DD} , V _{IL} = 0 V; V _{DD} = V _{DDPLL} = V _{DDPLL} = V _{DDLVD} | f _{PCLK} = 8 MHz | 6.4 | |
| f _{PCLK} = 22 MHz | | | | 13.7 | | |
| f _{PCLK} = 30 MHz | | | | 18.3 | | |
| CLK and D inputs are left open; all control inputs held static high or low; All CMOS outputs terminated with 10 pF; V _{IH} = V _{DD} , V _{IL} = 0 V; V _{DD} = V _{DDPLL} = V _{DDPLL} = V _{DDLVD} | Standby mode; RXEN = V _{IH} | 15 | 100 | μA | | |
| | Shutdown mode; RXEN = V _{IL} | 0.4 | 10 | | | |

(1) All typical values are at 25°C and with 1.8-V supply, unless otherwise noted.

INPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|---|---|---|--------------|--------------------|------------------|------------|
| D0+, D0-, D1+, D1-, CLK+, and CLK- | | | | | | |
| V_{thstby} | Input voltage common mode threshold to switch between receive/acquire mode and standby mode | RXEN at V_{DD} | 1.3 | | $0.9 V_{DDLVDs}$ | V |
| V_{THL} | Low-level differential input voltage threshold | $V_{D0+} - V_{D0-}$, $V_{D1+} - V_{D1-}$, $V_{CLK+} - V_{CLK-}$ | -40 | | | mV |
| V_{THH} | High-level differential input voltage threshold | | | | 40 | mV |
| I_{I+} , I_{I-} | Input leakage current | $V_{DD} = 1.95$ V; $V_{I+} = V_{I-}$; $V_I = 0.4$ V and $V_I = 1.5$ V | | | 75 | μ A |
| I_{IOFF} | Power-off input current | $V_{DD} = GND$; $V_I = 1.5$ V | | | -75 | μ A |
| R_{ID} | Differential input termination resistor value | | 78 | 100 | 122 | Ω |
| C_{IN} | Input capacitance | Measured between input terminal and GND | | 1 | | pF |
| ΔC_{IN} | Input capacitance variation | Within one signal pair Between all signals | | | 0.2 1 | pF |
| R_{BBDC} | Pullup resistor for standby detection | | 21 | 30 | 39 | k Ω |
| LS, CPOL, SWAP, RXEN, F/S | | | | | | |
| V_{IK} | Input clamp voltage | $I_I = -18$ mA, $V_{DD} = V_{DD}(\min)$ | | | -1.2 | V |
| I_{CMOS} | Input current ⁽²⁾ | 0 V $\leq V_{DD} \leq 1.95$ V; $V_I = GND$ or $V_I = 1.95$ V | | | 100 | nA |
| C_{IN} | Input capacitance | | | 2 | | pF |
| I_{IH} | High-level input current | $V_{IN} = 0.7 V_{DD}$ | -200 | | 200 | nA |
| I_{IL} | Low-level input current | $V_{IN} = 0.3 V_{DD}$ | -200 | | 200 | nA |
| V_{IH} | High-level input voltage | | $0.7 V_{DD}$ | | V_{DD} | V |
| V_{IL} | Low-level input voltage | | 0 | | $0.3 V_{DD}$ | V |

(1) All typical values are at 25°C and with 1.8-V supply unless otherwise noted.

(2) Do not leave any CMOS input unconnected or floating to minimize leakage currents. Every input must be connected to a valid logic level, V_{IH} or V_{OL} , while power is supplied to V_{DD} .

OUTPUT ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---------------------------|---|--------------|-----|--------------|---------|
| R[0:7], G[0:7], B[0:7], VS, HS, PCLK, CPE | | | | | | |
| V_{OH} | High-level output current | 1-ChM, F/S = L, $I_{OH} = -250$ μ A | $0.8 V_{DD}$ | | V_{DD} | V |
| | | 2-ChM, F/S = L, $I_{OH} = -500$ μ A | | | | |
| | | 1-ChM, F/S = H, $I_{OH} = -500$ μ A | | | | |
| | | 2-ChM, F/S = H, $I_{OH} = -2$ mA | | | | |
| V_{OL} | Low-level output current | 1-ChM, F/S = L, $I_{OL} = 250$ μ A | 0 | | $0.2 V_{DD}$ | V |
| | | 2-ChM, F/S = L, $I_{OL} = 500$ μ A | | | | |
| | | 1-ChM, F/S = H, $I_{OL} = 500$ μ A | | | | |
| | | 2-ChM, F/S = H, $I_{OL} = 2$ mA | | | | |
| I_{OH} | High-level output current | 1-ChM, F/S = L | | | | μ A |
| | | 2-ChM, F/S = L; 1-ChM, F/S = H | | | | |
| | | 2-ChM, F/S = H | | | | |
| I_{OL} | Low-level output current | 1-ChM, F/S = L | | | | μ A |
| | | 2-ChM, F/S = L; 1-ChM, F/S = H | | | | |
| | | 2-ChM, F/S = H | | | | |

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | | | |
|--|--|--|-------------------------|-----|------------------|----------------|----------------|---------|
| D0+, D0–, D1+, D1–, CLK+, and CLK– | | | | | | | | |
| $t_{r/f}$ | Input rise and fall times | RXEN at V_{DD} ; see Figure 10 | | | 800 | ps | | |
| $\Delta t_{r/f}$ | Input rise or fall time mismatch between all SubLVDS inputs | $t_{R(n)} - t_{R(m)}$ and $t_{F(n)} - t_{F(m)}$ with $n = D0, D1$ or CLK and $m = D0, D1$, or CLK | | | –100 | 100 | ps | |
| R[7:0], G[7:0], B[7:0], VS, HS, PCLK, CPE | | | | | | | | |
| $t_{r/f}$ | Rise and fall time 20% \leftrightarrow 80% of V_{DD} ⁽²⁾ | $C_L = 10$ pF ⁽³⁾ ; see Figure 9 | 1-channel mode, F/S = L | 8 | 16 | ns | | |
| | | | 2-channel mode, F/S = L | 4 | 8 | | | |
| | | | 1-channel mode, F/S = H | 4 | 8 | | | |
| | | | 2-channel mode, F/S = H | 1 | 2 | | | |
| t_{OUTP} | PCLK output duty cycle | 1-channel mode | 45% | 50% | 55% | | | |
| | | CPOL = V_{IL} , 2-channel mode | 48% | 53% | 59% | | | |
| | | CPOL = V_{IH} , 2-channel mode | 41% | 47% | 52% | | | |
| t_{OSK} | Output skew between PCLK and R[0:7], G[0:7], B[0:7], HS, VS, and DE | See Figure 9. | | | –500 | 500 | ps | |
| INPUT TO OUTPUT RESPONSE TIME | | | | | | | | |
| $t_{PD(L)}$ | Propagation delay time from CLK+ input to PCLK output | RXEN at V_{DD} , $V_{IH} = V_{DD}$, $V_{IL} = GND$, $C_L = 10$ pF, See Figure 14 | | | $1.4/f_{PCLK}$ | $1.9/f_{PCLK}$ | $2.5/f_{PCLK}$ | s |
| t_{GS} | RXEN glitch suppression pulse width ⁽⁴⁾ | $V_{IH} = V_{DD}$, $V_{IL} = GND$, RXEN toggles between V_{IL} and V_{IH} ; see Figure 15 and Figure 16. | | | 3.8 | | | μ s |
| t_{pwrap} | Enable time from power down (\uparrow RXEN) | Time from RXEN pulled high to data outputs enabled and transmit valid data; see Figure 16. | | | 2 | | | ms |
| t_{pwrdn} | Disable time from active mode (\downarrow RXEN) | RXEN is pulled low during receive mode; time measurement until all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high, DE = PCLK = low and PLL is shut down; see Figure 16. | | | 11 | | | μ s |
| t_{wakeup} | Enable time from standby (\uparrow CLK) | RXEN at V_{DD} ; device is in standby; time measurement from CLK input starts switching to PCLK and data outputs enabled and transmit valid data; see Figure 17. | | | 2 | | | ms |
| t_{sleep} | Disable time from active mode (CLK transitions to high-impedance) | RXEN at V_{DD} ; device is receiving data; time measurement from CLK input signal stops (input open or input common mode V_{ICM} exceeds threshold voltage V_{thslby}) until all outputs held static: R[0:7] = G[0:7] = B[0:7] = VS = HS = high; DE = PCLK = low and PLL is shut down; see Figure 17. | | | 3 | | | μ s |
| f_{BW} | PLL bandwidth ⁽⁵⁾ | Tested from CLK input to PCLK output; 2-ChM; $f_{PCLK} = 22$ MHz | | | $0.087 f_{PCLK}$ | | | MHz |

- (1) All typical values are at 25°C and with 1.8-V supply, unless otherwise noted.
- (2) $t_{R/F}$ depends on the F/S setting and the capacitive load connected to each output. Some application information of how to calculate $t_{R/F}$ based on the output load and how to estimate the timing budget to interconnect to an LCD driver are provided in the application section near the end of this data sheet.
- (3) The output rise and fall times are optimized for an output load of 10 pF. The rise and fall times can be adjusted by changing the output load capacitance.
- (4) The RXEN input incorporates glitch-suppression logic to disregard short input pulses. t_{GS} is the duration of either a high-to-low or low-to-high transition that is suppressed.
- (5) When using the SN65LVDS304 receiver in conjunction with the SN65LVDS303 transmitter in one link, the PLL bandwidth of the SN65LVDS304 receiver always exceeds the bandwidth of the SN65LVDS303 transmit PLL. This ensures stable PLL tracking under all operating conditions and maximizes the receiver skew margin.

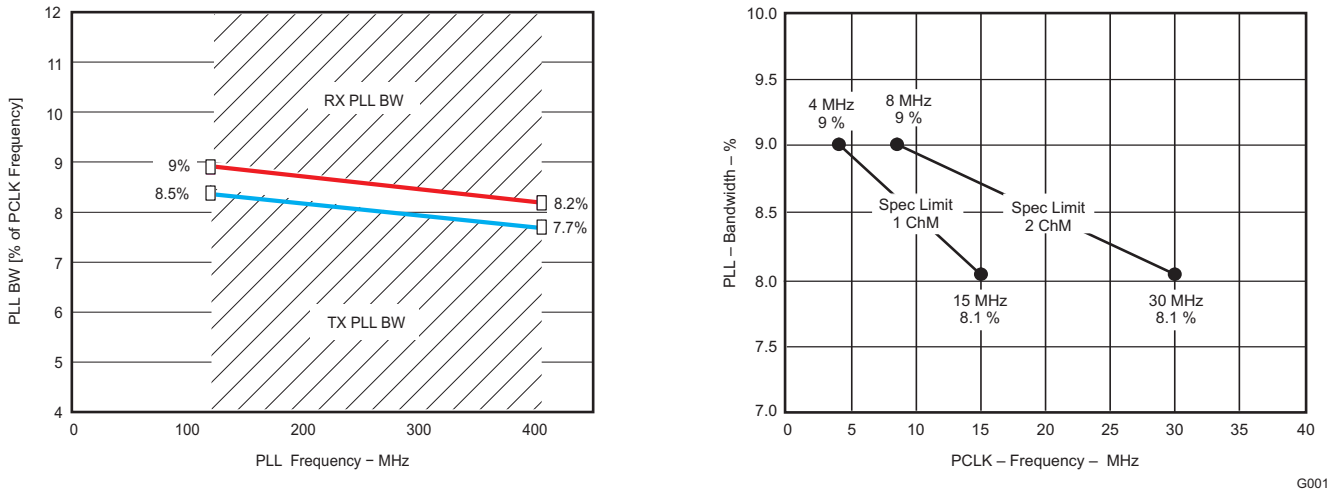


Figure 6. SN65LVDS304 PLL Bandwidth (Also Showing the SN65LVDS303 PLL Bandwidth)

TIMING CHARACTERISTICS

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|--|--|---|------|
| t_{RSKMx} (1)(2) Receiver input skew margin; see (3) and Figure 36 | 1ChM: $x = 0..29$, $f_{PCLK} = 15$ MHz; RXEN at V_{DD} , $V_{IH} = V_{DD}$, $V_{IL} = GND$, $R_L = 100 \Omega$, test setup as in Figure 8, test pattern as in Table 11 | $f_{CLK} = 15$ MHz ⁽⁴⁾ | 630 | ps |
| | | $f_{CLK} = 4$ MHz to 15 MHz ⁽⁵⁾ | $\frac{1}{2 \cdot 30 \cdot f_{CLK}} - 480$ ps | |
| | 2ChM: $x = 0..14$, $f_{PCLK} = 30$ MHz; RXEN at V_{DD} , $V_{IH} = V_{DD}$, $V_{IL} = GND$, $R_L = 100 \Omega$, test setup as in Figure 8, test pattern as in Table 12 | $f_{CLK} = 30$ MHz ⁽⁴⁾ | 630 | |
| | | $f_{CLK} = 8$ MHz to 30 MHz ⁽⁵⁾ | $\frac{1}{2 \cdot 15 \cdot f_{CLK}} - 480$ ps | |

- (1) Receiver input skew margin (t_{RSKM}) is the timing margin available for transmitter output pulse position (t_{PPoS}), interconnect skew, and interconnect inter-symbol interference. t_{RSKM} represents the remainder of the serial bit time not taken up by the receiver strobe uncertainty. t_{RSKM} assumes a bit error rate better than 10^{-12} .
- (2) t_{RSKM} is inversely proportional to the internal setup and hold time uncertainty, ISI and duty cycle distortion from the front end receiver, the skew mismatch between CLK and data D0 and D1, as well as the PLL cycle-to-cycle jitter.
- (3) This includes the receiver internal setup and hold time uncertainty, all PLL related high-frequency random and deterministic jitter components that impact the jitter budget, ISI and duty cycle distortion from the front-end receiver, and the skew between CLK and data D0 and D1; the pulse position minimum/maximum variation is given with a bit error rate target of 10^{-12} ; measurements of the total jitter are taken over $>10^{-12}$ samples.
- (4) The minimum and maximum limits are based on statistical analysis of the device performance over process, voltage, and temperature ranges.
- (5) These minimum and maximum limits are simulated only.

PARAMETER MEASUREMENT INFORMATION

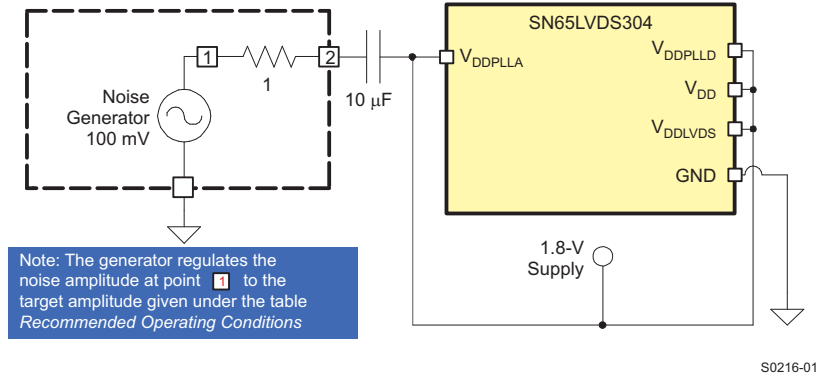


Figure 7. Power-Supply Noise Test Setup

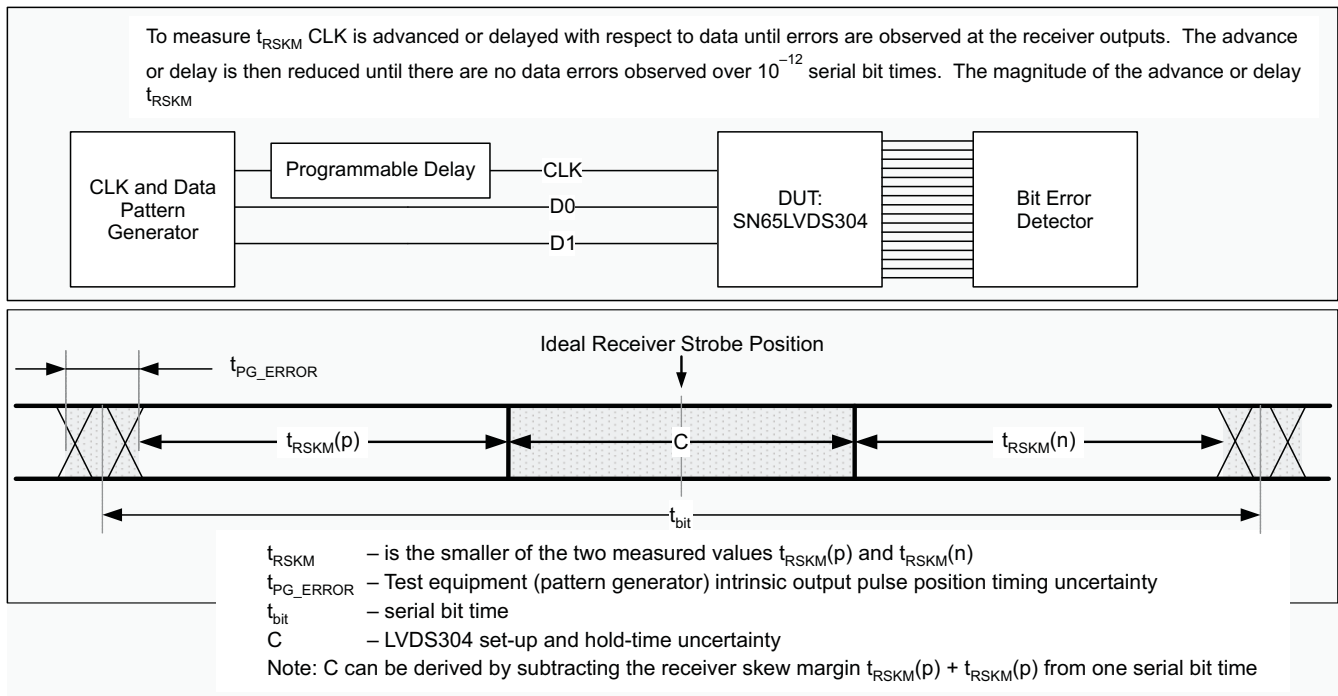


Figure 8. Receiver Jitter-Budget Test Setup

PARAMETER MEASUREMENT INFORMATION (continued)

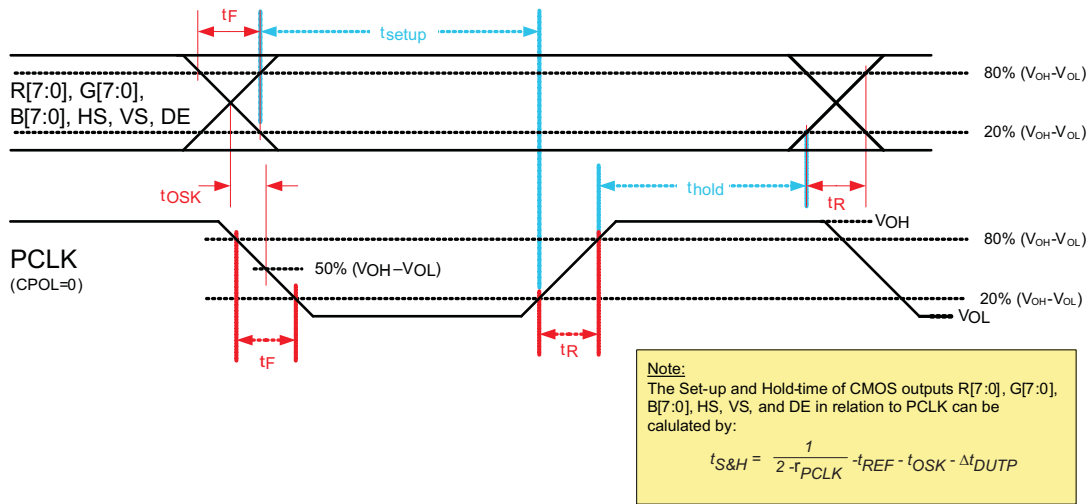


Figure 9. Output Rise/Fall, Setup/Hold Time

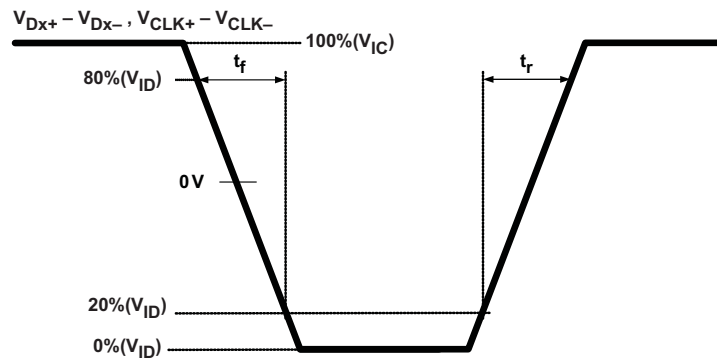
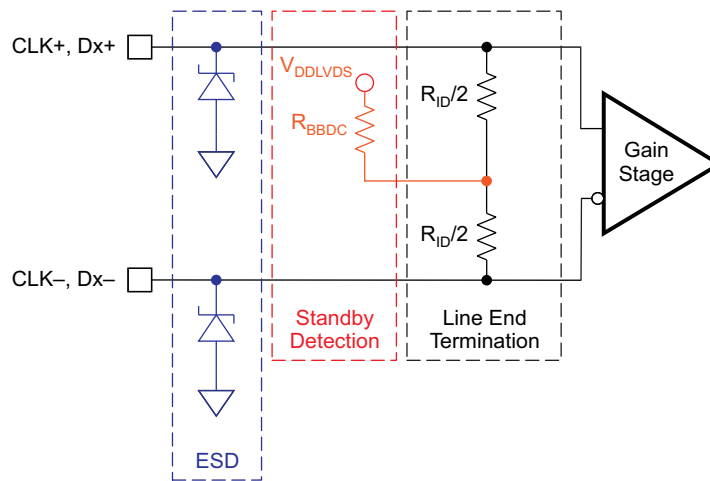


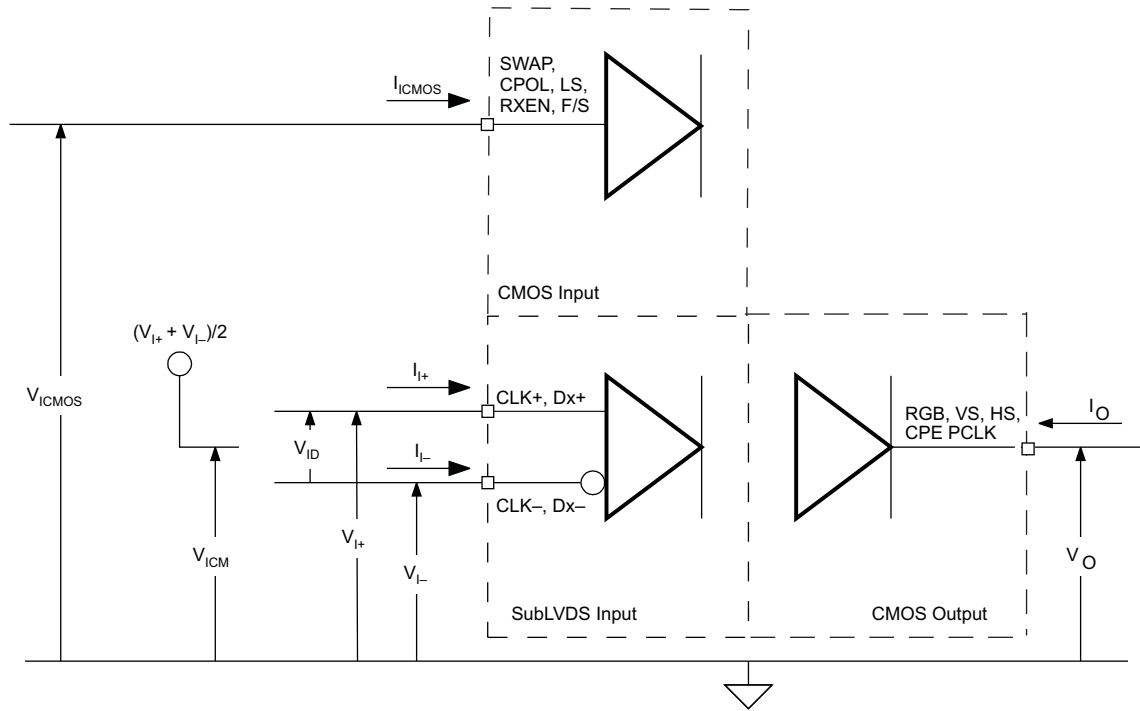
Figure 10. SubLVDS Differential Input Rise and Fall Time Definition



S0224-02

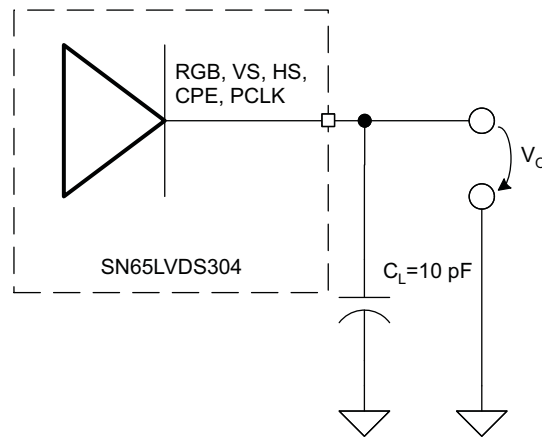
Figure 11. Equivalent Input Circuit Design

PARAMETER MEASUREMENT INFORMATION (continued)



S0217-01

Figure 12. I/O Voltage and Current Definition



S0218-01

Figure 13. CMOS Output Test Circuit, Signal, and Timing Definition

PARAMETER MEASUREMENT INFORMATION (continued)

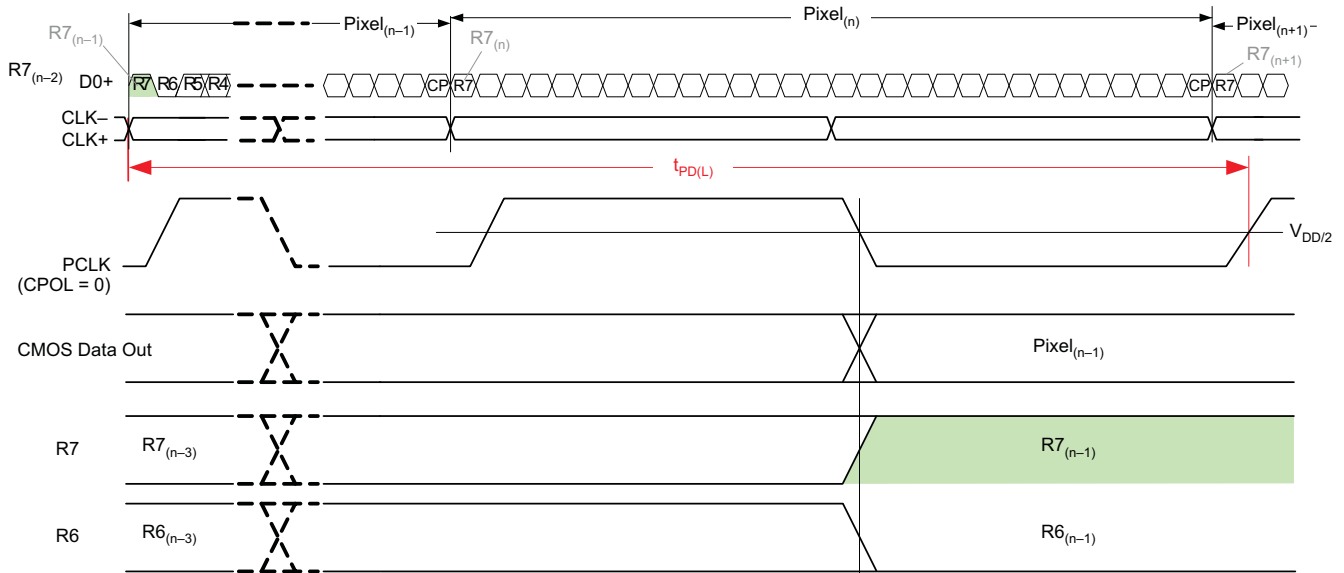


Figure 14. Propagation Delay, Input to Output (LS = 0)

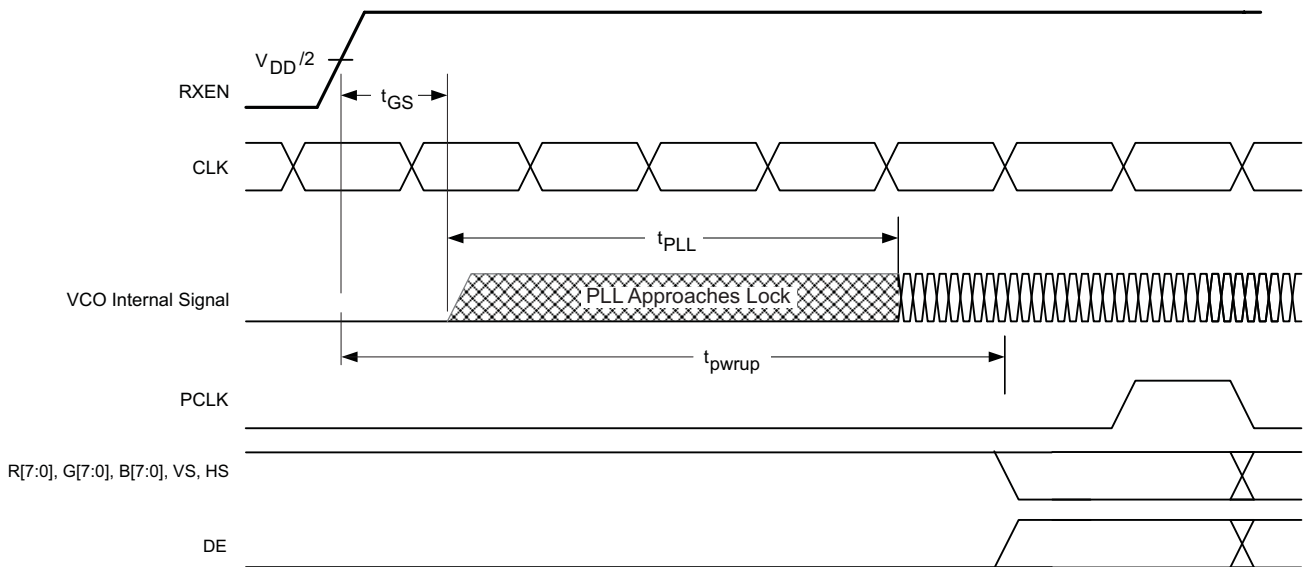


Figure 15. Receiver Phase-Locked Loop Set Time and Receiver Enable Time

PARAMETER MEASUREMENT INFORMATION (continued)

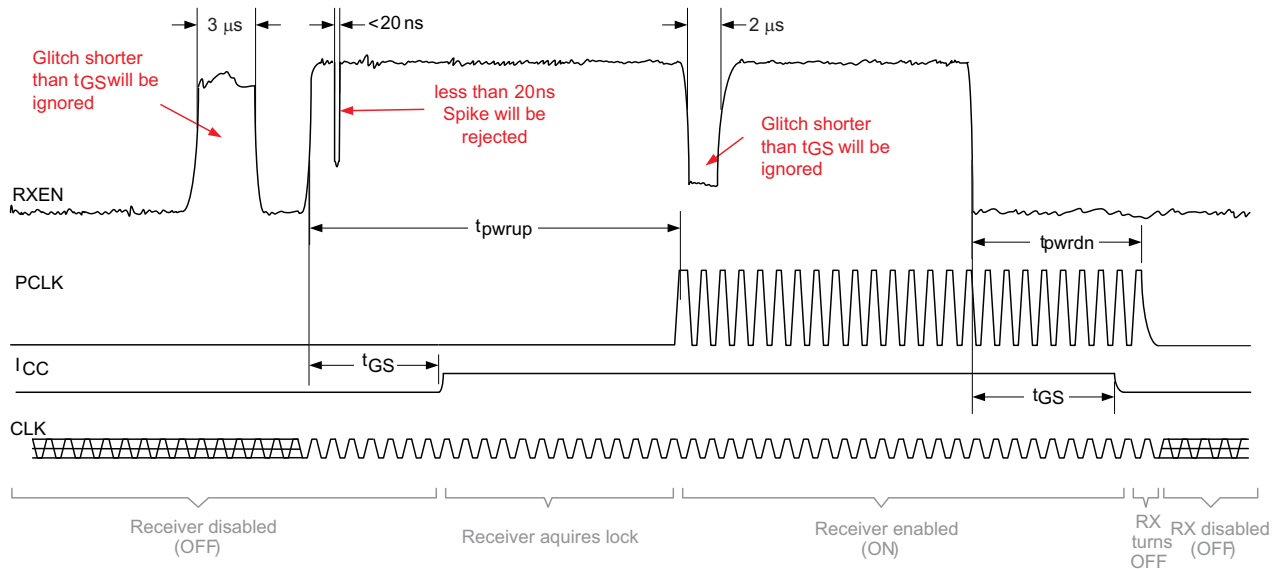


Figure 16. Receiver Enable/Disable Glitch Suppression Time

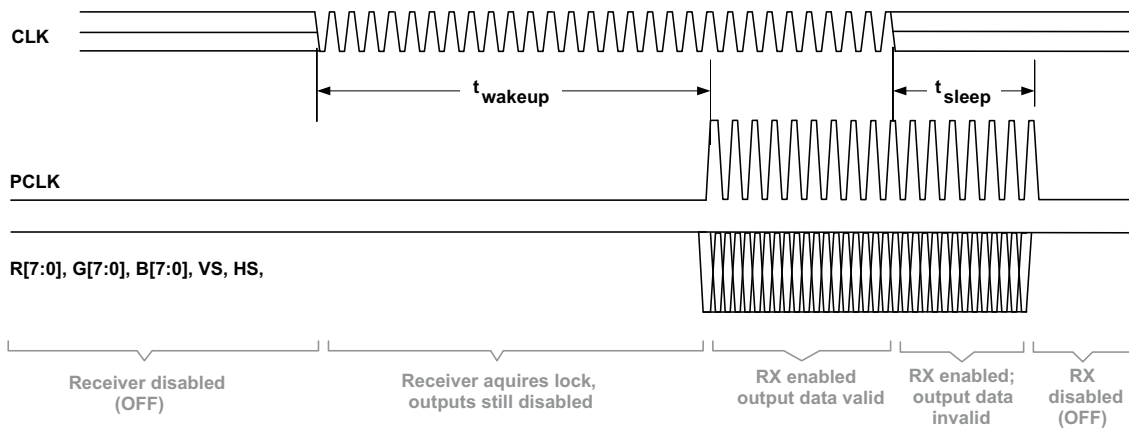


Figure 17. Standby Detection

POWER CONSUMPTION TESTS

Table 6 shows an example test pattern word.

Table 6. Example Test Pattern Word

| WORD | R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|------|---|
| 1 | 0x7C3E1E7 |

| 7 | | | | C | | | | 3 | | | | E | | | | 1 | | | | E | | | | 7 | | | |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|----|----|----|
| R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | G7 | G6 | G5 | G4 | G3 | G2 | G1 | G0 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | 0 | VS | HS | DE |
| 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

TYPICAL IC POWER-CONSUMPTION TEST PATTERN

Typical power-consumption test patterns consist of sixteen 30-bit transmit words in 1-channel mode and eight 30-bit transmit words in 2-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

Table 7. Typical IC Power-Consumption Test Pattern, 1-Channel Mode

| WORD | TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|------|--|
| 1 | 0x0000007 |
| 2 | 0xFFFF007 |
| 3 | 0x01FFF47 |
| 4 | 0xF0E07F7 |
| 5 | 0x7C3E1E7 |
| 6 | 0xE707C37 |
| 7 | 0xE1CE6C7 |
| 8 | 0xF1B9237 |
| 9 | 0x91BB347 |
| 10 | 0xD4CCC67 |
| 11 | 0xAD53377 |
| 12 | 0xACB2207 |
| 13 | 0xAAB2697 |
| 14 | 0x5556957 |
| 15 | 0xAAAAAB3 |
| 16 | 0xAAAAAA5 |

Table 8. Typical IC Power-Consumption Test Pattern, 2-Channel Mode

| WORD | TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|------|--|
| 1 | 0x0000001 |
| 2 | 0x03F03F1 |
| 3 | 0xBFFBFF1 |
| 4 | 0x1D71D71 |
| 5 | 0x4C74C71 |
| 6 | 0xC45C451 |
| 7 | 0xA3aA3A5 |
| 8 | 0x5555553 |

MAXIMUM POWER CONSUMPTION TEST PATTERN

The maximum (or worst-case) power consumption of the SN65LVDS304 is tested using the two different test patterns shown in [Table 9](#) and [Table 10](#). Test patterns consist of sixteen 30-bit transmit words in 1-channel mode and eight 30-bit transmit words in 2-channel mode. The pattern repeats itself throughout the entire measurement. It is assumed that every possible transmit code on RGB inputs has the same probability to occur during typical device operation.

**Table 9. Worst-Case Power-Consumption
Test Pattern 1**

| WORD | TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|------|--|
| 1 | 0xAAAAA5 |
| 2 | 0x555555 |

**Table 10. Worst-Case Power-Consumption
Test Pattern 2**

| WORD | TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|------|--|
| 1 | 0x000000 |
| 2 | 0xFFFFF7 |

OUTPUT SKEW PULSE POSITION and JITTER PERFORMANCE

The following test patterns are used to measure the output skew pulse position and the jitter performance of the SN65LVDS304. The jitter test pattern stresses the interconnect, particularly to test for ISI, using very long run-lengths of consecutive bits, and incorporating very high and low data rates, maximizing switching noise. Each pattern is self-repeating for the duration of the test.

Table 11. Transmit Jitter Test Pattern, 1-Channel Mode

| WORD | TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0, VS, HS, DE |
|------|--|
| 1 | 0x0000001 |
| 2 | 0x0000031 |
| 3 | 0x00000F1 |
| 4 | 0x00003F1 |
| 5 | 0x0000FF1 |
| 6 | 0x0003FF1 |
| 7 | 0x000FFF1 |
| 8 | 0x0F0F0F1 |
| 9 | 0x0C30C31 |
| 10 | 0x0842111 |
| 11 | 0x1C71C71 |
| 12 | 0x18C6311 |
| 13 | 0x1111111 |
| 14 | 0x3333331 |
| 15 | 0x2452413 |
| 16 | 0x22A2A25 |
| 17 | 0x5555553 |
| 18 | 0xDB6DB65 |
| 19 | 0xCCCCC1 |
| 20 | 0xEEEEE1 |
| 21 | 0xE739CE1 |
| 22 | 0xE38E381 |
| 23 | 0xF7BDEE1 |
| 24 | 0xF3CF3C1 |
| 25 | 0xF0F0F01 |
| 26 | 0xFFFF001 |
| 27 | 0xFFFC001 |
| 28 | 0xFFFF001 |
| 29 | 0xFFFFC01 |
| 30 | 0xFFFFF01 |
| 31 | 0xFFFFFC1 |
| 32 | 0xFFFFF1 |

Table 12. Transmit Jitter Test Pattern, 2-Channel Mode

| WORD | TEST PATTERN: R[7:4], R[3:0], G[7:4], G[3:0], B[7:4], B[3:0], 0,VS,HS,DE |
|------|---|
| 1 | 0x0000001 |
| 2 | 0x000FFF3 |
| 3 | 0x8008001 |
| 4 | 0x0030037 |
| 5 | 0xE00E001 |
| 6 | 0x00FF001 |
| 7 | 0x007E001 |
| 8 | 0x003C001 |
| 9 | 0x0018001 |
| 10 | 0x1C7E381 |
| 11 | 0x3333331 |
| 12 | 0x555AAA5 |
| 13 | 0x6DBDB61 |
| 14 | 0x7777771 |
| 15 | 0x555AAA3 |
| 16 | 0xAAAAAA5 |
| 17 | 0x5555553 |
| 18 | 0xAAA5555 |
| 19 | 0x8888881 |
| 20 | 0x9242491 |
| 21 | 0xAAA5571 |
| 22 | 0xCCCCC1 |
| 23 | 0xE3E1C71 |
| 24 | 0xFFE7FF1 |
| 25 | 0xFFC3FF1 |
| 26 | 0xFF81FF1 |
| 27 | 0xFE00FF1 |
| 28 | 0x1FF1FF1 |
| 29 | 0xFFCFFC3 |
| 30 | 0x7FF7FF1 |
| 31 | 0xFFF0007 |
| 32 | 0xFFFFF1 |

TYPICAL CHARACTERISTIC CURVES

Some of the plots in this section show more than one curve representing various device pin relationships. Taken together, they represent a working range for the tested parameter.

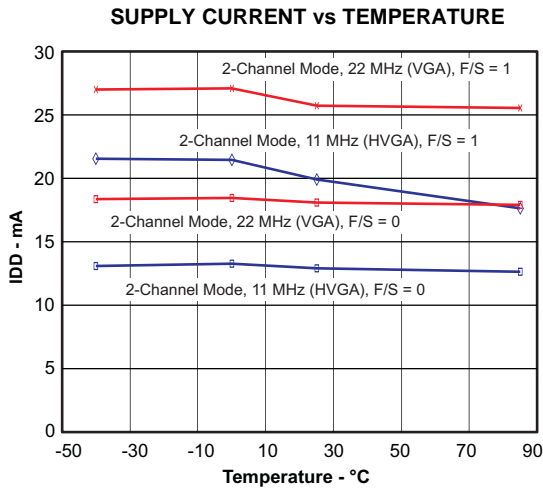


Figure 18.

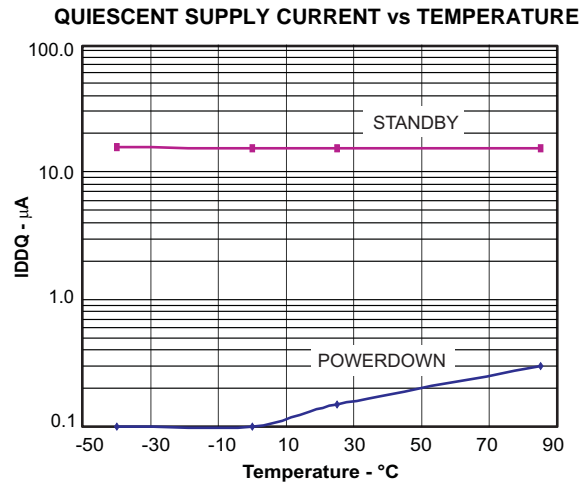


Figure 19.

SUPPLY CURRENT vs FREQUENCY, 1-CHANNEL MODE

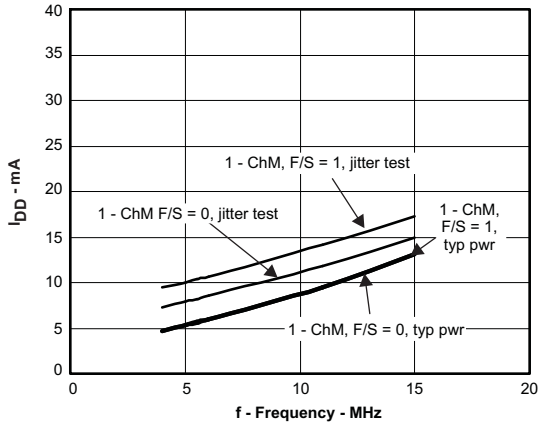


Figure 20.

SUPPLY CURRENT vs FREQUENCY, 2-CHANNEL MODE

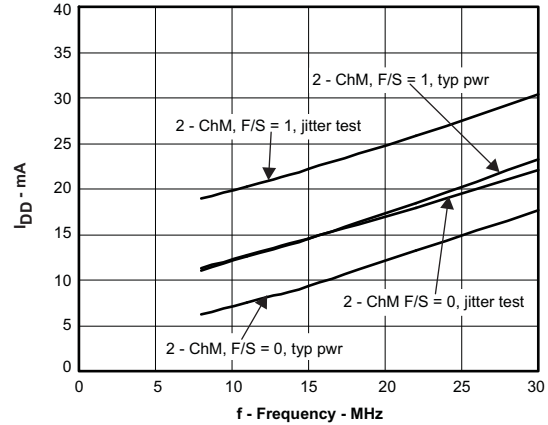


Figure 21.

RECEIVER STROBE POSITION vs TEMPERATURE

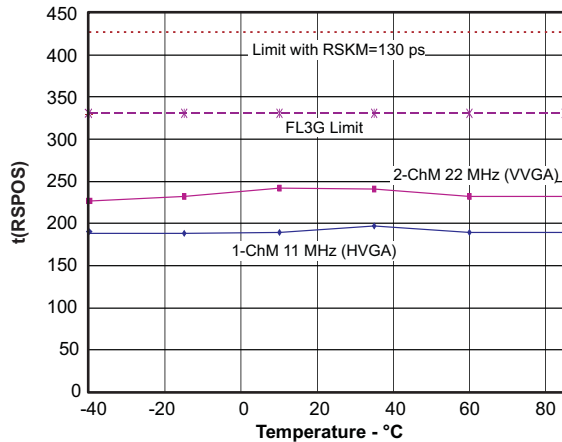


Figure 22.

PLL BANDWIDTH

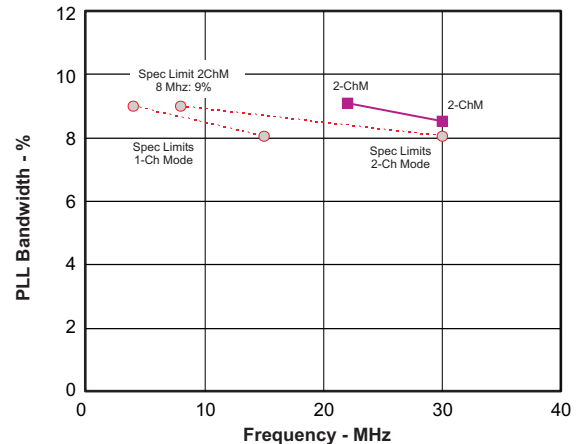


Figure 23.

TYPICAL CHARACTERISTIC CURVES (continued)

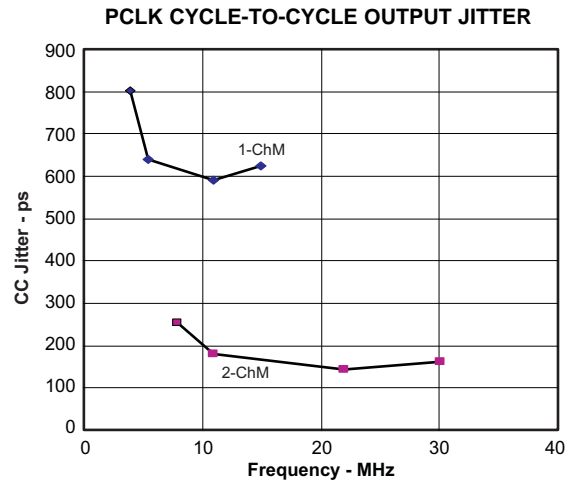


Figure 24.

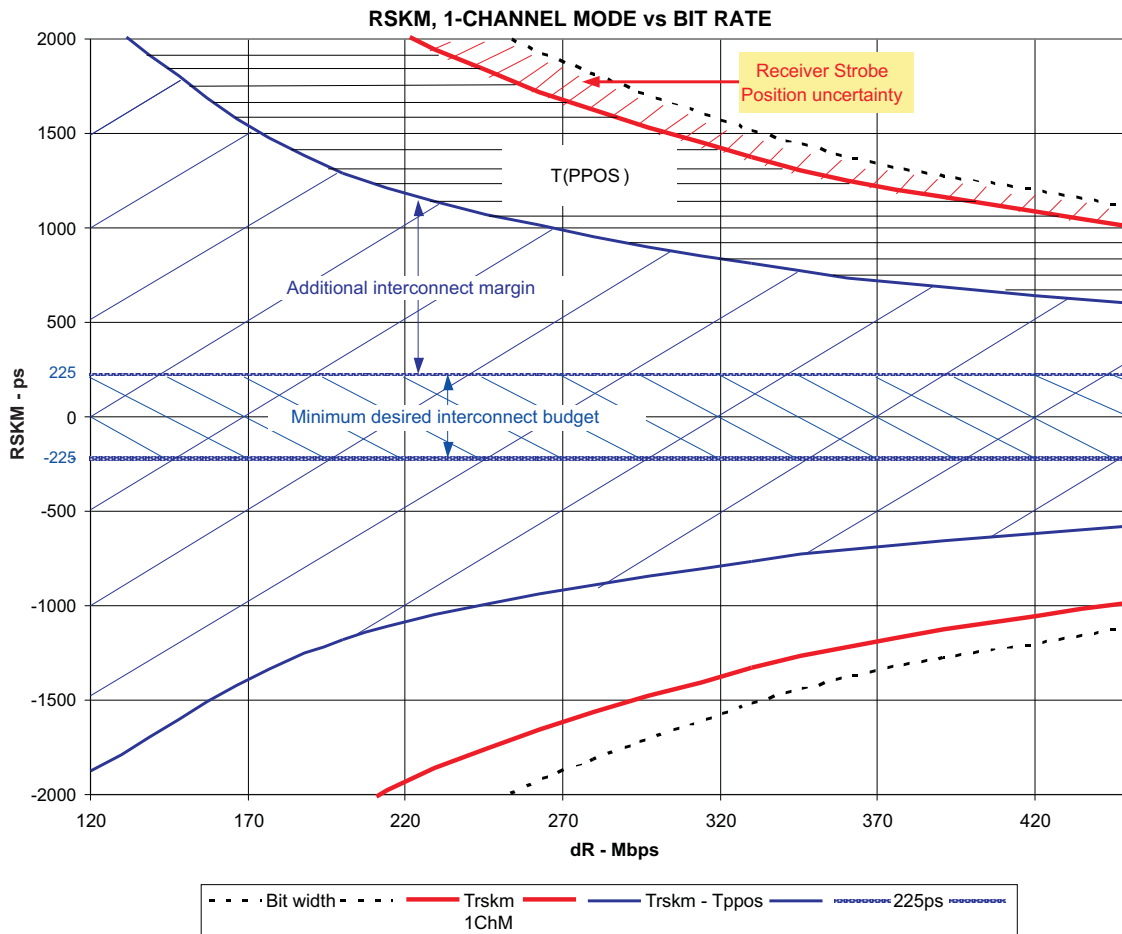


Figure 25.

TYPICAL CHARACTERISTIC CURVES (continued)

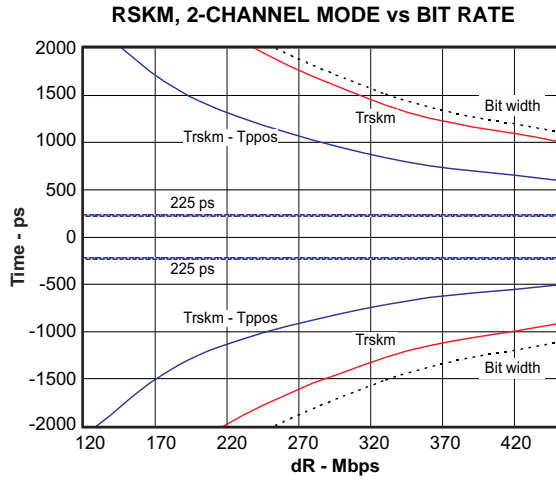


Figure 26.

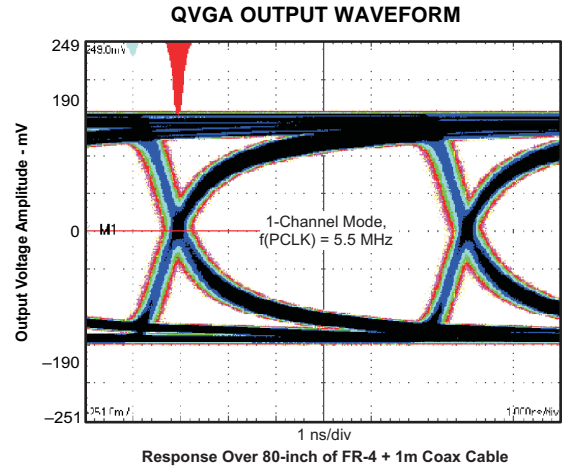


Figure 27.

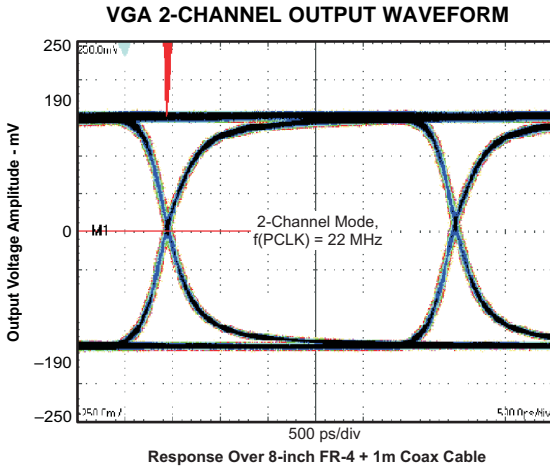


Figure 28.

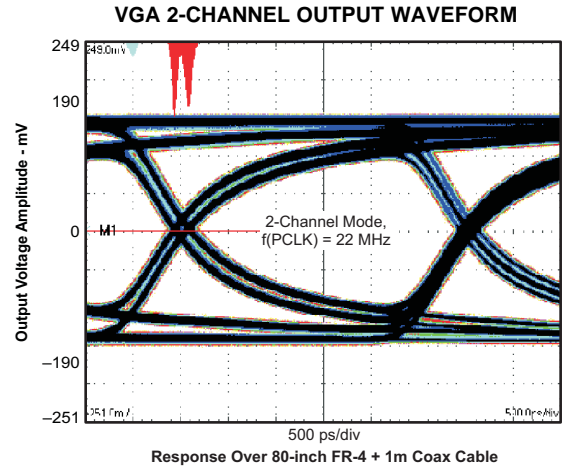


Figure 29.

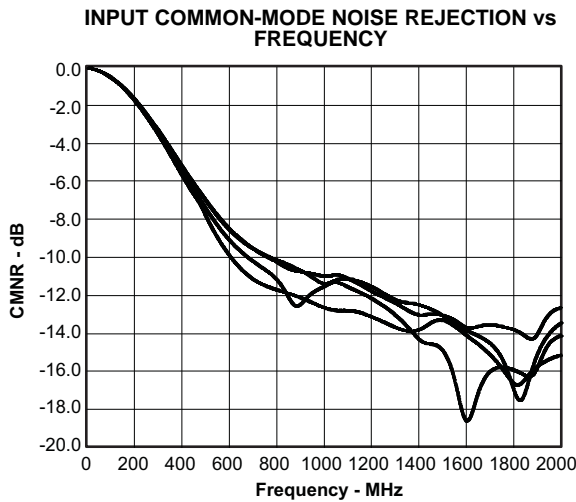


Figure 30.

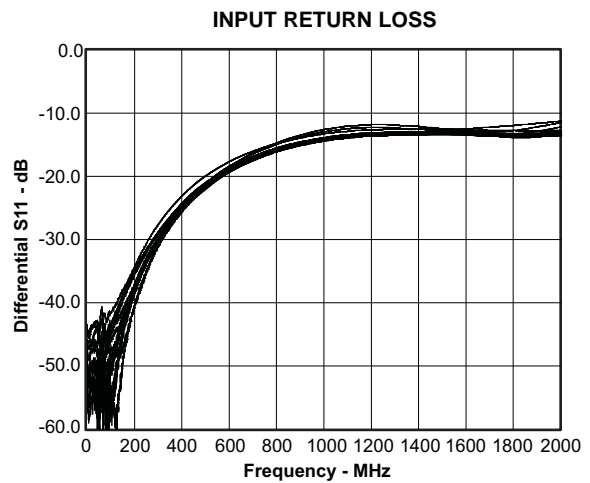


Figure 31.

TYPICAL CHARACTERISTIC CURVES (continued)

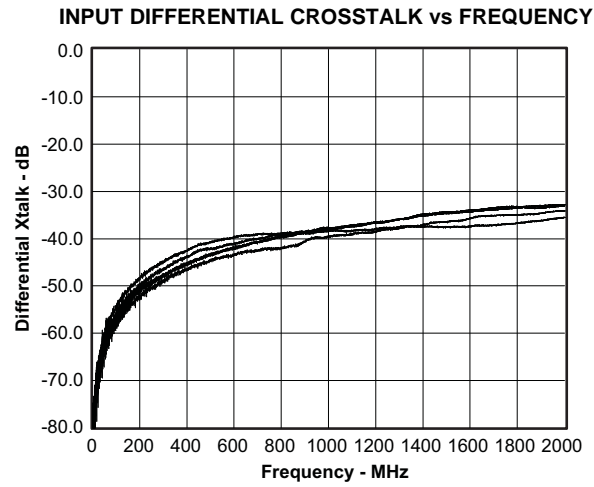


Figure 32.

APPLICATION INFORMATION

PREVENTING INCREASED LEAKAGE CURRENTS IN CONTROL INPUTS

A floating (left open) CMOS input allows leakage currents to flow from V_{DD} to GND. Do not leave any CMOS input unconnected or floating. Every input must be connected to a valid logic level, V_{IH} or V_{OL} , while power is supplied to V_{DD} . This also minimizes the power consumption of standby and power-down modes.

POWER-SUPPLY DESIGN RECOMMENDATION

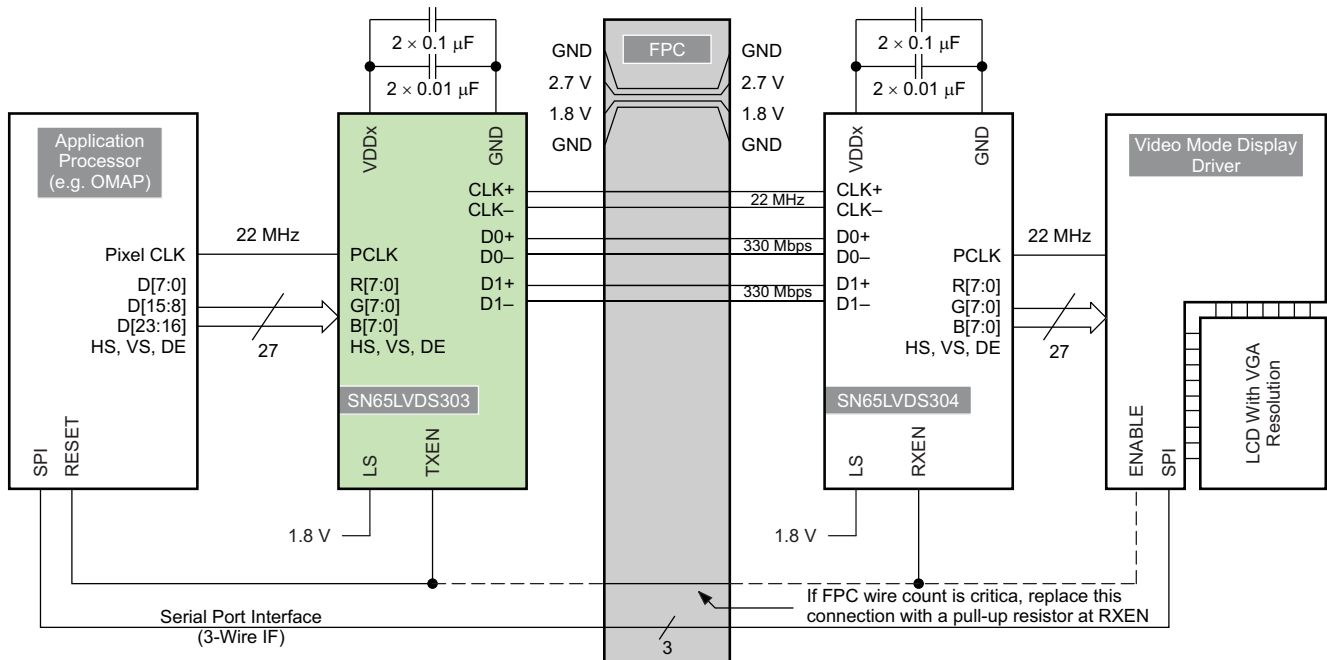
For a multilayer PCB, it is recommended to keep one common GND layer underneath the device and connect all ground terminals directly to this plane.

SN65LVDS304 DECOUPLING RECOMMENDATION

The SN65LVDS304 was designed to operate reliably in a constricted environment with other digital switching ICs. In cell phone designs, the SN65LVDS304 often shares a power supply with various other ICs. The SN65LVDS304 can operate with power supply noise as specified in the *Recommended Operating Conditions*. To minimize the power-supply noise floor, provide good decoupling near the SN65LVDS304 power pins. The use of four ceramic capacitors (two 0.01- μ F and two 0.1- μ F) provides good performance. At the very least, it is recommended to install one 0.1- μ F and one 0.01- μ F capacitor near the SN65LVDS304. To avoid large current loops and trace inductance, the trace length between the decoupling capacitors and IC power input pins must be minimized. Placing the capacitor underneath the SN65LVDS304 on the bottom of the PCB is often a good choice.

VGA APPLICATION

Figure 33 shows a possible implementation of a standard 640 × 480 VGA display. The SN65LVDS303 interfaces to the SN65LVDS304, which is the corresponding receiver device to deserialize the data and drive the display driver. The pixel clock rate of 22 MHz assumes ~10% blanking overhead and 60-Hz display refresh rate. The application assumes 24-bit color resolution. Also shown is how the application processor provides a power-down (reset) signal for both serializer and the display driver. The signal count over the flexible printed circuit board (FPC) could be further decreased by using the standby option on the SN65LVDS304 and pulling RXEN high with a 30-k Ω resistor to V_{DD} .



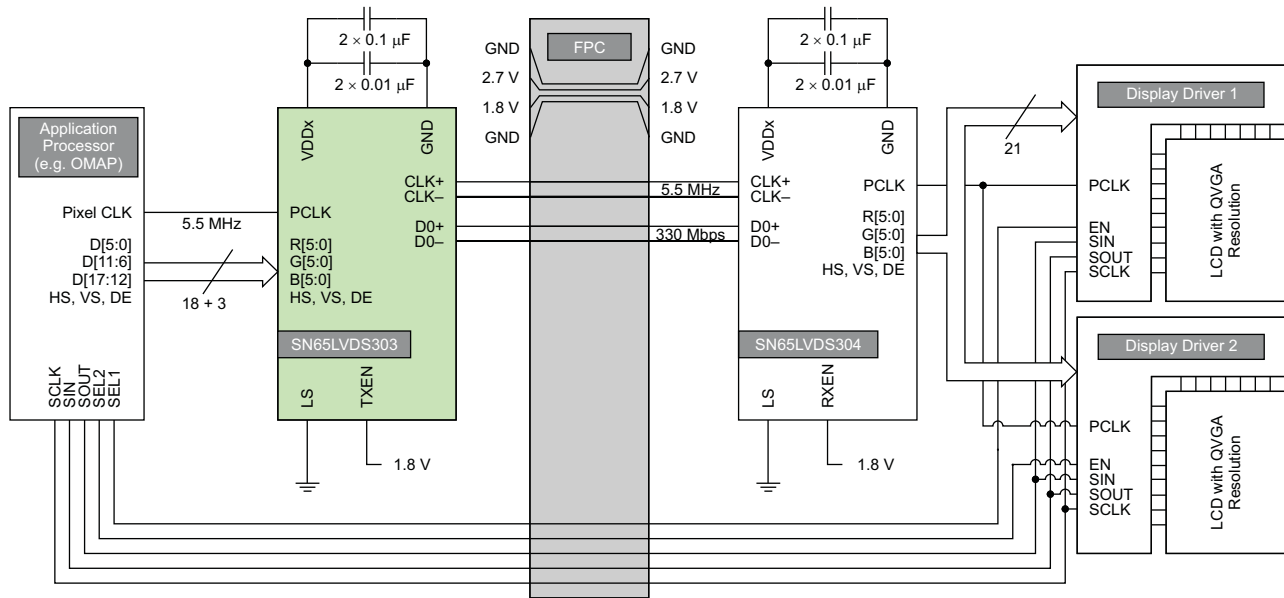
B0178-01

Figure 33. Typical VGA Display Application

APPLICATION INFORMATION (continued)

DUAL LCD-DISPLAY APPLICATION

The example in Figure 34 shows a possible application setup driving two video-mode displays from one application processor. The data rate of 330 Mbps at a pixel clock rate of 5.5 MHz corresponds to a 320 × 240 QVGA resolution at 60-Hz refresh rate and 10% blanking overhead.



B0179-01

Figure 34. Example Dual-QVGA Display Application

TYPICAL APPLICATION FREQUENCIES

The SN65LVDS304 supports pixel clock frequencies from 4 MHz to 30 MHz over 1 or 2 data pairs. Table 13 provides a few typical display resolution examples and shows the number of data pairs necessary to connect the SN65LVDS304 with the display. The blanking overhead is assumed to be 20%. Often, blanking overhead is smaller, resulting in a lower data rate. Furthermore, the examples in the table assumes a display frame refresh rate of 60 Hz. The actual refresh rate may differ, depending on the application-processor clock implementation.

Table 13. Typical Application Data Rates and Serial Lane Usage

| Display Screen Resolution | Visible Pixel Count | Blanking Overhead | Display Refresh Rate | Pixel Clock Frequency [MHz] | Serial Data Rate Per Pair | |
|---------------------------|---------------------|-------------------|----------------------|-----------------------------|---------------------------|----------|
| | | | | | 1-ChM | 2-ChM |
| 176 × 220 (QCIF+) | 38,720 | 20% | 90 Hz | 4.2 MHz | 125 Mbps | |
| 240 × 320 (QVGA) | 76,800 | 20% | 60 Hz | 5.5 MHz | 166 Mbps | |
| 640 × 200 | 128,000 | 20% | 60 Hz | 9.2 MHz | 276 Mbps | 138 Mbps |
| 352 × 416 (CIF+) | 146,432 | 20% | 60 Hz | 10.5 MHz | 316 Mbps | 158 Mbps |
| 352 × 440 | 154,880 | 20% | 60 Hz | 11.2 MHz | 335 Mbps | 167 Mbps |
| 320 × 480 (HVGA) | 153,600 | 20% | 60 Hz | 11.1 MHz | 332 Mbps | 166 Mbps |
| 800 × 250 | 200,000 | 20% | 60 Hz | 14.4 MHz | 432 Mbps | 216 Mbps |
| 640x320 | 204,800 | 20% | 60 Hz | 14.7 MHz | 442 Mbps | 221 Mbps |
| 640 × 480 (VGA) | 307,200 | 20% | 60 Hz | 22.1 MHz | | 332 Mbps |
| 1024 × 320 | 327,680 | 20% | 60 Hz | 23.6 MHz | | 354 Mbps |
| 854 × 480 (WVGA) | 409,920 | 20% | 60 Hz | 29.5 MHz | | 443 Mbps |

CALCULATION EXAMPLE: HVGA DISPLAY

The following calculation shows an example for a half-VGA display with the following parameters:

| | |
|----------------------------|-------------|
| Display resolution: | 480 × 320 |
| Frame refresh rate: | 58.4 Hz |
| Vertical visible pixels: | 320 lines |
| Vertical front porch: | 10 lines |
| Vertical sync: | 5 lines |
| Vertical back porch: | 3 lines |
| Horizontal visible pixels: | 480 columns |
| Horizontal front porch: | 20 columns |
| Horizontal sync: | 5 columns |
| Horizontal back porch: | 3 columns |

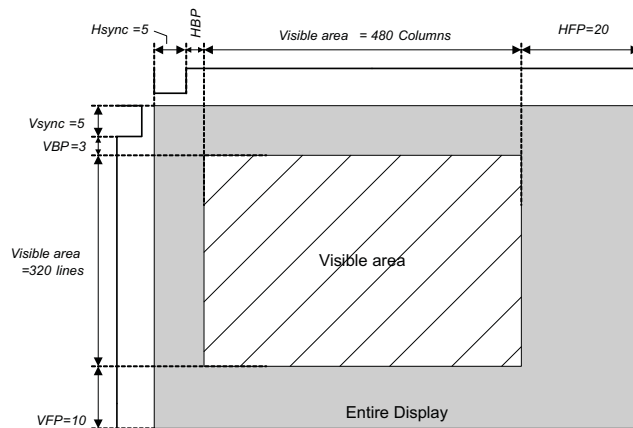


Figure 35. HVGA Display

Calculation of the total number of pixels and blanking overhead:

| | |
|---------------------------|---|
| Visible area pixel count: | $480 \times 320 = 153,600$ pixels |
| Total frame pixel count: | $(320 + 10 + 5 + 3) \times (480 + 20 + 5 + 3) = 171,704$ pixels |
| Blanking overhead: | $(171,704 - 153,600) \div 153,600 \approx 11.8\%$ |

The application requires the following serial-link parameters:

| | |
|------------------------|--|
| Pixel clock frequency: | $171,704 \times 58.4 \text{ Hz} = 10 \text{ MHz}$ |
| Serial data rate: | 1-channel mode: $10 \text{ MHz} \times 30 \text{ bits/channel} = 300 \text{ Mbps}$ |
| | 2-channel mode: $10 \text{ MHz} \times 15 \text{ bits/channel} = 150 \text{ Mbps}$ |

HOW TO DETERMINE INTERCONNECT SKEW AND JITTER BUDGET

Designing a reliable data link requires examining the interconnect skew and jitter budget. The sum of all transmitter, PCB, connector, FPC, and receiver uncertainties must be smaller than the available serial bit time. The highest pixel clock frequency defines the available serial bit time. The transmitter timing uncertainty is defined by t_{PPOS} in the transmitter data sheet. For a bit-error-rate target of $\leq 10^{-12}$, the measurement duration for t_{PPOS} is $\geq 10^{12}$. The SN65LVDS304 receiver can tolerate a maximum timing uncertainty defined by t_{RSKM} . The interconnect budget is calculated by:

$$t_{interconnect} = t_{RSKM} - t_{PPOS}$$

Example:

$f_{PCLK}(\max) = 23 \text{ MHz}$ (VGA display resolution, 60 Hz)

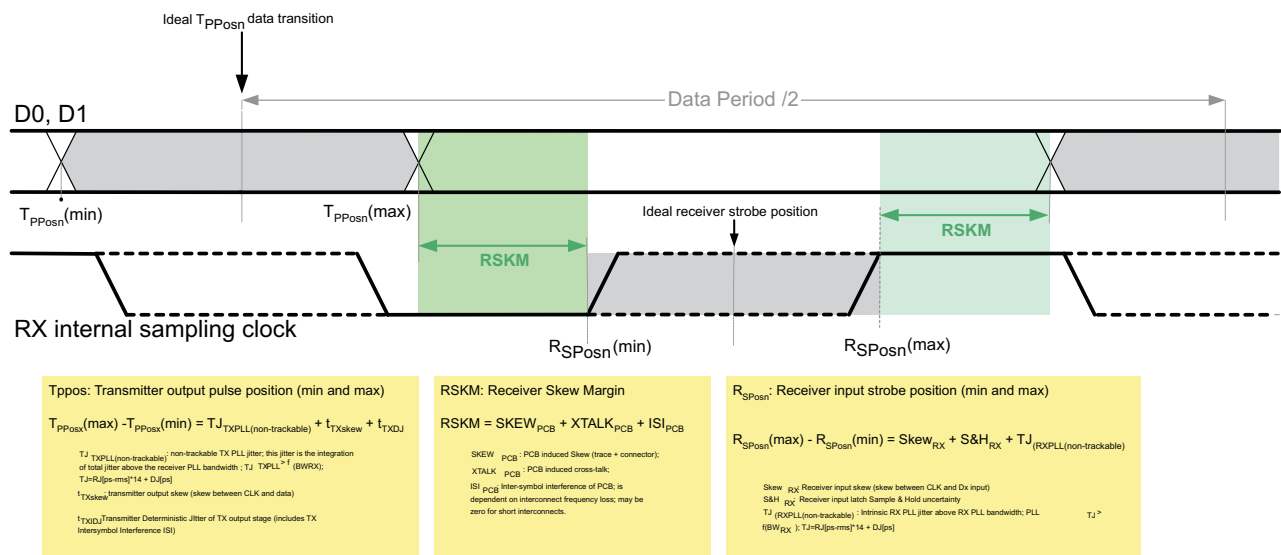
Transmission mode: 2-ChM; $t_{PPOS}(\text{SN65LVDS303}) = 330 \text{ ps}$

Target bit error rate: 10^{-12}

$t_{RSKM}(\text{SN65LVDS304}) = 1/(2 \times 15 \times f_{PCLK}) - 480 \text{ ps} = 969 \text{ ps}$

The interconnect budget for cable skew and ISI must be smaller than:

$$t_{interconnect} = t_{RSKM} - t_{PPOS} = 639 \text{ ps}$$



T0165-01

Figure 36. Jitter Budget

F/S-PIN SETTING AND CONNECTING THE SN65LVDS304 TO AN LCD DRIVER

NOTE:

Receiver PLL tracking: To maximize the design margin for the interconnect, good RX PLL tracking of the TX PLL is important. FlatLink3G requires the RX PLL to have a bandwidth higher than the bandwidth of the TX PLL. The SN65LVDS304 PLL design is optimized to track the SN65LVDS303 PLL particularly well, thus providing a very large receiver skew margin. A FlatLink3G-compliant link must provide at least ± 225 ppm of receiver skew margin for the interconnect.

It is important to understand the tradeoff between power consumption, EMI, and maximum speed when selecting the F/S signal. It is beneficial to choose the slowest rise time possible to minimize EMI and power consumption. Unfortunately a slower rise time also reduces the timing margin left for the LCD driver. Hence, it is necessary to calculate the timing margin to select the correct F/S pin setting.

The output rise time depends on the output driver strength and the output load. An LCD driver typical capacitive load is assumed with ~ 10 pF. The higher the capacitive load, the slower is the rise time. Rise time of the SN65LVDS304 is measured as the time duration it takes the output voltage to rise from 20% of V_{DD} to 80% of V_{DD} , and fall time is defined as the time for the output voltage to transition from 80% of V_{DD} down to 20% of V_{DD} .

Within one mode of operation and one F/S pin setting, the rise time of the output stage is fixed and does not adjust to the pixel frequency. Due to the short bit time at very fast pixel clock speeds and the real capacitive load of the display driver, the output amplitude might not reach V_{DD} and GND saturation fully. To ensure sufficient signal swing and verify the design margin, it becomes necessary to determine that the output amplitude under any circumstance reaches the display driver's input stage logic threshold (usually 30% and 70% of V_{DD}).

Figure 37 shows a worst-case rise time simulation assuming an LCD driver load of 16 pF at VGA display resolution. PCLK is the fastest-switching output. With F/S set to GND (Figure 37-a), the PCLK output voltage amplitude is significantly reduced. The voltage amplitude of the output data RGB[7:0], VS, HS, and DE shows less amplitude attenuation because these outputs carry random data patterns and toggle at half of the PCLK frequency or less. It is necessary to determine the timing margin between the SN65LVDS304 output and LCD driver input.

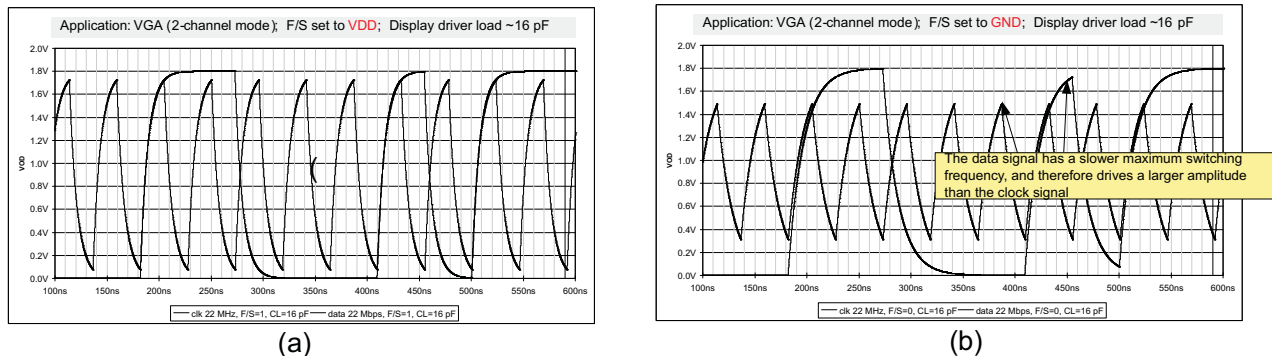


Figure 37. Output Amplitude as a Function of Output Toggling Frequency, Capacitive Load, and F/S Setting

HOW TO DETERMINE THE LCD DRIVER TIMING MARGIN

To determine the timing margin, it is necessary to specify the frequency of operation, identify the setup and hold times of the LCD driver, and specify the output load of the SN65LVDS304 as a combination of the LCD driver input parasitics plus any capacitance caused by the connecting PCB trace. Furthermore, the setting of pin F/S and the SN65LVDS304 output skew impact the margin. The total remaining design margin calculates as follows:

$$t_{DM} = \frac{1}{2 \times f_{PCLK}} - t_{DUTP(max_error)} - \frac{t_{rise(max)} \times C_{LOAD}}{10 \text{ pF}} - |t_{OSK}| \quad (3)$$

where:

- t_{DM} – Design margin
- f_{PCLK} – Pixel clock frequency
- $t_{DUTP(max_error)}$ – maximum duty cycle error
- $t_{rise(max)}$ – maximum rise or fall time; see $t_{R/F}$ under switching characteristics
- C_L – parasitic capacitance (sum of LCD driver input parasitics + connecting PCB trace)
- t_{skew} – clock to data output skew SN65LVDS304

Example:

At a pixel clock frequency of 5.5MHz (QVGA), and an assumed LCD driver load of 15 pF, the remaining timing margin is:

$$t_{DUTP(max_error)} = \frac{|t_{DUTP(max)} - 50|}{100\%} \times t_{PCLK} = \frac{5\%}{100\%} \times \frac{1}{5.5\text{MHz}} = 9.1\text{ns}$$

$$t_{DM} = \frac{1}{2 \times 5.5\text{MHz}} - 9\text{ns} - \frac{16\text{ns}_{(F/S=GND)} \times 15\text{pF}}{10\text{pF}} - 500\text{ps} = 57.3\text{ns}$$

As long as the setup and hold times of the LCD driver are each less than 57 ns, the timing budget is met sufficiently.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|------------------|-----------------------|----------------------------------|-----------------|------|-------------|----------------------------|------------------|------------------------------|
| SN65LVDS304ZQER | ACTIVE | BGA MI CROSTA R JUNI OR | ZQE | 80 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|----------------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN65LVDS304ZQER | BGA MICROSTAR JUNIOR | ZQE | 80 | 2500 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



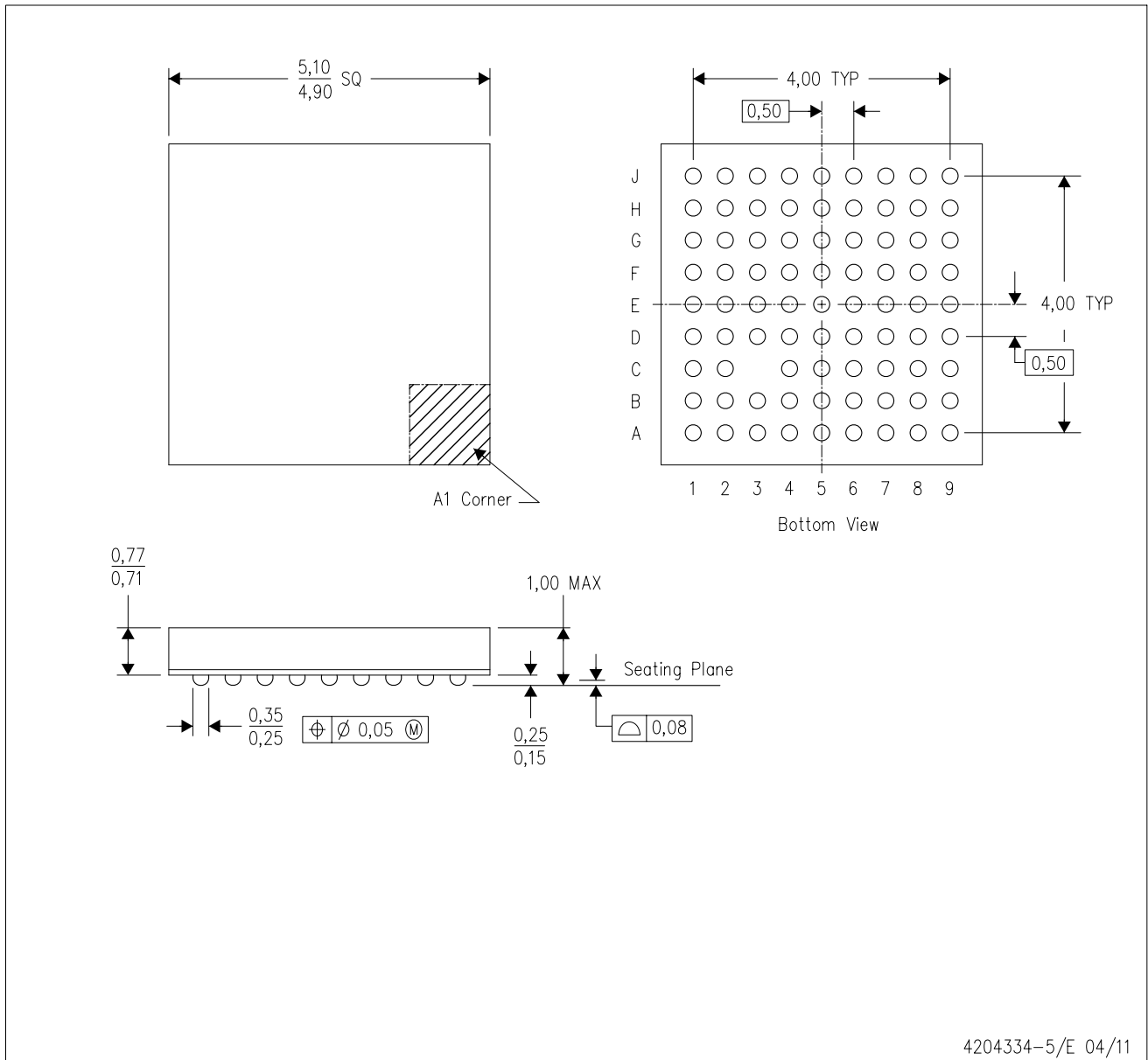
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|----------------------|-----------------|------|------|-------------|------------|-------------|
| SN65LVDS304ZQER | BGA MICROSTAR JUNIOR | ZQE | 80 | 2500 | 340.5 | 333.0 | 20.6 |

MECHANICAL DATA

ZQE (S-PBGA-N80)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225
 - D. This is a Pb-free solder ball design.

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