

FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **Member of the Texas Instruments Widebus™ Family**
- **State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$**
- **High-Impedance State During Power Up and Power Down**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **Flow-Through Architecture Optimizes PCB Layout**
- **High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)**
- **Latch-Up Performance Exceeds 500 mA Per JESD 70**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model ($C = 200$ pF, $R = 0$)**
- **Shrink Small-Outline (DL) Package**

- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DL PACKAGE
(TOP VIEW)

1DIR	1	48	1 \overline{OE}
1B1	2	47	1A1
1B2	3	46	1A2
GND	4	45	GND
1B3	5	44	1A3
1B4	6	43	1A4
V_{CC}	7	42	V_{CC}
1B5	8	41	1A5
1B6	9	40	1A6
GND	10	39	GND
1B7	11	38	1A7
1B8	12	37	1A8
2B1	13	36	2A1
2B2	14	35	2A2
GND	15	34	GND
2B3	16	33	2A3
2B4	17	32	2A4
V_{CC}	18	31	V_{CC}
2B5	19	30	2A5
2B6	20	29	2A6
GND	21	28	GND
2B7	22	27	2A7
2B8	23	26	2A8
2DIR	24	25	2 \overline{OE}

DESCRIPTION/ORDERING INFORMATION

The SN74ABT16245A-EP is a 16-bit noninverting 3-state transceiver designed for synchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74ABT16245A-EP is characterized for operation from -55°C to 125°C .



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SN74ABT16245A-EP

16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCBS807B–OCTOBER 2005–REVISED JANUARY 2006

ORDERING INFORMATION

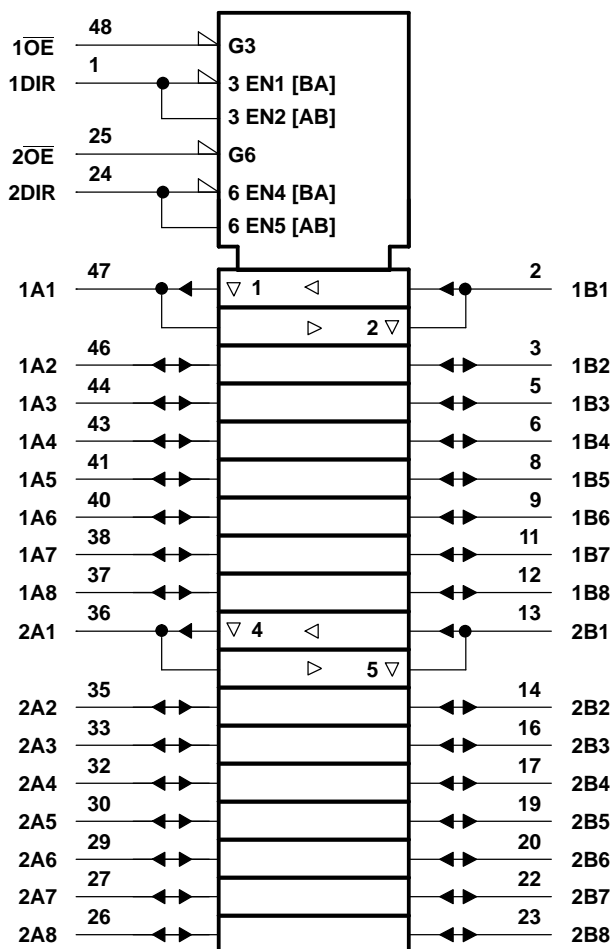
T _A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SSOP – DL	Reel of 1000	CABT16245AMDREP	ABT16245AMEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (EACH 8-BIT SECTION)

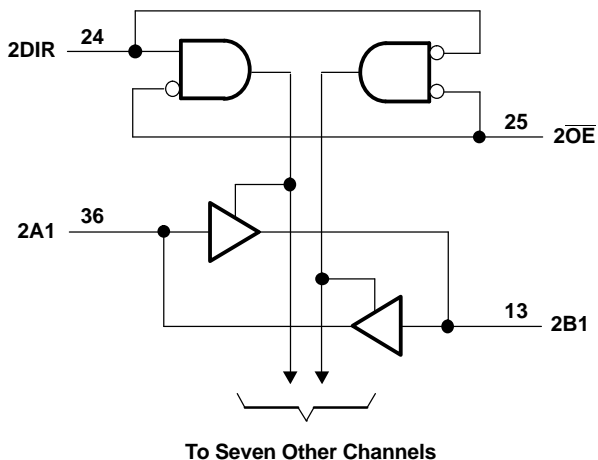
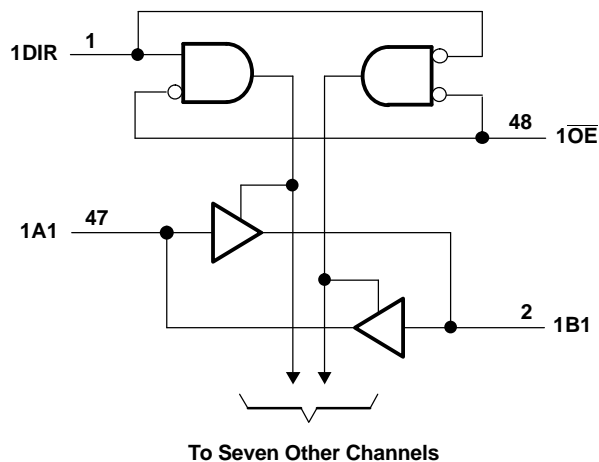
INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

LOGIC SYMBOL⁽¹⁾



(1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	7	V
V _I	Input voltage range (except I/O ports) ⁽²⁾		−0.5	7	V
V _O	Voltage range applied to any output in the high or power-off state		−0.5	5.5	V
I _O	Current into any output in the low state			96	mA
I _{IK}	Input clamp current	V _I < 0		−18	mA
I _{OK}	Output clamp current	V _O < 0		−50	mA
θ _{JA}	Package thermal impedance ⁽³⁾			94	°C/W
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		4.5	5.5	V
V _{IH}	High-level input voltage		2		V
V _{IL}	Low-level input voltage			0.8	V
V _I	Input voltage		0	V _{CC}	V
I _{OH}	High-level output current			−24	mA
I _{OL}	Low-level output current			48	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		μs/V
T _A	Operating free-air temperature		−55	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74ABT16245A-EP

16-BIT BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

SCBS807B–OCTOBER 2005–REVISED JANUARY 2006

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP ⁽¹⁾	MAX			
V _{IK}		V _{CC} = 4.5 V, I _I = –18 mA			–1.2		–1.2	V
V _{OH}		V _{CC} = 4.5 V, I _{OH} = –3 mA	2.5			2.5		V
		V _{CC} = 5 V, I _{OH} = –3 mA	3			3		
		V _{CC} = 4.5 V	2			2		
			2					
V _{OL}		V _{CC} = 4.5 V			0.55		0.55	V
					0.55			
V _{hys}				100				mV
I _I	Control inputs	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1	μA
	A or B port	V _{CC} = 2.1 V to 5.5 V, V _I = V _{CC} or GND			±20		±100	
I _{OZPU}		V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, \overline{OE} = X			±50			μA
I _{OZPD}		V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, \overline{OE} = X			±50			μA
I _{OZH} ⁽²⁾		V _{CC} = 2.7 V to 5.5 V, V _O = 2.7 V, \overline{OE} ≥ 2 V			10 ⁽³⁾		10	μA
I _{OZL} ⁽²⁾		V _{CC} = 2.7 V to 5.5 V, V _O = 0.5 V, \overline{OE} ≥ 2 V			–10 ⁽³⁾		–10	μA
I _{off}		V _{CC} = 0, V _I or V _O ≤ 5.5 V			±100			μA
I _{CEX}		V _{CC} = 5.5 V, V _O = 5.5 V			50		50	μA
I _O ⁽⁴⁾		V _{CC} = 5.5 V, V _O = 2.5 V	–50	–100	–180	–50	–180	mA
I _{CC}	A or B port	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND			2		2	mA
					32		32	
					2		2	
ΔI _{CC} ⁽⁵⁾	Data inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			2		1.5	mA
					0.05		1	
	Control inputs	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND			1.5		1.5	
C _i	Control inputs	V _I = 2.5 V or 0.5 V		3				pF
C _o	A or B port	V _O = 2.5 V or 0.5 V		6				pF

(1) All typical values are at V_{CC} = 5 V.

(2) The parameters I_{OZH} and I_{OZL} include the input leakage current.

(3) This limit may vary among suppliers.

(4) Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

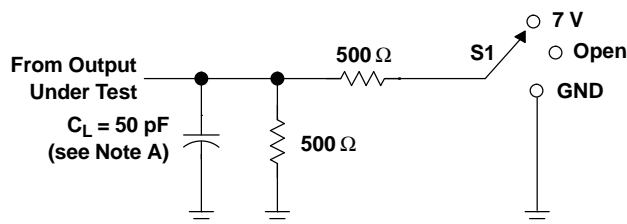
(5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Switching Characteristics

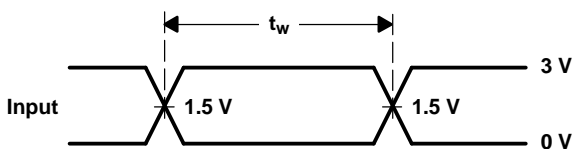
over recommended operating ranges of supply voltage and operating free-air temperature, $C_L = 50$ pF
(unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	B or A	0.5	2.2	3.4	0.5	4	ns
t_{PHL}			0.5	2.3	3.8	0.5	4.6	
t_{PZH}	\overline{OE}	B or A	0.8	3.6	5.2	0.8	5.5	ns
t_{PZL}			0.9	3.7	6.1	0.1	7.3	
t_{PHZ}	\overline{OE}	B or A	1.3	4.4	5.8	1.3	6.3	ns
t_{PLZ}			1.4	3.3	4.7	1.4	5.5	

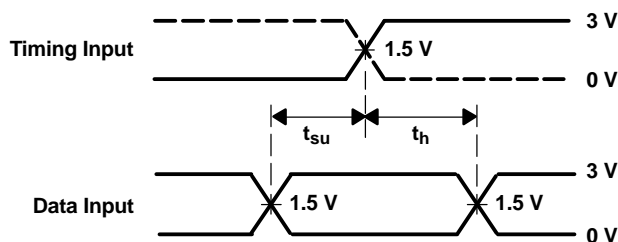
PARAMETER MEASUREMENT INFORMATION



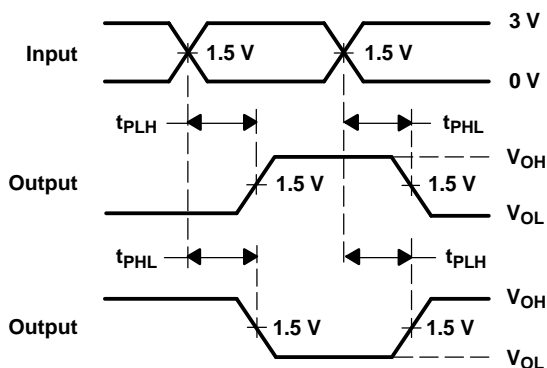
LOAD CIRCUIT



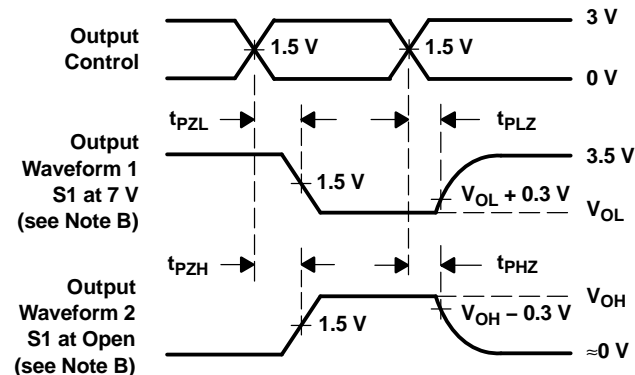
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



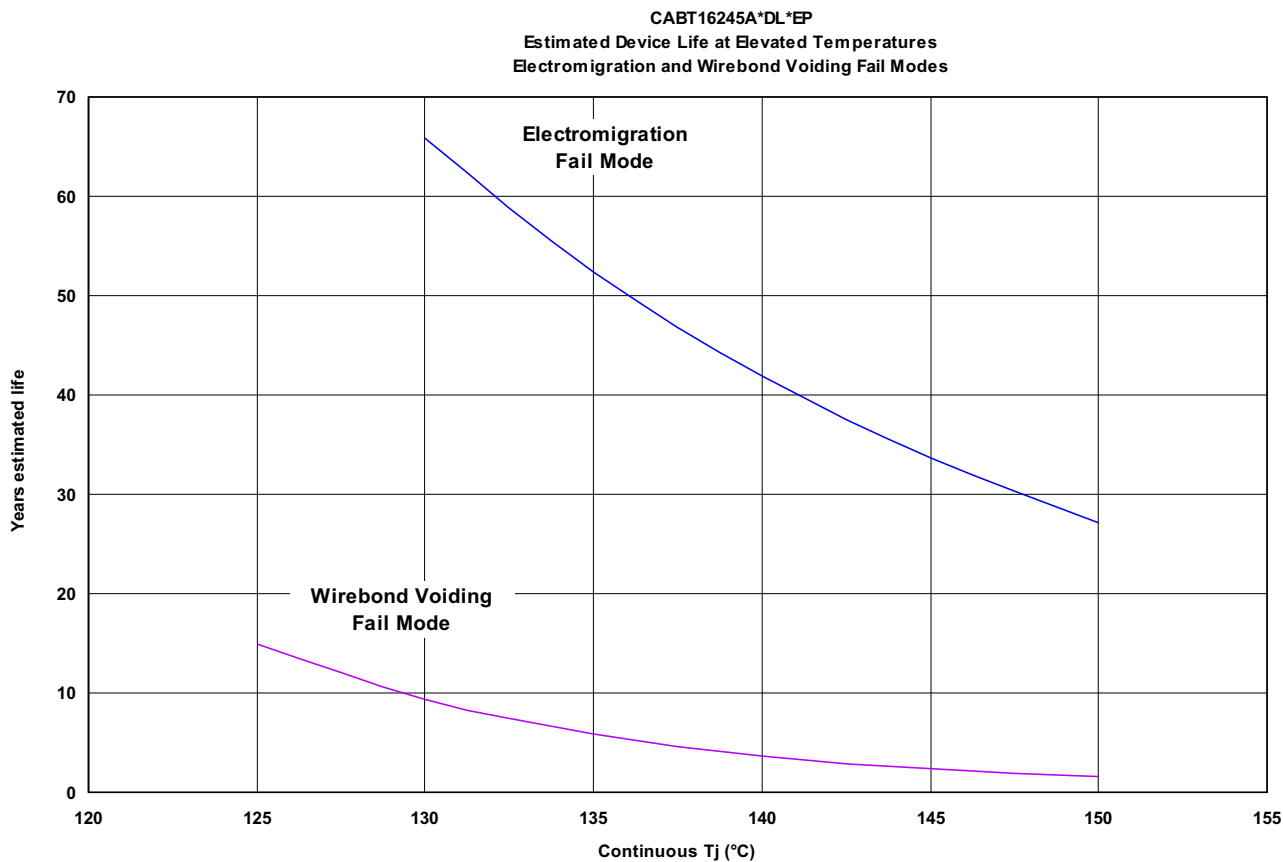
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms



PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CABT16245AMDREP	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06609-01XE	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74ABT16245A-EP :

- Catalog: [SN74ABT16245A](#)
- Military: [SN54ABT16245A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CABT16245AMDREP	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CABT16245AMDREP	SSOP	DL	48	1000	346.0	346.0	49.0

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