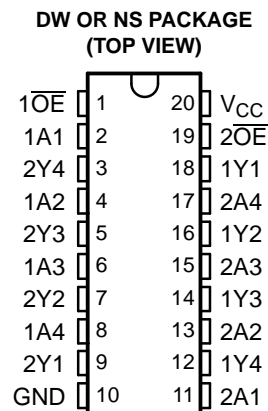


## FEATURES

- Controlled Baseline
  - One Assembly/Test Site, One Fabrication Site
- Extended Temperature Performance of up to  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product-Change Notification
- Qualification Pedigree <sup>(1)</sup>
- 4.5-V to 5.5-V  $V_{\text{CC}}$  Operation
- Inputs Accept Voltages to 5.5 V
- Max  $t_{\text{pd}}$  of 9.5 ns at 5 V
- Inputs Are TTL Compatible

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



## DESCRIPTION/ORDERING INFORMATION

The SN74ACT244-EP octal buffer/driver is designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device is organized as two 4-bit buffers/drivers with separate output-enable ( $\overline{\text{OE}}$ ) inputs. When  $\overline{\text{OE}}$  is low, the device passes noninverted data from the A inputs to the Y outputs. When  $\overline{\text{OE}}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SOIC – DW	Tape and reel	SN74ACT244MDWREP	SACT244MEP
	SOP – NS	Tape and reel	SN74ACT244MNSREP	SACT244MEP
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	SOIC – DW	Tape and reel	SN74ACT244IDWREP	SACT244IEP

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE (EACH BUFFER)

INPUTS		OUTPUT Y
$\overline{\text{OE}}$	A	
L	H	H
L	L	L
H	X	Z



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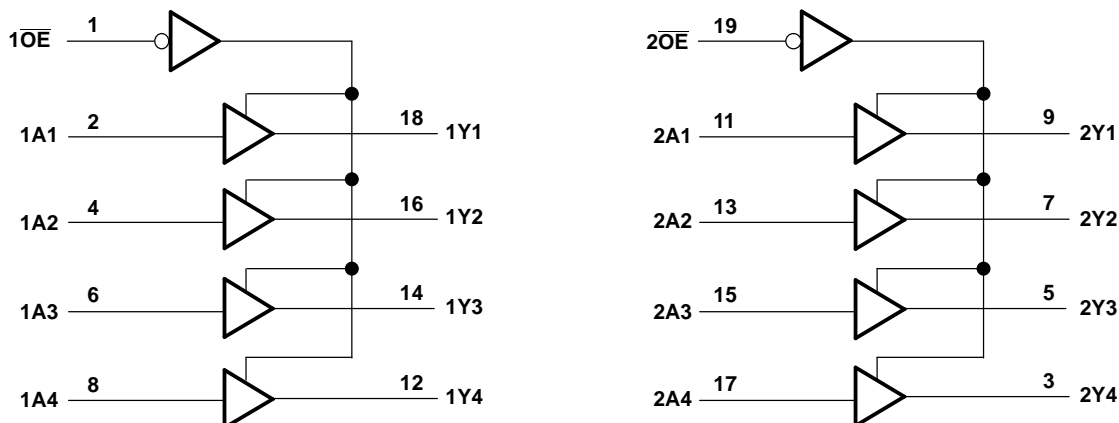
# SN74ACT244-EP

## OCTAL BUFFER/DRIVER

### WITH 3-STATE OUTPUTS

SCAS724B–OCTOBER 2003–REVISED MARCH 2006

#### LOGIC DIAGRAM (POSITIVE LOGIC)



#### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	−0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	−0.5	$V_{CC} + 0.5$	V
$V_O$	Output voltage range <sup>(2)</sup>	−0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$ or $V_I > V_{CC}$		±20 mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20 mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		±50 mA
	Continuous current through $V_{CC}$ or GND			±200 mA
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DW package		58 °C/W
		NS package		60 °C/W
$T_{stg}$	Storage temperature range <sup>(4)</sup>	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.
- (4) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See [http://www.ti.com/ep\\_quality](http://www.ti.com/ep_quality) for additional information on enhanced plastic packaging.

#### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		V
$V_{IL}$	Low-level input voltage		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current		−24	mA
$I_{OL}$	Low-level output current		24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		8	ns/V
$T_A$	Operating free-air temperature	SN74ACT244M-EP		−55 125 °C
		SN74ACT244I-EP		−40 85 °C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN74ACT244M-EP		SN74ACT244I-EP		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 µA	4.5 V	4.4	4.49		4.4		4.4		V
		5.5 V	5.4	5.49		5.4		5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.86			3.7		3.76		
		5.5 V	4.86			4.7		4.76		
	I <sub>OH</sub> = -75 mA <sup>(1)</sup>	5.5 V						3.85		
V <sub>OL</sub>	I <sub>OL</sub> = 50 µA	4.5 V		0.001	0.1		0.1		0.1	V
		5.5 V		0.001	0.1		0.1		0.1	
	I <sub>OL</sub> = 24 mA	4.5 V			0.36		0.5		0.44	
		5.5 V			0.36		0.5		0.44	
	I <sub>OL</sub> = 75 mA <sup>(1)</sup>	5.5 V							1.65	
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25		±5		±2.5	µA
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1		±1		±1	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		80		40	µA
ΔI <sub>CC</sub> <sup>(2)</sup>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.6			1.6		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5						pF
C <sub>o</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		8						pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Figure 1](#))

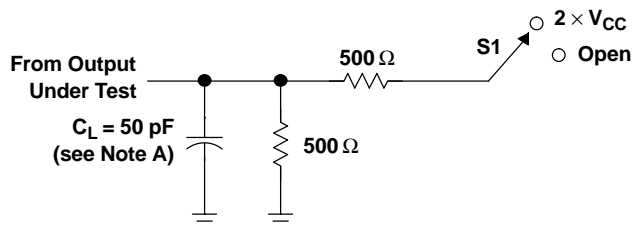
PARAMETER	FROM (INPUT)	TO (OUTPUT)	T <sub>A</sub> = 25°C			SN74ACT244M-EP		SN74ACT244I-EP		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	2	6.5	9	1	10	1.5	10	ns
t <sub>PHL</sub>			2	7	9	1	10	1.5	10	
t <sub>PZH</sub>	$\overline{OE}$	Y	1.5	7	8.5	1	9.5	1	9.5	ns
t <sub>PZL</sub>			2	7	9.5	1	11	1.5	10.5	
t <sub>PHZ</sub>	$\overline{OE}$	Y	2	8	9.5	1	11	1.5	10.5	ns
t <sub>PLZ</sub>			2.5	7.5	10	1	11.5	2	10.5	

## Operating Characteristics

V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

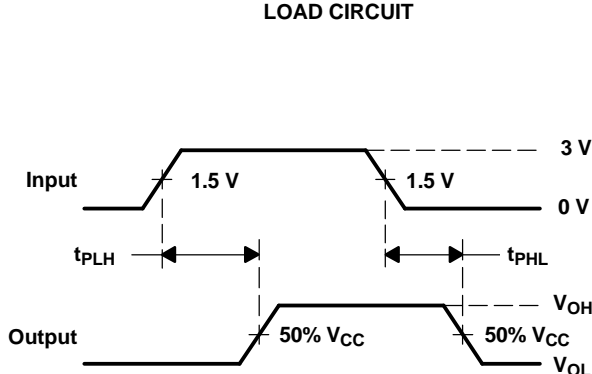
PARAMETER		TEST CONDITIONS		TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	C <sub>L</sub> = 50 pF, f = 1 MHz		45	pF

## PARAMETER MEASUREMENT INFORMATION

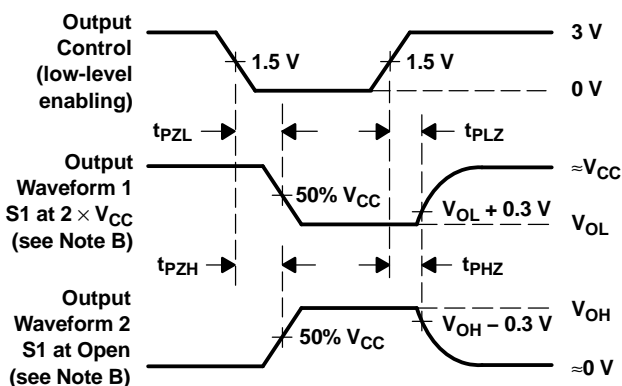


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	Open

**LOAD CIRCUIT**



**VOLTAGE WAVEFORMS**



**VOLTAGE WAVEFORMS**

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74ACT244IDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT244MDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ACT244MNSREP	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04620-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04620-01YE	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04620-02XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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**OTHER QUALIFIED VERSIONS OF SN74ACT244-EP :**

- Catalog: [SN74ACT244](#)
- Automotive: [SN74ACT244-Q1](#)
- Military: [SN54ACT244](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

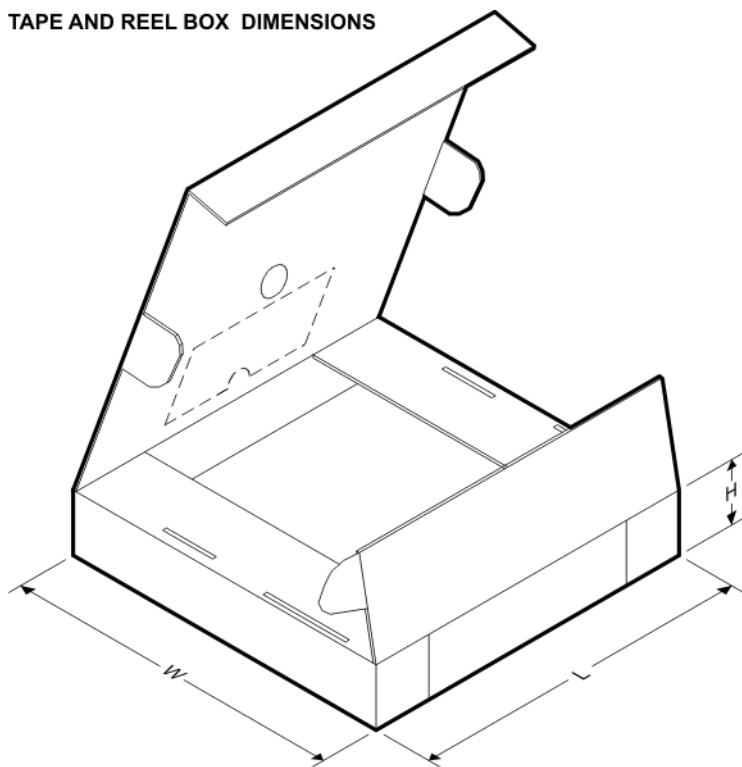
**TAPE AND REEL INFORMATION**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT244IDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ACT244MDWREP	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ACT244MNSREP	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1

## TAPE AND REEL BOX DIMENSIONS

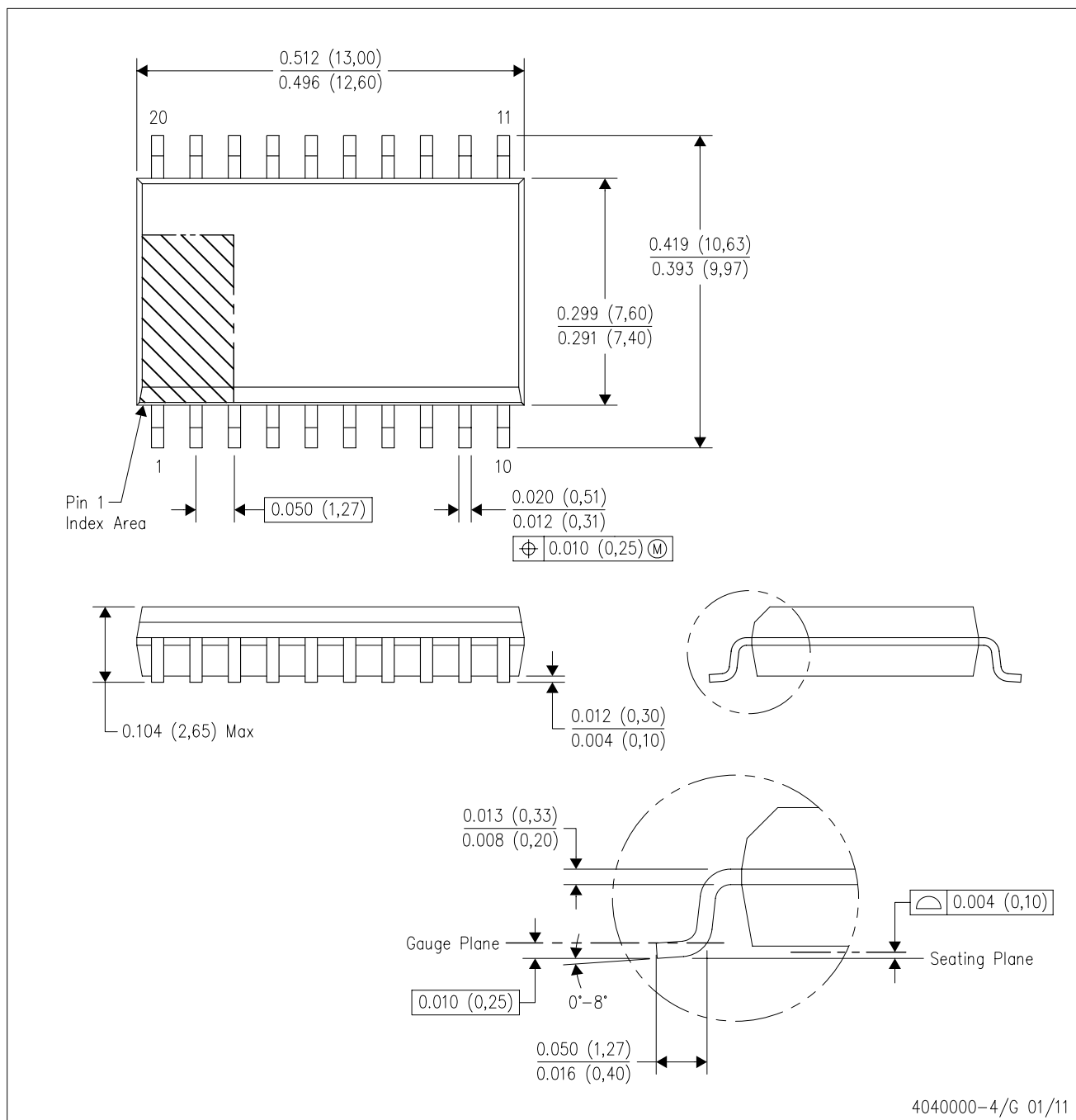


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT244IDWREP	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ACT244MDWREP	SOIC	DW	20	2000	346.0	346.0	41.0
SN74ACT244MNSREP	SO	NS	20	2000	346.0	346.0	41.0

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

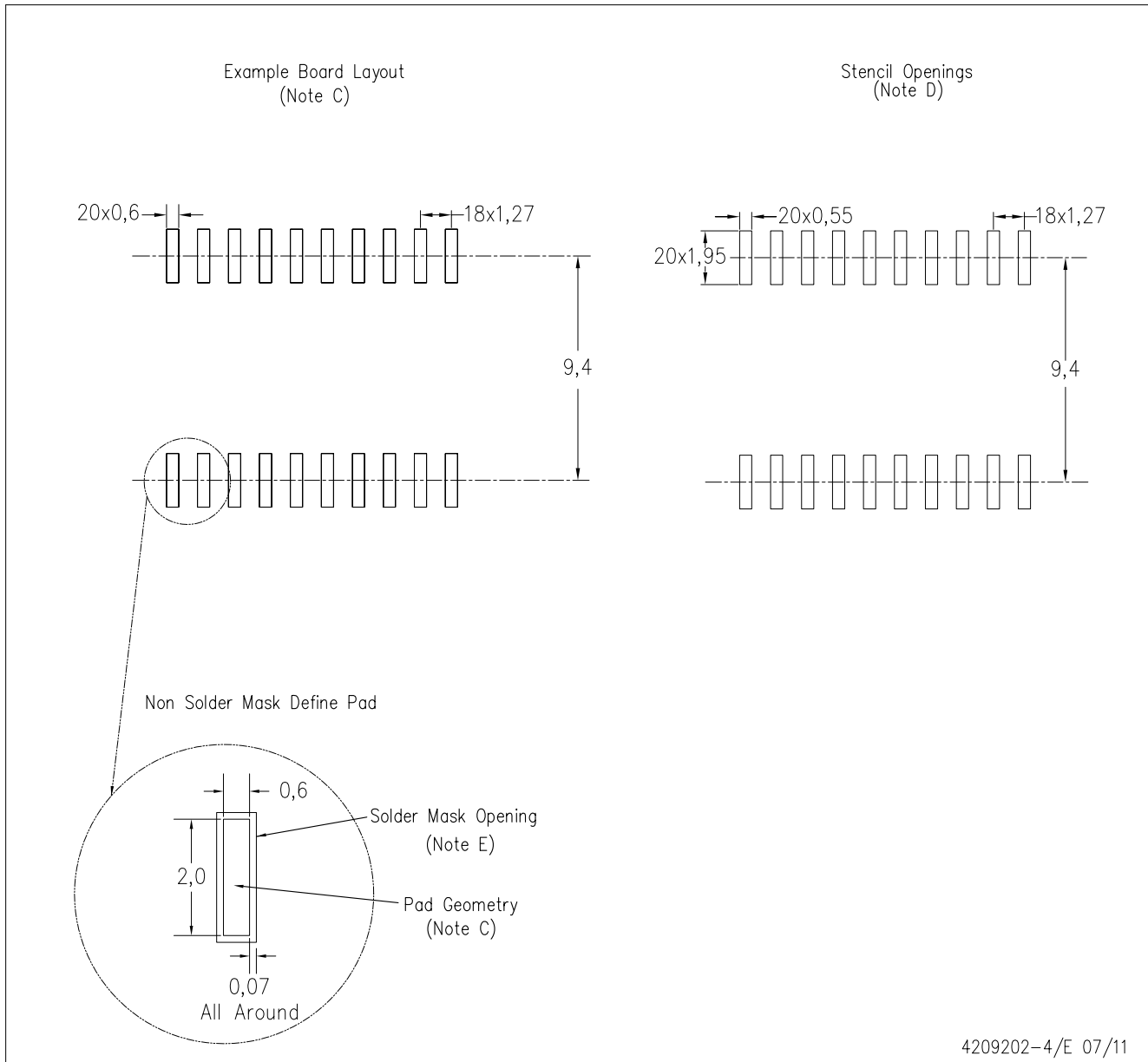


- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AC.



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



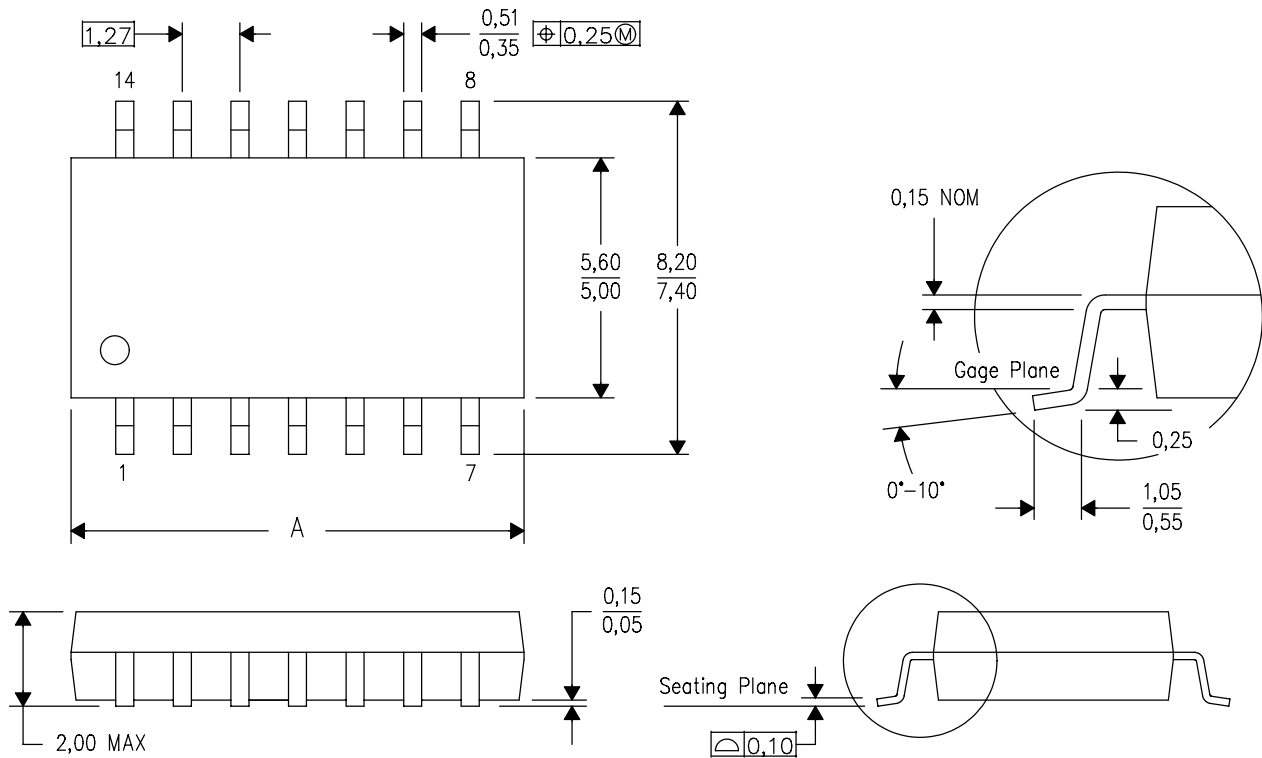
- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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