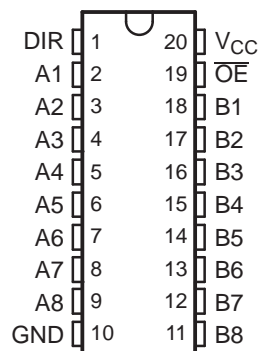


FEATURES

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **I_{off} and Power-Up 3-State Support Hot Insertion**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Latch-Up Performance Exceeds 500 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

DB OR PW PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This octal bus transceiver is designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

This device is designed for asynchronous communication between data buses. It transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

The logic diagram shows the internal structure of the 74VHC147 decoder. It features two 3-input AND gates at the top. The first AND gate has inputs DIR (pin 1), A1 (pin 2), and a common input. Its output is connected to OE (pin 19). The second AND gate has inputs DIR (pin 1), A1 (pin 2), and a common input. Its output is connected to B1 (pin 18). There are also two 3-input OR gates at the bottom. The first OR gate has inputs from DIR (pin 1), A1 (pin 2), and a common input. Its output is connected to OE (pin 19). The second OR gate has inputs from DIR (pin 1), A1 (pin 2), and a common input. Its output is connected to B1 (pin 18). The diagram also shows connections to other channels, indicated by arrows pointing to pins 18 and 19.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	−0.5	4.6	V
V_I	Input voltage range ⁽²⁾	−0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	−0.5	7	V
V_O	Voltage range applied to any output in the high state ⁽²⁾	−0.5	$V_{CC} + 0.5$	V
I_O	Current into any output in the low state		128	mA
I_O	Current into any output in the high state ⁽³⁾		64	mA
I_{IK}	Input clamp current	$V_I < 0$	−50	mA
I_{OK}	Output clamp current	$V_O < 0$	−50	mA
θ_{JA}	Package thermal impedance ⁽⁴⁾	DB package	69.5	°C/W
		PW package	83	
T_{stg}	Storage temperature range ⁽⁵⁾	−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) Long-term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.7	3.6	V
V _{IH}	High-level input voltage		2		V
V _{IL}	Low-level input voltage			0.8	V
V _I	Input voltage			5.5	V
I _{OH}	High-level output current			−32	mA
I _{OL}	Low-level output current			64	mA
Δt/Δv	Input transition rise or fall rate	Outputs enabled		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate		200		μs/V
T _A	Operating free-air temperature	I temp	−40	85	°C
		M temp	−55	125	

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVTH245A-EP

3.3-V ABT OCTAL BUS TRANSCEIVER

WITH 3-STATE OUTPUTS

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Electrical Characteristics

over recommended operating free-air temperature ranges (I or M) (unless otherwise noted)

PARAMETER		TEST CONDITIONS		M TEMP			I TEMP			UNIT
				MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{IK}		V _{CC} = 2.7 V, I _I = −18 mA		−1.2			−1.2			V
V _{OH}		V _{CC} = 2.7 V to 3.6 V, I _{OH} = −100 μA		V _{CC} − 0.2			V _{CC} − 0.2			V
		V _{CC} = 2.7 V, I _{OH} = −8 mA		2.4			2.4			
		V _{CC} = 3 V		I _{OH} = −24 mA						
				I _{OH} = −32 mA			2			
V _{OL}		V _{CC} = 2.7 V		I _{OL} = 100 μA			0.2			V
				I _{OL} = 24 mA			0.5			
		V _{CC} = 3 V		I _{OL} = 16 mA			0.4			
				I _{OL} = 32 mA			0.5			
				I _{OL} = 48 mA			0.55			
				I _{OL} = 64 mA			0.55			
I _I	Control inputs	V _{CC} = 3.6 V, V _I = V _{CC} or GND		±1			±1			μA
		V _{CC} = 0 or 3.6 V, V _I = 5.5 V		10			10			
	A or B port ⁽²⁾	V _{CC} = 3.6 V		V _I = 5.5 V			20			
				V _I = V _{CC}			1			
				V _I = 0			−5			
I _{off}		V _{CC} = 0, V _I or V _O = 0 V to 4.5 V					±100			μA
I _{I(hold)}	A or B port	V _{CC} = 3 V		V _I = 0.8 V			75			μA
				V _I = 2 V			−75			
		V _{CC} = 3.6 V, ⁽³⁾ V _I = 0 V to 3.6 V					500 −750			
I _{OZPU}		V _{CC} = 0 to 1.5 V, V _O = 0.5 V to 3 V, OE = don't care		±100			±100			μA
I _{OZPD}		V _{CC} = 1.5 V to 0, V _O = 0.5 V to 3 V, OE = don't care		±100			±100			μA
I _{CC}		V _{CC} = 3.6 V, I _O = 0, V _I = V _{CC} or GND		Outputs high			0.19			mA
				Outputs low			5			
				Outputs disabled			0.19			
ΔI _{CC} ⁽⁴⁾		V _{CC} = 3 V to 3.6 V, One input at V _{CC} − 0.6 V, Other inputs at V _{CC} or GND		0.2			0.2			mA
C _i		V _I = 3 V or 0		4			4			pF
C _o		V _O = 3 V or 0		9			9			pF

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) Unused terminals are at $V_{CC}\text{ or GND}$.

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}\text{ or GND}$.

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	M TEMP				I TEMP				UNIT	
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 3.3 V ± 0.3 V			V _{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP ⁽¹⁾	MAX	MIN		MAX
t _{PLH}	A or B	B or A	1.2	5.5	6		1.2	2.3	3.5	4		ns
t _{PHL}			1.2	5.5	6		1.2	2.1	3.5	4		
t _{PZH}	OE	A or B	1.3	7.9	9.5		1.3	3.2	5.5	7.1		ns
t _{PZL}			1.7	7	7.9		1.7	3.4	5.5	6.5		
t _{PHZ}	OE	A or B	2.2	7.2	7.8		2.2	3.5	5.9	6.5		ns
t _{PLZ}			2.2	7.1	7.2		2.2	3.4	5	5.1		

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

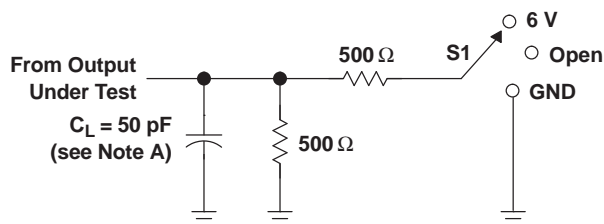
SN74LVTH245A-EP

3.3-V ABT OCTAL BUS TRANSCEIVER

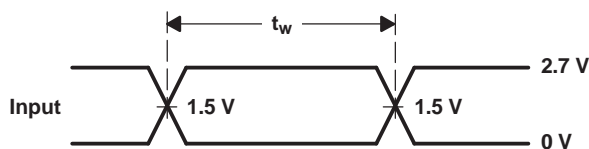
WITH 3-STATE OUTPUTS

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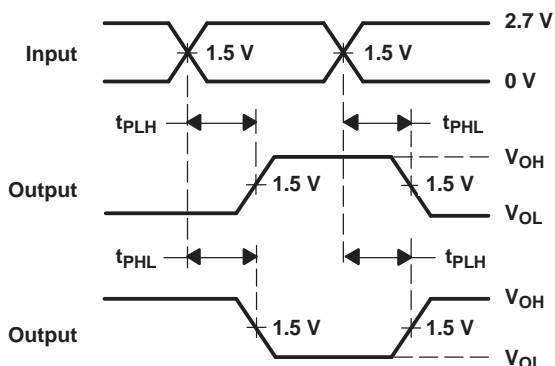
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

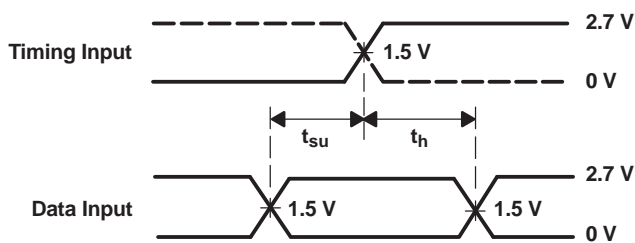


VOLTAGE WAVEFORMS
PULSE DURATION

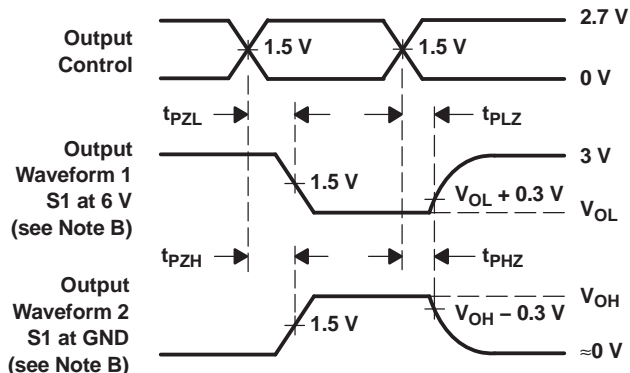


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR $\leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 - The outputs are measured one at a time, with one transition per measurement.
 - All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVTH245AIPWREP	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH245AMDBREP	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04723-01XE	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/04723-02YE	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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OTHER QUALIFIED VERSIONS OF SN74LVTH245A-EP :

- Catalog: [SN74LVTH245A](#)
- Military: [SN54LVTH245A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH245AIPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVTH245AMDBREP	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

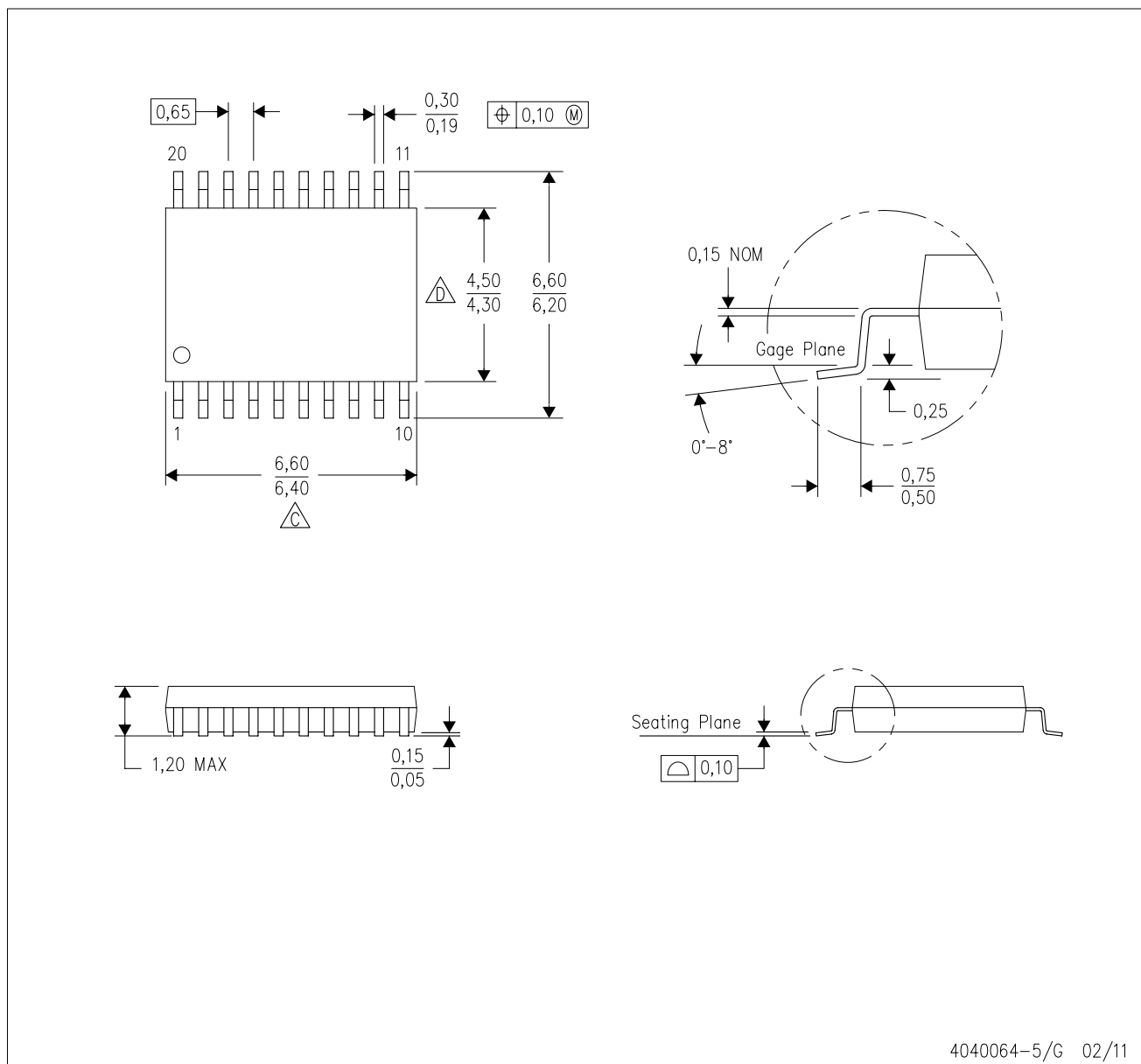


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH245AIPWREP	TSSOP	PW	20	2000	346.0	346.0	33.0
SN74LVTH245AMDBREP	SSOP	DB	20	2000	346.0	346.0	33.0

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

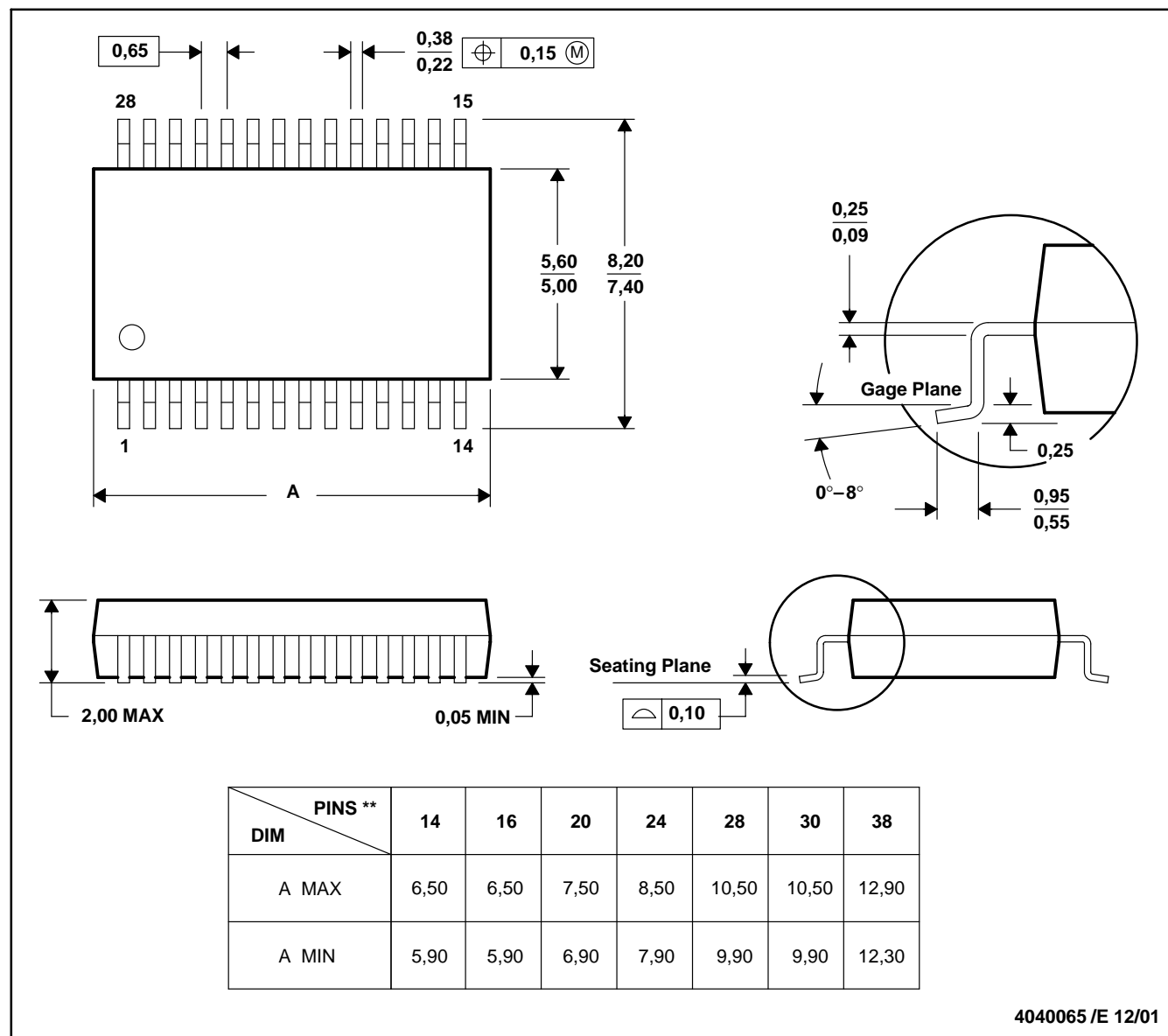


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

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