

SN74SSTL16847

20-BIT SSTL_3 INTERFACE BUFFER WITH 3-STATE OUTPUTS

SCBS709A – OCTOBER 1997 – REVISED MAY 1998

- Member of the Texas Instruments Widebus™ Family
- Supports SSTL_3 Signal Inputs and Outputs
- Flow-Through Architecture Optimizes PCB Layout
- Meets SSTL_3 Class I and Class II Specifications
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- Packaged in Plastic Thin Shrink Small-Outline Package

description

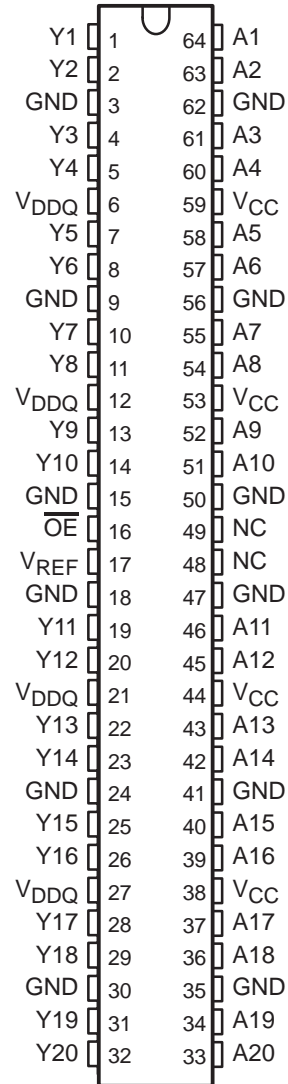
This 20-bit buffer is designed for 3-V to 3.6-V V_{CC} operation and SSTL_3 input levels.

Data flow from A to Y is controlled by the output-enable (\overline{OE}). When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74SSTL16847 is characterized for operation from 0°C to 70°C.

**DGG PACKAGE
(TOP VIEW)**



NC – No internal connection



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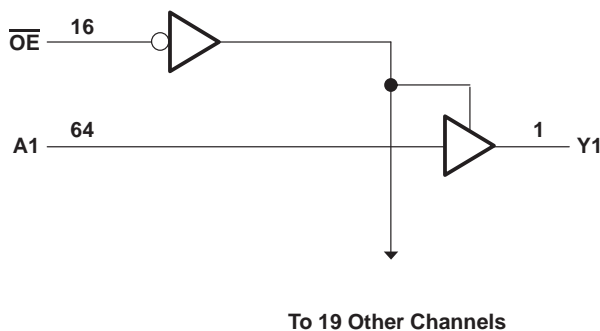
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FUNCTION TABLE

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} or V_{DDQ}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	–0.5 V to $V_{DDQ} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ})	±50 mA
Continuous current through each V_{CC} , V_{DDQ} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3):	73°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. This current will flow only when the output is in the high state and $V_O > V_{DDQ}$.
 3. The package thermal impedance is calculated in accordance with JESD 51.

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recommended operating conditions (see Note 4)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	V _{DDQ}		3.6	V
V _{DDQ}	Output supply voltage	3		3.6	V
V _{REF}	Reference voltage (V _{REF} = 0.45 × V _{DDQ})	1.3	1.5	1.7	V
V _{TT}	Termination voltage	V _{REF} -50mV	V _{REF}	V _{REF} +50mV	V
V _I	Input voltage	0		V _{CC}	V
V _{IH}	AC high-level input voltage	All inputs		V _{REF} +400mV	V
V _{IL}	AC low-level input voltage	All inputs		V _{REF} -400mV	V
V _{IH}	DC high-level input voltage	All inputs		V _{REF} +200mV	V
V _{IL}	DC low-level input voltage	All inputs		V _{REF} -200mV	V
I _{OH}	High-level output current			-20	mA
I _{OL}	Low-level output current			20	
T _A	Operating free-air temperature	0		70	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{IK}		I _I = -18 mA	3 V			-1.2	V
V _{OH}		I _{OH} = -100 μA	3 V to 3.6 V	V _{CC} -0.2			V
		I _{OH} = -16 mA	3 V	2.2			
		I _{OH} = -20 mA		2.1			
V _{OL}		I _{OL} = 100 μA	3 V to 3.6 V			0.2	V
		I _{OL} = 16 mA	3 V			0.5	
		I _{OL} = 20 mA				0.55	
I _I	Data inputs, \overline{OE}	V _I = 2.1 V or 0.9 V, V _{REF} = 1.3 V or 1.7 V	3.6 V			±5	μA
	V _{REF}	V _{REF} = 1.3 V or 1.7 V				±150	
I _{OZ}		V _O = 0.9 V or 2.1 V	3.6 V			±10	μA
I _{CC}		V _I = 2.1 V or 0.9 V, I _O = 0	3.6 V			90	mA
C _i	Control inputs	V _I = 2.1 V or 0.9 V	3.3 V			2	pF
	A port					2.5	
C _o	Y port	V _O = 2.1 V or 0.9 V	3.3 V			3.5	pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

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**switching characteristics over recommended operating free-air temperature range,
 Class I, $V_{REF} = V_{TT} = V_{DDQ} \times 0.45$ and $C_L = 10$ pF (unless otherwise noted) (see Figure 1)**

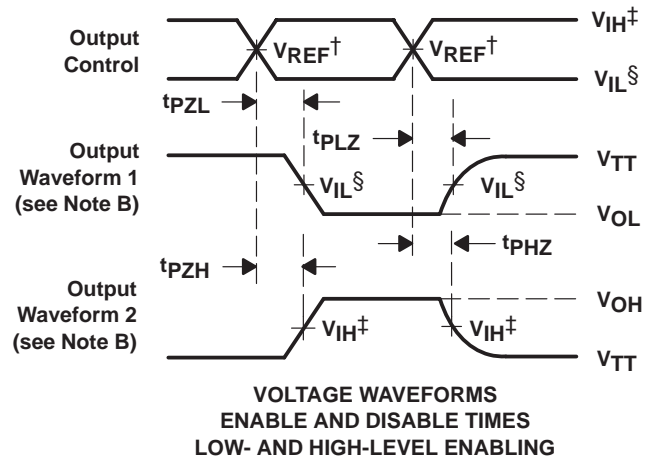
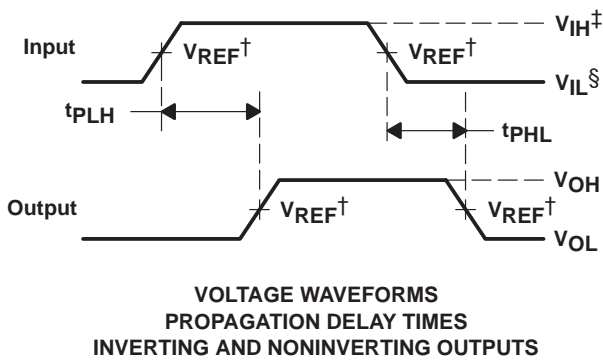
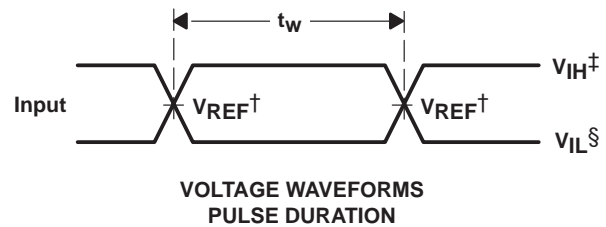
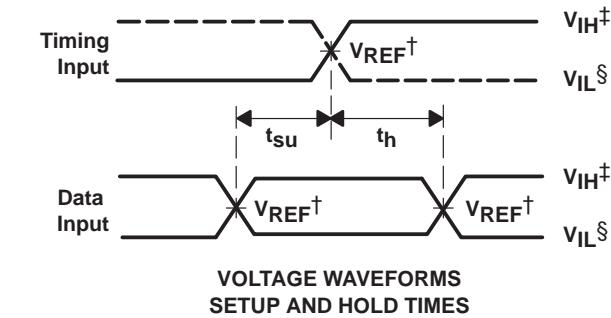
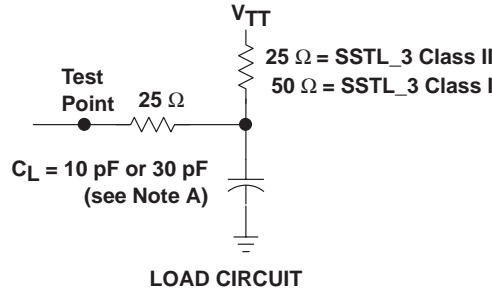
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}	A	Y	1.5	3	ns
t_{en}	\overline{OE}	Y	1.5	4	ns
t_{dis}	\overline{OE}	Y	1.6	4.9	ns

**switching characteristics over recommended operating free-air temperature range,
 Class II, $V_{REF} = V_{TT} = V_{DDQ} \times 0.45$ and $C_L = 30$ pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}	A	Y	1.5	3	ns
t_{en}	\overline{OE}	Y	1.5	4.1	ns
t_{dis}	\overline{OE}	Y	1.5	4.8	ns



PARAMETER MEASUREMENT INFORMATION



† $V_{REF} = 0.45 V_{DDQ}$

‡ $V_{IH} = V_{REF} + 400\text{mV}$ (AC voltage levels)

§ $V_{IL} = V_{REF} - 400\text{mV}$ (AC voltage levels)

NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 1.25\text{ ns/V}$, $t_f \leq 1.25\text{ ns/V}$.

D. The outputs are measured one at a time with one transition per measurement.

E. $V_{TT} = V_{REF} = V_{DDQ} \times 0.45$

F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

G. t_{PZL} and t_{PZH} are the same as t_{en} .

H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74SSTL16847DGGRE4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74SSTL16847DGGRG4	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74SSTL16847DGGR	ACTIVE	TSSOP	DGG	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

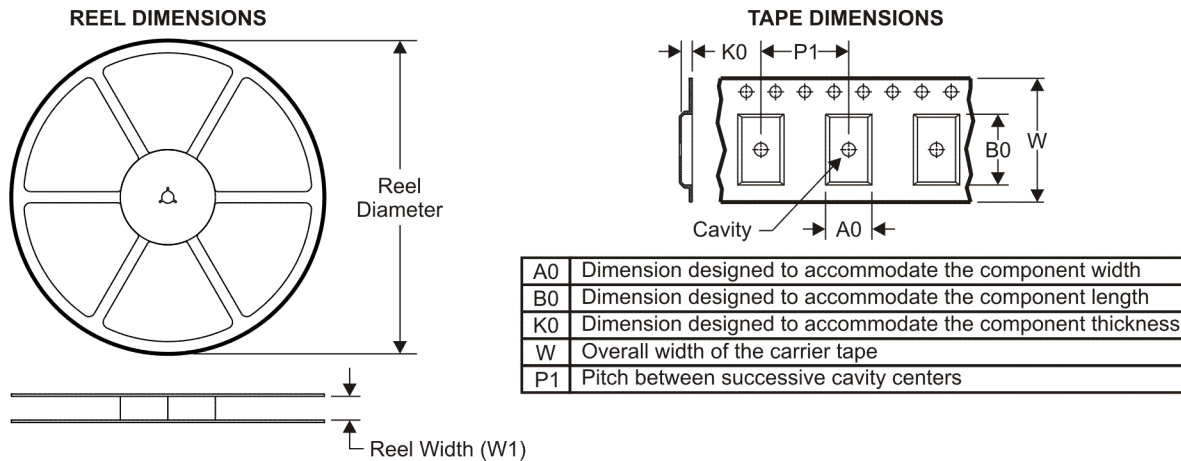
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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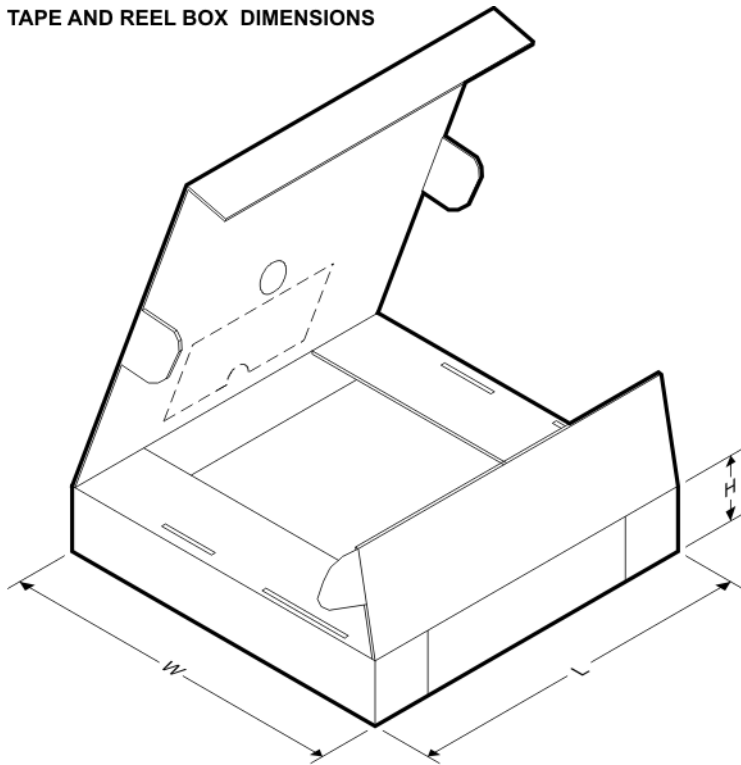
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74SSTL16847DGGR	TSSOP	DGG	64	2000	330.0	24.4	8.4	17.3	1.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



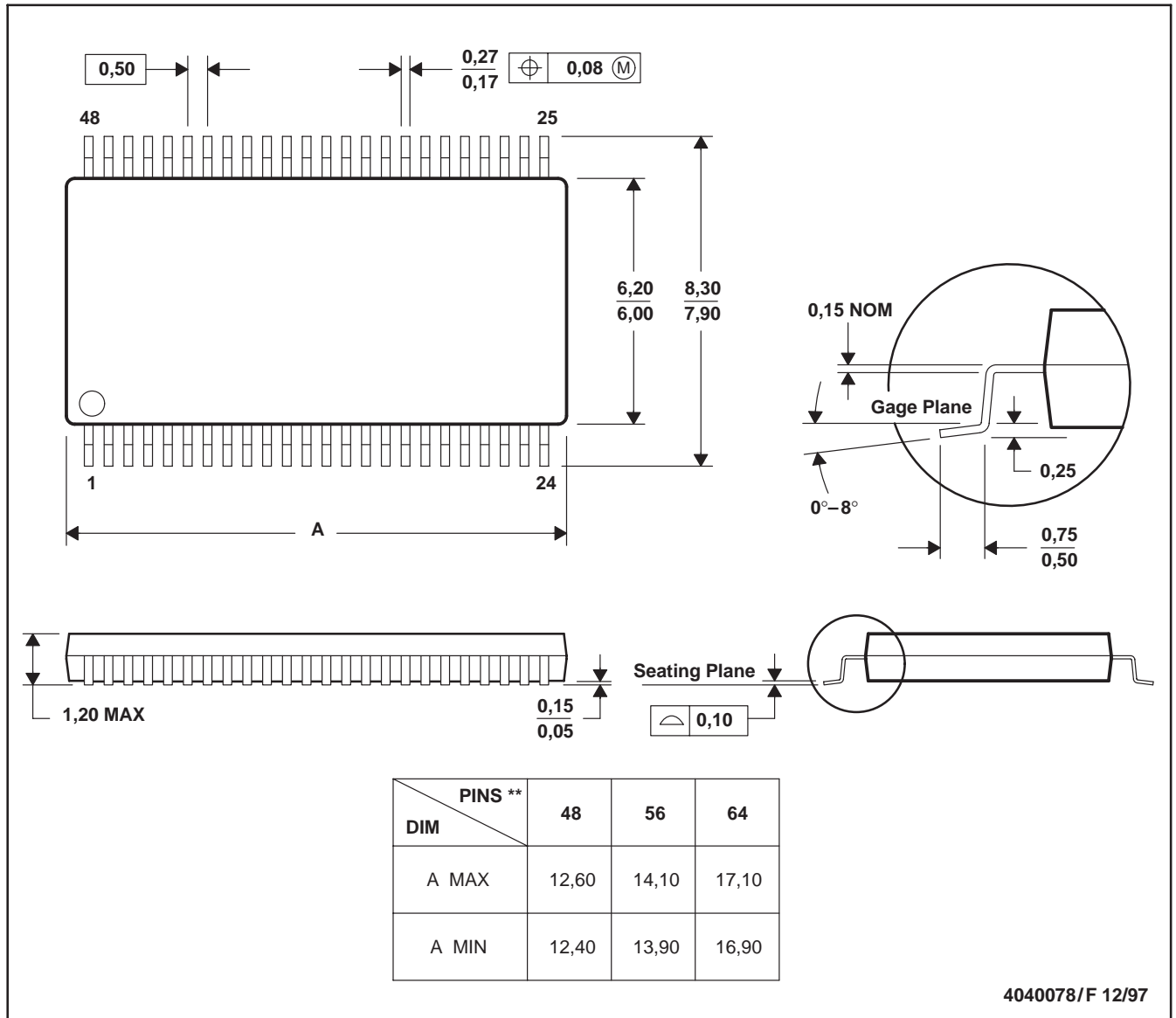
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74SSTL16847DGGR	TSSOP	DGG	64	2000	346.0	346.0	41.0

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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