

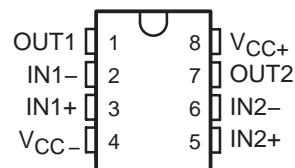
TL3414A

DUAL HIGH-OUTPUT-CURRENT OPERATIONAL AMPLIFIER

SLOS453A – DECEMBER 2004 – REVISED JANUARY 2005

- Single/Dual Power-Supply Operation
- High Output Current . . . 70 mA, $V_{CC+} = 5\text{ V}$
- Wide Operating Voltage . . . 3 V to 15 V (Single Supply)
- Ideal for Headphone Drivers

D (SOIC), P (PDIP), OR PW (TSSOP) PACKAGE
(TOP VIEW)



description/ordering information

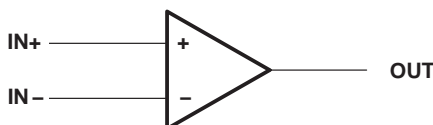
The TL3414A device is a dual operational amplifier that can be operated with single or dual power supplies. In addition to high gain and high output voltage swing, it is capable of driving a 70-mA load, making it ideally suited for simple, low-cost audio-amplifier applications, such as headphone amplifiers in DVD and CDRW applications.

ORDERING INFORMATION

| TA | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------|--------------|-----------------------|------------------|
| -40°C to 85°C | PDIP (P) | Tube of 50 | TL3414AIP | TL3414AIP |
| | SOIC (D) | Tube of 75 | TL3414AID | Z3414A |
| | | Reel of 2500 | TL3414AIDR | |
| | TSSOP (PW) | Tube of 150 | TL3414AIPW | Z3414A |
| | | Reel of 2000 | TL3414AIPWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

symbol (each amplifier)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

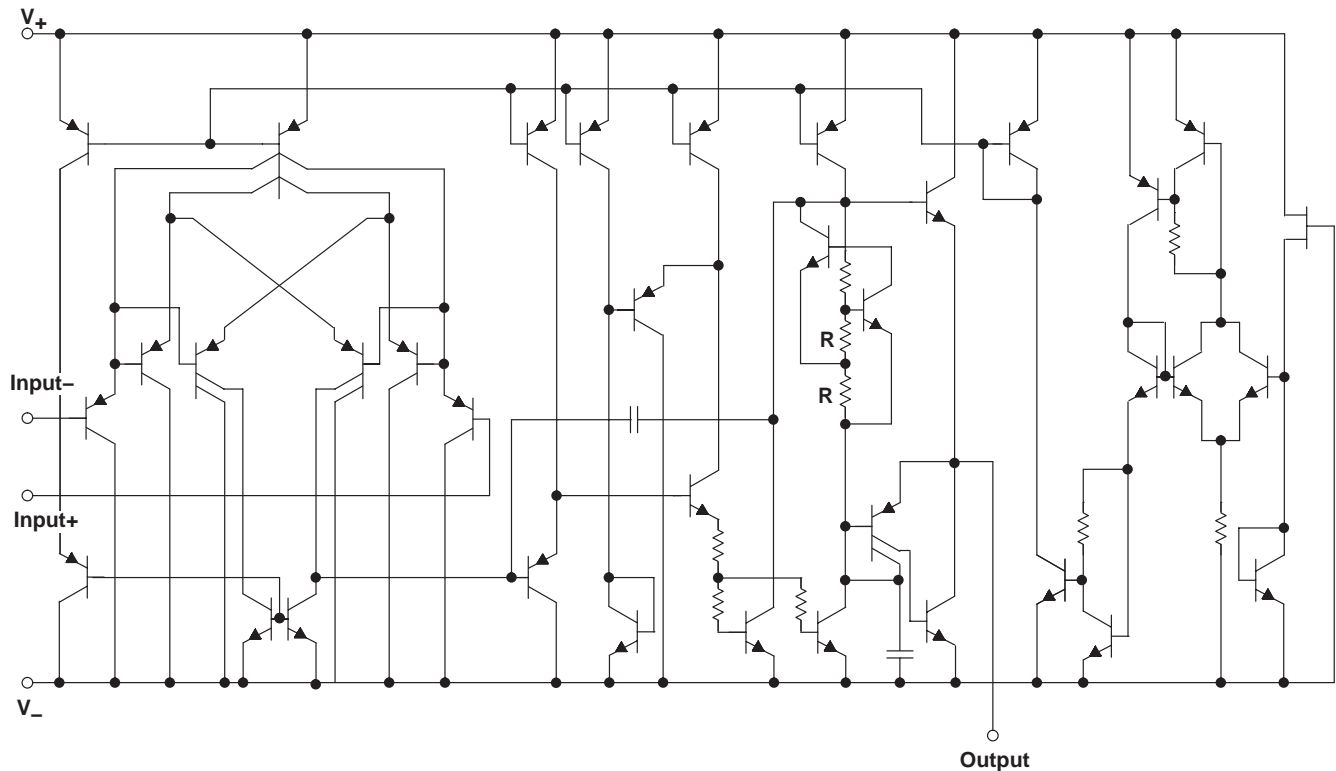
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TL3414A DUAL HIGH-OUTPUT-CURRENT OPERATIONAL AMPLIFIER

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simplified schematic



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|------------------------|
| Supply voltage, V_{CC+} (single supply) | 15 V |
| Supply voltage, V_{CC-} (single supply) | 0 V |
| Supply voltage, V_{CC+} (dual supply) | 7.5 V |
| Supply voltage, V_{CC-} (dual supply) | -7.5 V |
| Supply voltage, (V_{CC-} to V_{CC+}) | 15 V |
| Input voltage, either input (see Note 1) | V_{CC-} or V_{CC+} |
| Input current (see Note 2) | ± 10 mA |
| Duration of output short circuit (see Note 3) | Unlimited |
| Package thermal impedance, θ_{JA} (see Notes 4 and 5): D package | 97°C/W |
| P package | 85°C/W |
| PW package | 149°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Storage temperature range, T_{stg} | -40°C to 125°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
 2. Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
 3. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
 4. Maximum power dissipation is a function of $T_J(\max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
 5. The package thermal impedance is calculated in accordance with JESD 51-7.

TL3414A

DUAL HIGH-OUTPUT-CURRENT OPERATIONAL AMPLIFIER

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recommended operating conditions

| | | MIN | MAX | UNIT |
|-----------|--------------------------------------|------|------|------|
| V_{CC} | Supply voltage (single supply) | 3 | 15 | V |
| V_{CC+} | Supply voltage (dual supply) | 1.5 | 7.5 | V |
| V_{CC-} | Supply voltage (dual supply) | -1.5 | -7.5 | V |
| V_{ID} | Differential input voltage | | 15 | V |
| V_I | Input voltage | -0.3 | 15 | V |
| T_A | Operating free-air temperature range | -40 | 85 | °C |

DC electrical characteristics, $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-------------------|---|---|------------------------|-----|------|----|
| V_{IO} | Input offset voltage $R_S = 0\ \Omega$ | | 2 | 5 | mV | |
| I_{IO} | Input offset current | | 15 | 100 | nA | |
| I_{IB} | Input bias current | | 300 | 600 | nA | |
| A_{VD} | Large-signal differential voltage amplification $R_L = 2\text{ k}\Omega$ | | 77 | 100 | dB | |
| V_{ICR} | Common-mode input voltage range | | $V_{CC+} - 2\text{ V}$ | | V | |
| V_{OM} | Output voltage swing $R_L > 2\text{ k}\Omega$, $V_{CC+} = 5\text{ V}$ | | 3.5 | | V | |
| | | $I_O = 70\text{ mA}$, $V_{CC+} = 5\text{ V}$ | 3.2 | | | |
| CMRR | Common-mode rejection ratio | | 70 | 79 | dB | |
| k_{SVR}^\dagger | Supply-voltage rejection ratio | | 80 | 90 | dB | |
| I_{CC} | Supply current (all amplifiers) $R_L = \text{open circuit}$ (full temperature range) | | 3 | 4 | 6 | mA |

† Measured with $V_{CC\pm}$ differentially and simultaneously varied from 5 V to 8.6 V

AC electrical characteristics, $V_{CC+} = 5\text{ V}$, $V_{CC-} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------|--|------|------------------------|
| SR | Slew rate at unity gain | 0.83 | V/ μs |
| GBW | Gain bandwidth product | 1.1 | MHz |
| V_n | Equivalent input noise voltage $f = 1\text{ kHz}$ | 18 | nV/ $\sqrt{\text{Hz}}$ |

DC electrical characteristics, $V_{CC+} = 8.6\text{ V}$, $V_{CC-} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|-------------------|---|---|------------------------|-----|------|----|
| V_{IO} | Input offset voltage $R_S = 0\ \Omega$ | | 2 | 5 | mV | |
| I_{IO} | Input offset current | | 15 | 100 | nA | |
| I_{IB} | Input bias current | | 300 | 600 | nA | |
| A_{VD} | Large-signal differential voltage amplification $R_L = 2\text{ k}\Omega$ | | 88 | 105 | dB | |
| V_{ICR} | Common-mode input voltage range | | $V_{CC+} - 2\text{ V}$ | | V | |
| V_{OM} | Output voltage swing $R_L > 2\text{ k}\Omega$, $V_{CC+} = 8.6\text{ V}$ | | 7 | | V | |
| | | $I_O = 70\text{ mA}$, $V_{CC+} = 8.6\text{ V}$ | 6.7 | | | |
| CMRR | Common-mode rejection ratio | | 80 | 90 | dB | |
| k_{SVR}^\dagger | Supply-voltage rejection ratio | | 80 | 90 | dB | |
| I_{CC} | Supply current (all amplifiers) $R_L = \text{open circuit}$ (full temperature range) | | 3 | 4 | 6 | mA |

† Measured with $V_{CC\pm}$ differentially and simultaneously varied from 5 V to 8.6 V

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AC electrical characteristics, $V_{CC+} = 8.6\text{ V}$, $V_{CC-} = 0\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TYP | UNIT |
|-----------|--------------------------------|--------------------|-----|------------------------------|
| SR | Slew rate at unity gain | | 1.3 | V/ μs |
| GBW | Gain bandwidth product | | 2 | MHz |
| V_n | Equivalent input noise voltage | $f = 1\text{ kHz}$ | 18 | $\text{nV}/\sqrt{\text{Hz}}$ |

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|----------------------|------------------------------|-----------------------------|
| TL3414AID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIDE4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIDRE4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIP E4 | ACTIVE | PDIP | P | 8 | | TBD | Call TI | Call TI | |
| TL3414AIPW | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIPWE4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIPWG4 | ACTIVE | TSSOP | PW | 8 | 150 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIPWR | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIPWRE4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TL3414AIPWRG4 | ACTIVE | TSSOP | PW | 8 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL3414AIDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TL3414AIPWR | TSSOP | PW | 8 | 2000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

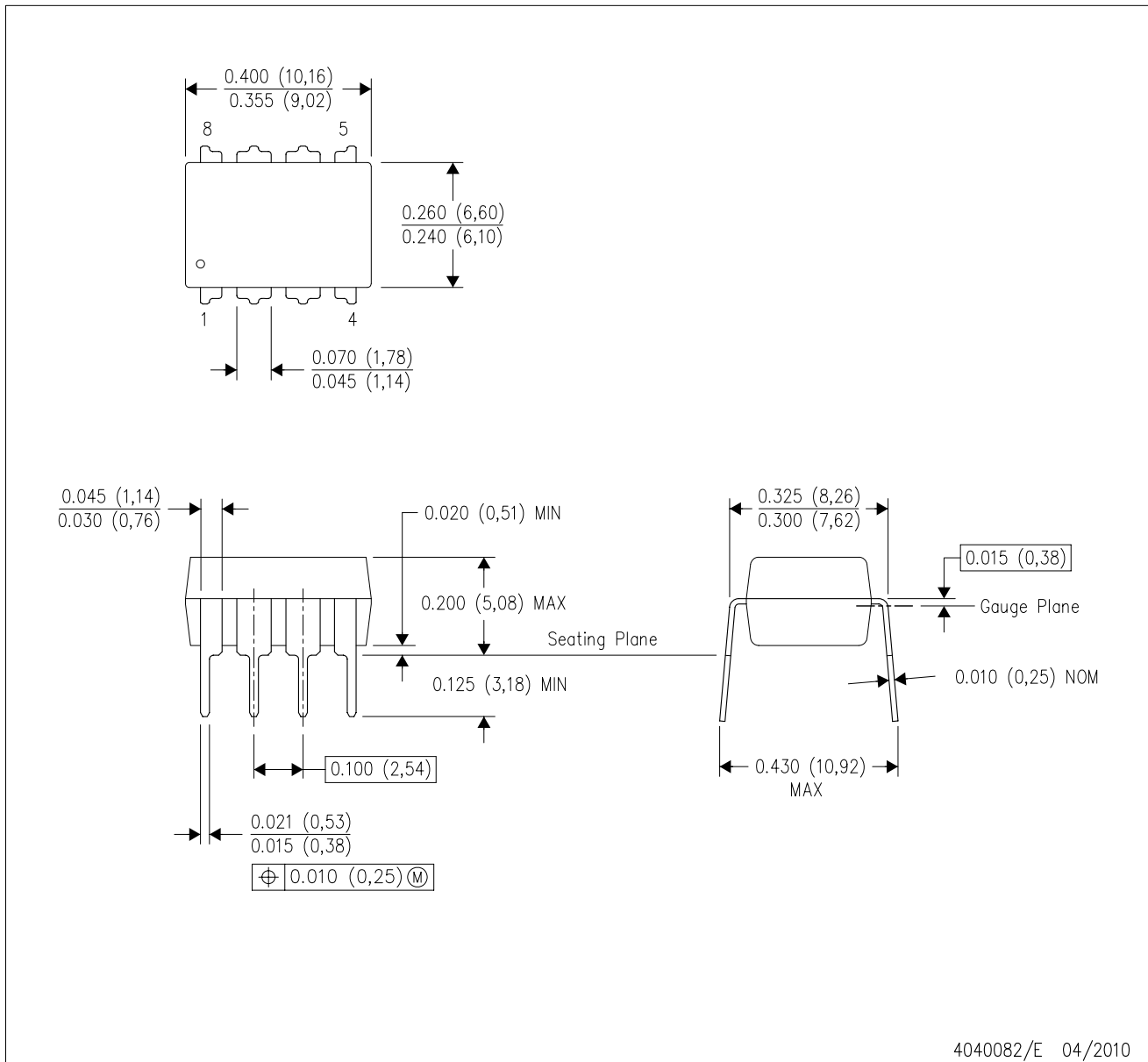


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL3414AIDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TL3414AIPWR | TSSOP | PW | 8 | 2000 | 346.0 | 346.0 | 29.0 |

P (R-PDIP-T8)

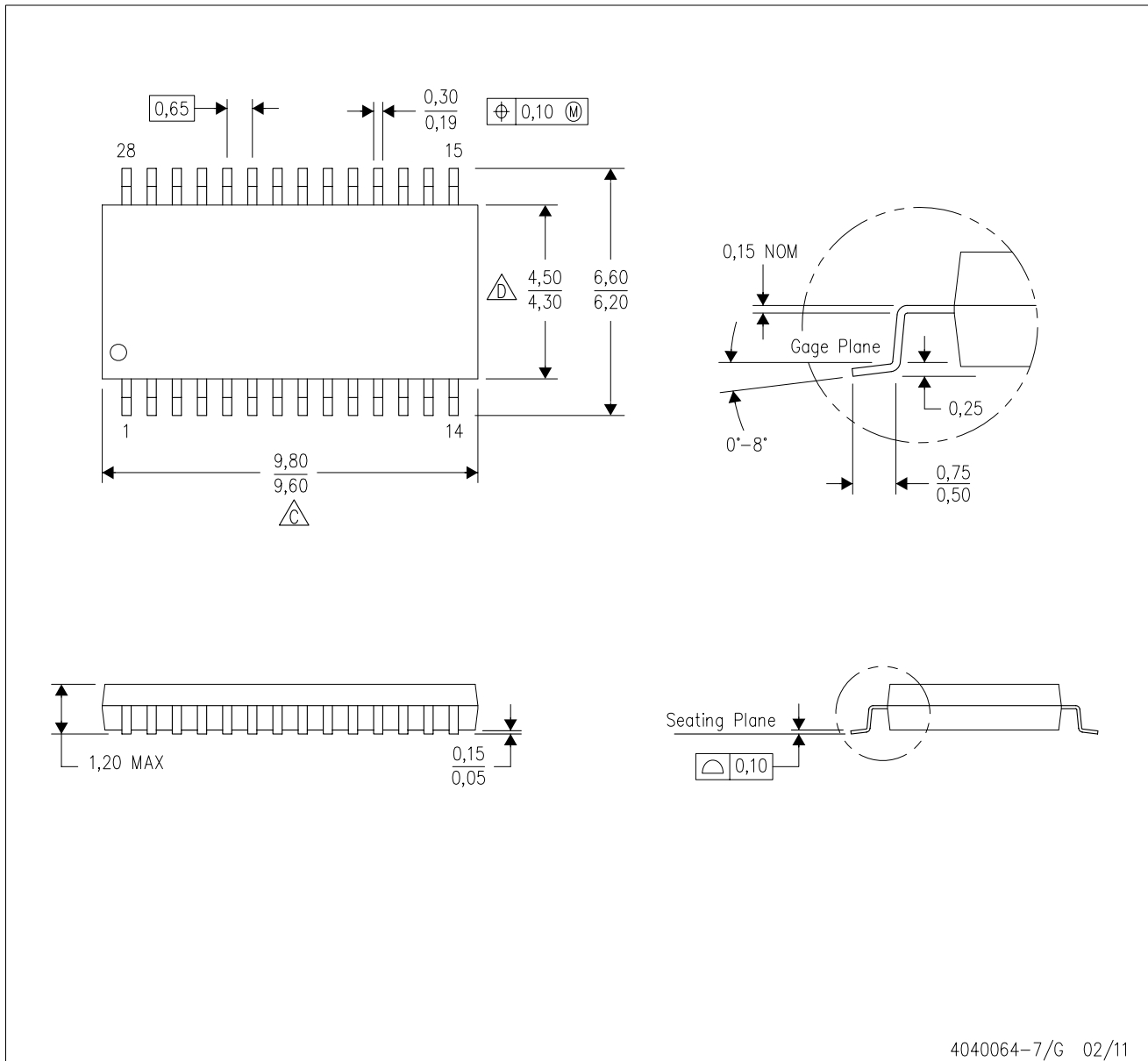
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

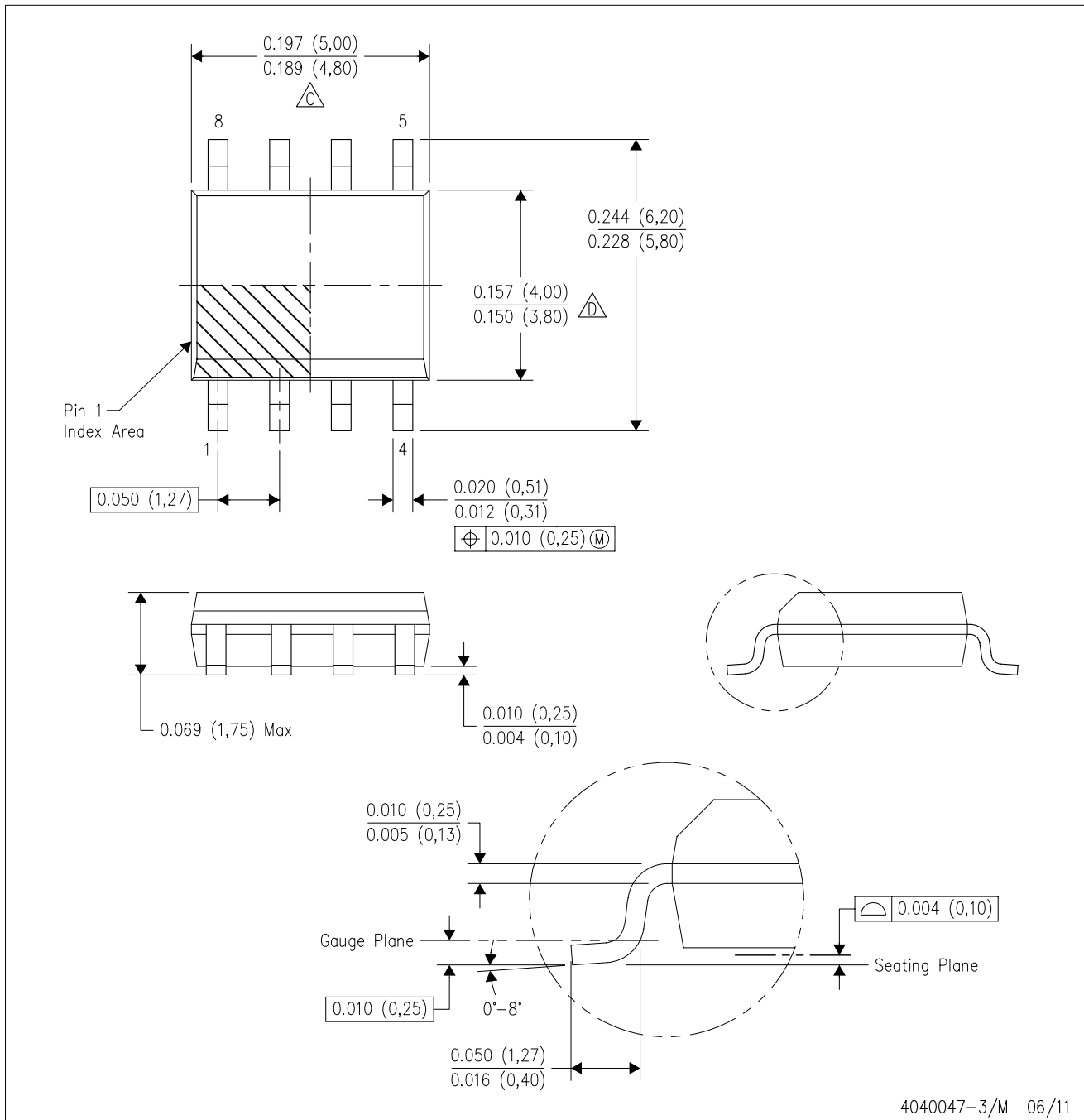




4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

D (R-PDSO-G8)

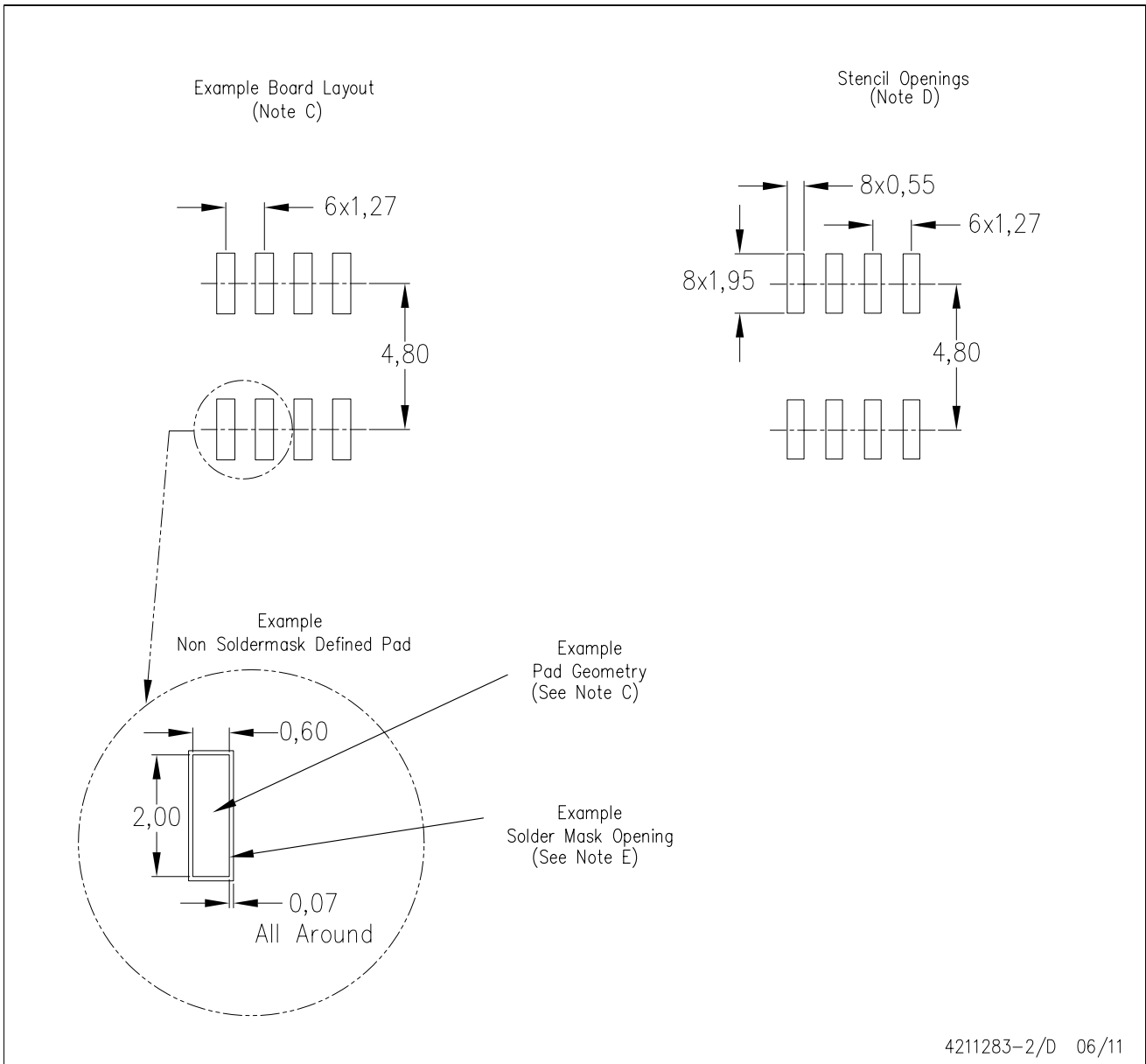
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

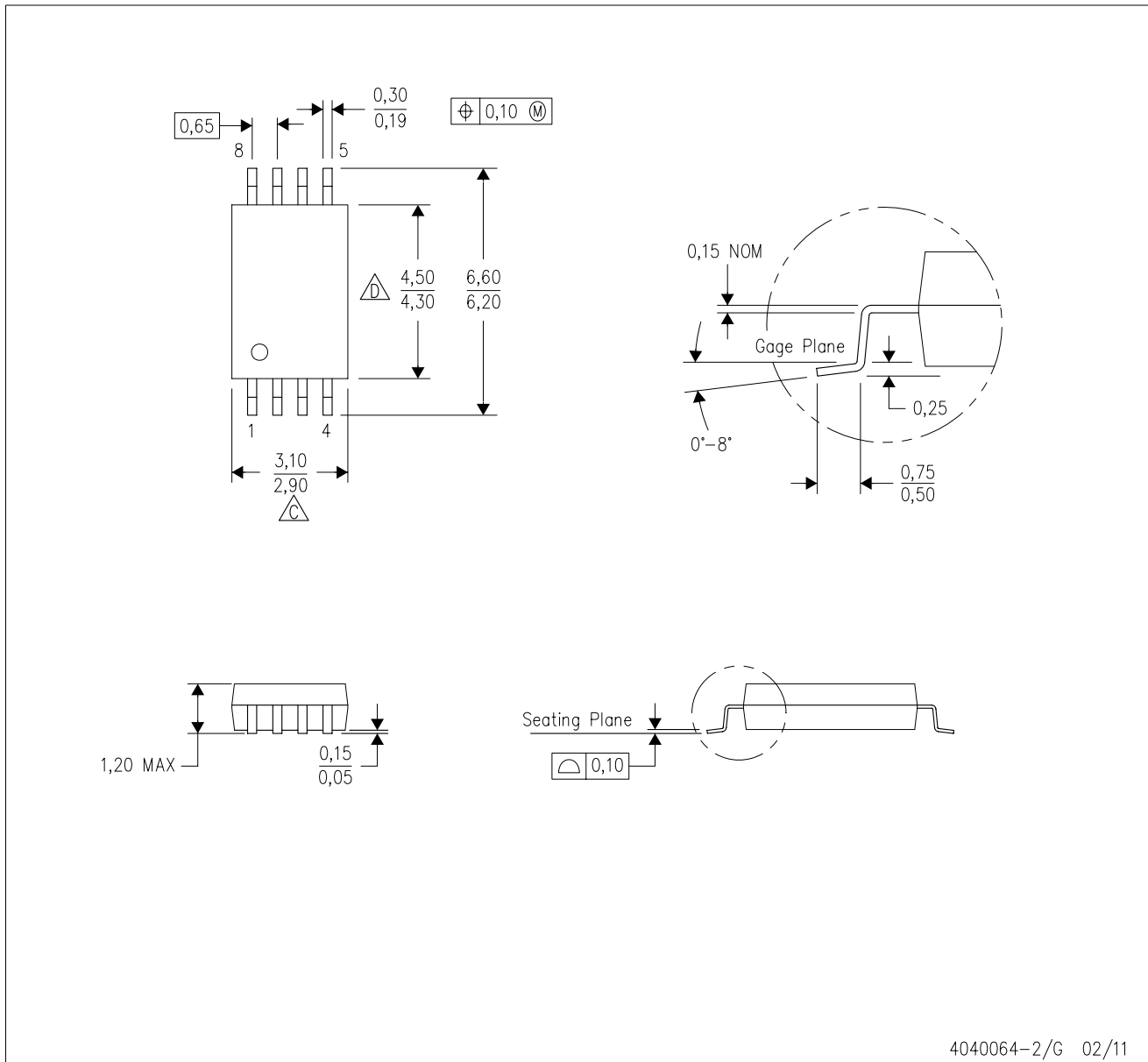
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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