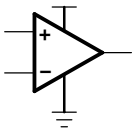
# FAMILY OF LOW-POWER WIDE BANDWIDTH SINGLE SUPPLY OPERATIONAL AMPLIFIERS WITH SHUTDOWN

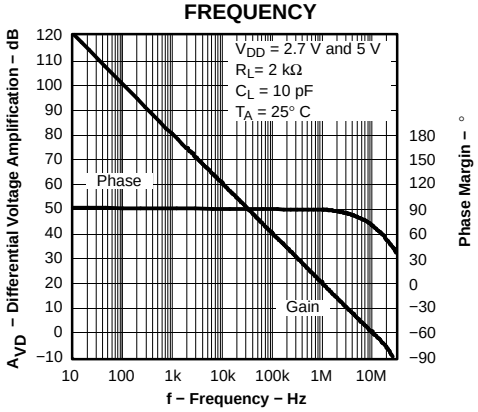
## FEATURES

- CMOS Rail-To-Rail Output
- $V_{ICR}$ Includes Positive Rail
- Wide Bandwidth . . . 11 MHz
- Slew Rate . . . 10 V/µs
- Supply Current . . . 800 µA/Channel
- Input Noise Voltage . . . 27 nV/$\sqrt{Hz}$
- Ultralow Power-Down Mode: $I_{DD(SHDN)}$ = 4 µA/Channel
- Supply Voltage Range . . . 2.7 V to 5.5 V
- Specified Temperature Range: -40°C to 125°C . . . Industrial Grade
- Ultrasmall Packaging: 5 or 6 Pin SOT-23 (TLV2620/1) 8 or 10 Pin MSOP (TLV2622/3)
- Universal Opamp EVM (See SLOU060 for More Information)

**Operational Amplifier**



**DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE vs FREQUENCY**




## DESCRIPTION

The TLV262x single supply operational amplifiers provide rail-to-rail output with an input range that includes the positive rail. The TLV262x takes the minimum operating supply voltage down to 2.7 V over the extended industrial temperature range (-40°C to 125°C) while adding the rail-to-rail output swing feature. The TLV262x also provides 11-MHz bandwidth from only 800 µA of supply current. The maximum recommended supply voltage is 5.5 V, which, when coupled with a 2.7-V minimum, allows the devices to be operated from lithium ion cells. The combination of wide bandwidth, low noise, and low distortion makes it ideal for high speed and high resolution data converter applications. The positive input range allows it to directly interface to positive rail referred systems. All members are available in PDIP and SOIC with the singles in the small SOT-23 package, duals in the MSOP, and quads in the TSSOP package.

The 2.7-V operation makes it compatible with Li-Ion powered systems and the operating supply voltage range of many micro-power micro-controllers available today including TI's MSP430.

**AMPLIFIER SELECTION TABLE**

| DEVICE | $V_{DD}$ [V] | $I_{DD}$/ch [µA] | $V_{IO}$ [µV] | $I_{IB}$ [pA] | $V_{ICR}$ [V] | GBW [MHz] | SLEW RATE [V/µs] | $V_n$, 1 kHz [nV/$\sqrt{Hz}$] | $I_O$ [mA] | SHUT-DOWN |
|---|---|---|---|---|---|---|---|---|---|---|
| TLV262x | 2.7-5.5 | 750 | 250 | 1 | 1 V to $V_{DD}$ + 0.2 | 11 | 10 | 27 | 28 | Y |
| TLV263x | 2.7-5.5 | 750 | 250 | 1 | GND to $V_{DD}$ - 0.8 | 10 | 9 | 27 | 28 | Y |
| TLV278x | 1.8-3.6 | 650 | 250 | 2.5 | -0.2 to $V_{DD}$ + 0.2 | 8 | 5 | 9 | 10 | Y |
| TLC07x | 4.5 - 16 | 1900 | 60 | 1.5 | 0.5 to $V_{DD}$ - 0.8 | 10 | 19 | 7 | 55 | Y |
| TLC08x | 4.5 - 16 | 1900 | 60 | 3 | GND to $V_{DD}$ - 1 | 10 | 19 | 8.5 | 55 | Y |

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## TLV2620 AND TLV2621 AVAILABLE OPTIONS(1)

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | | |
|---|---|---|---|---|---|
| | | SMALL OUTLINE (D)(2) | SOT-23 | | PLASTIC DIP (P) |
| | | | (DBV)(3) | SYMBOL | |
| -40°C to 125°C | 3500 µV | TLV2620ID<br>TLV2621ID | TLV2620IDBV<br>TLV2621IDBV | VBAI<br>VBBI | TLV2620IP<br>TLV2621IP |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2620IDR).
(3) The SOT23 package devices are only available taped and reeled. The **R** Suffix denotes quantities (3,000 pieces per reel). For smaller quantities (250 pieces per mini-reel), add a **T** suffix to the part number (e.g. TLV2620IDBVT).

## TLV2622 AND TLV2623 AVAILABLE OPTIONS(1)

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | SMALL OUTLINE(2) (D) | MSOP | | | | PLASTIC DIP (N) | PLASTIC DIP (P) |
| | | | (DGK)(2) | SYMBOL | (DGS)(2) | SYMBOL | | |
| -40°C to 125°C | 3500 µV | TLV2622ID<br>TLV2623ID | TLV2622IDGK<br>— | xxTIAKM<br>— | —<br>TLV2623IDGS | —<br>xxTIALC | —<br>TLV2623IN | TLV2622IP<br>— |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2622IDR).

## TLV2624 AND TLV2625 AVAILABLE OPTIONS(1)

| $T_A$ | $V_{IO}$max AT 25°C | PACKAGED DEVICES | | |
|---|---|---|---|---|
| | | SMALL OUTLINE (D)(2) | PLASTIC DIP (N) | TSSOP (PW) |
| -40°C to 125°C | 3500 µV | TLV2624ID<br>TLV2625ID | TLV2624IN<br>TLV2625IN | TLV2624IPW<br>TLV2625IPW |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This package is available taped and reeled. To order this packaging option, add an **R** suffix to the part number (e.g., TLV2624IDR).



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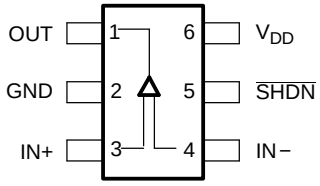
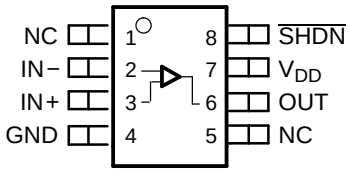
## TLV262X PACKAGE PINOUTS(1)

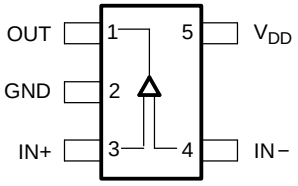
**TLV2620**
**DBV PACKAGE**
**(TOP VIEW)**



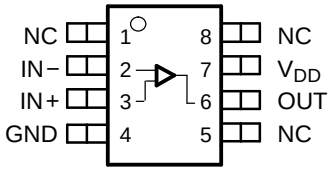

**TLV2620**
**D OR P PACKAGE**
**(TOP VIEW)**



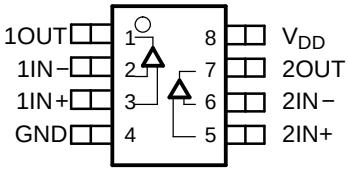

**TLV2621**
**DBV PACKAGE**
**(TOP VIEW)**



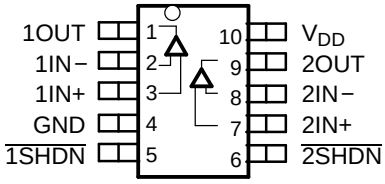

**TLV2621**
**D OR P PACKAGE**
**(TOP VIEW)**



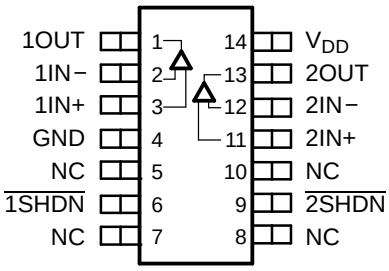

**TLV2622**
**D, DGK, OR P PACKAGE**
**(TOP VIEW)**



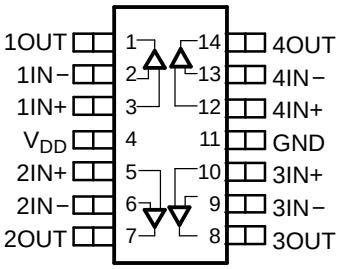

**TLV2623**
**DGS PACKAGE**
**(TOP VIEW)**



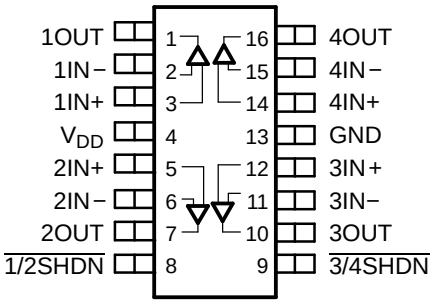

**TLV2623**
**D OR N PACKAGE**
**(TOP VIEW)**




**TLV2624**
**D, N, OR PW PACKAGE**
**(TOP VIEW)**




**TLV2625**
**D, N, OR PW PACKAGE**
**(TOP VIEW)**



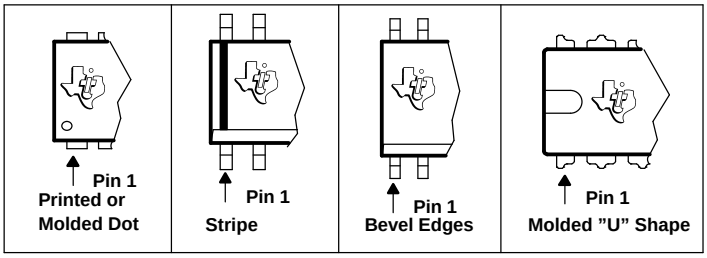

NC − No internal connection

$\overline{1/2SHDN}$ Pin (8) controls amplifiers 1 and 2.

$\overline{3/4SHDN}$ Pin (9) controls amplifiers 3 and 4.

(1) SOT-23 may or may not be indicated.

## TYPICAL PIN 1 INDICATORS




**NOTE:**

If there is not a Pin 1 indicator, turn device to enable reading the symbol from left to right. Pin 1 is at the lower left corner of the device.



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## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | |
|---|---|---|
| $V_{DD}$ | Supply voltage (2) | 6 V |
| $V_{ID}$ | Differential input voltage | $\pm V_{DD}$ |
| $V_I$ | Input voltage range (2) | +1 to $V_{DD}$ + 0.2 V |
| $I_I$ | Input current (any input) | ± 10 mA |
| $I_O$ | Output current | ±40 mA |
| | Continuous total power dissipation | See Dissipation Rating Table |
| $T_A$ | Operating free-air temperature range: I-suffix | -40°C to 125°C |
| $T_J$ | Maximum junction temperature | 150°C |
| $T_{stg}$ | Storage temperature range | -65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to GND.

## DISSIPATION RATING TABLE

| PACKAGE | $\theta_{JC}$ (°C/W) | $\theta_{JA}$ (°C/W) | $T_A \le 25°C$ POWER RATING | $T_A = 125°C$ POWER RATING |
|---|---|---|---|---|
| D (8) | 38.3 | 176 | 710 mW | 142 mW |
| D (14) | 26.9 | 122.3 | 1022 mW | 204.4 mW |
| D (16) | 25.7 | 114.7 | 1090 mW | 218 mW |
| DBV (5) | 55 | 324.1 | 385 mW | 77.1 mW |
| DBV (6) | 55 | 294.3 | 425 mW | 85 mW |
| DGK (8) | 54.2 | 259.9 | 481 mW | 96.1 mW |
| DGS (10) | 54.1 | 259.7 | 485 mW | 97 mW |
| N (14, 16) | 32 | 78 | 1600 mW | 320.5 mW |
| P (8) | 41 | 104 | 1200 mW | 240.4 mW |
| PW (14) | 29.3 | 173.6 | 720 mW | 144 mW |
| PW (16) | 28.7 | 161.4 | 774 mW | 154.9 mW |

## RECOMMENDED OPERATING CONDITIONS

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | Single supply | 2.7 | 5.5 | V |
| | | Split supply | ±1.35 | ±2.75 | |
| $V_{ICR}$ | Common-mode input voltage range | | 1 | $V_{DD}$+0.2 | V |
| $T_A$ | Operating free-air temperature | I-suffix | -40 | 125 | °C |
| | Shutdown on/off voltage level(1) | $V_{IL}$ | | 0.4 | V |
| | | $V_{IH}$ | 2 | | |

(1) Relative to GND.



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## ELECTRICAL CHARACTERISTICS

at specified free-air temperature, $V_{DD}$ = 2.7 V, 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **DC PERFORMANCE** | | | | | | | | |
| $V_{IO}$ | Input offset voltage | $V_{IC}$ = $V_{DD}$/2, $V_O$ = $V_{DD}$/2, $R_S$ = 50 Ω | | 25°C | | 250 | 3500 | μV |
| | | | | Full range | | | 4500 | |
| $\alpha_{VIO}$ | Temperature coefficient of input offset voltage | | | 25°C | | 3 | | μV/°C |
| CMRR | Common-mode rejection ratio | $V_{IC}$ = 1 to $V_{DD}$, $R_S$ = 50 Ω | $V_{DD}$ = 2.7 V | 25°C | 77 | 98 | | dB |
| | | | | Full range | 63 | | | |
| | | | $V_{DD}$ = 5 V | 25°C | 78 | 99 | | |
| | | | | Full range | 75 | | | |
| $A_{VD}$ | Large-signal differential voltage amplification | $V_{DD}$ = 2.7 V, $R_L$ = 2 kΩ, $V_{O(PP)}$ = 1.7 V | | 25°C | 90 | 100 | | dB |
| | | | | Full range | 82 | | | |
| | | $V_{DD}$ = 5 V, $R_L$ = 2 kΩ, $V_{O(PP)}$ = 4 V | | 25°C | 95 | 100 | | |
| | | | | Full range | 90 | | | |
| **INPUT CHARACTERISTICS** | | | | | | | | |
| $I_{IO}$ | Input offset current | $V_{IC}$ = $V_{DD}$/2, $V_O$ = $V_{DD}$/2, $R_S$ = 50Ω | | 25°C | | 2 | 50 | pA |
| | | | | Full Range | | | 100 | |
| $I_{IB}$ | Input bias current | | | 25°C | | 2 | 50 | |
| | | | | Full Range | | | 200 | |
| $r_{i(d)}$ | Differential input resistance | | | 25°C | | 100 | | GΩ |
| $C_{i(c)}$ | Common-mode input capacitance | f = 1 kHz | | 25°C | | 8 | | pF |
| **OUTPUT CHARACTERISTICS** | | | | | | | | |
| $V_{OH}$ | High-level output voltage | $V_{IC}$ = $V_{DD}$/2, $I_{OH}$ = -1 mA | $V_{DD}$ = 2.7 V | 25°C | 2.6 | 2.67 | | V |
| | | | | Full range | 2.55 | | | |
| | | | $V_{DD}$ = 5 V | 25°C | 4.95 | 4.98 | | |
| | | | | Full range | 4.9 | | | |
| | | $V_{IC}$ = $V_{DD}$/2, $I_{OH}$ = -10 mA | $V_{DD}$ = 2.7 V | 25°C | 2.3 | 2.43 | | |
| | | | | Full range | 2.2 | | | |
| | | | $V_{DD}$ = 5 V | 25°C | 4.7 | 4.8 | | |
| | | | | Full range | 4.6 | | | |
| $V_{OL}$ | Low-level output voltage | $V_{IC}$ = $V_{DD}$/2, $I_{OL}$ = 1 mA | $V_{DD}$ = 2.7 V | 25°C | | 0.03 | 0.1 | V |
| | | | | Full range | | | 0.15 | |
| | | | $V_{DD}$ = 5 V | 25°C | | 0.025 | 0.05 | |
| | | | | Full range | | | 0.1 | |
| | | $V_{IC}$ = $V_{DD}$/2, $I_{OL}$ = 10 mA | $V_{DD}$ = 2.7 V | 25°C | | 0.26 | 0.4 | |
| | | | | Full range | | | 0.45 | |
| | | | $V_{DD}$ = 5 V | 25°C | | 0.2 | 0.25 | |
| | | | | Full range | | | 0.35 | |
| $I_O$ | Output current | $V_{DD}$ = 2.7 V, $V_O$ = 0.5 V from rail | Sourcing | 25°C | | 14 | | mA |
| | | | Sinking | | | 19 | | |
| | | $V_{DD}$ = 5 V, $V_O$ = 0.5 V from rail | Sourcing | | | 28 | | |
| | | | Sinking | | | 28 | | |
| $I_{OS}$ | Short-circuit output current | Sourcing | $V_{DD}$ = 2.7 V | 25°C | | 50 | | mA |
| | | | $V_{DD}$ = 5 V | | | 95 | | |
| | | Sinking | $V_{DD}$ = 2.7 V | | | 50 | | |
| | | | $V_{DD}$ = 5 V | | | 95 | | |

(1) Full range is -40°C to 125°C for the I-suffix.



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## ELECTRICAL CHARACTERISTICS (continued)

at specified free-air temperature, $V_{DD}$ = 2.7 V, 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A$ (1) | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | |
| $I_{DD}$ | Supply current (per channel) | $V_O = V_{DD}/2$, | $\overline{SHDN} = V_{DD}$ | 25°C | | 800 | 1000 | µA |
| | | | | Full range | | | 1300 | |
| PSRR | Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$) | $V_{DD}$ = 2.7 V to 3.3 V, $V_{IC} = V_{DD}/2$ | No load | 25°C | 80 | 98 | | dB |
| | | | | Full range | 75 | | | |
| | | $V_{DD}$ = 2.7 V to 5 V, $V_{IC} = V_{DD}/2$ | | 25°C | 75 | 90 | | |
| | | | | Full range | 70 | | | |
| **DYNAMIC PERFORMANCE** | | | | | | | | |
| UGBW | Unity gain bandwidth | $R_L$ = 2 kΩ, $C_L$ = 10 pF | | 25°C | | 11 | | MHz |
| SR+ | Positive slew rate at unity gain | $R_L$ = 2 kΩ, $C_L$ = 50 pF | $V_{DD}$ = 2.7 V, $V_{O(PP)}$ = 1.7 V | 25°C | 3.5 | 4.5 | | V/µs |
| | | | | Full range | 2.7 | | | |
| | | | $V_{DD}$ = 5 V, $V_{O(PP)}$ = 3.5 V | 25°C | 5.4 | 7 | | |
| | | | | Full range | 3.4 | | | |
| SR- | Negative slew rate at unity gain | $R_L$ = 2 kΩ, $C_L$ = 50 pF | $V_{DD}$ = 2.7 V, $V_{O(PP)}$ = 1.7 V | 25°C | 2.7 | 5 | | V/µs |
| | | | | Full range | 2.3 | | | |
| | | | $V_{DD}$ = 5 V, $V_{O(PP)}$ = 3.5 V | 25°C | 4.5 | 6 | | |
| | | | | Full range | 3.2 | | | |
| $\phi_m$ | Phase margin | $R_L$ = 2 kΩ, $C_L$ = 10 pF | | 25°C | | 63° | | |
| | Gain margin | | | | | 8 | | dB |
| **NOISE/DISTORTION PERFORMANCE** | | | | | | | | |
| THD + N | Total harmonic distortion plus noise | $V_{O(PP)} = V_{DD}/2$, $R_L$ = 2 kΩ, f = 10 kHz | $A_V$ = 1 | 25°C | | 0.002% | | |
| | | | $A_V$ = 10 | | | 0.019% | | |
| | | | $A_V$ = 100 | | | 0.095% | | |
| $V_n$ | Equivalent input noise voltage | f = 1 kHz | | | | 53 | | nV/√Hz |
| | | f = 10 kHz | | | | 27 | | |
| $I_n$ | Equivalent input noise current | f = 1 kHz | | | | 0.9 | | fA/√Hz |
| **SHUTDOWN CHARACTERISTICS** | | | | | | | | |
| $I_{DD(SHDN)}$ | Supply current, per channel in shutdown mode (TLV2620, TLV2623, TLV2625) | $\overline{SHDN}$ = 0.4 V | | 25°C | | 4 | 11 | µA |
| | | | | Full range | | | 13 | |
| $t_{(on)}$ | Amplifier turnon time (2) | $R_L$ = 2 kΩ | $V_{DD}$ = 2.7 V | 25°C | | 4.5 | | µs |
| | | | $V_{DD}$ = 5 V | | | 1.5 | | |
| $t_{(off)}$ | Amplifier turnoff time (2) | $R_L$ = 2 kΩ | | | | 200 | | ns |

(2) Disable time and enable time are defined as the interval between application of the logic signal to $\overline{SHDN}$ and the point at which the supply current has reached half its final value.



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## TYPICAL CHARACTERISTICS

### TABLE OF GRAPHS

| | | | FIGURE |
|---|---|---|---|
| $V_{IO}$ | Input offset voltage | vs Common-mode input voltage | 1, 2 |
| CMRR | Common-mode rejection ratio | vs Frequency | 3 |
| $V_{OH}$ | High-level output voltage | vs High-level output current | 4, 6 |
| $V_{OL}$ | Low-level output voltage | vs Low-level output current | 5, 7 |
| $I_{DD}$ | Supply current | vs Supply voltage | 8 |
| $I_{DD}$ | Supply current | vs Free-air temperature | 9 |
| PSRR | Power supply rejection ratio | vs Frequency | 10 |
| $A_{VD}$ | Differential voltage amplification & phase | vs Frequency | 11 |
| | Gain-bandwidth product | vs Free-air temperature | 12 |
| SR | Slew rate | vs Supply voltage | 13 |
| | | vs Free-air temperature | 14, 15 |
| $\phi_m$ | Phase margin | vs Load capacitance | 16 |
| $V_n$ | Equivalent input noise voltage | vs Frequency | 17 |
| | Voltage-follower large-signal pulse response | | 18 |
| | Voltage-follower small-signal pulse response | | 19 |
| | Crosstalk | vs Frequency | 20 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Free-air temperature | 21 |
| $I_{DD(SHDN)}$ | Shutdown supply current | vs Supply voltage | 22 |
| $I_{DD(SHDN)}$ | Shutdown supply current/output voltage | vs Time | 23 |

**INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

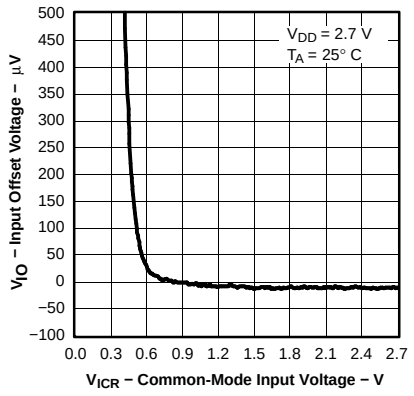


**Figure 1.**

**INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE**

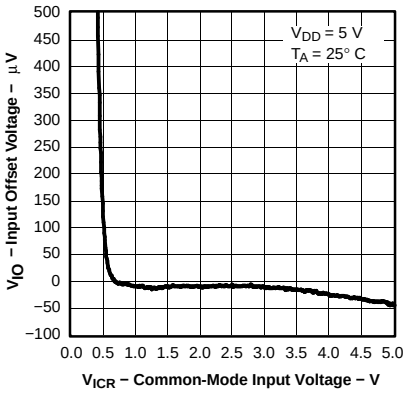


**Figure 2.**

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

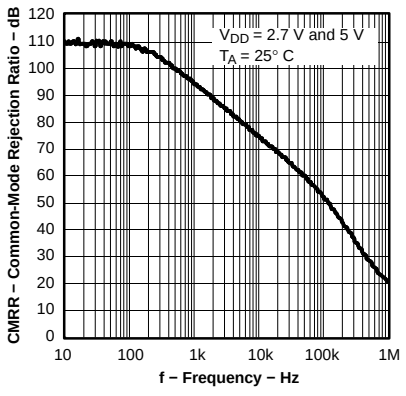


**Figure 3.**



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**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

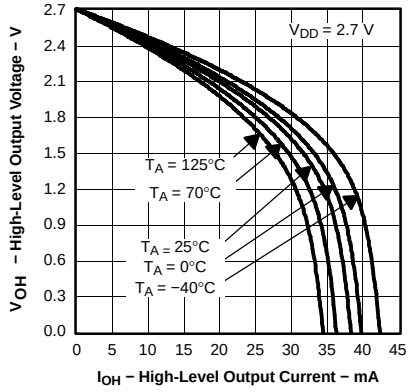


Figure 4.

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

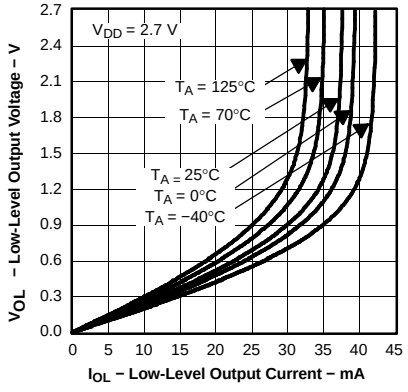


Figure 5.

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

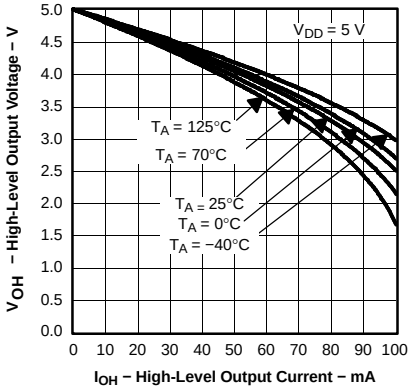


Figure 6.

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

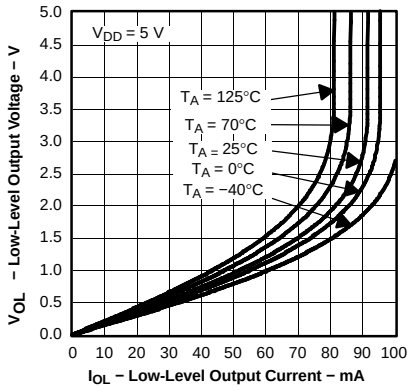


Figure 7.

**SUPPLY CURRENT vs SUPPLY VOLTAGE**

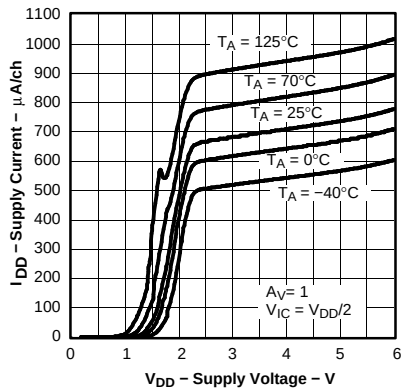


Figure 8.

**SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

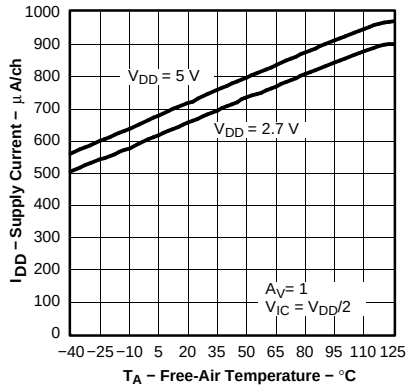


Figure 9.

**POWER SUPPLY REJECTION RATIO vs FREQUENCY**

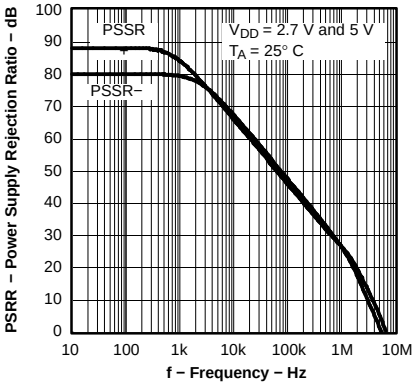


Figure 10.

**DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE vs FREQUENCY**

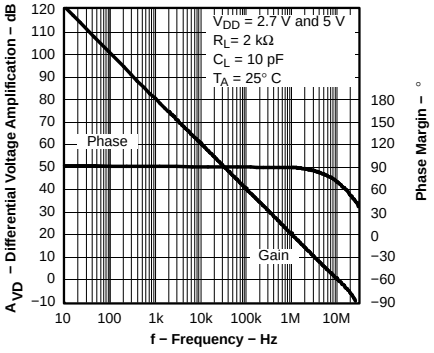


Figure 11.

**GAIN-BANDWIDTH PRODUCT vs FREE-AIR TEMPERATURE**

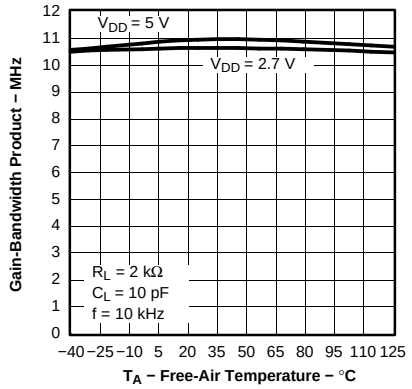


Figure 12.



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**SLEW RATE vs SUPPLY VOLTAGE**

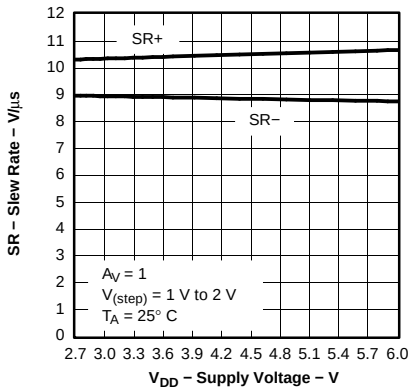


Figure 13.

**SLEW RATE vs FREE-AIR TEMPERATURE**

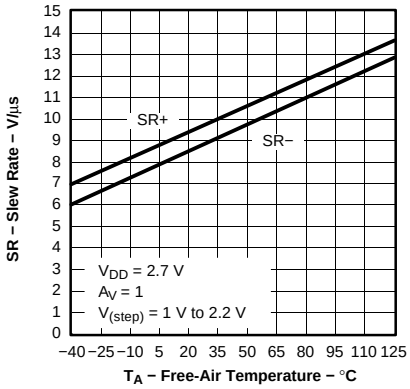


Figure 14.

**SLEW RATE vs FREE-AIR TEMPERATURE**

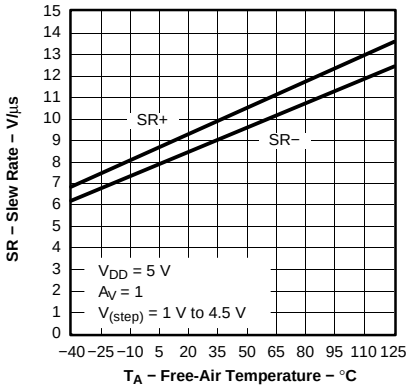


Figure 15.

**PHASE MARGIN vs LOAD CAPACITANCE**

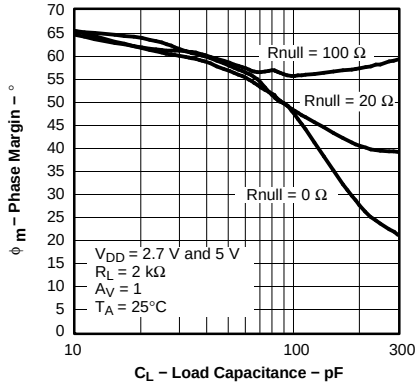


Figure 16.

**EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY**

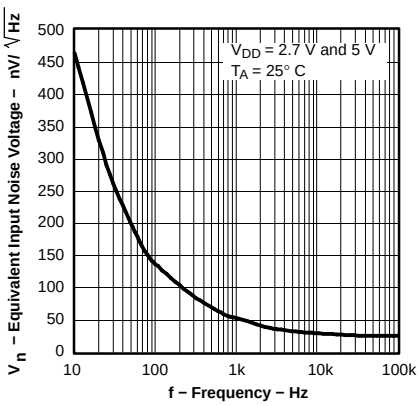


Figure 17.

**VOLTAGE-FOLLOWER LARGE-SIGNAL PULSE RESPONSE**

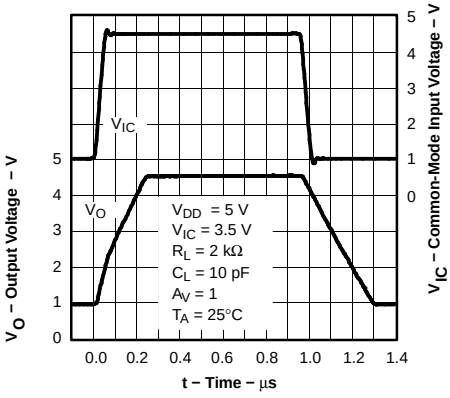


Figure 18.

**VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE**

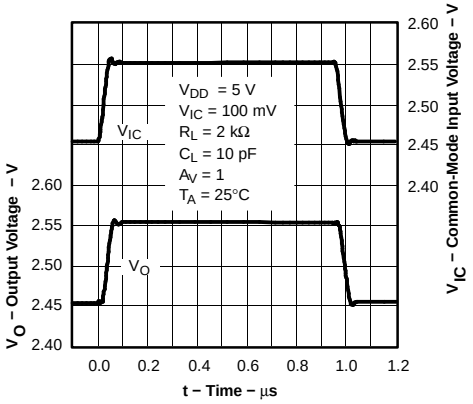


Figure 19.



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**CROSSTALK vs FREQUENCY**

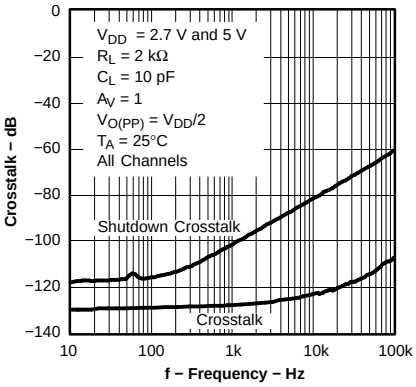


Figure 20.

**SHUTDOWN SUPPLY CURRENT vs FREE-AIR TEMPERATURE**

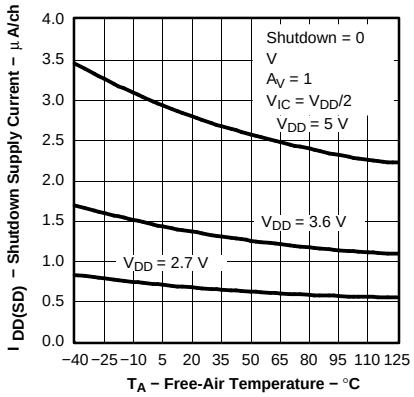


Figure 21.

**SHUTDOWN SUPPLY CURRENT vs SUPPLY VOLTAGE**

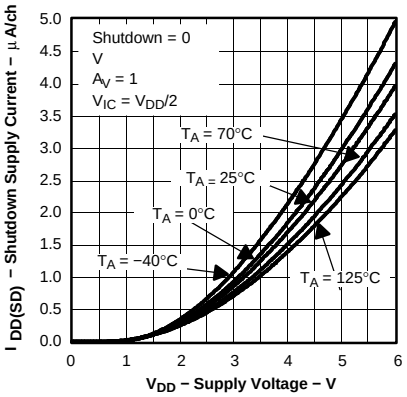


Figure 22.

**SHUTDOWN SUPPLY CURRENT/OUTPUT VOLTAGE vs TIME**

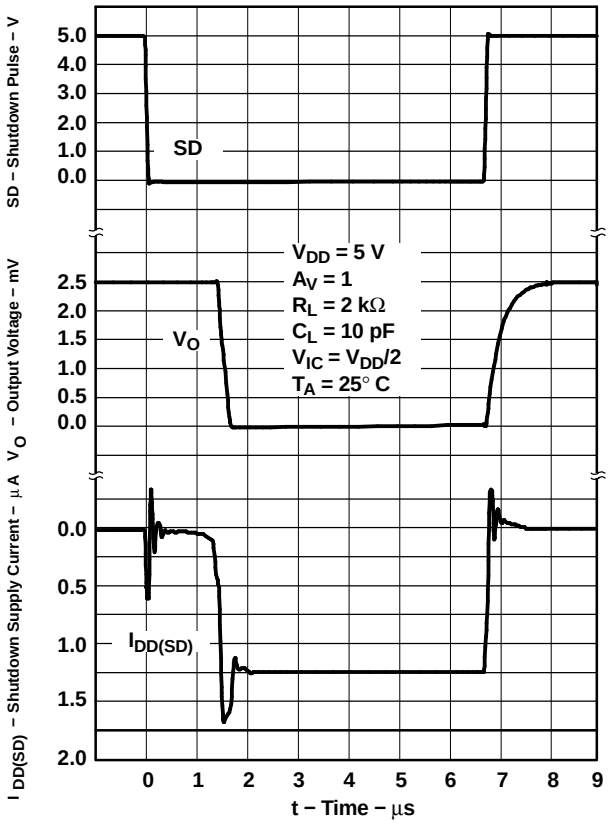


Figure 23.



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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TLV2620IDBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2620IDBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2620IDBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2620IDBVTG4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2620IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2620IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2621IDBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2621IDBVRG4 | ACTIVE | SOT-23 | DBV | 5 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2621IDBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2621IDBVTG4 | ACTIVE | SOT-23 | DBV | 5 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2621IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2621IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2622ID | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2622IDG4 | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2622IDGK | ACTIVE | MSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2622IDGKG4 | ACTIVE | MSOP | DGK | 8 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2622IDGKR | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

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| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TLV2622IDGKRG4 | ACTIVE | MSOP | DGK | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2622IDR | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2622IDRG4 | ACTIVE | SOIC | D | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2623IDGS | ACTIVE | MSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2623IDGSG4 | ACTIVE | MSOP | DGS | 10 | 80 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2623IDGSR | ACTIVE | MSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2623IDGSRG4 | ACTIVE | MSOP | DGS | 10 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2623IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2623IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2624ID | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2624IDG4 | ACTIVE | SOIC | D | 14 | 50 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2624IDR | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2624IDRG4 | ACTIVE | SOIC | D | 14 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2624IPW | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2624IPWG4 | ACTIVE | TSSOP | PW | 14 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2624IPWR | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2624IPWRG4 | ACTIVE | TSSOP | PW | 14 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |
| TLV2625IDR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

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| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TLV2625IDRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

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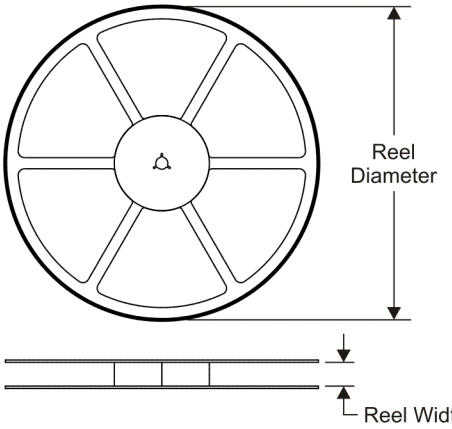
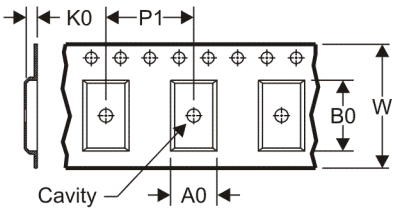
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

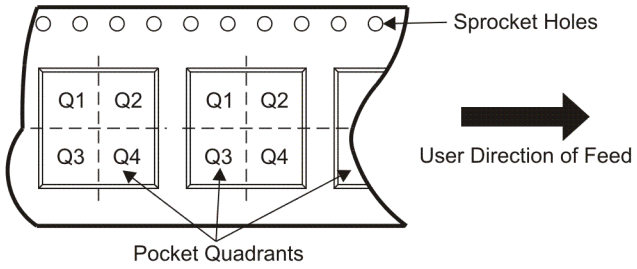



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TLV2620IDBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2620IDBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2620IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2621IDBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2621IDBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TLV2621IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2622IDGKR | MSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2622IDR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| TLV2623IDGSR | MSOP | DGS | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| TLV2623IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2624IDR | SOIC | D | 14 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| TLV2624IPWR | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2624IPWRG4 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TLV2625IDR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |



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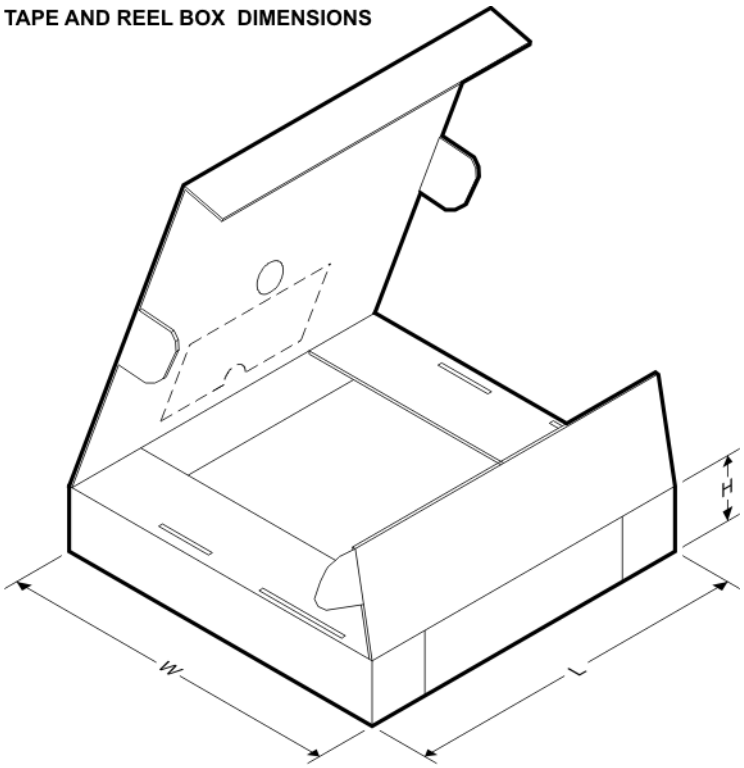
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TLV2620IDBVR | SOT-23 | DBV | 6 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2620IDBVT | SOT-23 | DBV | 6 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2620IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2621IDBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TLV2621IDBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TLV2621IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2622IDGKR | MSOP | DGK | 8 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2622IDR | SOIC | D | 8 | 2500 | 340.5 | 338.1 | 20.6 |
| TLV2623IDGSR | MSOP | DGS | 10 | 2500 | 358.0 | 335.0 | 35.0 |
| TLV2623IDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLV2624IDR | SOIC | D | 14 | 2500 | 333.2 | 345.9 | 28.6 |
| TLV2624IPWR | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |
| TLV2624IPWRG4 | TSSOP | PW | 14 | 2000 | 346.0 | 346.0 | 29.0 |
| TLV2625IDR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |



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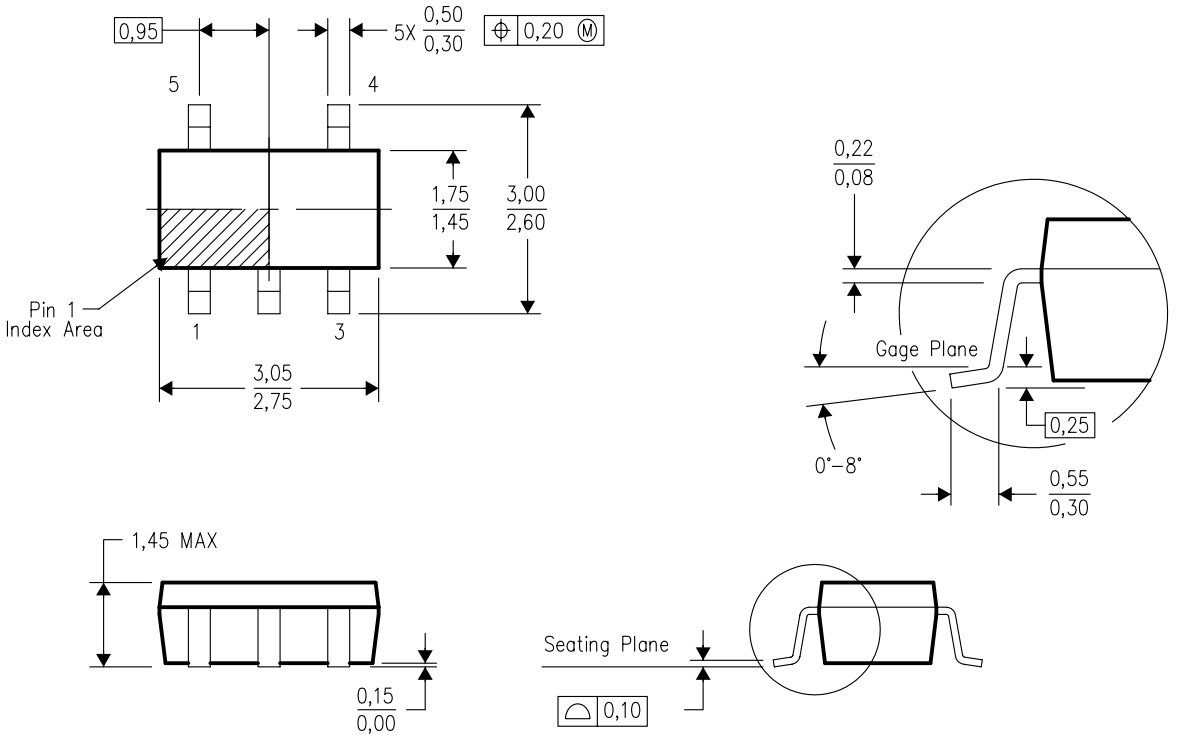
## DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.



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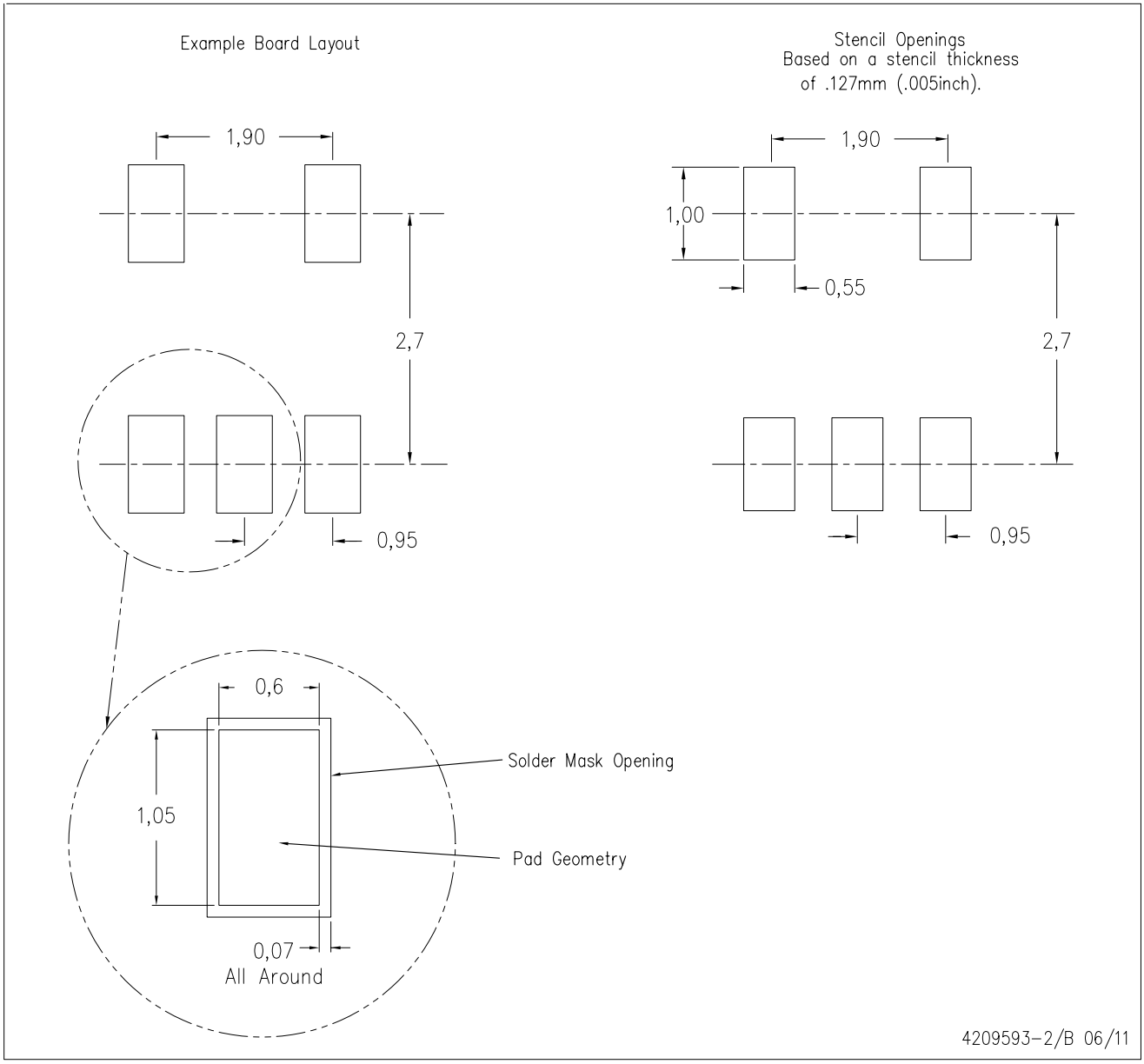
DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.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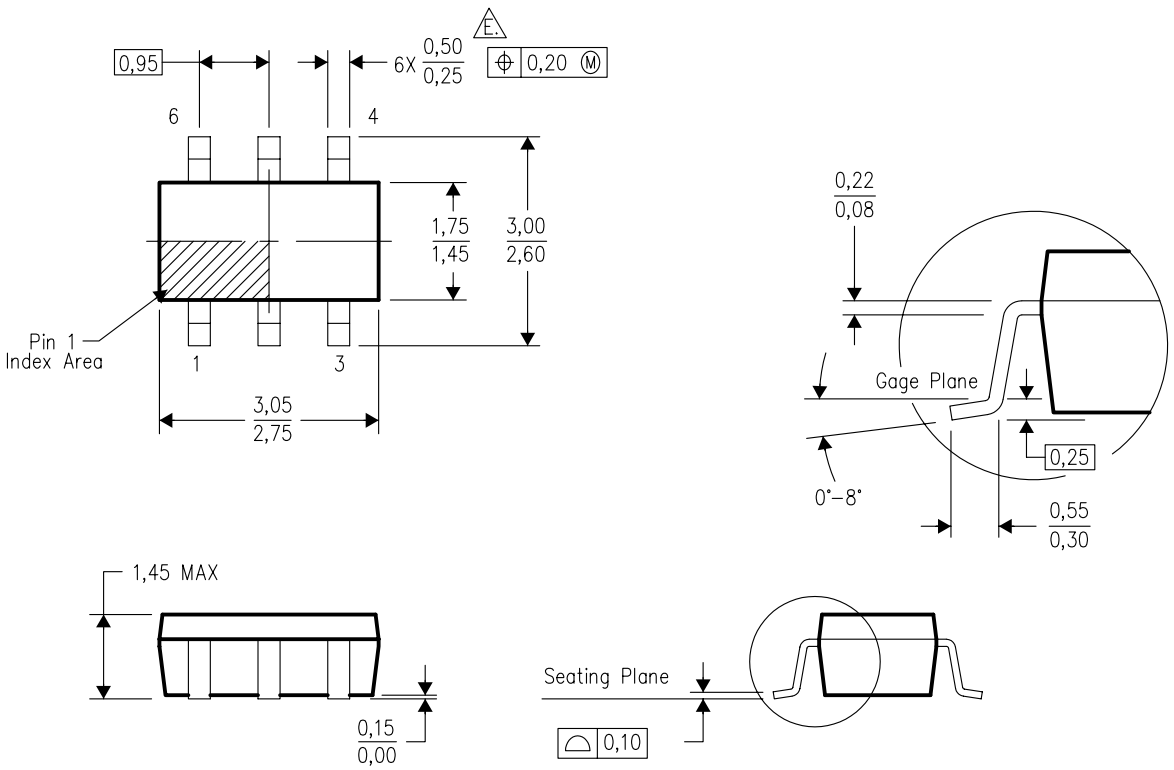
## DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE




4073253–5/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.



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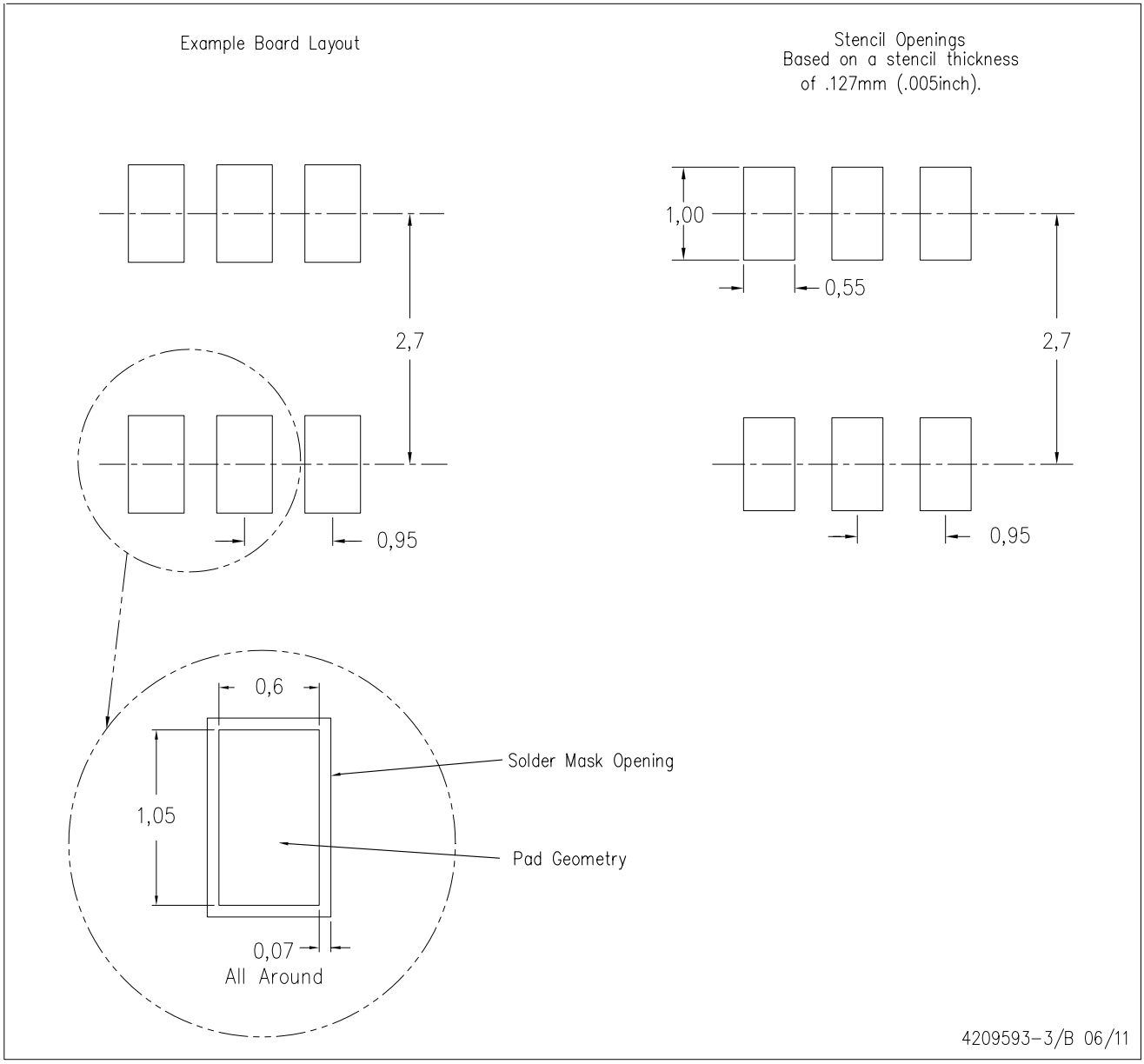
DBV (R-PDSO-G6)




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.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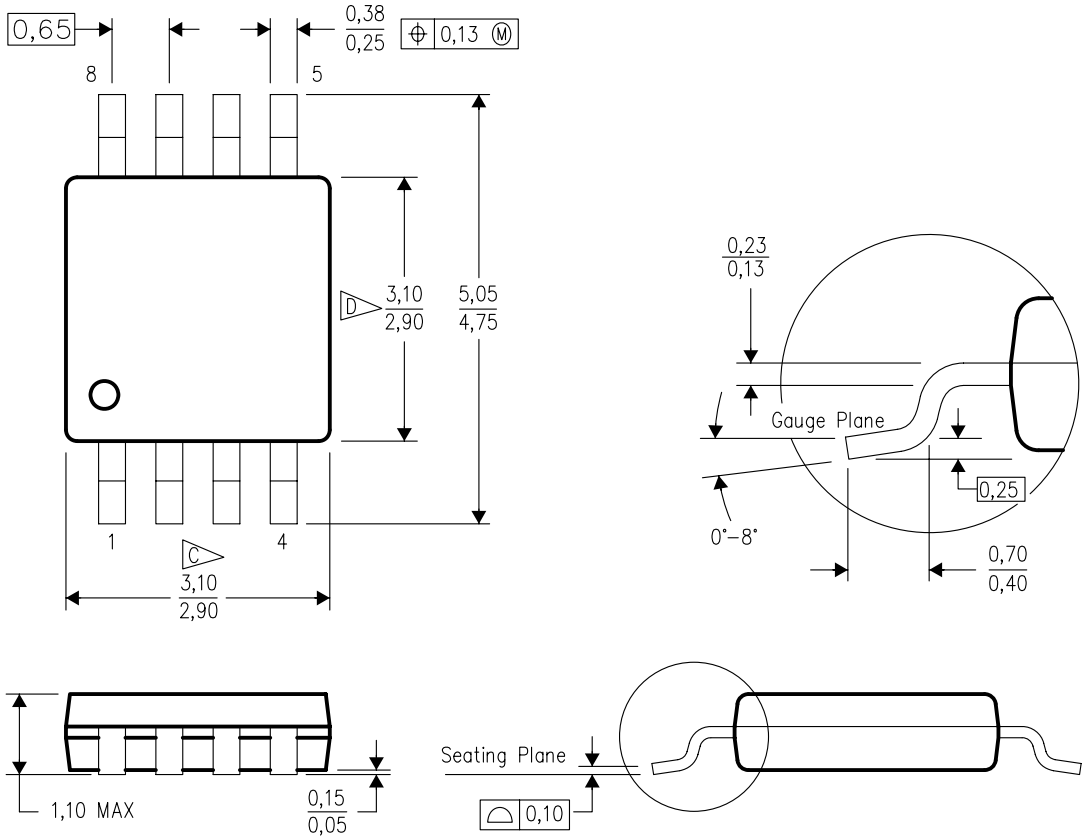
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

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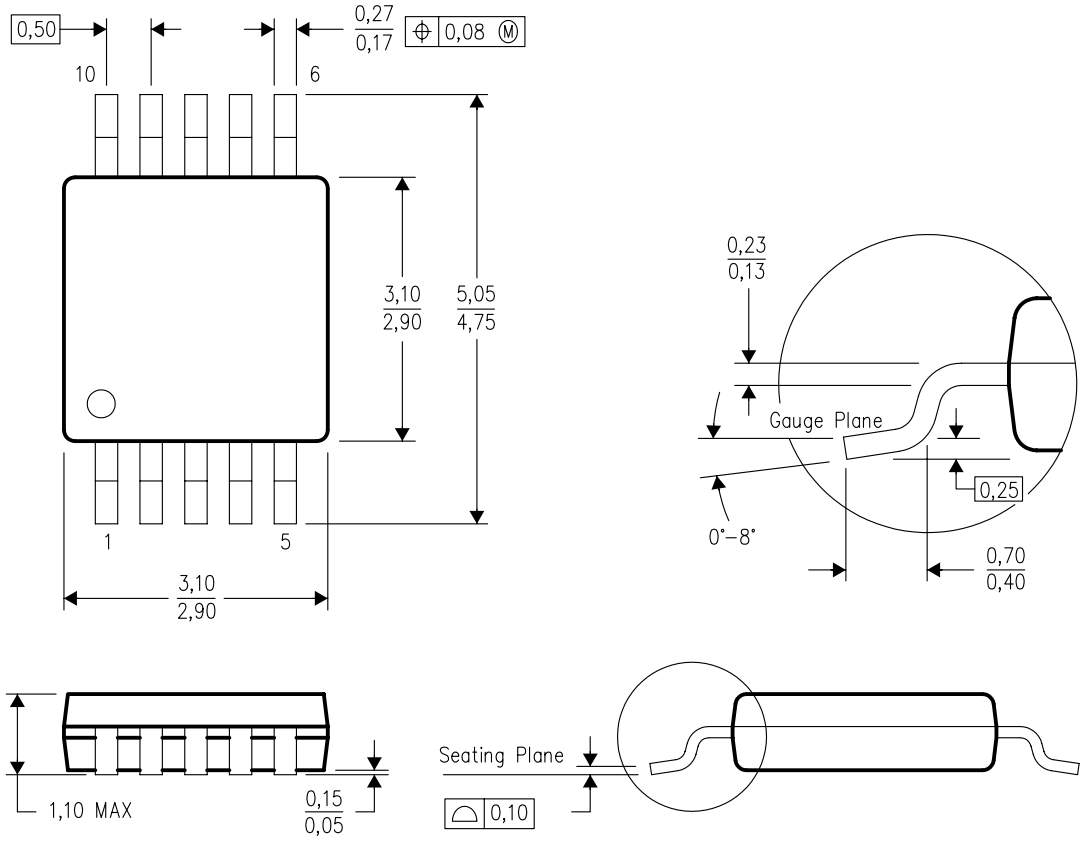
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE




4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

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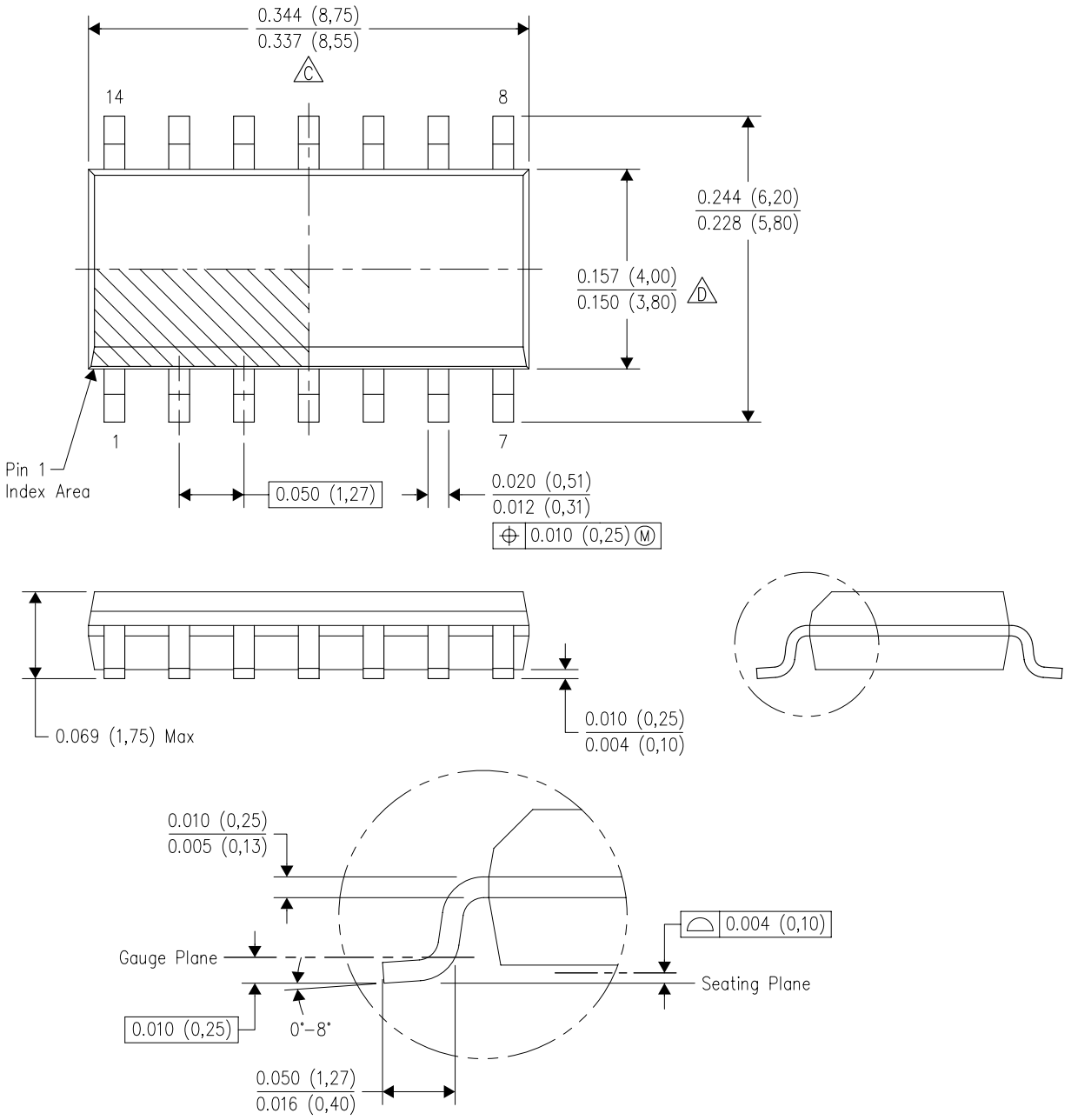
D (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.



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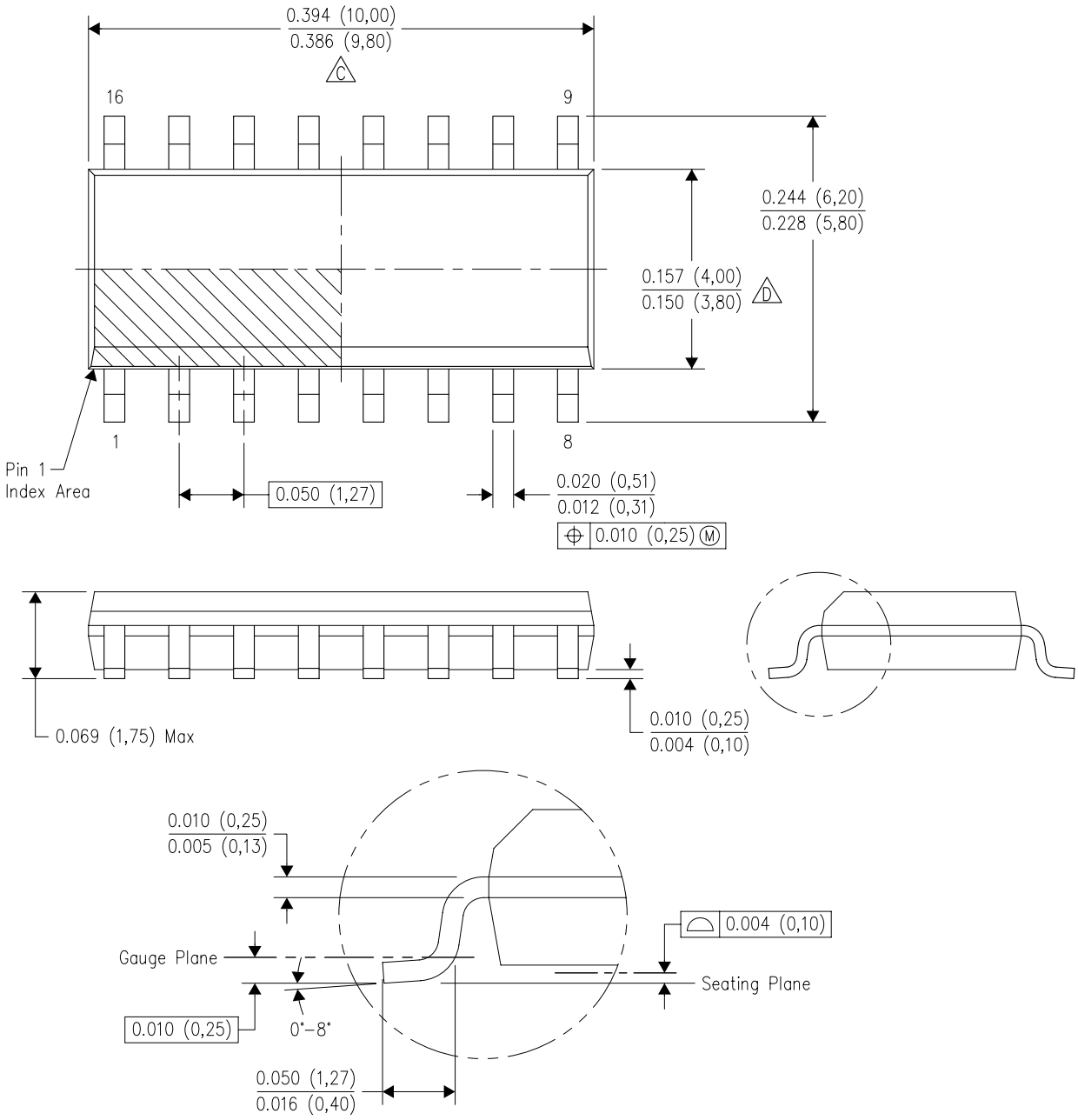
D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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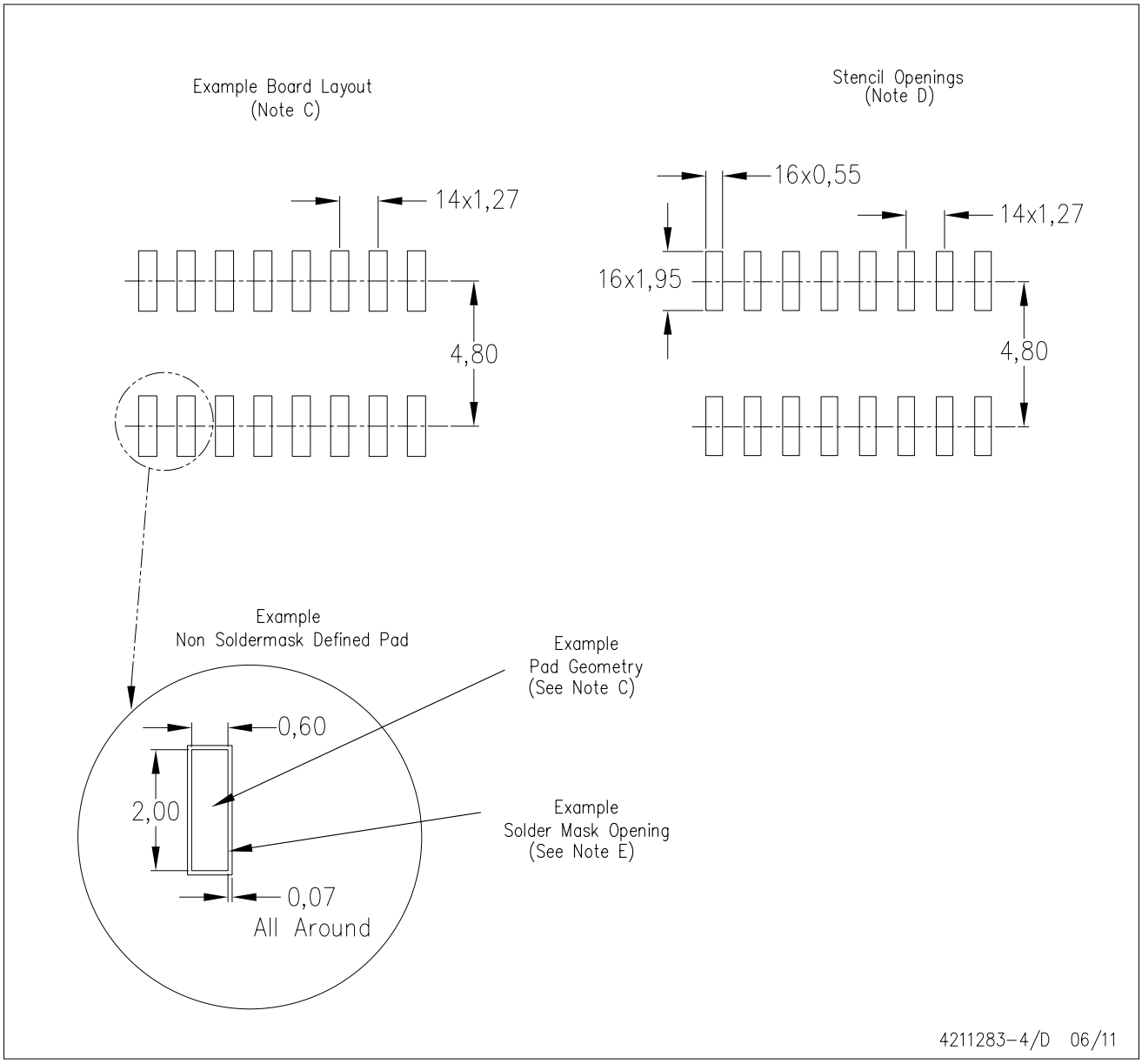
D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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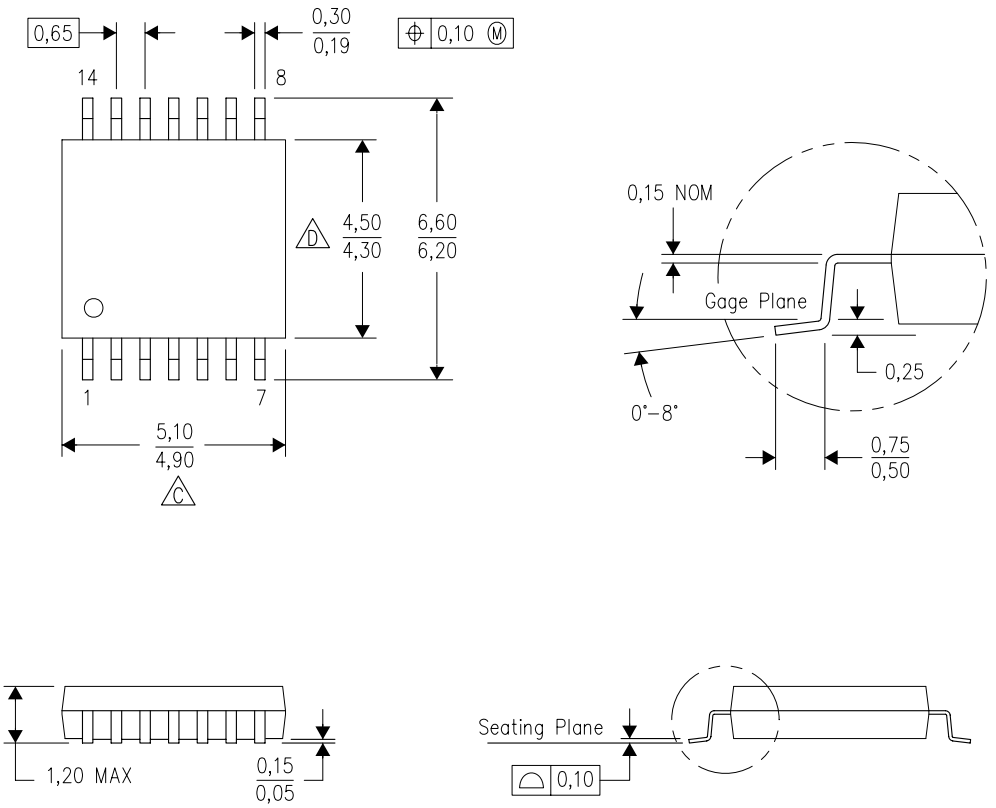
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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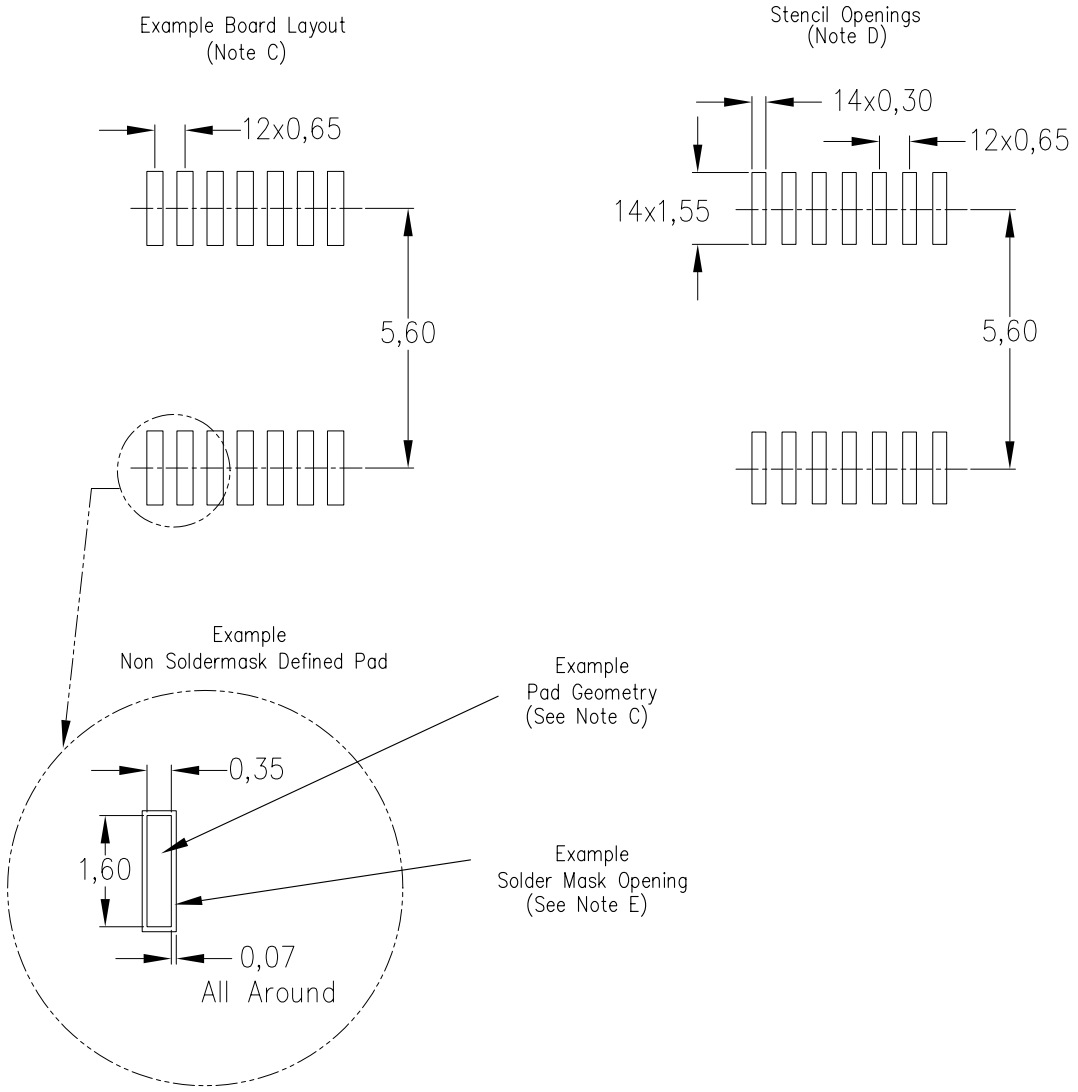
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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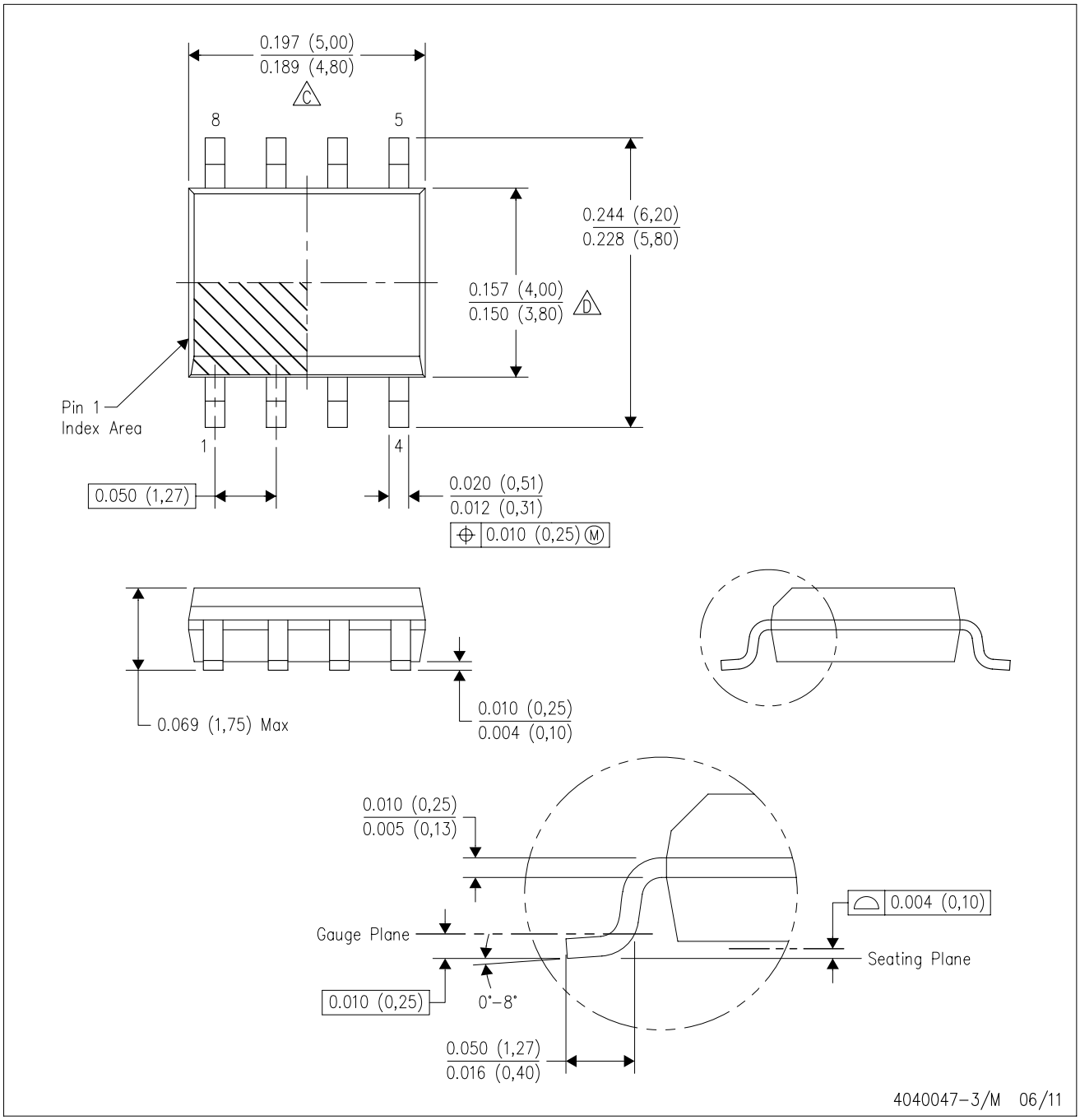
D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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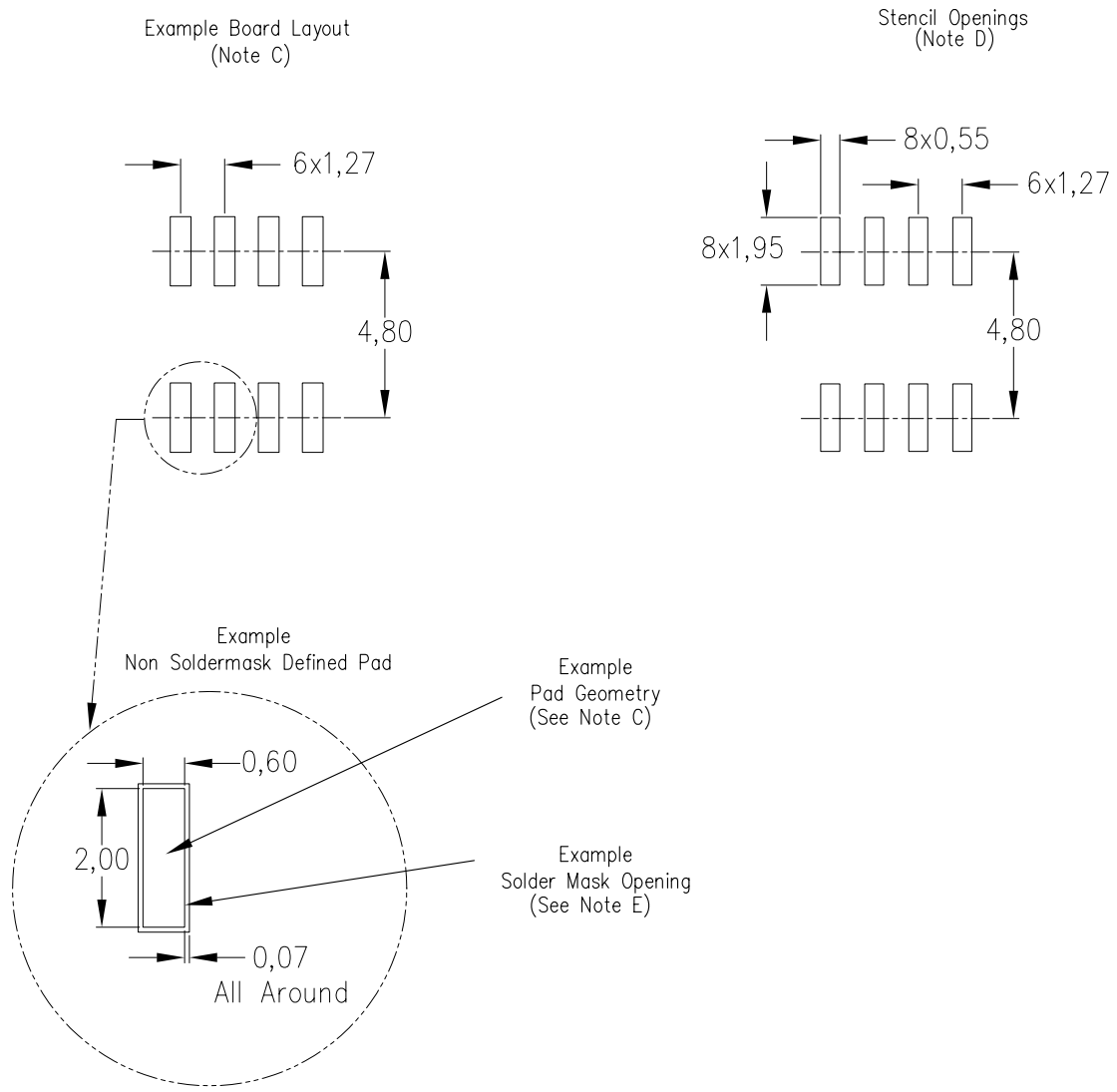
D (R–PDSO–G8) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



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