LOW-POWER STEREO AUDIO CODEC FOR PORTABLE AUDIO/TELEPHONY

FEATURES

- Stereo Audio DAC:
  - 100-dB (A-Weighted) Signal-to-Noise Ratio
  - 16-/20-/24-/32-Bit Data
  - Supports Rates From 8 kHz to 96 kHz
  - 3D/Bass/Treble/EQ/De-Emphasis Effects
- Stereo Audio ADC:
  - 92-dB (A-Weighted) Signal-to-Noise Ratio
  - Supports Rates From 8 kHz to 96 kHz
- Six Audio Input Pins:
  - Two Stereo Differential/Single-Ended Inputs
- Six Audio Output Drivers:
  - Stereo 8-Ω, 500-mW/Channel Speaker Drive Capability
  - Stereo Fully-Differential or Single-Ended Headphone Drivers
  - Fully Differential Stereo Line Outputs
- Low Power: 14-mW Stereo, 48-kHz Playback With 3.3-V Analog Supply
- Programmable Input/Output Analog Gains
- Automatic Gain Control (AGC) for Recording
- Programmable Microphone Bias Level
- Programmable PLL for Flexible Clock Generation
- I^2C™ Control Bus
- Audio Serial Data Bus Supports I^2S™, Left-/Right-Justified, DSP, and TDM Modes
- Extensive Modular Power Control
- Power Supplies:
  - Analog: 2.7 V to 3.6 V
  - Digital Core: 1.65 V to 1.95 V
  - Digital I/O: 1.1 V to 3.6 V
- Available Packages: 5-mm × 5-mm, 32-Pin QFN

DESCRIPTION

The TLV320AIC31 is a low-power stereo audio codec with a stereo headphone amplifier, as well as multiple inputs and outputs, programmable in single-ended or fully-differential configurations. Extensive register-based power control is included, enabling stereo 48-kHz digital-to-analog converter (DAC) playback as low as 14 mW from a 3.3-V analog supply, making it ideal for portable, battery-powered audio and telephony applications.

The record path of the TLV320AIC31 contains integrated microphone bias, a digitally-controlled stereo microphone pre-amp, and automatic gain control (AGC), with mix/mux capability among the multiple analog inputs. The playback path includes mix/mux capability from the stereo DAC and selected inputs, through programmable volume controls to the various outputs.

The TLV320AIC31 contains four high-power output drivers as well as two fully differential output drivers. The high-power output drivers are capable of driving a variety of load configurations, including up to four channels of single-ended, 16-Ω headphones using ac-coupling capacitors, or stereo 16-Ω headphones in a capless output configuration. In addition, pairs of drivers can be used to drive 8-Ω speakers in a BTL configuration at 500 mW per channel.

The stereo audio DAC supports sampling rates from 8 kHz to 96 kHz and includes programmable digital filtering in the DAC path for 3D, bass/treble/midrange effects, speaker equalization, and de-emphasis for 32-kHz, 44.1-kHz, and 48-kHz rates. The stereo-audio analog-to-digital converter (ADC) supports sampling rates from 8 kHz to 96 kHz and is preceded by programmable gain amplifiers providing up to +59.5 dB analog gain for low-level microphone inputs.

The serial control bus supports the I^2C protocol, while the serial-audio data bus is programmable for I^2S, left-/right-justified, DSP, or TDM modes. A highly programmable PLL is included for flexible clock generation and support for all standard audio rates from a wide range of available MCLKs, varying from 512 kHz to 50 MHz, with special attention paid to the most popular cases of 12-MHz, 13-MHz, 16-MHz, 19.2-MHz, and 19.68-MHz system clocks.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

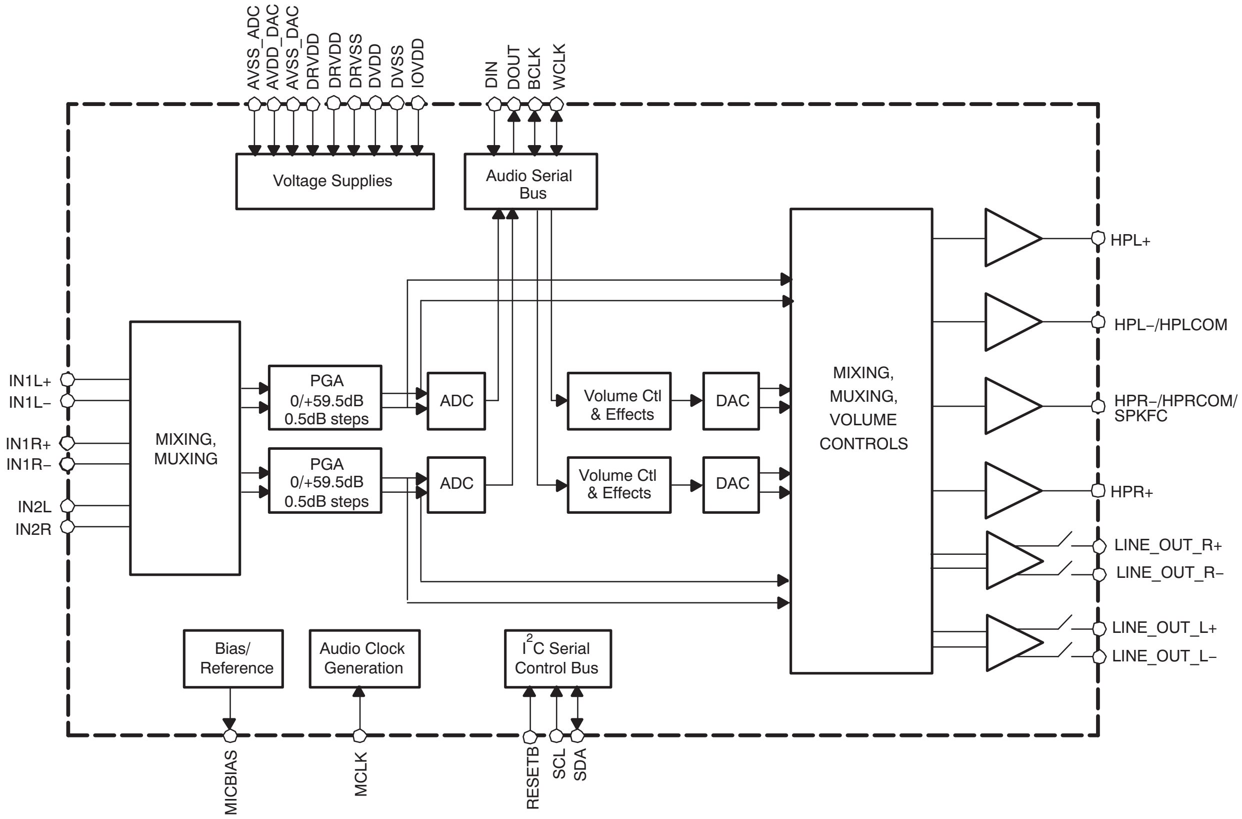
DESCRIPTION, CONTINUED

The TLV320AIC31 operates from an analog supply of 2.7 V to 3.6 V, a digital core supply of 1.65 V to 1.95 V, and a digital I/O supply of 1.1 V to 3.6 V. The device is available in a 5 × 5 mm, 32-lead QFN package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

SIMPLIFIED BLOCK DIAGRAM


AVSS_ADC
AVDD_DAC
AVSS_DAC
DRVDD
DRVDD
DRVSS
DVDD
DVSS
IOVDD
DIN
DOUT
BCLK
WCLK
Voltage Supplies
Audio Serial Bus
IN1L+
IN1L−
IN1R+
IN1R−
IN2L
IN2R
MIXING, MUXING
PGA 0/+59.5dB 0.5dB steps
PGA 0/+59.5dB 0.5dB steps
ADC
ADC
Volume Ctl & Effects
Volume Ctl & Effects
DAC
DAC
MIXING, MUXING, VOLUME CONTROLS
HPL+
HPL−/HPLCOM
HPR−/HPRCOM/ SPKFC
HPR+
LINE_OUT_R+
LINE_OUT_R−
LINE_OUT_L+
LINE_OUT_L−
Bias/ Reference
Audio Clock Generation
I2C Serial Control Bus
MICBIAS
MCLK
RESETB
SCL
SDA

Simplified Codec Block Diagram

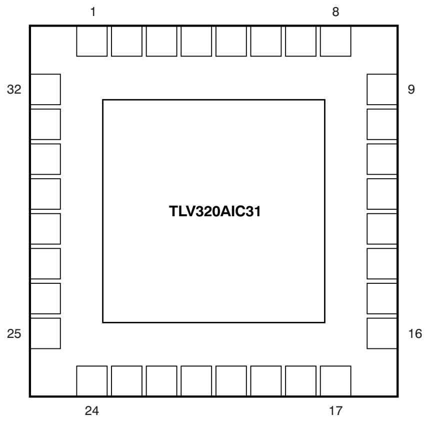
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLV320AIC31	QFN-32	RHB	–40°C to +85°C	TLV320AIC31IRHBT	Tape and Reel, 250
				TLV320AIC31IRHBR	Tape and Reel, 3000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

DEVICE INFORMATION

PIN ASSIGNMENTS



TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	PIN NO.	I/O	
MCLK	1	I	Master clock input
BCLK	2	I/O	Audio serial data bus bit clock input/output
WCLK	3	I/O	Audio serial data bus word clock input/output
DIN	4	I	Audio serial data bus data input
DOUT	5	O	Audio serial data bus data output
DVSS	6	I/O	Digital core / I/O Ground Supply, 0 V
IOVDD	7	I/O	Digital I/O voltage supply, 1.1 V to 3.6 V
SCL	8	I/O	I^{2}C serial clock input
SDA	9	I/O	I^{2}C serial data input/output
IN1LP	10	I	Left input 1 (Single-ended) or Left Input + (Differential)
IN1LM	11	I	Left input – (Diff only)
IN1RP	12	I	Right input 1 (Single-ended) or Right Input + (Differential)
IN1RM	13	I	Right input – (Differential only)
IN2L	14	I	Left input 2 (Single-ended)
MICBIAS	15	O	Microphone bias voltage output
IN2R	16	I	Right input 2 (Single-ended)
AVSS1	17	I	Analog ADC ground supply, 0 V
DRVDD	18	O	Analog ADC and output driver voltage supply, 2.7 V to 3.6 V
HPLOUT	19	O	High power output driver (Left +)
HPLCOM	20	O	High power output driver (Left – or multi-functional)
DRVSS	21	O	Analog output driver ground supply, 0 V
HPRCOM	22	O	High power output driver (Right – or multi-functional)
HPROUT	23	O	High power output driver (Right +)
DRVDD	24	O	Analog output driver voltage supply, 2.7 V to 3.6 V
AVDD	25	I	Analog DAC voltage supply, 2.7 V to 3.6 V
AVSS2	26	I	Analog DAC ground supply, 0 V
LEFT_LOP	27	O	Left line output (+)
LEFT_LOM	28	O	Left line output (–)
RIGHT_LOP	29	O	Right line output (+)
RIGHT_LOM	30	O	Right line output (–)
$\overline{\text{RESET}}$	31		Reset
DVDD	32	I	Digital core voltage supply, 1.65 V to 1.95 V

ABSOLUTE MAXIMUM RATINGS[1]

Over operating free-air temperature range (unless otherwise noted).

			TLV320AIC31	UNIT
	AVDD to AVSS1/2, DRVDD1/2 to DRVSS		–0.3 to 3.9	V
	AVDDA1 to DRVSS		–0.3 to 3.9	V
	IOVDD to DVSS		–0.3 to 3.9	V
	DVDD to DVSS		–0.3 to 2.5	V
	AVDD to DRVDD1/2		–0.1 to 0.1	V
	Digital input voltage to DVSS		–0.3 V to IOVDD+0.3	V
	Analog input voltage to AVSS		–0.3 V to AVDD+0.3	V
	Operating temperature range		–40 to +85	°C
	Storage temperature range		–65 to +105	°C
T_J Max	Junction temperature		+105	°C
	QFN package	Power dissipation	$(T_J \text{ Max} – T_A) / \theta_{JA}$	
		θ_{JA} Thermal impedance	44	°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS[1]

T_A = +25°C POWER RATING	DERATING FACTOR	T_A = +75°C POWER RATING	T_A = +85°C POWER RATING
1.82 W	22.7 mW/°C	681 mW	454 mW

(1) This data was taken using a 2 oz. trace and copper pad that is soldered directly to a JEDEC standard 4-layer 3 in. × 3 in. printed circuit board (PCB).

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
AVDD, DRVDD1/2[1]	Analog supply voltage	2.7	3.3	3.6	V
DVDD[1]	Digital core supply voltage	1.65	1.8	1.95	V
IOVDD[1]	Digital I/O supply voltage	1.1	1.8	3.6	V
V_I	Analog full-scale 0-dB input voltage (DRVDD1 = 3.3 V)		0.707		V_{RMS}
	Stereo line-output load resistance	10			kΩ
	Stereo headphone-output load resistance	16			Ω
	Digital output load capacitance		10		pF
T_A	Operating free-air temperature	–40		+85	°C

(1) Analog voltage values are with respect to AVSS1, AVSS2, DRVSS; digital voltage values are with respect to DVSS.

ELECTRICAL CHARACTERISTICS

At +25°C, AVDD, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, F_S = 48 kHz, 16-bit audio data (unless otherwise noted).

PARAMETER		TEST CONDITIONS	TLV320AIC31			UNIT
			MIN	TYP	MAX	
AUDIO ADC						
	Input signal level (0 dB)	Single-ended input		0.707		V_{RMS}
	Signal-to-noise ratio, A-weighted[1] [2]	F_S = 48 kHz, 0-dB PGA gain, IN1 inputs selected and ac-shorted together	80	92		dB
	Dynamic range, A-weighted[1] [2]	F_S = 48 kHz, 1-kHz –60 dB full-scale input applied at IN1 inputs, 0-dB PGA gain		92		dB
THD	Total harmonic distortion	F_S = 48 kHz, 1-kHz –2dB full-scale input applied at IN1 inputs, 0-dB PGA gain		–90	–75	dB
				0.003%	0.018%	
	Power-supply rejection ratio	1 kHz, 100 mV_{PP} on AVDD, DRVDD, single-ended input		46		dB
		1 kHz, 100 mV_{PP} on AVDD, DRVDD, differential input		68		
	ADC channel separation	1 kHz, –1 dB IN2L to IN2R		–87		dB
	ADC gain error	1-kHz input, 0-dB PGA gain		0.7		dB
	ADC programmable gain amplifier maximum gain	1-kHz input tone, R_{SOURCE} < 50 Ω		59.5		dB
	ADC programmable gain amplifier step size			0.5		dB
	Input resistance	IN1 inputs, routed to single ADC Input mix attenuation = 0 dB		20		kΩ
		IN2 inputs, input mix attenuation = 0 dB		20		
		IN1 inputs, Input mix attenuation = –12 dB		80		
		IN2 inputs, Input mix attenuation = –12 dB		80		
	Input capacitance	IN1 inputs		10		pF
	Input level control minimum attenuation setting			0		dB
	Input level control maximum attenuation setting			12		dB
	Input level control attenuation step size			1.5		dB
ADC DIGITAL DECIMATION FILTER, F_S = 48 kHz						
	Filter gain from 0 to 0.39 F_S			±0.1		dB
	Filter gain at 0.4125 F_S			–0.25		dB
	Filter gain at 0.45 F_S			–3		dB
	Filter gain at 0.5 F_S			–17.5		dB
	Filter gain from 0.55 F_S to 64 F_S			–75		dB
	Filter group delay			$17/F_S$		Sec
MICROPHONE BIAS						
	Bias voltage	Programmable settings, load = 750 Ω		2.0		V
			2.25	2.5	2.75	
				AVDD – 0.2		
	Current sourcing	2.5 V setting			4	mA

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(1) Ratio of output level with 1-kHz full-scale sine wave input, to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements made with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

ELECTRICAL CHARACTERISTICS (continued)

At +25°C, AVDD, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, F_S = 48 kHz, 16-bit audio data (unless otherwise noted).

PARAMETER	TEST CONDITIONS	TLV320AIC31			UNIT
		MIN	TYP	MAX	
AUDIO DAC	**Differential Line Output, load = 10 kΩ, 50 pF**				
Full-scale differential output voltage	0-dB gain to line outputs. DAC output common-mode setting = 1.35 V, output level control gain = 0 dB		1.414		V_{RMS}
			4.0		V_{PP}
Signal-to-noise ratio, A-weighted(3)	F_S = 48 kHz, 0-dB gain to line outputs, zero signal applied, referenced to full-scale input level	90	100		dB
Dynamic range, A-weighted	F_S = 48 kHz, 0-dB gain to line outputs, 1 kHz –60 dB signal applied		100		dB
Total harmonic distortion	F_S = 48 kHz, 1 kHz 0-dB input signal applied		–93	–75	dB
Power-supply rejection ratio	234 Hz, 100 mV_{PP} on AVDD, DRVDD1/2		81		dB
DAC channel separation (left to right)	1 kHz, 0 dB		–100		dB
DAC interchannel gain mismatch	1-kHz input, 0-dB gain		0.1		dB
DAC Gain Error	1-kHz input, 0-dB gain		–0.26		dB
DAC DIGITAL INTERPOLATION FILTER, F_S = 48 kHz					
Passband	High-pass filter disabled			0.45 × F_S	Hz
Passband ripple	High-pass filter disabled		±0.06		dB
Transition band		0.45 × F_S		0.55 × F_S	Hz
Stop band		0.55 × F_S		7.5 × F_S	Hz
Stop band attenuation			65		dB
Group delay			$21/F_S$		Sec
STEREO HEADPHONE DRIVER	**AC-Coupled Output Configuration(3)**				
0-dB full-scale output voltage	0-dB gain to high-power outputs. Output common-mode voltage setting = 1.35 V		0.707		V_{RMS}
Programmable output common mode voltage (applicable to Line Outputs also)	First option		1.35		V
	Second option		1.50		
	Third option		1.65		
	Fourth option		1.8		
Maximum programmable output level control gain			9		dB
Programmable output level control gain step size			1		dB
P_O Maximum output power	R_L = 32 Ω		15		mW
	R_L = 16 Ω		30		
Signal-to-noise ratio, A-weighted(4)			94		dB

(3) Unless otherwise noted, all measurements use output common-mode voltage setting of 1.35 V, 0-dB output level control gain, 16-Ω single-ended load.

(4) Ratio of output level with a 1-kHz full-scale input, to the output level playing an all-zero signal, measured A-weighted over a 20-Hz to 20-kHz bandwidth.

ELECTRICAL CHARACTERISTICS (continued)

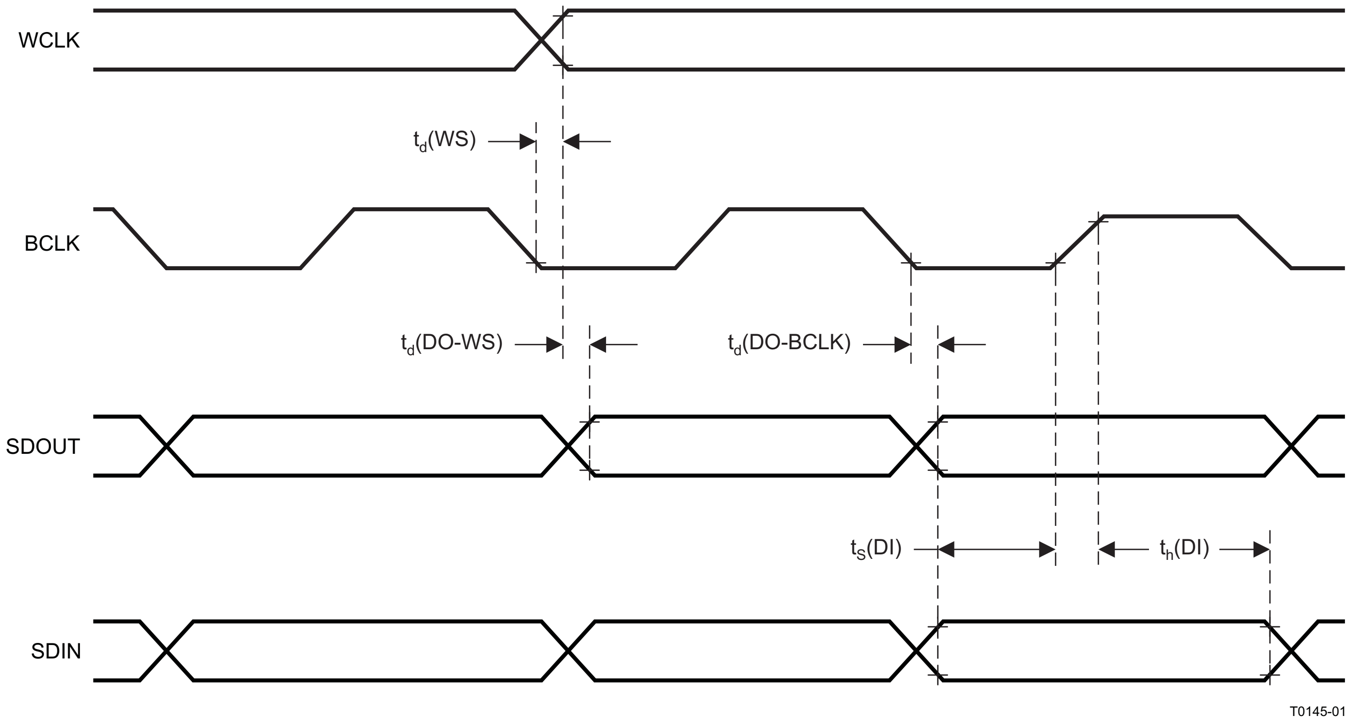
At +25°C, AVDD, DRVDD, IOVDD = 3.3 V, DVDD = 1.8 V, F_S = 48 kHz, 16-bit audio data (unless otherwise noted).

PARAMETER	TEST CONDITIONS		TLV320AIC31 MIN	TYP	MAX	UNIT
STEREO HEADPHONE DRIVER, continued						
Total harmonic distortion	1-kHz output, P_O = 10 mW, R_L = 32 Ω			–77		dB
				0.014%		
	1-kHz output, P_O = 20 mW, R_L = 32 Ω			–80		
				0.01%		
	1-kHz output, P_O = 20 mW, R_L = 16 Ω			–77		
				0.014%		
	1-kHz output, P_O = 30 mW, R_L = 16 Ω			–76		
				0.016%		
Channel separation	1 kHz, 0-dB input			96		dB
Power-supply rejection ratio	217 Hz, 100 mV_{PP} on AVDD, DRVDD1/2			48		dB
Mute attenuation	1-kHz output			107		dB
DIGITAL I/O						
V_{IL} Input low level	I_{IL} = +5 μA		–0.3		0.3 × IOVDD	V
V_{IH} Input high level[5]	I_{IH} = +5 μA		0.7 × IOVDD			V
V_{OL} Output low level	I_{IH} = 2 TTL loads				0.1 × IOVDD	V
V_{OH} Output high level	I_{OH} = 2 TTL loads		0.8 × IOVDD			V
SUPPLY CURRENT, F_S = 48 kHz						
Stereo line playback	AVDD + DRVDD	F_S = 48 kHz, PLL off, headphone drivers off, DAC Direct Mode		3.0		mA
	DVDD			2.0		
Mono record	AVDD + DRVDD	F_S = 48 kHz, PLL and AGC off		2.3		mA
	DVDD			1.1		
Stereo record	AVDD + DRVDD	F_S = 48 kHz, PLL and AGC off		4.3		mA
	DVDD			1.3		
PLL	AVDD + DRVDD	Additional power consumed when PLL is powered		1.3		mA
	DVDD			0.9		
Headphone amplifier	AVDD + DRVDD	Analog bypass to single-ended headphones, DAC and PLL off, no signal applied		1.5		mA
	DVDD			0		
Power down	AVDD + DRVDD	All supply voltages applied, all blocks programmed in lowest power state		0.1		µA
	DVDD			0.5		

(5) When IOVDD < 1.6V, minimum V_{IH} is 1.1 V.

AUDIO DATA SERIAL INTERFACE TIMING DIAGRAMS

All specifications at 25°C, DVDD = 1.8 V.

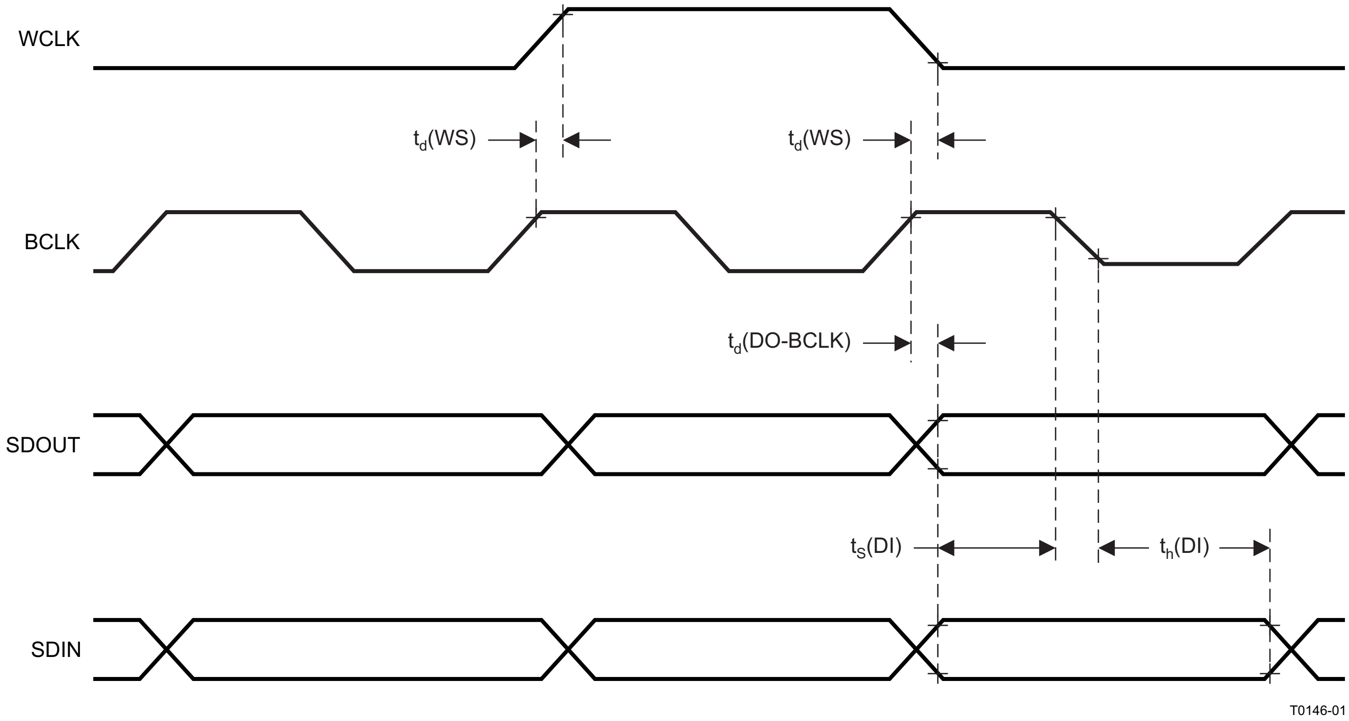


PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	ADWS/WCLK delay time		50		15	ns
t_d(DO-WS)	ADWS/WCLK to DOUT delay time		50		20	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		15	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		30		10	ns
t_f	Fall time		30		10	ns

NOTE: All timing specifications are measured at characterization but not tested at final test.

Figure 1. I^2S/LJF/RJF Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V.

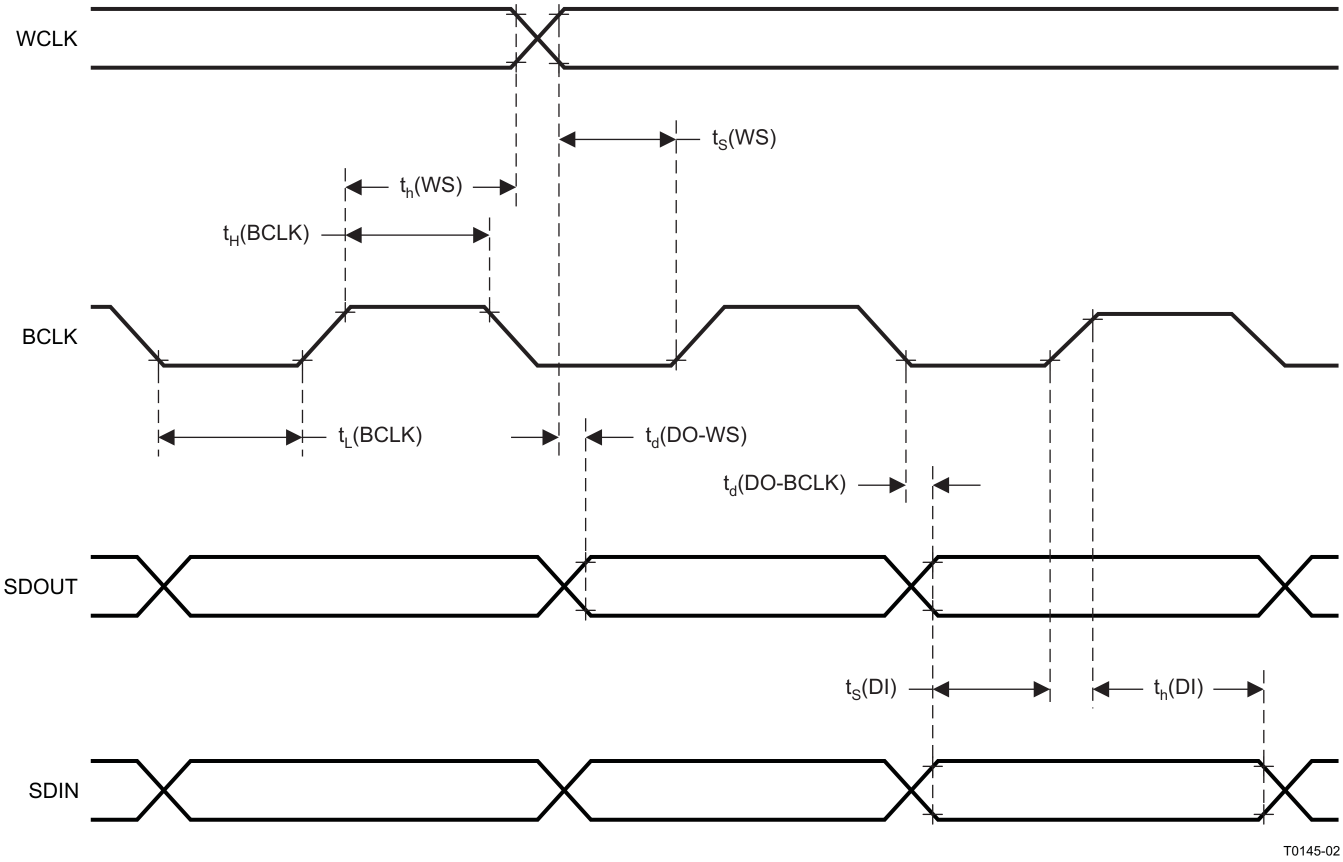


PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	ADWS/WCLK delay time		50		15	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		15	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		30		10	ns
t_f	Fall time		30		10	ns

NOTE: All timing specifications are measured at characterization but not tested at final test.

Figure 2. DSP Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V.

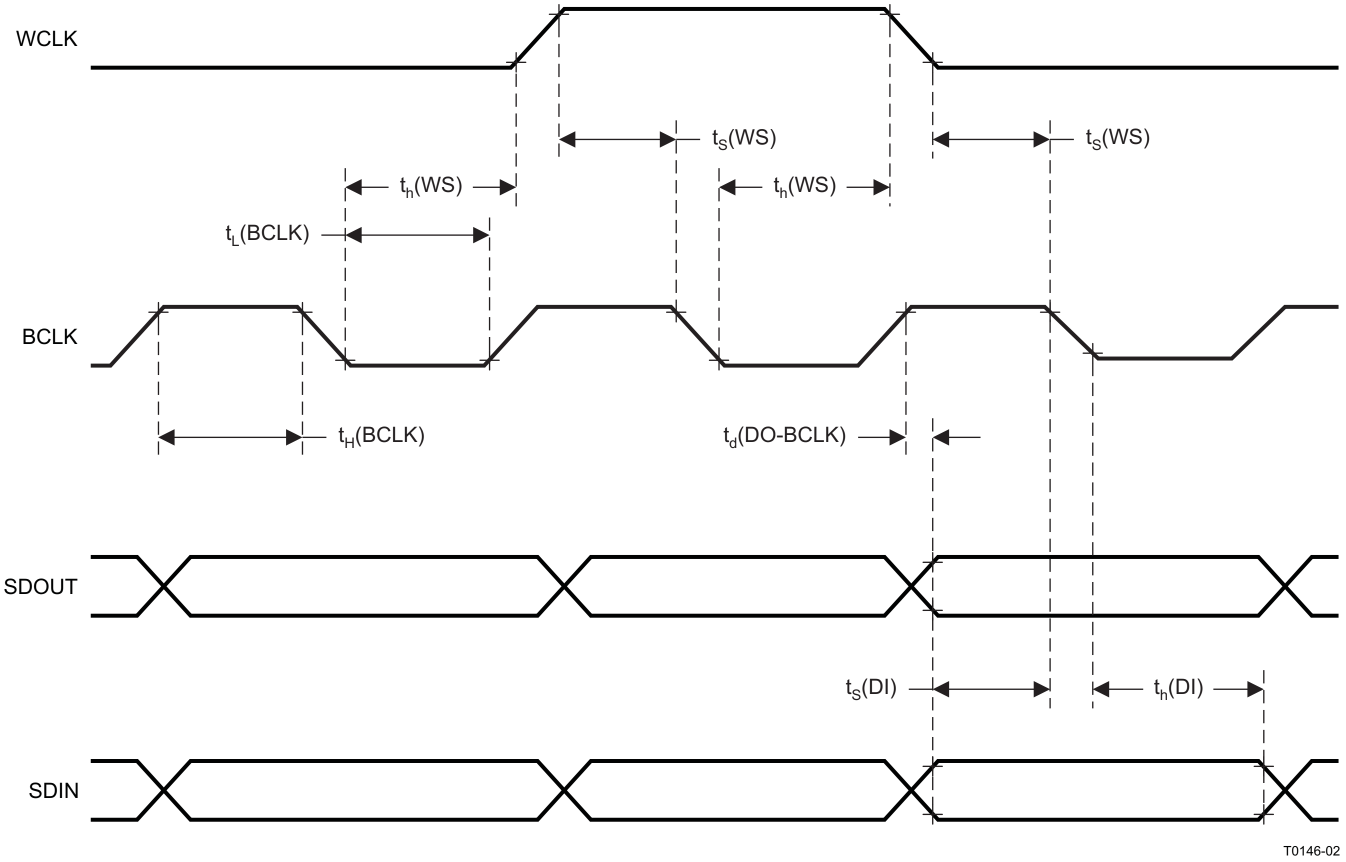

WCLK
t_S(WS)
t_h(WS)
t_H(BCLK)
BCLK
t_L(BCLK)
t_d(DO-WS)
t_d(DO-BCLK)
SDOUT
t_S(DI)
t_h(DI)
SDIN
T0145-02

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	70		35		ns
t_L(BCLK)	BCLK low period	70		35		ns
t_s(WS)	ADWS/WCLK setup time	10		6		ns
t_h(WS)	ADWS/WCLK hold time	10		6		ns
t_d(DO-WS)	ADWS/WCLK to DOUT delay time (for LJF Mode only)		50		35	ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		20	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns

NOTE: All timing specifications are measured at characterization but not tested at final test.

Figure 3. I^{2}S/LJF/RJF Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V.


WCLK
BCLK
SDOUT
SDIN
t_S(WS)
t_S(WS)
t_h(WS)
t_h(WS)
t_L(BCLK)
t_H(BCLK)
t_d(DO-BCLK)
t_S(DI)
t_h(DI)
T0146-02

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	70		35		ns
t_L(BCLK)	BCLK low period	70		35		ns
t_s(WS)	ADWS/WCLK setup time	10		8		ns
t_h(WS)	ADWS/WCLK hold time	10		8		ns
t_d(DO-BCLK)	BCLK to DOUT delay time		50		20	ns
t_s(DI)	DIN setup time	10		6		ns
t_h(DI)	DIN hold time	10		6		ns
t_r	Rise time		8		4	ns
t_f	Fall time		8		4	ns

NOTE: All timing specifications are measured at characterization but not tested at final test.

Figure 4. DSP Timing in Slave Mode

TYPICAL CHARACTERISTICS

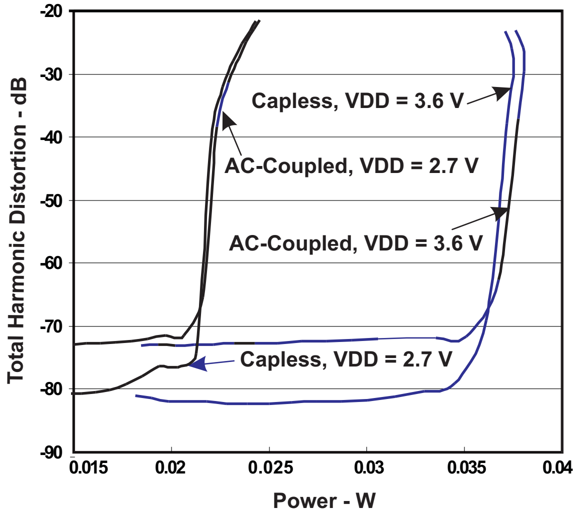


Figure 5. Headphone Power vs THD, 16-Ω Load

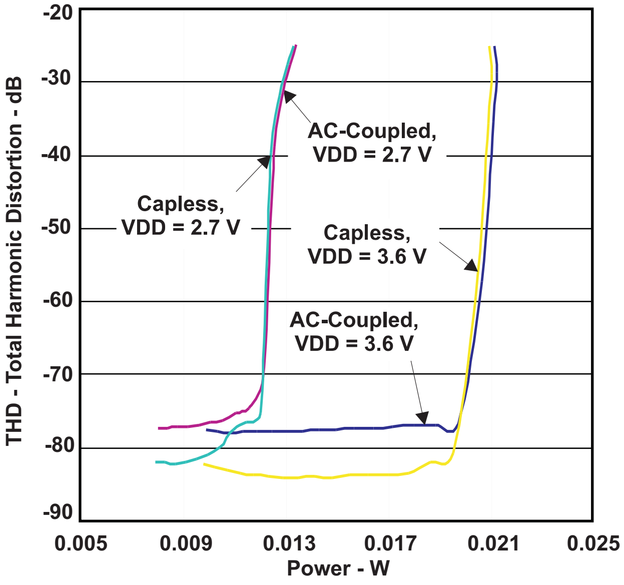


Figure 6. Headphone Power vs THD, 32-Ω Load

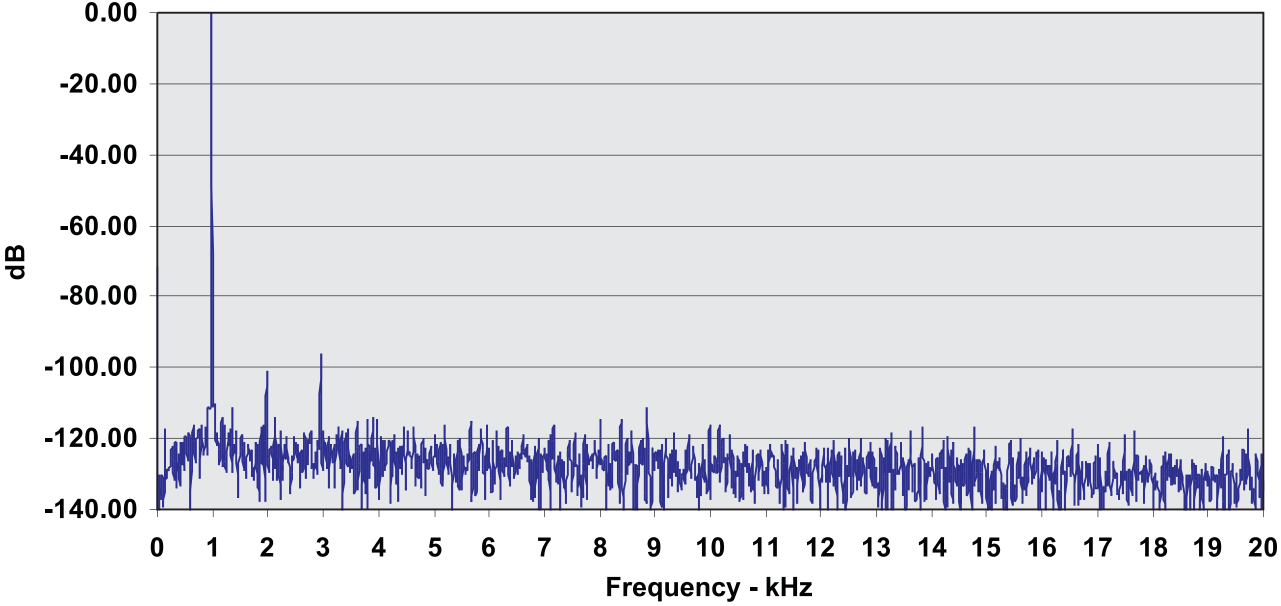


Figure 7. DAC to Line Output FFT Plot

TYPICAL CHARACTERISTICS (continued)

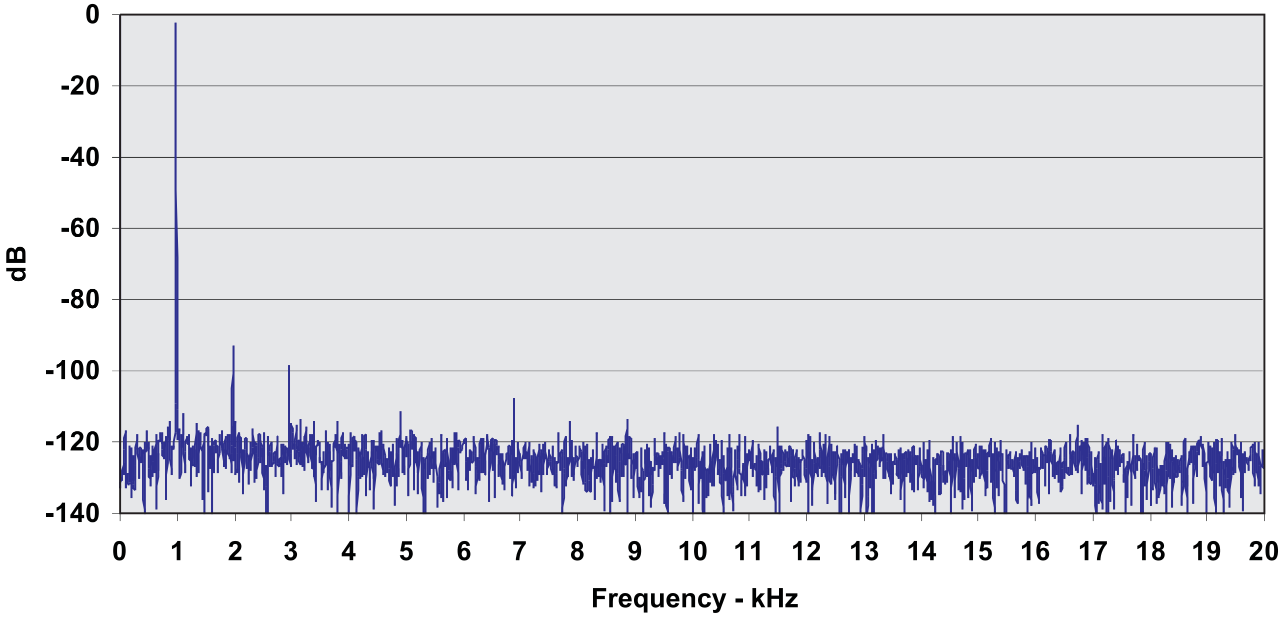


Figure 8. Line Input to ADC FFT Plot

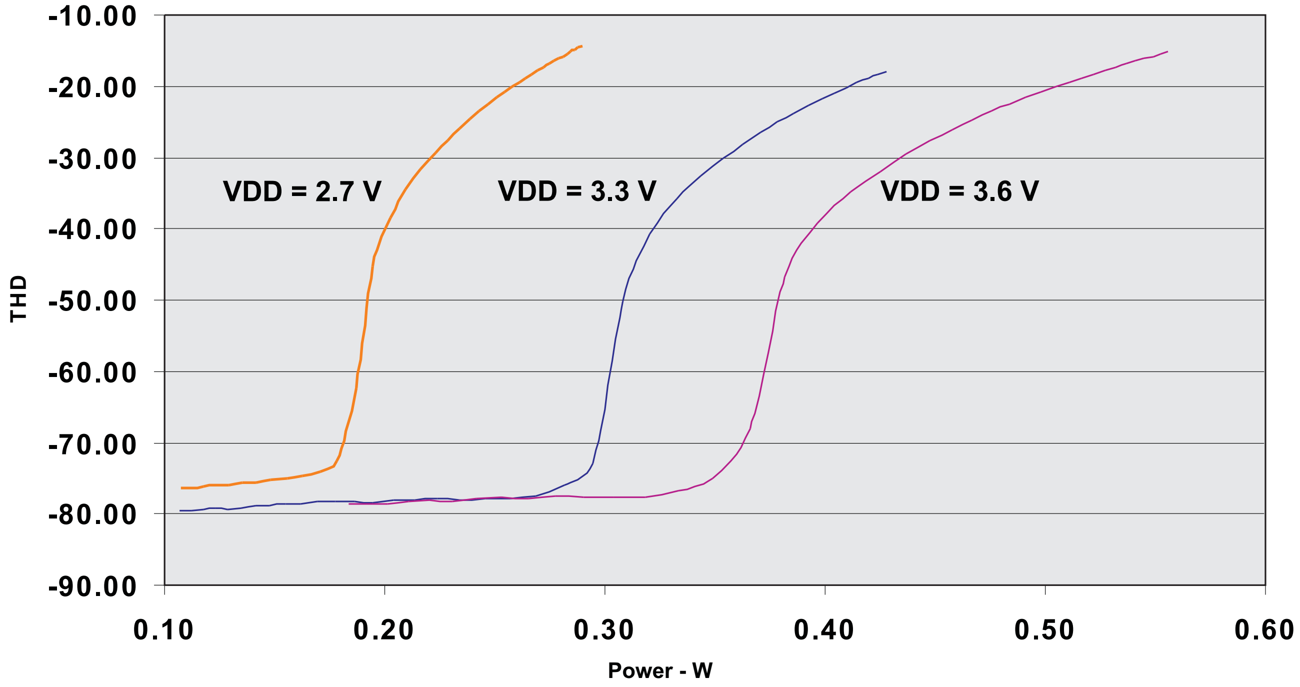


Figure 9. Speaker Power vs THD, 8 Ω Load

TYPICAL CHARACTERISTICS (continued)

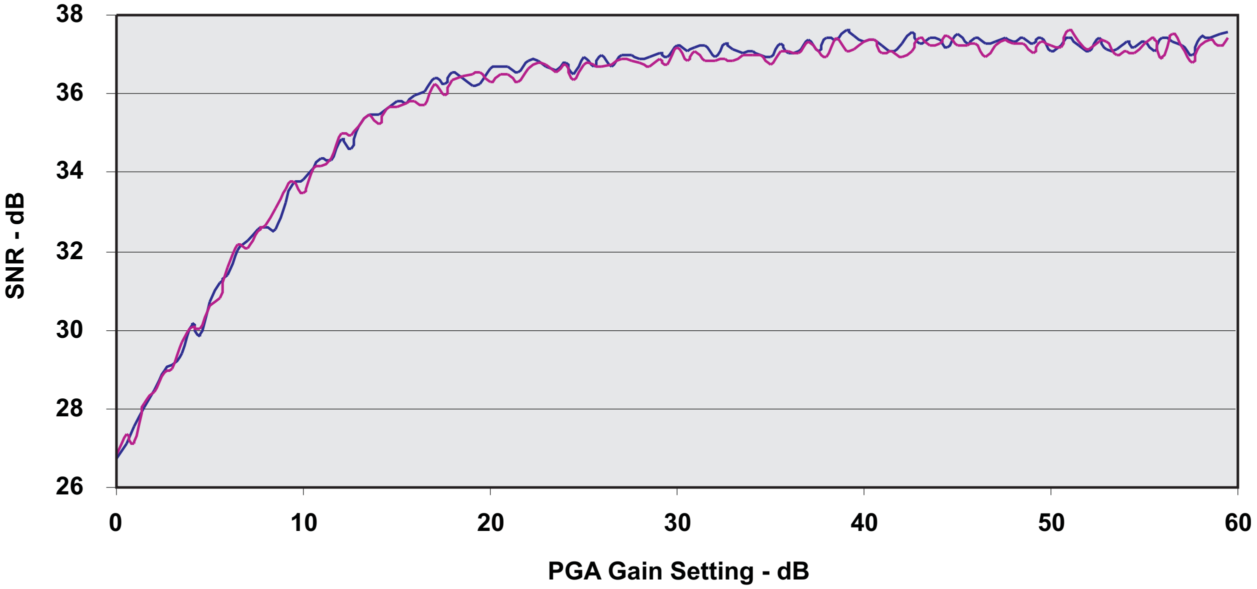


Figure 10. ADC SNR vs PGA Gain Setting, –65 dBFS Input

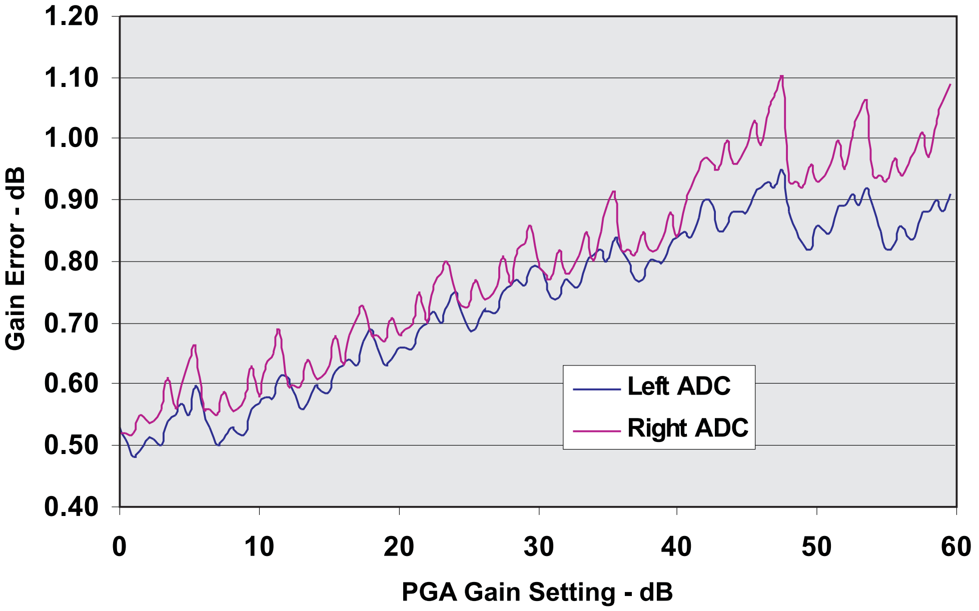


Figure 11. ADC Gain Error vs PGA Gain Setting

TYPICAL CHARACTERISTICS (continued)

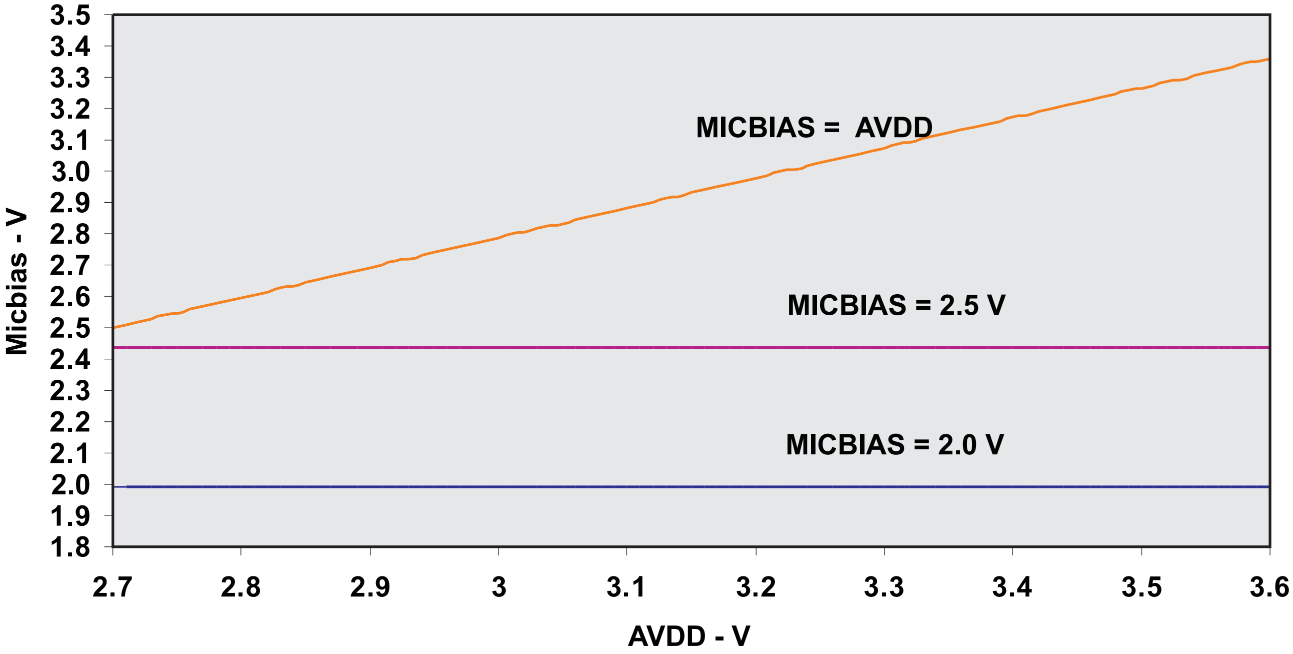


Figure 12. MICBIAS Output Voltage vs AVDD

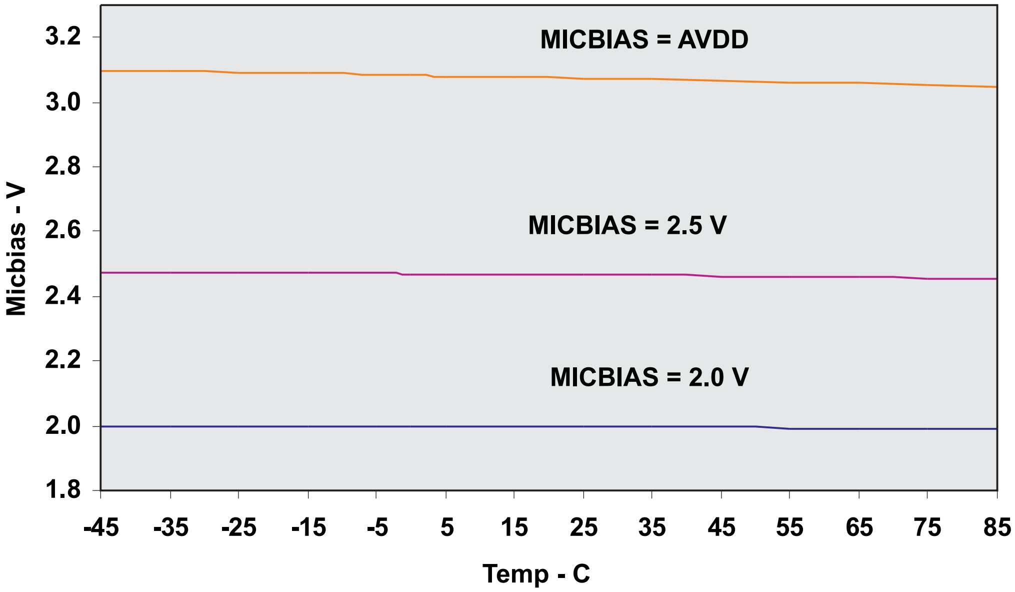


Figure 13. MICBIAS Output Voltage vs Ambient Temperature

TYPICAL CIRCUIT CONFIGURATION

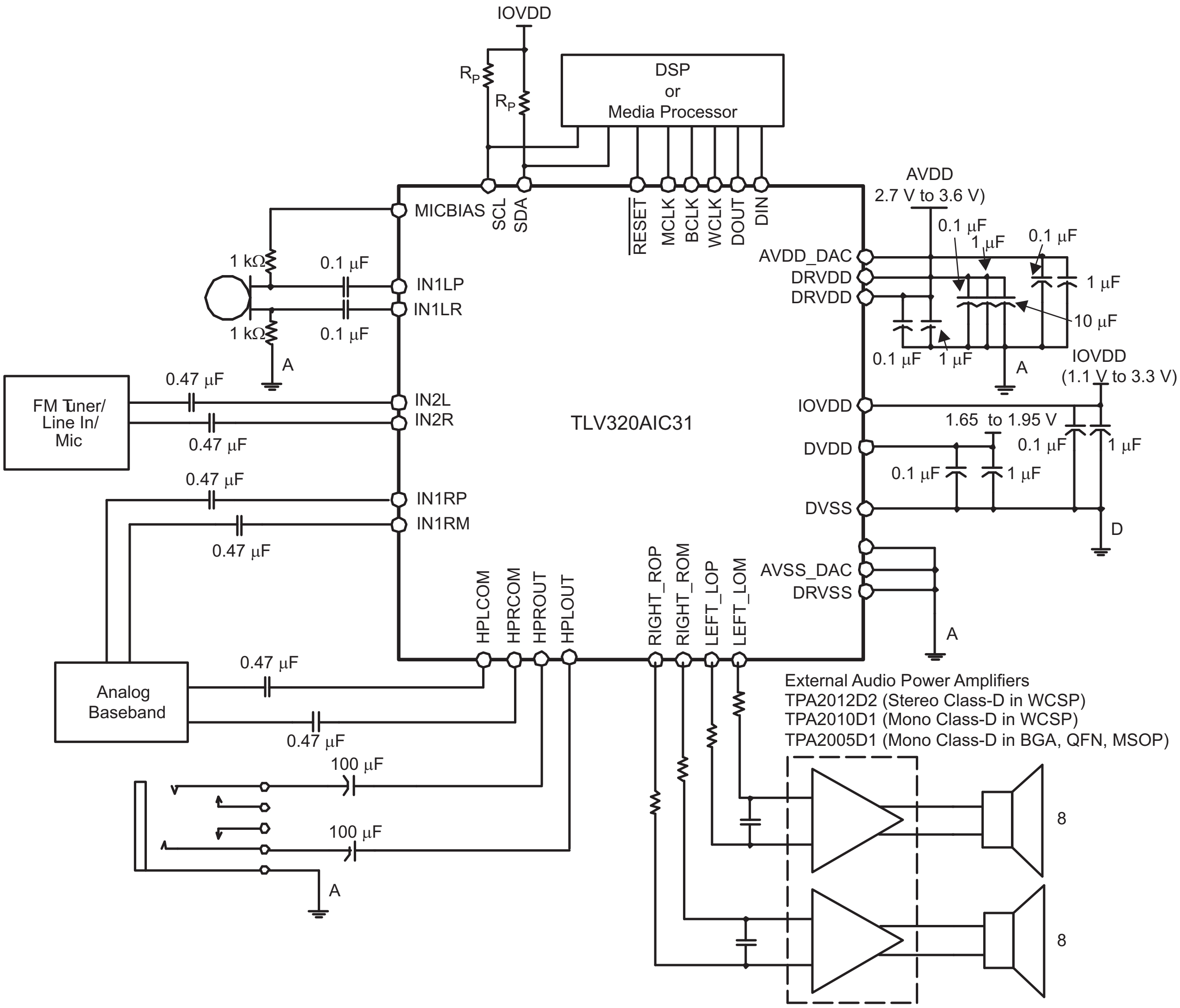

IOVDD
DSP
or
Media Processor
R_P
R_P
MICBIAS
SCL
SDA
RESET
MCLK
BCLK
WCLK
DOUT
DIN
AVDD
2.7 V to 3.6 V)
0.1 µF
1 µF
0.1 µF
AVDD_DAC
DRVDD
DRVDD
1 µF
10 µF
0.1 µF
1 µF
A
IOVDD
(1.1 V to 3.3 V)
1 kΩ
0.1 µF
IN1LP
IN1LR
1 kΩ
0.1 µF
A
0.47 µF
FM Tuner/
Line In/
Mic
IN2L
IN2R
0.47 µF
TLV320AIC31
IOVDD
1.65 to 1.95 V
DVDD
0.1 µF
1 µF
0.1 µF
1 µF
DVSS
D
0.47 µF
IN1RP
IN1RM
0.47 µF
HPLCOM
HPRCOM
HPROUT
HPLOUT
RIGHT_ROP
RIGHT_ROM
LEFT_LOP
LEFT_LOM
AVSS_DAC
DRVSS
A
Analog
Baseband
0.47 µF
0.47 µF
100 µF
100 µF
A
External Audio Power Amplifiers
TPA2012D2 (Stereo Class-D in WCSP)
TPA2010D1 (Mono Class-D in WCSP)
TPA2005D1 (Mono Class-D in BGA, QFN, MSOP)
8
8

Figure 14. Typical Connections for Headphone and Speaker Driver

OVERVIEW

The TLV320AIC31 is a highly flexible, low-power, stereo audio codec with extensive feature integration, intended for applications in smartphones, PDAs, and portable computing, communication, and entertainment applications. Available in a 5 x 5 mm, 32-lead QFN, the product integrates a host of features to reduce cost, board space, and power consumption in space-constrained, battery-powered, portable applications.

The TLV320AIC31 consists of the following blocks:

- Stereo audio multi-bit delta-sigma DAC (8 kHz to 96 kHz)
- Stereo audio multi-bit delta-sigma ADC (8 kHz to 96 kHz)
- Programmable digital audio effects processing (3D, bass/treble/midrange, EQ, de-emphasis)
- Four audio inputs
- Four high-power audio output drivers (headphone/speaker drive capability)
- Two fully differential line output drivers
- Fully programmable PLL
- Headphone/headset jack detection with interrupt

HARDWARE RESET

The TLV320AIC31 requires a hardware reset after power-up for proper operation. After all power supplies are at their specified values, the $\overline{\text{RESET}}$ pin must be driven low for at least 10 ns. If this reset sequence is not performed, the TLV320AIC31 may not respond properly to register reads/writes.

DIGITAL CONTROL SERIAL INTERFACE

The register map of the TLV320AIC31 actually consists of multiple pages of registers, with each page containing 128 registers. The register at address 0 on each page is used as a page-control register, and writing to this register determines the active page for the device. All subsequent read/write operations will access the page that is active at the time, unless a register write is performed to change the active page. Only two pages of registers are implemented in this product, with the active page defaulting to page 0 upon device reset.

For example, at device reset, the active page defaults to page 0, and thus all register read/write operations for addresses 1 to 127 will access registers in page 0. If registers on page 1 must be accessed, the user must write the 8-bit sequence 0x01 to register 0, the page control register, to change the active page from page 0 to page 1. After this write, it is recommended the user also read back the page control register, to safely ensure the change in page control has occurred properly. Future read/write operations to addresses 1 to 127 will now access registers in page 1. When page 0 registers must be accessed again, the user writes the 8-bit sequence 0x00 to register 0, the page control register, to change the active page back to page 0. After a recommended read of the page control register, all further read/write operations to addresses 1 to 127 will now access page 0 registers again.

I^{2}C CONTROL INTERFACE

The TLV320AIC31 supports the I2C control protocol using 7-bit addressing and is capable of both standard and fast modes. For I2C fast mode, note that the minimum timing for each of tHD-STA, tSU-STA, and tSU-STO is 2.0 us, as seen in Figure 15. The TLV320AIC31 will respond to the I^{2}C address of 0011000. I^{2}C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^{2}C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pull-up resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

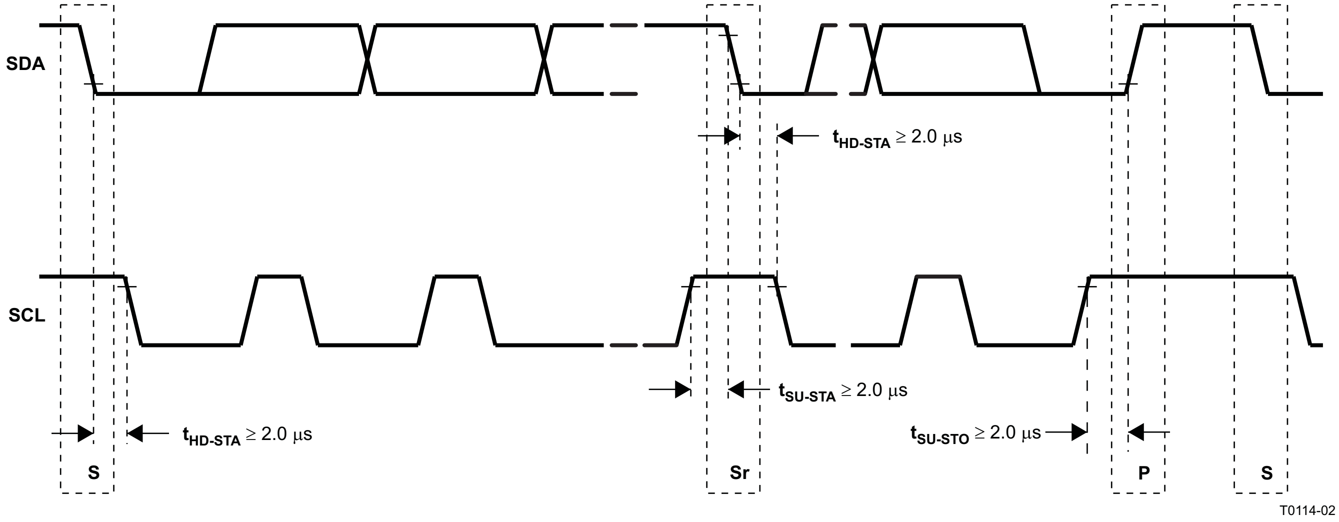


Figure 15. I^{2}C Interface Timing

Communication on the I^{2}C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^{2}C devices can act as masters or slaves, but the TLV320AIC31 can only act as a slave device.

An I^{2}C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data are transmitted across the I^{2}C bus in groups of eight bits. To send a bit on the I^{2}C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is '0'; a HIGH indicates the bit is '1'). Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receiver shift register.

The I^{2}C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. Under most circumstances the master drives the clock line.

Most of the time the bus is idle; no communication takes place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start a communication. They do this by causing a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I^{2}C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^{2}C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^{2}C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit.

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not-acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320AIC31 also responds to and acknowledges a General Call, which consists of the master issuing a command with a slave address byte of 00h.

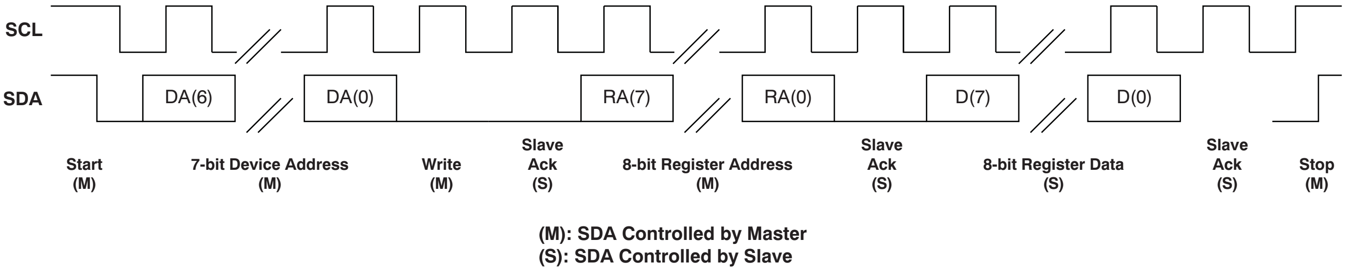

SCL
SDA
DA(6)
DA(0)
RA(7)
RA(0)
D(7)
D(0)
Start (M)
7-bit Device Address (M)
Write (M)
Slave Ack (S)
8-bit Register Address (M)
Slave Ack (S)
8-bit Register Data (S)
Slave Ack (S)
Stop (M)
(M): SDA Controlled by Master
(S): SDA Controlled by Slave

Figure 16. I^{2}C Write

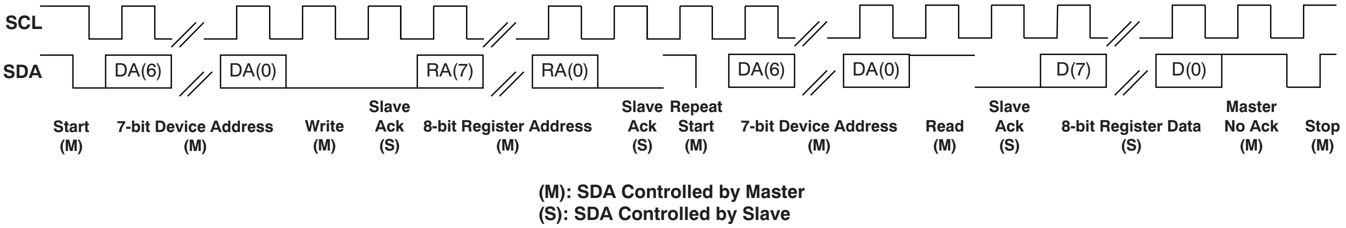

SCL
SDA
DA(6)
DA(0)
RA(7)
RA(0)
DA(6)
DA(0)
D(7)
D(0)
Start (M)
7-bit Device Address (M)
Write (M)
Slave Ack (S)
8-bit Register Address (M)
Slave Ack (S)
Repeat Start (M)
7-bit Device Address (M)
Read (M)
Slave Ack (S)
8-bit Register Data (S)
Master No Ack (M)
Stop (M)
(M): SDA Controlled by Master
(S): SDA Controlled by Slave

Figure 17. I^{2}C Read

In the case of an I^2C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA are treated as data for the next incremental register.

Similarly, in the case of an I^2C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues a ACKNOWLEDGE, the slave takes over control of SDA bus and transmit for the next eight clocks the data of the next incremental register.

DIGITAL AUDIO DATA SERIAL INTERFACE

Audio data are transferred between the host processor and the TLV320AIC31 via the digital audio data serial interface, or *audio bus*. The audio bus of the TLV320AIC31 can be configured for left- or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard telephony PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16-, 20-, 24-, or 32-bits. In addition, the word clock (WCLK) and bit clock (BCLK) can be independently configured in either Master or Slave mode for flexible connectivity to a wide variety of processors

The word clock (WCLK) is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock (BCLK) is used to clock in and out the digital audio data across the serial bus. When in Master mode, this signal can be programmed in two further modes: continuous transfer mode and 256-clock mode. In continuous transfer mode, only the minimal number of bit clocks needed to transfer the audio data are generated, so in general the number of bit clocks per frame will be two times the data width. For example, if data width is chosen as 16-bit, then 32 bit clocks will be generated per frame. If the bit clock signal in master mode will be used by a PLL in another device, it is recommended that the 16-bit or 32-bit data width selections be used. These cases result in a low jitter bit clock signal being generated, having frequencies of $32 \times F_S$ or $64 \times F_S$. In the cases of 20-bit and 24-b-t data width in master mode, the bit clocks generated in each frame will not all be of equal period, due to the device not having a clean $40 \times F_S$ or $48 \times F_S$ clock signal readily available. The average frequency of the bit clock signal is still accurate in these cases (being $40 \times F_S$ or $48 \times F_S$), but the resulting clock signal has higher jitter than in the 16-bit and 32-bit cases.

In 256-clock mode, a constant 256 bit clocks per frame are generated, independent of the data width chosen. The TLV320AIC31 further includes programmability to 3-state the DOUT line during all bit clocks when valid data are not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data will begin, time-division multiplexing (TDM) can be accomplished, resulting in multiple codecs able to use a single audio serial data bus.

When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface will be put into a 3-state output condition.

RIGHT-JUSTIFIED MODE

In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

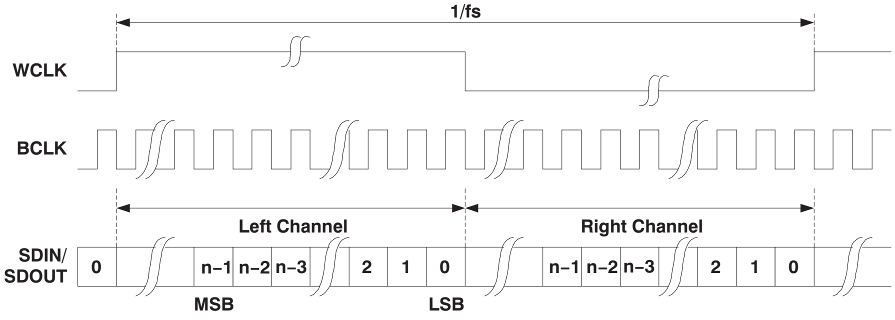

1/fs
WCLK
BCLK
Left Channel
Right Channel
SDIN/
SDOUT
0
n–1
n–2
n–3
2
1
0
n–1
n–2
n–3
2
1
0
MSB
LSB

Figure 18. Right-Justified Serial Bus Mode Operation

LEFT-JUSTIFIED MODE

In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly, the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

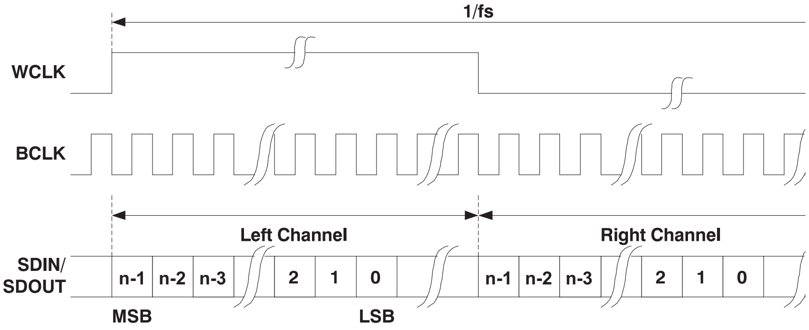

1/fs
WCLK
BCLK
Left Channel
Right Channel
SDIN/
SDOUT
n-1
n-2
n-3
2
1
0
n-1
n-2
n-3
2
1
0
MSB
LSB

Figure 19. Left-Justified Serial Data Bus Mode Operation

I²S MODE

In I²S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

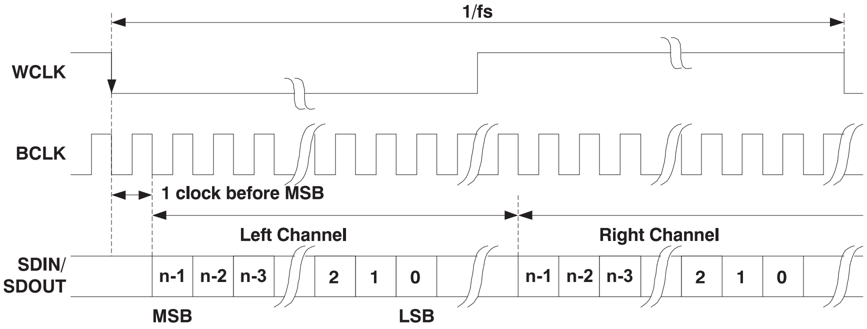

1/fs
WCLK
BCLK
1 clock before MSB
Left Channel
Right Channel
SDIN/
SDOUT
n-1
n-2
n-3
2
1
0
n-1
n-2
n-3
2
1
0
MSB
LSB

Figure 20. I²S Serial Data Bus Mode Operation

DSP MODE

In DSP mode, the rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data. Each data bit is valid on the falling edge of the bit clock.

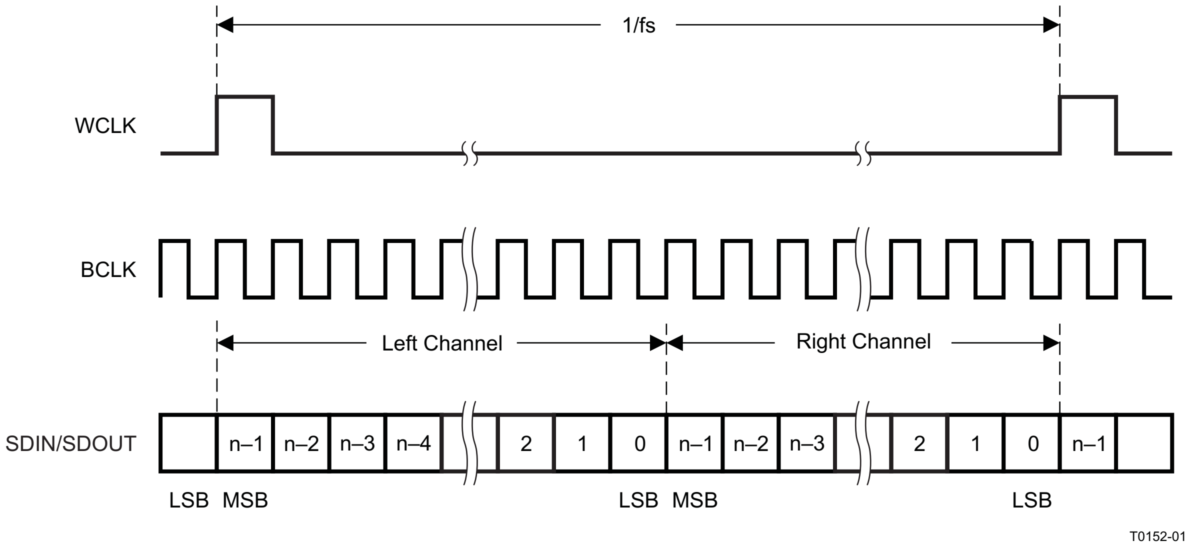


Figure 21. DSP Serial Bus Mode Operation

TDM DATA TRANSFER

Time-division multiplexed (TDM) data transfer can be realized in any of the above transfer modes if the 256-clock bit clock mode is selected, although it is recommended to be used in either left-justified mode or DSP mode. By changing the programmable offset, the bit clock in each frame where the data begin can be changed, and the serial data output driver (DOUT) can also be programmed to 3-state during all bit clocks except when valid data are being put onto the bus. This allows other codecs to be programmed with different offsets and to drive their data onto the same DOUT line, just in a different slot. For incoming data, the codec simply ignores data on the bus except where it is expected based on the programmed offset.

Note that the location of the data when an offset is programmed is different, depending on what transfer mode is selected. In DSP mode, both left and right channels of data are transferred immediately adjacent to each other in the frame. This differs from left-justified mode, where the left and right channel data will always be a half-frame apart in each frame. In this case, as the offset is programmed from zero to some higher value, both the left and right channel data move across the frame, but still stay a full half-frame apart from each other. This is depicted in Figure 22 for the two cases.

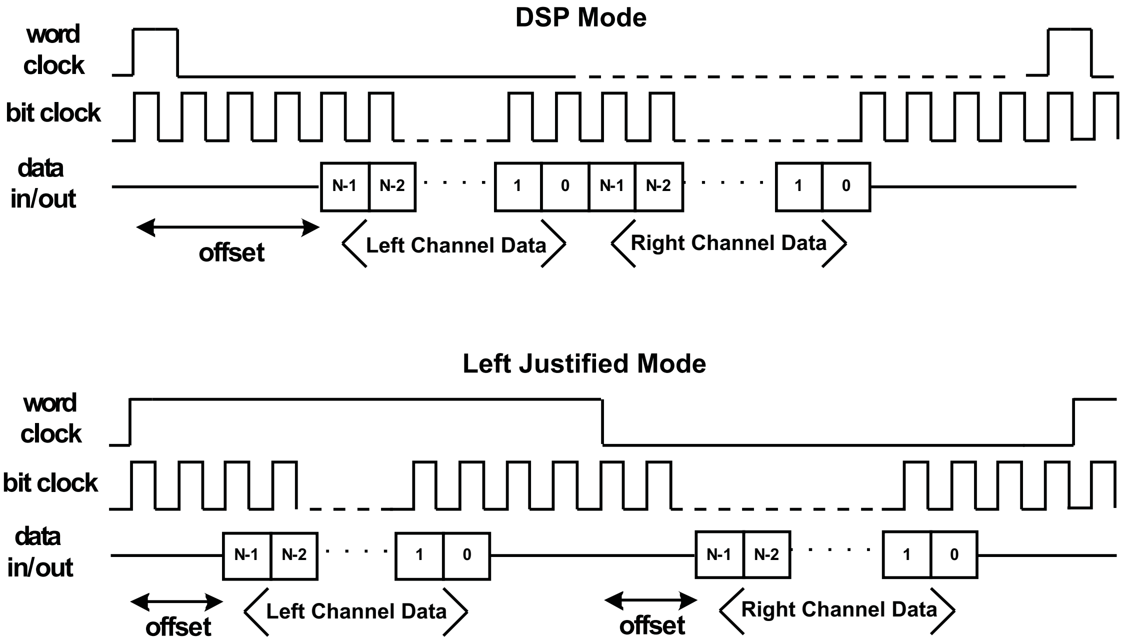

DSP Mode
word clock
bit clock
data in/out
N-1
N-2
1
0
N-1
N-2
1
0
offset
Left Channel Data
Right Channel Data
Left Justified Mode
word clock
bit clock
data in/out
N-1
N-2
1
0
N-1
N-2
1
0
offset
Left Channel Data
offset
Right Channel Data

Figure 22. DSP Mode and Left-Justified Modes, Showing the Effect of a Programmed Data Word Offset

AUDIO DATA CONVERTERS

The TLV320AIC31 supports the following standard audio sampling rates: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz. The converters can also operate at different sampling rates in various combinations, which are described further below.

The data converters are based on the concept of an F_{Sref} rate that is used internal to the part, and it is related to the actual sampling rates of the converters through a series of ratios. For typical sampling rates, F_{Sref} will be either 44.1 kHz or 48 kHz, although it can realistically be set over a wider range of rates up to 53 kHz, with additional restrictions applying if the PLL is used. This concept is used to set the sampling rates of the ADC and DAC, and also to enable high quality playback of low sampling rate data, without high frequency audible noise being generated.

The sampling rate of the ADC and DAC can be set to F_{Sref} / NDAC or 2 × F_{Sref} / NDAC, with NDAC being 1, 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, or 6.

AUDIO CLOCK GENERATION

The audio converters in the TLV320AIC31 need an internal audio master clock at a frequency of 256 × F_{Sref}, which can be obtained in a variety of manners from an external clock signal applied to the device.

A more detailed diagram of the audio clock section of the TLV320AIC31 is shown in Figure 23.

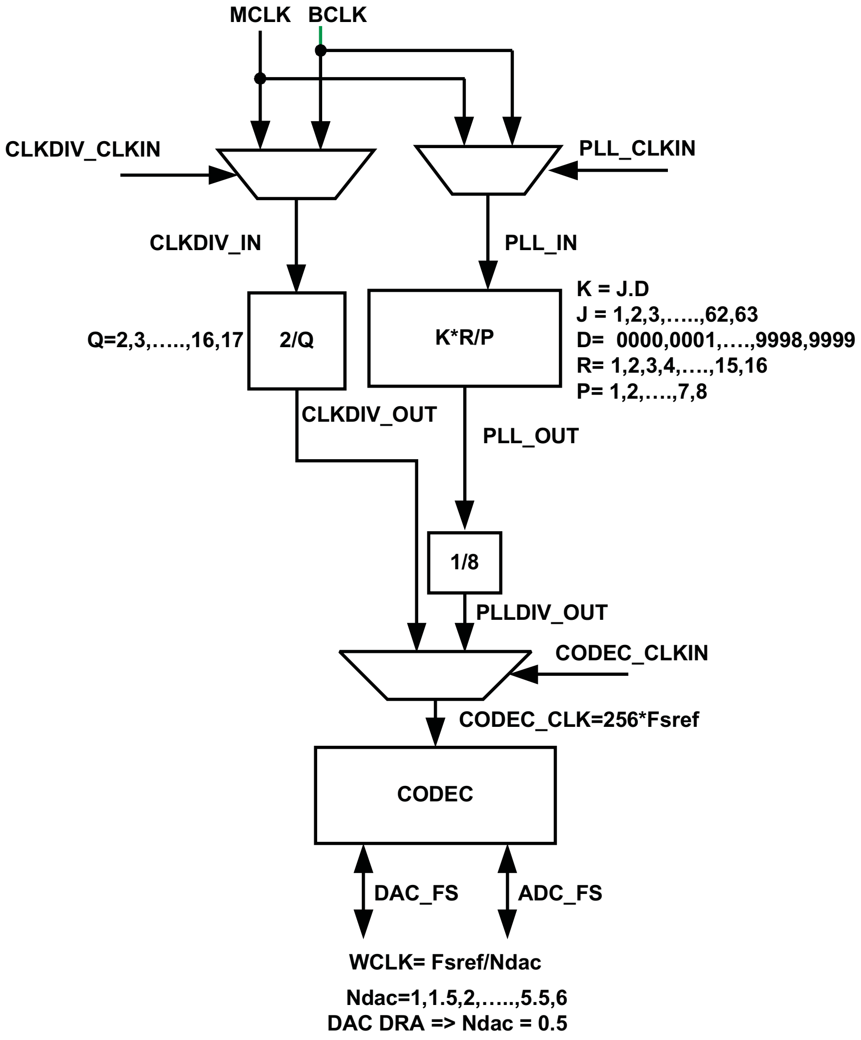

MCLK
BCLK
CLKDIV_CLKIN
PLL_CLKIN
CLKDIV_IN
PLL_IN
K = J.D
J = 1,2,3,…..,62,63
D= 0000,0001,….,9998,9999
R= 1,2,3,4,….,15,16
P= 1,2,….,7,8
Q=2,3,…..,16,17
2/Q
K*R/P
CLKDIV_OUT
PLL_OUT
1/8
PLLDIV_OUT
CODEC_CLKIN
CODEC_CLK=256*Fsref
CODEC
DAC_FS
ADC_FS
WCLK= Fsref/Ndac
Ndac=1,1.5,2,…..,5.5,6
DAC DRA => Ndac = 0.5

Figure 23. Audio Clock Generation Processing

The part can accept an MCLK input from 512 kHz to 50 MHz, which can then be passed through either a programmable divider or a PLL, to get the proper internal audio master clock needed by the part. The BCLK input can also be used to generate the internal audio master clock.

A primary concern is proper operation of the codec at various sample rates with the limited MCLK frequencies available in the system. This device includes a highly programmable PLL to accommodate such situations easily. The integrated PLL can generate audio clocks from a wide variety of possible MCLK inputs, with particular focus paid to the standard MCLK rates already widely used.

When the PLL is disabled,

F_{Sref} = CLKDIV_IN / (128 × Q)

Where Q = 2, 3, …, 17

CLKDIV_IN can be MCLK or BCLK, selected by Page 0, register 102, bits D7-D6.

NOTE: When NDAC = 1.5, 2.5, 3.5, 4.5, or 5.5, odd values of Q are not allowed. In this mode, MCLK can be as high as 50 MHz, and F_{Sref} should fall within 39 kHz to 53 kHz.

When the PLL is enabled,

F_{Sref} = (PLLCLK_IN × K × R) / (2048 × P), where

P = 1, 2, 3,…, 8
R = 1, 2, …, 16
K = J.D
J = 1, 2, 3, …, 63
D = 0000, 0001, 0002, 0003, …, 9998, 9999
PLLCLK_IN can be MCLK or BCLK, selected by register 102, bits D5-D4

P, R, J, and D are register programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

Examples:

If K = 8.5, then J = 8, D = 5000
If K = 7.12, then J = 7, D = 1200
If K = 14.03, then J = 14, D = 0300
If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, the following conditions must be satisfied to meet specified performance:

$2\ \text{MHz} \leq (\text{PLLCLK\_IN} / P) \leq 20\ \text{MHz}$
$80\ \text{MHz} \leq (\text{PLLCLK\_IN} \times K \times R / P) \leq 110\ \text{MHz}$
$4 \leq J \leq 55$

When the PLL is enabled and D ≠ 0000, the following conditions must be satisfied to meet specified performance:

$10\ \text{MHz} \leq \text{PLLCLK\_IN} / P \leq 20\ \text{MHz}$
$80\ \text{MHz} \leq \text{PLLCLK\_IN} \times K \times R / P \leq 110\ \text{MHz}$
$4 \leq J \leq 11$
R = 1

Example:

MCLK = 12 MHz and F_{Sref} = 44.1 kHz
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example:

MCLK = 12 MHz and F_{Sref} = 48.0 kHz
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

Table 1 lists several example cases of typical MCLK rates and how to program the PLL to achieve F_{Sref} = 44.1 kHz or 48 kHz.

Table 1. TYPICAL MCLK RATES

F_{Sref} = 44.1 kHz						
MCLK (MHz)	**P**	**R**	**J**	**D**	**ACHIEVED F_{Sref}**	**% ERROR**
2.8224	1	1	32	0	44100.00	0.0000
5.6448	1	1	16	0	44100.00	0.0000
12.0	1	1	7	5264	44100.00	0.0000
13.0	1	1	6	9474	44099.71	0.0007
16.0	1	1	5	6448	44100.00	0.0000
19.2	1	1	4	7040	44100.00	0.0000
19.68	1	1	4	5893	44100.30	–0.0007
48.0	4	1	7	5264	44100.00	0.0000
F_{Sref} = 48 kHz						
MCLK (MHz)	**P**	**R**	**J**	**D**	**ACHIEVED F_{Sref}**	**% ERROR**
2.048	1	1	48	0	48000.00	0.0000
3.072	1	1	32	0	48000.00	0.0000
4.096	1	1	24	0	48000.00	0.0000
6.144	1	1	16	0	48000.00	0.0000
8.192	1	1	12	0	48000.00	0.0000
12.0	1	1	8	1920	48000.00	0.0000
13.0	1	1	7	5618	47999.71	0.0006
16.0	1	1	6	1440	48000.00	0.0000
19.2	1	1	5	1200	48000.00	0.0000
19.68	1	1	4	9951	47999.79	0.0004
48.0	4	1	8	1920	48000.00	0.0000

STEREO AUDIO ADC

The TLV320AIC31 includes a stereo audio ADC, which uses a delta-sigma modulator with 128x oversampling in single-rate mode, followed by a digital decimation filter. The ADC supports sampling rates from 8 kHz to 48 kHz in single-rate mode, and up to 96 kHz in dual-rate mode. Whenever the ADC or DAC is in operation, the device requires an audio master clock be provided and appropriate audio clock generation be setup within the part.

In order to provide optimal system power dissipation, the stereo ADC can be powered one channel at a time, to support the case where only mono record capability is required. In addition, both channels can be fully powered or entirely powered down.

The integrated digital decimation filter removes high-frequency content and downsamples the audio data from an initial sampling rate of 128 F_S to the final output sampling rate of F_S. The decimation filter provides a linear phase output response with a group delay of 17/F_S. The –3 dB bandwidth of the decimation filter extends to 0.45 F_S and scales with the sample rate (F_S). The filter has minimum 75dB attenuation over the stop band from 0.55 F_S to 64 F_S. Independent digital high-pass filters are also included with each ADC channel, with a corner frequency that can be independently set to three different settings or can be disabled entirely.

Because of the oversampling nature of the audio ADC and the integrated digital decimation filtering, requirements for analog anti-aliasing filtering are very relaxed. The TLV320AIC31 integrates a second order analog anti-aliasing filter with 20-dB attenuation at 1 MHz. This filter, combined with the digital decimation filter, provides sufficient anti-aliasing filtering without requiring additional external components.

The ADC is preceded by a programmable gain amplifier (PGA), which allows analog gain control from 0 dB to 59.5 dB in steps of 0.5 dB. The PGA gain changes are implemented with an internal soft-stepping algorithm that only changes the actual volume level by one 0.5-dB step every one or two ADC output samples, depending on the register programming (see registers Page-0/Reg-19 and Page-0/Reg-22). This soft-stepping ensures that volume control changes occur smoothly with no audible artifacts. On reset, the PGA gain defaults to a mute condition, and upon power down, the PGA soft-steps the volume to mute before shutting down. A read-only flag is set whenever the gain applied by PGA equals the desired value set by the register. The soft-stepping control can also be disabled by programming a register bit. When soft stepping is enabled, the audio master clock must be applied to the part after the ADC power down register is written to ensure the soft-stepping to mute has completed. When the ADC powerdown flag is no longer set, the audio master clock can be shut down.

AUTOMATIC GAIN CONTROL (AGC)

An automatic gain control (AGC) circuit is included with the ADC and can be used to maintain nominally constant output signal amplitude when recording speech signals (it can be fully disabled if not desired). This circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer or farther from the microphone. The AGC algorithm has several programmable settings, including target gain, attack and decay time constants, noise threshold, and maximum PGA gain applicable that allow the algorithm to be fine tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal.

Note that completely independent AGC circuitry is included with each ADC channel with entirely independent control over the algorithm from one channel to the next. This is attractive in cases where two microphones are used in a system, but may have different placement in the end equipment and require different dynamic performance for optimal system operation.

Target gain represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The TLV320AIC31 allows programming of eight different target gains, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Since the device reacts to the signal absolute average and not to peak levels, it is recommended that the larger gain be set with enough margin to avoid clipping at the occurrence of loud sounds.

Attack time determines how quickly the AGC circuitry reduces the PGA gain when the input signal is too loud. It can be varied from 8 ms to 20 ms.

Decay time determines how quickly the PGA gain is increased when the input signal is too low. It can be varied in the range from 100 ms to 500 ms.

Noise gate threshold determines the level below which if the input speech average value falls, AGC considers it as a silence, and thus reduces the gain to 0 dB in steps of 0.5 dB every F_S and sets the noise threshold flag. The gain stays at 0 dB unless the input speech signal average rises above the noise threshold setting. This ensures that noise does not get gained up in the absence of speech. Noise threshold level in the AGC algorithm is programmable from –30 dB to –90 dB relative to full scale. A disable noise gate feature is also available. This operation includes programmable debounce and hysteresis functionality to avoid the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. When the noise threshold flag is set, the status of gain applied by the AGC and the saturation flag should be ignored.

Maximum PGA gain applicable allows the user to restrict the maximum PGA gain that can be applied by the AGC algorithm. This can be used for limiting PGA gain in situations where environmental noise is greater than programmed noise threshold. It can be programmed from 0 dB to +59.5 dB in steps of 0.5 dB.

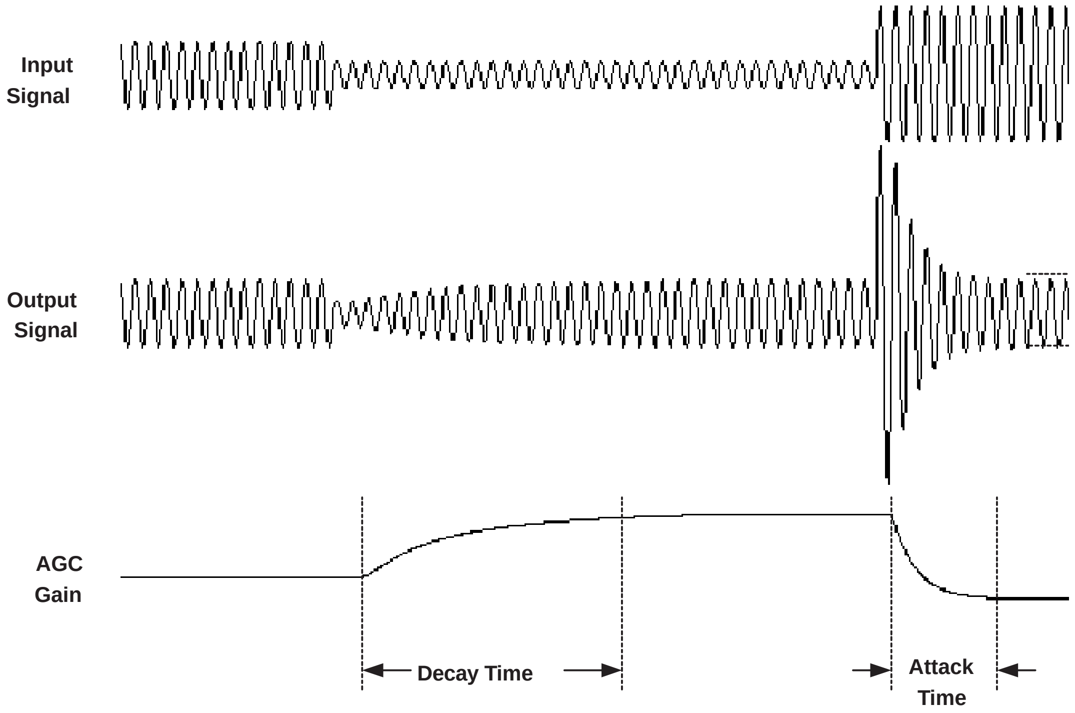


Figure 24. Typical Operation of the AGC Algorithm During Speech Recording

Note that the time constants here are correct when the ADC is not in double-rate audio mode. The time constants are achieved using the F_{Sref} value programmed in the control registers. However, if the F_{Sref} is set in the registers to, for example, 48 kHz, but the actual audio clock or PLL programming actually results in a different F_{Sref} in practice, then the time constants would not be correct.

STEREO AUDIO DAC

The TLV320AIC31 includes a stereo audio DAC supporting sampling rates from 8 kHz to 96 kHz. Each channel of the stereo audio DAC consists of a digital audio processing block, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20 kHz. This is realized by keeping the upsampled rate constant at $128 \times F_{Sref}$ and changing the oversampling ratio as the input sample rate is changed. For an F_{Sref} of 48 kHz, the digital delta-sigma modulator always operates at a rate of 6.144 MHz. This ensures that quantization noise generated within the delta-sigma modulator stays low within the frequency band below 20 kHz at all sample rates. Similarly, for an F_{Sref} rate of 44.1 kHz, the digital delta-sigma modulator always operates at a rate of 5.6448 MHz.

The following restrictions apply in the case when the PLL is powered down and double-rate audio mode is enabled in the DAC.

Allowed Q values = 4, 8, 9, 12, 16

Q values where equivalent F_{Sref} can be achieved by turning on PLL

Q = 5, 6, 7 (set P = 5 / 6 / 7 and K = 16.0 and PLL enabled)

Q = 10, 14 (set P = 5, 7 and K = 8.0 and PLL enabled)

DIGITAL AUDIO PROCESSING

The DAC channel consists of optional filters for de-emphasis and bass/treble/midrange level adjustment, speaker equalization, and 3D effects processing. The de-emphasis function is implemented by a programmable digital filter block with fully programmable coefficients (see Page-1/Reg-21 through Page-1/Reg-26 for left channel, Page-1/Reg-47 through Page-1/Reg-52 for right channel). If de-emphasis is not required in a particular application, this programmable filter block can be used for some other purpose. The de-emphasis filter transfer function is given by Equation 1:

$$H(z) = \frac{N0 + N1 \times z^{-1}}{32768 - D1 \times z^{-1}} \tag{1}$$

where the N0, N1, and D1 coefficients are fully programmable individually for each channel. The coefficients that should be loaded to implement standard de-emphasis filters are given in Table 2.

Table 2. De-Emphasis Coefficients for Common Audio Sampling Rates

SAMPLING FREQUENCY	N0	N1	D1
32-kHz	16950	–1220	17037
44.1-kHz	15091	–2877	20555
48-kHz (1)	14677	–3283	21374

(1) Default de-emphasis coefficients

In addition to the de-emphasis filter block, the DAC digital effects processing includes a fourth order digital IIR filter with programmable coefficients (one set per channel). This filter is implemented as cascade of two biquad sections with frequency response given by Equation 2:

$$\left(\frac{N0 + 2 \times N1 \times z^{-1} + N2 \times z^{-2}}{32768 - 2 \times D1 \times z^{-1} - D2 \times z^{-2}}\right)\left(\frac{N3 + 2 \times N4 \times z^{-1} + N5 \times z^{-2}}{32768 - 2 \times D4 \times z^{-1} - D5 \times z^{-2}}\right) \tag{2}$$

The N and D coefficients are fully programmable, and the entire filter can be enabled or bypassed. The structure of the filtering when configured for independent channel processing is shown below in Figure 25, with LB1 corresponding to the first left-channel biquad filter using coefficients N0, N1, N2, D1, and D2. LB2 similarly corresponds to the second left-channel biquad filter using coefficients N3, N4, N5, D4, and D5. The RB1 and RB2 filters refer to the first and second right-channel biquad filters, respectively.

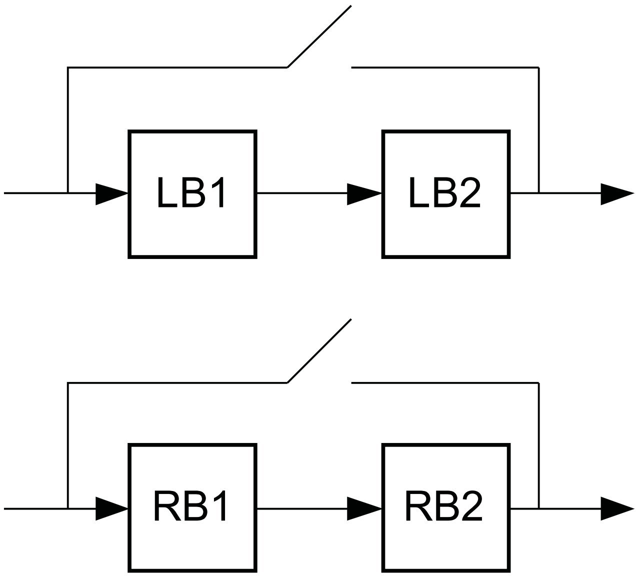


Figure 25. Structure of the Digital Effects Processing for Independent Channel Processing

The coefficients for this filter implement a variety of sound effects, with bass-boost or treble boost being the most commonly used in portable audio applications. The default N and D coefficients in the part are given in Table 3 and implement a shelving filter with 0-dB gain from dc to approximately 150 Hz, at which point it rolls off to a 3-dB attenuation for higher frequency signals, thus giving a 3-dB boost to signals below 150 Hz. The N and D coefficients are represented by 16-bit twos complement numbers with values ranging from –32768 to 32767.

Table 3. Default Digital Effects Processing Filter Coefficients, When in Independent Channel Processing Configuration

Coefficients				
N0 = N3	**D1 = D4**	**N1 = N4**	**D2 = D5**	**N2 = N5**
27619	32131	–27034	–31506	26461

The digital processing also includes capability to implement 3D processing algorithms by providing means to process the mono mix of the stereo input, and then combine this with the individual channel signals for stereo output playback. The architecture of this processing mode, and the programmable filters available for use in the system, is shown in Figure 26. Note that the programmable attenuation block provides a method of adjusting the level of 3D effect introduced into the final stereo output. This combined with the fully programmable biquad filters in the system enables the user to fully optimize the audio effects for a particular system and provide extensive differentiation from other systems using the same device.

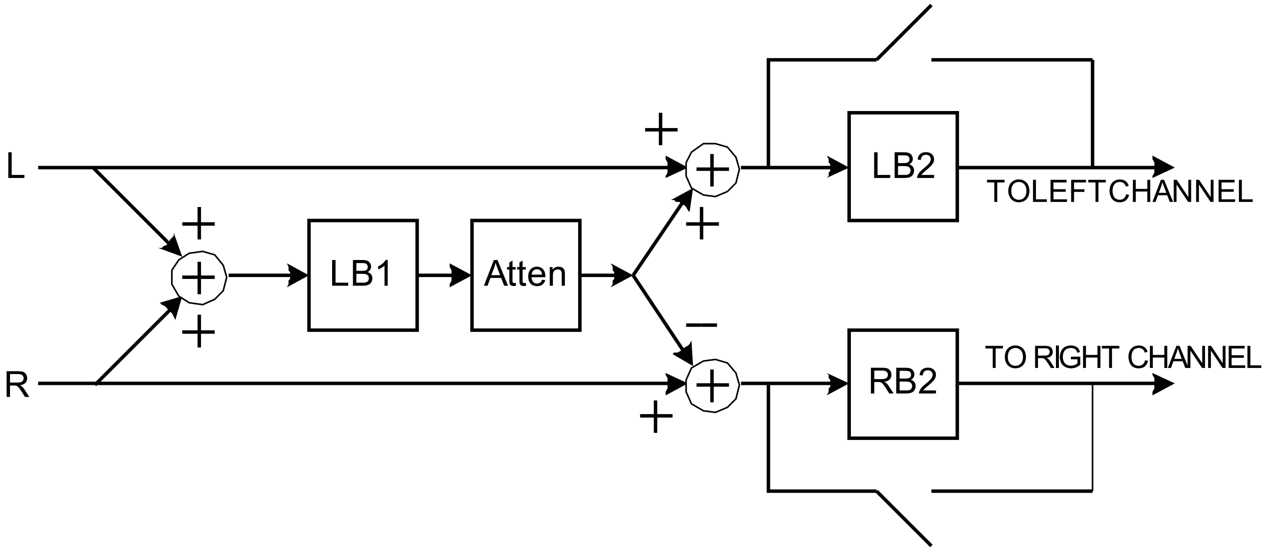


Figure 26. Architecture of the Digital Audio Processing When 3D Effects are Enabled

It is recommended that the digital effects filters be disabled while the filter coefficients are being modified. While new coefficients are being written to the device over the control port, it is possible that a filter using partially updated coefficients may actually implement an unstable system and lead to oscillation or objectionable audio output. By disabling the filters, changing the coefficients, and then re-enabling the filters, these types of effects can be entirely avoided.

DIGITAL INTERPOLATION FILTER

The digital interpolation filter upsamples the output of the digital audio processing block by the required oversampling ratio before data are provided to the digital delta-sigma modulator and analog reconstruction filter stages. The filter provides a linear phase output with a group delay of 21/F_S. In addition, programmable digital interpolation filtering is included to provide enhanced image filtering and reduce signal images caused by the upsampling process that are below 20 kHz. For example, upsampling an 8-kHz signal produces signal images at multiples of 8-kHz (that is, 8 kHz, 16 kHz, 24 kHz, etc.). The images at 8 kHz and 16 kHz are below 20 kHz and still audible to the listener; therefore, they must be filtered heavily to maintain a good quality output. The interpolation filter is designed to maintain at least 65-dB rejection of images that land below 7.455 F_S. In order to utilize the programmable interpolation capability, the F_{Sref} should be programmed to a higher rate (restricted to be in the range of 39 kHz to 53 kHz when the PLL is in use), and the actual F_S is set using the NDAC divider. For example, if F_S = 8 kHz is required, then F_{Sref} can be set to 48 kHz, and the DAC F_S set to F_{Sref}/6. This ensures that all images of the 8-kHz data are sufficiently attenuated well beyond a 20-kHz audible frequency range.

DELTA-SIGMA AUDIO DAC

The stereo audio DAC incorporates a third order, multi-bit delta-sigma modulator followed by an analog reconstruction filter. The DAC provides high-resolution, low-noise performance, using oversampling and noise shaping techniques. The analog reconstruction filter design consists of a 6-tap analog FIR filter followed by a continuous time RC filter. The analog FIR operates at a rate of 128 × F_{Sref} (6.144 MHz when F_{Sref} = 48 kHz, 5.6448 MHz when F_{Sref} = 44.1 kHz). Note that the DAC analog performance may be degraded by excessive clock jitter on the MCLK input. Therefore, care must be taken to keep jitter on this clock to a minimum.

AUDIO DAC DIGITAL VOLUME CONTROL

The audio DAC includes a digital volume control block which implements a programmable digital gain. The volume level can be varied from 0 dB to –63.5 dB in 0.5-dB steps, in addition to a mute bit, independently for each channel. The volume level of both channels can also be changed simultaneously by the master volume control. Gain changes are implemented with a soft-stepping algorithm, which only changes the actual volume by one step per input sample, either up or down, until the desired volume is reached. The rate of soft-stepping can be slowed to one step per two input samples through a register bit.

Because of soft-stepping, the host does not know when the DAC has been actually muted. This may be important if the host wishes to mute the DAC before making a significant change, such as changing sample rates. In order to help with this situation, the device provides a flag back to the host via a read-only register bit that alerts the host when the part has completed the soft-stepping and the actual volume has reached the desired volume level. The soft-stepping feature can be disabled through register programming. If soft-stepping is enabled, the MCLK signal should be kept applied to the device until the DAC power-down flag is set. When this flag is set, the internal soft-stepping process and power down sequence is complete, and the MCLK can then be stopped if desired.

The TLV320AIC31 also includes functionality to detect when the user switches on or off the de-emphasis or digital audio processing functions, to (1) soft-mute the DAC volume control, (2) change the operation of the digital effects processing, and (3) soft-unmute the part. This avoids any possible pop/clicks in the audio output due to instantaneous changes in the filtering. A similar algorithm is used when first powering up or down the DAC. The circuit begins operation at power up with the volume control muted, then soft-steps it up to the desired volume level. At power down, the logic first soft-steps the volume down to a mute level, then powers down the circuitry.

ANALOG OUTPUT COMMON-MODE ADJUSTMENT

The output common-mode voltage and output range of the analog output are determined by an internal bandgap reference, in contrast to other codecs that may use a divided version of the supply. This scheme is used to reduce the coupling of noise that may be on the supply (such as 217-Hz noise in a GSM cellphone) into the audio signal path.

However, due to the possible wide variation in analog supply range (2.7 V to 3.6 V), an output common-mode voltage setting of 1.35 V, which would be used for a 2.7 V supply case, will be overly conservative if the supply is actually much larger, such as 3.3 V or 3.6 V. In order to optimize device operation, the TLV320AIC31 includes a programmable output common-mode level, which can be set by register programming to a level most appropriate to the actual supply range used by a particular customer. The output common-mode level can be varied among four different values, ranging from 1.35 V (more appropriate for low supply ranges, near 2.7 V) to 1.8 V (more appropriate for high supply ranges, near 3.6 V). Note that there is also some limitation on the range of DVDD voltage as well in determining which setting is most appropriate.

Table 4. Appropriate Settings

CM SETTING	RECOMMENDED AVDD, DRVDD	RECOMMENDED DVDD
1.35	2.7 V to 3.6 V	1.65 V to 1.95 V
1.50	3.0 V to 3.6 V	1.65 V to 1.95 V
1.65 V	3.3 V to 3.6 V	1.8 V to 1.95 V
1.8 V	3.6 V	1.95 V

AUDIO DAC POWER CONTROL

The stereo DAC can be fully powered up or down, and in addition, the analog circuitry in each DAC channel can be powered up or down independently. This provides power savings when only a mono playback stream is needed.

AUDIO ANALOG INPUTS

The TLV320AIC31 includes six analog audio input pins, which can be configured as two fully-differential pair plus one single-ended pair of audio inputs, or four single-ended audio inputs. These six pins connect through series resistors and switches to the virtual ground terminals of two fully differential opamps (one per ADC/PGA channel). By selecting to turn on only one set of switches per opamp at a time, the inputs can be effectively muxed to each ADC PGA channel

By selecting to turn on multiple sets of switches per op amp at a time, mixing can also be achieved. However, single-ended and fully-differential audio inputs cannot be mixed into the same ADC PGA at the same time. Mixing of multiple inputs can easily lead to PGA outputs that exceed the range of the internal opamps, resulting in saturation and clipping of the mixed output signal. Whenever mixing is being implemented, the user should take adequate precautions to avoid such a saturation case from occurring. In general, the mixed signal should not exceed $2V_{PP}$ single-ended or $4V_{PP}$ fully-differential.

In most mixing applications, there is also a general need to adjust the levels of the individual signals being mixed. For example, if a soft signal and a large signal are to be mixed and played together, the soft signal generally should be amplified to a level comparable to the large signal before mixing. In order to accommodate this need, the TLV320AIC31 includes input level control on each of the individual inputs before they are mixed or muxed into the ADC PGAs, with gain programmable from 0 dB to –12 dB in 1.5-dB steps. Note that this input level control is not intended to be a volume control, but instead used occasionally for level setting. Soft-stepping of the input level control settings is implemented in this device, with the speed and functionality following the settings used by the ADC PGA for soft-stepping.

The TLV320AIC31 supports the ability to mix up to two fully-differential analog inputs into each ADC PGA channel. Figure 27 shows the mixing configuration for the left channel, which can mix the signals IN1LP-IN1LM and IN1RP-IN1RM.

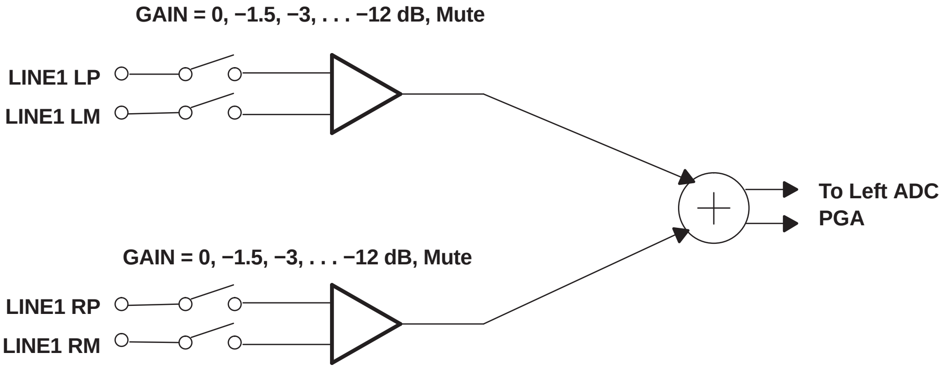

GAIN = 0, −1.5, −3, . . . −12 dB, Mute
LINE1 LP
LINE1 LM
To Left ADC
PGA
GAIN = 0, −1.5, −3, . . . −12 dB, Mute
LINE1 RP
LINE1 RM

Figure 27. Left Channel Fully-Differential Analog Mixing Capability

Two fully-differential analog inputs can similarly be mixed into the right ADC PGA as well, consisting of IN1RP-IN1RM and IN1LP-IN1LM. Note that it is not necessary to mix both fully-differential signals if this is not desired—unnecessary inputs can simply be muted using the input level control registers.

Inputs can also be selected as single-ended instead of fully-differential, and mixing or muxing into the ADC PGAs is also possible in this mode. It is not possible, however, for an input pair to be selected as fully-differential for connection to one ADC PGA and simultaneously selected as single-ended for connection to the other ADC PGA channel. However, it is possible for an input to be selected or mixed into both left and right channel PGAs, as long as it has the same configuration for both channels (either both single-ended or both fully-differential).

Figure 28 shows the single-ended mixing configuration for the left channel ADC PGA, which enables mixing of the signals IN11LP, IN1RP, IN2L, and IN2R. The right channel ADC PGA mix is similar, enabling mixing of the signals IN11LP, IN1RP, IN2L, and IN2R.

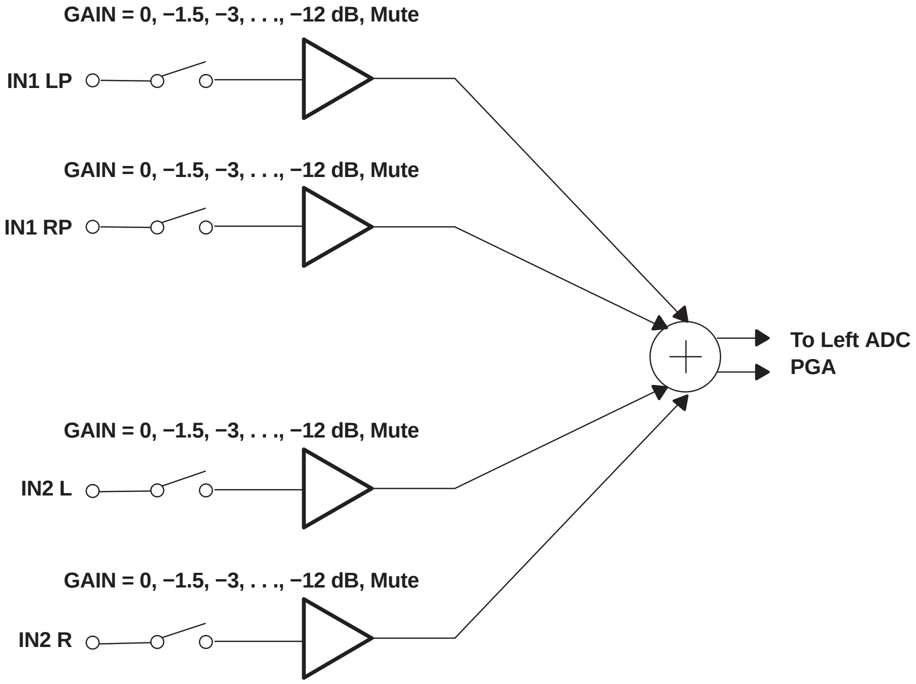

GAIN = 0, −1.5, −3, . . ., −12 dB, Mute
IN1 LP
GAIN = 0, −1.5, −3, . . ., −12 dB, Mute
IN1 RP
To Left ADC
PGA
GAIN = 0, −1.5, −3, . . ., −12 dB, Mute
IN2 L
GAIN = 0, −1.5, −3, . . ., −12 dB, Mute
IN2 R

Figure 28. Left Channel Single-Ended Analog Input Mixing Configuration

ADC PGA SIGNAL BYPASS PATH FUNCTIONALITY

In addition to the input bypass path described above, the TLV320AIC31 also includes the ability to route the ADC PGA output signals past the ADC, for mixing with other analog signals and then direction connection to the output drivers. These bypass functions are described in more detail in the sections on output mixing and output driver configurations.

INPUT IMPEDANCE AND VCM CONTROL

The TLV320AIC31 includes several programmable settings to control analog input pins, particularly when they are not selected for connection to an ADC PGA. The default option allows unselected inputs to be put into a 3-state condition, such that the input impedance seen looking into the device is extremely high. Note, however, that the pins on the device do include protection diode circuits connected to AVDD and AVSS. Thus, if any voltage is driven onto a pin approximately one diode drop (~0.6 V) above AVDD or one diode drop below AVSS, these protection diodes will begin conducting current, resulting in an effective impedance that no longer appears as a 3-state condition.

Another programmable option for unselected analog inputs is to weakly hold them at the common-mode input voltage of the ADC PGA (which is determined by an internal bandgap voltage reference). This is useful to keep the ac-coupling capacitors connected to analog inputs biased up at a normal dc level, thus avoiding the need for them to charge up suddenly when the input is changed from being unselected to selected for connection to an ADC PGA. This option is controlled in Page-0/Reg-20 and Page-0/Reg-23. The user should ensure this option is disabled when an input is selected for connection to an ADC PGA or selected for the analog input bypass path, since it can corrupt the recorded input signal if left operational when an input is selected.

In most cases, the analog input pins on the TLV320AIC31 should be ac-coupled to analog input sources, the only exception to this generally being if an ADC is being used for dc voltage measurement. The ac-coupling capacitor will cause a high-pass filter pole to be inserted into the analog signal path, so the size of the capacitor must be chosen to move that filter pole sufficiently low in frequency to cause minimal effect on the processed analog signal. The input impedance of the analog inputs when selected for connection to an ADC PGA varies with the setting of the input level control, starting at approximately 20 kΩ with an input level control setting of 0 dB, and increasing to approximately 80 kΩ when the input level control is set at –12 dB. For example, using a 0.1-µF ac-coupling capacitor at an analog input will result in a high-pass filter pole of 80 Hz when the 0-dB input level control setting is selected.

MICBIAS GENERATION

The TLV320AIC31 includes a programmable microphone bias output voltage (MICBIAS), capable of providing output voltages of 2.0 V or 2.5 V (both derived from the on-chip bandgap voltage) with 4-mA output current drive. In addition, MICBIAS may be programmed to be switched to AVDD directly through an on-chip switch, or it can be powered down completely when not needed, for power savings. This function is controlled by register programming in Page-0/Reg-25.

ANALOG FULLY DIFFERENTIAL LINE OUTPUT DRIVERS

The TLV320AIC31 has two fully differential line output drivers, each capable of driving a 10-kΩ differential load. The output stage design leading to the fully differential line output drivers is shown in Figure 29 and Figure 30. This design includes extensive capability to adjust signal levels independently before any mixing occurs, beyond that already provided by the PGA gain and the DAC digital volume control.

The PGA_L/R signals refer to the outputs of the ADC PGA stages that are similarly passed around the ADC to the output stage. Note that since both left and right channel signals are routed to all output drivers, a mono mix of any of the stereo signals can easily be obtained by setting the volume controls of both left and right channel signals to –6 dB and mixing them. Undesired signals can also be disconnected from the mix as well through register control.

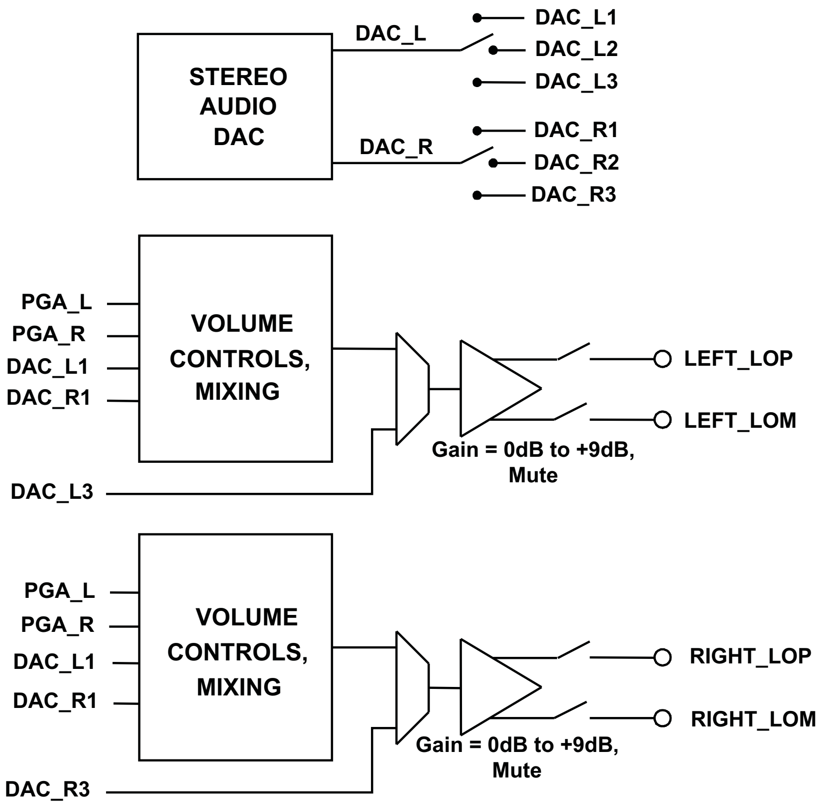

STEREO AUDIO DAC
DAC_L
DAC_R
DAC_L1
DAC_L2
DAC_L3
DAC_R1
DAC_R2
DAC_R3
PGA_L
PGA_R
DAC_L1
DAC_R1
VOLUME CONTROLS, MIXING
DAC_L3
LEFT_LOP
LEFT_LOM
Gain = 0dB to +9dB, Mute
PGA_L
PGA_R
DAC_L1
DAC_R1
VOLUME CONTROLS, MIXING
DAC_R3
RIGHT_LOP
RIGHT_LOM
Gain = 0dB to +9dB, Mute

Figure 29. Architecture of the Output Stage Leading to the Fully Differential Line Output Drivers

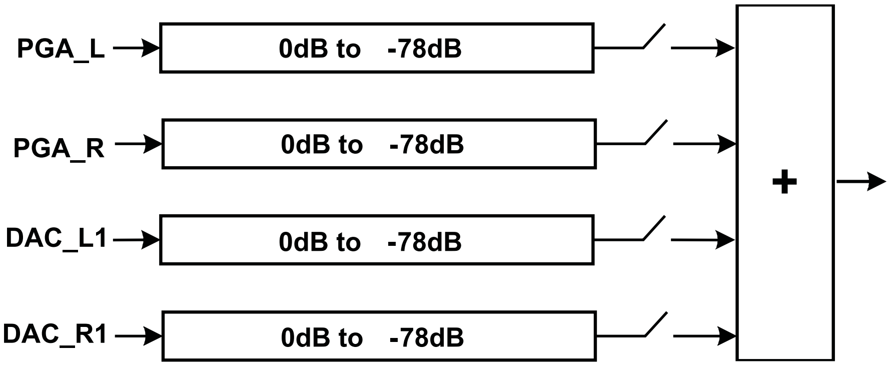

PGA_L
0dB to -78dB
PGA_R
0dB to -78dB
DAC_L1
0dB to -78dB
DAC_R1
0dB to -78dB
+

Figure 30. Detail of the Volume Control and Mixing Function Shown in Figure 25 and Figure 16

The DAC_L/R signals are the outputs of the stereo audio DAC, which can be steered by register control based on the requirements of the system. If mixing of the DAC audio with other signals is not required, and the DAC output is only needed at the stereo line outputs, then it is recommended to use the routing through path DAC_L3/R3 to the fully differential stereo line outputs. This results not only in higher quality output performance, but also in lower power operation, since the analog volume controls and mixing blocks ahead of these drivers can be powered down. This connection path will attenuate the signal by a factor of 1 dB.

If instead the DAC analog output must be routed to multiple output drivers simultaneously (such as to LEFT_LOP/M, and RIGHT_LOP/M) or must be mixed with other analog signals, then the DAC outputs should be switched through the DAC_L1/R1 path. This option provides the maximum flexibility for routing of the DAC analog signals to the output drivers

The TLV320AIC31 includes an output level control on each output driver with limited gain adjustment from 0 dB to 9 dB. The output driver circuitry in this device are designed to provide a low distortion output while playing full-scale stereo DAC signals at a 0-dB gain setting. However, a higher amplitude output can be obtained at the cost of increased signal distortion at the output. This output level control allows the user to make this tradeoff based on the requirements of the end equipment. Note that this output level control is not intended to be used as a standard output volume control. It is expected to be used only sparingly for level setting, that is, adjustment of the full-scale output range of the device.

Each differential line output driver can be powered down independently of the others when it is not needed in the system. When placed into powerdown through register programming, the driver output pins will be placed into a 3-state, high-impedance state.

ANALOG HIGH POWER OUTPUT DRIVERS

The TLV320AIC31 includes four high-power output drivers with extensive flexibility in their usage. These output drivers are individually capable of driving 40 mW each into a 16-Ω load in single-ended configuration, and they can be used in pairs to drive up to 500 mW into an 8-Ω load connected in bridge-terminated load (BTL) configuration between two driver outputs.

The high-power output drivers can be configured in a variety of ways, including:

1. driving up to two fully differential output signals
2. driving up to four single-ended output signals
3. driving two single-ended output signals, with one or two of the remaining drivers driving a fixed VCM level, for a pseudo-differential stereo output
4. driving one or two 8-Ω speakers connected BTL between pairs of driver output pins
5. driving stereo headphones in single-ended configuration with two drivers, while the remaining two drivers are connected in BTL configuration to an 8-Ω speaker.

The output stage architecture leading to the high-power output drivers is shown in Figure 31, with the volume control and mixing blocks being effectively identical to that shown in Figure 30. Note that each of these drivers have a output level control block like those included with the line output drivers, allowing gain adjustment up to +9 dB on the output signal. As in the previous case, this output level adjustment is not intended to be used as a standard volume control, but instead is included for additional full-scale output signal level control.

Two of the output drivers, HPROUT and HPLOUT, include a direct connection path for the stereo DAC outputs to be passed directly to the output drivers and bypass the analog volume controls and mixing networks, using the DAC_L2/R2 path. As in the line output case, this functionality provides the highest quality DAC playback performance with reduced power dissipation, but can only be utilized if the DAC output does not need to route to multiple output drivers simultaneously, and if mixing of the DAC output with other analog signals is not needed. This direct connection path will attenuate the signal by a factor of 1 dB.

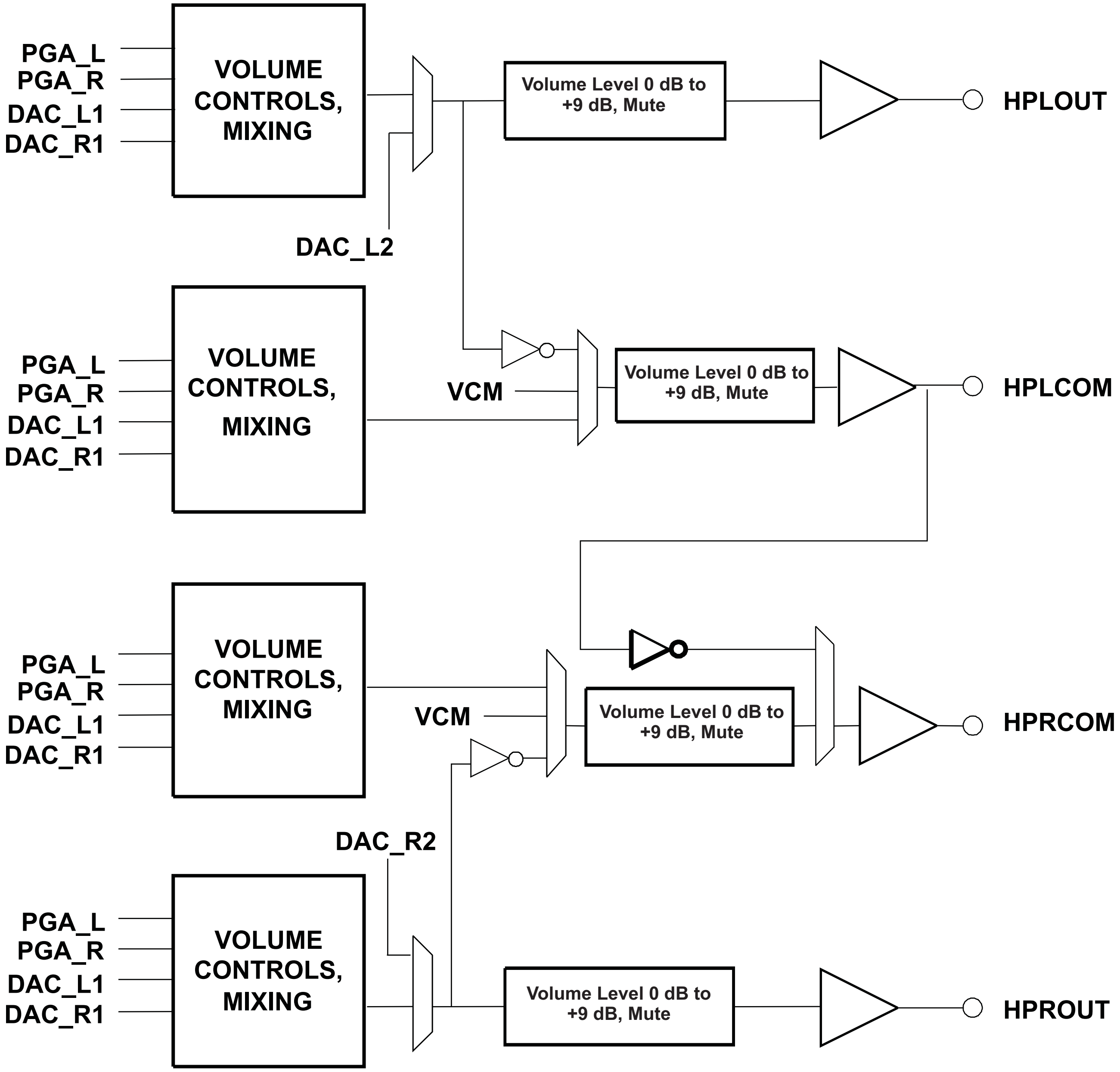

PGA_L
PGA_R
DAC_L1
DAC_R1
VOLUME CONTROLS, MIXING
DAC_L2
Volume Level 0 dB to +9 dB, Mute
HPLOUT
VCM
HPLCOM
HPRCOM
DAC_R2
HPROUT

Figure 31. Architecture of the Output Stage Leading to the High-Power Output Drivers

The high-power output drivers include additional circuitry to avoid artifacts on the audio output during power-on and power-off transient conditions. The user should first program the type of output configuration being used in Page-0/Reg-14, to allow the device to select the optimal power-up scheme to avoid output artifacts. The power-up delay time for the high-power output drivers is also programmable over a wide range of time delays, from instantaneous up to four seconds, using Page-0/Reg-42.

When these output drivers are powered down, they can be placed into a variety of output conditions based on register programming. If lowest power operation is desired, then the outputs can be placed into a 3-state condition, and all power to the output stage is removed. However, this generally results in the output nodes drifting to rest near the upper or lower analog supply, due to small leakage currents at the pins. This then results in a longer delay requirement to avoid output artifacts during driver power-on. In order to reduce this required power-on delay, the TLV320AIC31 includes an option for the output pins of the drivers to be weakly driven to the V_{CM} level they would normally rest at when powered with no signal applied. This output V_{CM} level is determined by an internal bandgap voltage reference, and thus results in extra power dissipation when the drivers are in power-down. However, this option provides the fastest method for transitioning the drivers from power-down to full power operation without any output artifact introduced.

The device includes a further option that falls between the other two: while it requires less power drawn while the output drivers are in power-down, it also takes a slightly longer delay to power-up without artifacts than if the bandgap reference is kept alive. In this alternate mode, the powered-down output driver pin is weakly driven to a voltage of approximately half the DRVDD supply level using an internal voltage divider. This voltage will not match the actual VCM of a fully powered driver, but due to the output voltage being close to its final value, a much shorter power-up delay time setting can be used and still avoid any audible output artifacts. These output voltage options are controlled in Page-0/Reg-42.

The high-power output drivers can also be programmed to power up first with the output level control in a highly-attenuated state, then the output driver will automatically slowly reduce the output attenuation to reach the desired output level setting programmed. This capability is enabled by default but can be enabled in Page-0/Reg-40, D1-D0.

SHORT-CIRCUIT OUTPUT PROTECTION

The TLV320AIC31 includes programmable short-circuit protection for the high-power output drivers, for maximum flexibility in a given application. By default, if these output drivers are shorted, they will automatically limit the maximum amount of current that can be sourced to or sunk from a load, thereby protecting the device from an over-current condition. In this mode, the user can read Page-0/Reg-95 to determine whether the part is in short-circuit protection or not, and then decide whether to program the device to power down the output drivers. However, the device includes further capability to automatically power down an output driver whenever it does into short-circuit protection, without requiring intervention from the user. In this case, the output driver will stay in a power down condition until the user specifically programs it to power down and then power back up again, to clear the short-circuit flag.

CONTROL REGISTERS

The control registers for the TLV320AIC31 are described in detail below. All registers are 8-bit in width, with D7 referring to the most significant bit of each register, and D0 referring to the least significant bit.

Page 0 / Register 0: Page Select Register

BIT[1]	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	X	0000000	Reserved; write only 0s to these register bits
D0	R/W	0	Page Select Bit Writing zero to this bit sets Page-0 as the active page for following register accesses. Writing a one to this bit sets Page-1 as the active page for following register accesses. It is recommended that the user read this register bit back after each write, to ensure that the proper page is being accessed for future register read/writes.

(1) When resetting registers related to routing and volume controls of output drivers, it is recommended to reset them by writing directly to the registers instead of using software reset.

Page 0 / Register 1: Software Reset Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	W	0	Software Reset Bit 0 : Don't Care 1 : Self clearing software reset
D6–D0	W	0000000	Reserved; don't write

Page 0 / Register 2: Codec Sample Rate Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	ADC Sample Rate Select 0000: ADC $F_S = F_{Sref}/1$ 0001: ADC $F_S = F_{Sref}/1.5$ 0010: ADC $F_S = F_{Sref}/2$ 0011: ADC $F_S = F_{Sref}/2.5$ 0100: ADC $F_S = F_{Sref}/3$ 0101: ADC $F_S = F_{Sref}/3.5$ 0110: ADC $F_S = F_{Sref}/4$ 0111: ADC $F_S = F_{Sref}/4.5$ 1000: ADC $F_S = F_{Sref}/5$ 1001: ADC $F_S = F_{Sref}/5.5$ 1010: ADC $F_S = F_{Sref}/ 6$ 1011–1111: Reserved; do not write these sequences. Note: ADC sample rate must be programmed to same value as DAC sample rate
D3-D0	R/W	0000	DAC Sample Rate Select 0000 : DAC $F_S = F_{Sref}/1$ 0001 : DAC $F_S = F_{Sref}/1.5$ 0010 : DAC $F_S = F_{Sref}/2$ 0011 : DAC $F_S = F_{Sref}/2.5$ 0100 : DAC $F_S = F_{Sref}/3$ 0101 : DAC $F_S = F_{Sref}/3.5$ 0110 : DAC $F_S = F_{Sref}/4$ 0111 : DAC $F_S = F_{Sref}/4.5$ 1000 : DAC $F_S = F_{Sref}/5$ 1001: DAC $F_S = F_{Sref}/5.5$ 1010: DAC $F_S = F_{Sref}/ 6$ 1011–1111 : Reserved; do not write these sequences.

Page 0 / Register 3: PLL Programming Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PLL Control Bit 0: PLL is disabled 1: PLL is enabled
D6–D3	R/W	0010	PLL Q Value 0000: Q = 16 0001 : Q = 17 0010 : Q = 2 0011 : Q = 3 0100 : Q = 4 … 1110: Q = 14 1111: Q = 15
D2–D0	R/W	000	PLL P Value 000: P = 8 001: P = 1 010: P = 2 011: P = 3 100: P = 4 101: P = 5 110: P = 6 111: P = 7

Page 0 / Register 4: PLL Programming Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	000001	PLL J Value 000000: Reserved, do not write this sequence 000001: J = 1 000010: J = 2 000011: J = 3 … 111110: J = 62 111111: J = 63
D1–D0	R/W	00	Reserved; write only '0' to these bits

Page 0 / Register 5: PLL Programming Register C(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	PLL D value. Eight most significant bits of a 14-bit unsigned integer valid values for D are from 0 to 9999, represented by a 14-bit integer located in Page-0/Reg-5-6. Values should not be written into these registers that would result in a D value outside the valid range.

(1) Note that whenever the D value is changed, Register 5 should be written, immediately followed by Register 6. Even if only the MSB or LSB of the value changes, both registers should be written.

Page 0 / Register 6: PLL Programming Register D

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	000000	PLL D value. Six least significant bits of a 14-bit unsigned integer valid values for D are from 0 to 9999, represented by a 14-bit integer located in Page-0/Reg-5-6. Values should not be written into these registers that would result in a D value outside the valid range.
D1-D0	R	00	Reserved; write only '0' to these bits.

Page 0 / Register 7: Codec Datapath Setup Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	F_{Sref} setting This register setting controls timers related to the AGC time constants. 0: F_{Sref} = 48 kHz 1: F_{Sref} = 44.1 kHz
D6	R/W	0	ADC Dual rate control 0: ADC dual rate mode is disabled 1: ADC dual rate mode is enabled Note: ADC Dual Rate Mode must match DAC Dual Rate Mode
D5	R/W	0	DAC Dual Rate Control 0: DAC dual rate mode is disabled 1: DAC dual rate mode is enabled
D4–D3	R/W	00	Left DAC Datapath Control 00: Left DAC datapath is off (muted) 01: Left DAC datapath plays left channel input data 10: Left DAC datapath plays right channel input data 11: Left DAC datapath plays mono mix of left and right channel input data
D2–D1	R/W	00	Right DAC Datapath Control 00: Right DAC datapath is off (muted) 01: Right DAC datapath plays right channel input data 10: Right DAC datapath plays left channel input data 11: Right DAC datapath plays mono mix of left and right channel input data
D0	R/W	0	Reserved. Only write '0' to this register.

Page 0 / Register 8: Audio Serial Data Interface Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Bit Clock Directional Control 0: Bit clock is an input (slave mode) 1: Bit clock is an output (master mode)
D6	R/W	0	Word Clock Directional Control 0: Word clock is an input (slave mode) 1: Word clock is an output (master mode)
D5	R/W	0	Serial Output Data Driver (DOUT) 3-state control 0: Do not 3-state DOUT when valid data is not being sent 1: 3-state DOUT when valid data is not being sent
D4	R/W	0	Bit/ Word Clock Drive Control 0: Bit clock and word clock will not be transmitted when in master mode if codec is powered down 1: Bit clock and word clock will continue to be transmitted when in master mode, even if codec is powered down
D3	R/W	0	Reserved. Only write '0' to this register.
D2	R/W	0	3D Effect Control 0: Disable 3-D digital effect processing 1: Enable 3-D digital effect processing
D1-D0	R/W	00	Reserved. Only write '00' to this register

Page 0 / Register 9: Audio Serial Data Interface Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Audio Serial Data Interface Transfer Mode 00: Serial data bus uses I^2S mode 01: Serial data bus uses DSP mode 10: Serial data bus uses right-justified mode 11: Serial data bus uses left-justified mode
D5–D4	R/W	00	Audio Serial Data Word Length Control 00: Audio data word length = 16-bits 01: Audio data word length = 20-bits 10: Audio data word length = 24-bits 11: Audio data word length = 32-bits
D3	R/W	0	Bit Clock Rate Control This register only has effect when bit clock is programmed as an output 0: Continuous-transfer mode used to determine master mode bit clock rate 1: 256-clock transfer mode used, resulting in 256 bit clocks per frame
D2	R/W	0	DAC Re-Sync 0: Don’t Care 1: Re-Sync Stereo DAC with Codec Interface if the group delay changes by more than $\pm DACF_S/4$.
D1	R/W	0	ADC Re-Sync 0: Don’t Care 1: Re-Sync Stereo ADC with Codec Interface if the group delay changes by more than $\pm ADCF_S/4$.
D0	R/W		Re-Sync Mute Behavior 0: Re-Sync is done without soft-muting the channel. (ADC/DAC) 1: Re-Sync is done by internally soft-muting the channel. (ADC/DAC)

Page 0 / Register 10: Audio Serial Data Interface Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	00000000	Audio Serial Data Word Offset Control This register determines where valid data are placed or expected in each frame, by controlling the offset from beginning of the frame where valid data begins. The offset is measured from the rising edge of word clock when in DSP mode. Note: In continuous transfer mode, the maximum offset is 17 for I2S/LJF/RJF modes and 16 for DSP mode. In 256-clock mode, the maximum offset is 241 for DSP modes. 00000000: Data offset = 0 bit clocks 00000001: Data offset = 1 bit clock 00000010: Data offset = 2 bit clocks … 11110001: Data offset = 241 bit clocks. 11110010: Data offset = 242 bit clocks 11110011-11111111: Reserved. Do not write these values to this register.

Page 0 / Register 11: Audio Codec Overflow Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left ADC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to '0' after it is read. 0: No overflow has occurred 1: An overflow has occurred
D6	R	0	Right ADC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to '0' after it is read. 0: No overflow has occurred 1: An overflow has occurred
D5	R	0	Left DAC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to '0' after it is read. 0: No overflow has occurred 1: An overflow has occurred
D4	R	0	Right DAC Overflow Flag This is a sticky bit, so will stay set if an overflow occurs, even if the overflow condition is removed. The register bit reset to '0' after it is read. 0: No overflow has occurred 1: An overflow has occurred
D3–D0	R/W	0001	PLL R Value 0000: R = 16 0001 : R = 1 0010 : R = 2 0011 : R = 3 0100 : R = 4 … 1110: R = 14 1111: R = 15

Page 0 / Register 12: Audio Codec Digital Filter Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left ADC High-pass Filter Control 00: Left ADC High-pass filter disabled 01: Left ADC High-pass filter –3-dB frequency = 0.0045 × ADC F_S 10: Left ADC High-pass filter –3-dB frequency = 0.0125 × ADC F_S 11: Left ADC High-pass filter –3-dB frequency = 0.025 × ADC F_S
D5–D4	R/W	00	Right ADC High-pass Filter Control 00: Right ADC High-pass filter disabled 01: Right ADC High-pass filter –3-dB frequency = 0.0045 × ADC F_S 10: Right ADC High-pass filter –3-dB frequency = 0.0125 × ADC F_S 11: Right ADC High-pass filter –3-dB frequency = 0.025 × ADC F_S
D3	R/W	0	Left DAC Digital Effects Filter Control 0: Left DAC digital effects filter disabled (bypassed) 1: Left DAC digital effects filter enabled
D2	R/W	0	Left DAC De-emphasis Filter Control 0: Left DAC de-emphasis filter disabled (bypassed) 1: Left DAC de-emphasis filter enabled
D1	R/W	0	Right DAC Digital Effects Filter Control 0: Right DAC digital effects filter disabled (bypassed) 1: Right DAC digital effects filter enabled
D0	R/W	0	Right DAC De-emphasis Filter Control 0: Right DAC de-emphasis filter disabled (bypassed) 1: Right DAC de-emphasis filter enabled

Page 0 / Register 13: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	00000000	Reserved. Write only '00000000' to this register.

Page 0 / Register 14: Headset Configuration Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Driver Capacitive Coupling 0: Programs high-power outputs for capless driver configuration 1: Programs high-power outputs for ac-coupled driver configuration
D6(1)	R/W	0	Stereo Output Driver Configuration A Note: do not set bits D6 and D3 both high at the same time. 0: A stereo fully-differential output configuration is not being used 1: A stereo fully-differential output configuration is being used
D5–D4	R	00	Reserved. Write only '00' to these bits.
D3(1)	R/W	0	Stereo Output Driver Configuration B Note: do not set bits D6 and D3 both high at the same time. 0: A stereo pseudo-differential output configuration is not being used 1: A stereo pseudo-differential output configuration is being used
D2–D0	R	000	Reserved. Write only 0s to these bits.

(1) Do not set D6 and D3 to 1 simultaneously

Page 0 / Register 15: Left ADC PGA Gain Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left ADC PGA Mute 0: The left ADC PGA is not muted 1: The left ADC PGA is muted

Page 0 / Register 15: Left ADC PGA Gain Control Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6-D0	R/W	0000000	Left ADC PGA Gain Setting 0000000: Gain = 0.0-dB 0000001: Gain = 0.5-dB 0000010: Gain = 1.0-dB … 1110110: Gain = 59.0-dB 1110111: Gain = 59.5-dB 1111000: Gain = 59.5-dB … 1111111: Gain = 59.5-dB

Page 0 / Register 16: Right ADC PGA Gain Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Right ADC PGA Mute 0: The right ADC PGA is not muted 1: The right ADC PGA is muted
D6-D0	R/W	0000000	Right ADC PGA Gain Setting 0000000: Gain = 0.0-dB 0000001: Gain = 0.5-dB 0000010: Gain = 1.0-dB … 1110110: Gain = 59.0-dB 1110111: Gain = 59.5-dB 1111000: Gain = 59.5-dB … 1111111: Gain = 59.5-dB

Page 0 / Register 17: IN2L/R to Left ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	1111	IN2L Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects IN2L to the left ADC PGA mix 0000: Input level control gain = 0.0-dB 0001: Input level control gain = –1.5-dB 0010: Input level control gain = –3.0-dB 0011: Input level control gain = –4.5-dB 0100: Input level control gain = –6.0-dB 0101: Input level control gain = –7.5-dB 0110: Input level control gain = –9.0-dB 0111: Input level control gain = –10.5-dB 1000: Input level control gain = –12.0-dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: IN2L is not connected to the left ADC PGA
D3-D0	R/W	1111	IN2R Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects IN2R to the left ADC PGA mix 0000: Input level control gain = 0.0-dB 0001: Input level control gain = –1.5-dB 0010: Input level control gain = –3.0-dB 0011: Input level control gain = –4.5-dB 0100: Input level control gain = –6.0-dB 0101: Input level control gain = –7.5-dB 0110: Input level control gain = –9.0-dB 0111: Input level control gain = –10.5-dB 1000: Input level control gain = –12.0-dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: IN2R is not connected to the left ADC PGA

Page 0 / Register 18: IN2L/R to Right ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	1111	IN2L Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects IN2L to the right ADC PGA mix 0000: Input level control gain = 0.0-dB 0001: Input level control gain = –1.5-dB 0010: Input level control gain = –3.0-dB 0011: Input level control gain = –4.5-dB 0100: Input level control gain = –6.0-dB 0101: Input level control gain = –7.5-dB 0110: Input level control gain = –9.0-dB 0111: Input level control gain = –10.5-dB 1000: Input level control gain = –12.0-dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: IN2L is not connected to the right ADC PGA
D3–D0	R/W	1111	IN2R Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects IN2R to the right ADC PGA mix 0000: Input level control gain = 0.0-dB 0001: Input level control gain = –1.5-dB 0010: Input level control gain = –3.0-dB 0011: Input level control gain = –4.5-dB 0100: Input level control gain = –6.0-dB 0101: Input level control gain = –7.5-dB 0110: Input level control gain = –9.0-dB 0111: Input level control gain = –10.5-dB 1000: Input level control gain = –12.0-dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: IN2R is not connected to right ADC PGA

Page 0 / Register 19: IN1L to Left ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	IN1L Single-Ended vs Fully Differential Control If IN1L is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully-differential mode). 0: IN1L is configured in single-ended mode 1: IN1L is configured in fully-differential mode
D6–D3	R/W	1111	IN1L Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects IN1L to the left ADC PGA mix 0000: Input level control gain = 0.0-dB 0001: Input level control gain = –1.5-dB 0010: Input level control gain = –3.0-dB 0011: Input level control gain = –4.5-dB 0100: Input level control gain = –6.0-dB 0101: Input level control gain = –7.5-dB 0110: Input level control gain = –9.0-dB 0111: Input level control gain = –10.5-dB 1000: Input level control gain = –12.0-dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: IN1L is not connected to the left ADC PGA
D2	R/W	0	Left ADC Channel Power Control 0: Left ADC channel is powered down 1: Left ADC channel is powered up
D1–D0	R/W	00	Left ADC PGA Soft-Stepping Control 00: Left ADC PGA soft-stepping at once per F_S 01: Left ADC PGA soft-stepping at once per two F_S 10–11: Left ADC PGA soft-stepping is disabled

Page 0 / Register 20: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111000	Reserved. Do not write to this register.

Page 0 / Register 21: IN1R to Left ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	IN1R Single-Ended vs Fully-Differential Control If IN1R is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully-differential mode). 0: IN1R is configured in single-ended mode 1: IN1R is configured in fully-differential mode
D6–D3	R/W	1111	IN1R Input Level Control for Left ADC PGA Mix Setting the input level control to a gain below automatically connects IN1R to the left ADC PGA mix 0000: Input level control gain = 0.0-dB 0001: Input level control gain = –1.5-dB 0010: Input level control gain = –3.0-dB 0011: Input level control gain = –4.5-dB 0100: Input level control gain = –6.0-dB 0101: Input level control gain = –7.5-dB 0110: Input level control gain = –9.0-dB 0111: Input level control gain = –10.5-dB 1000: Input level control gain = –12.0-dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: IN1R is not connected to the left ADC PGA
D2–D0	R	000	Reserved. Write only 0s to these register bits.

Page 0 / Register 22: IN1R to Right ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	IN1R Single-Ended vs Fully-Differential Control If IN1R is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully-differential mode). 0: IN1R is configured in single-ended mode 1: IN1R is configured in fully-differential mode
D6–D3	R/W	1111	IN1R Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects IN1R to the right ADC PGA mix 0000: Input level control gain = 0.0-dB 0001: Input level control gain = –1.5-dB 0010: Input level control gain = –3.0-dB 0011: Input level control gain = –4.5-dB 0100: Input level control gain = –6.0-dB 0101: Input level control gain = –7.5-dB 0110: Input level control gain = –9.0-dB 0111: Input level control gain = –10.5-dB 1000: Input level control gain = –12.0-dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: IN1R is not connected to the right ADC PGA
D2	R/W	0	Right ADC Channel Power Control 0: Right ADC channel is powered down 1: Right ADC channel is powered up
D1–D0	R/W	00	Right ADC PGA Soft-Stepping Control 00: Right ADC PGA soft-stepping at once per F_S 01: Right ADC PGA soft-stepping at once per two F_S 10-11: Right ADC PGA soft-stepping is disabled

Page 0 / Register 23: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	01111000	Reserved. Do not write to this register.

Page 0 / Register 24: IN1L to Right ADC Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	IN1L Single-Ended vs Fully-Differential Control If IN1L is selected to both left and right ADC channels, both connections must use the same configuration (single-ended or fully-differential mode). 0: IN1L is configured in single-ended mode 1: IN1L is configured in fully-differential mode
D6–D3	R/W	1111	IN1L Input Level Control for Right ADC PGA Mix Setting the input level control to a gain below automatically connects IN1L to the right ADC PGA mix 0000: Input level control gain = 0.0-dB 0001: Input level control gain = –1.5-dB 0010: Input level control gain = –3.0-dB 0011: Input level control gain = –4.5-dB 0100: Input level control gain = –6.0-dB 0101: Input level control gain = –7.5-dB 0110: Input level control gain = –9.0-dB 0111: Input level control gain = –10.5-dB 1000: Input level control gain = –12.0-dB 1001–1110: Reserved. Do not write these sequences to these register bits 1111: IN1L is not connected to the right ADC PGA
D2–D0	R	000	Reserved. Write only 0s to these register bits.

Page 0 / Register 25: MICBIAS Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	MICBIAS Level Control 00: MICBIAS output is powered down 01: MICBIAS output is powered to 2.0 V 10: MICBIAS output is powered to 2.5 V 11: MICBIAS output is connected to AVDD
D5–D3	R	000	Reserved. Write only 0s to these register bits.
D2–D0	R	XXX	Reserved. Write only 0s to these register bits.

Page 0 / Register 26: Left AGC Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left AGC Enable 0: Left AGC is disabled 1: Left AGC is enabled
D6–D4	R/W	000	Left AGC Target Gain 000: Left AGC target gain = –5.5-dB 001: Left AGC target gain = –8-dB 010: Left AGC target gain = –10-dB 011: Left AGC target gain = –12-dB 100: Left AGC target gain = –14-dB 101: Left AGC target gain = –17-dB 110: Left AGC target gain = –20-dB 111: Left AGC target gain = –24-dB
D3–D2	R/W	00	Left AGC Attack Time These time constants(1) will not be accurate when double rate audio mode is enabled. 00: Left AGC attack time = 8-msec 01: Left AGC attack time = 11-msec 10: Left AGC attack time = 16-msec 11: Left AGC attack time = 20-msec
D1–D0	R/W	00	Left AGC Decay Time These time constants(1) will not be accurate when double rate audio mode is enabled. 00: Left AGC decay time = 100-msec 01: Left AGC decay time = 200-msec 10: Left AGC decay time = 400-msec 11: Left AGC decay time = 500-msec

(1) Time constants are valid when DRA is not enabled. The values would change if DRA is enabled.

Page 0 / Register 27: Left AGC Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	R/W	1111111	Left AGC Maximum Gain Allowed 0000000: Maximum gain = 0.0-dB 0000001: Maximum gain = 0.5-dB 0000010: Maximum gain = 1.0-dB … 1110110: Maximum gain = 59.0-dB 1110111–111111: Maximum gain = 59.5-dB
D0	R/W	0	Reserved. Write only '0' to this register bit.

Page 0 / Register 28: Left AGC Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Noise Gate Hysteresis Level Control 00: Hysteresis is disabled 01: Hysteresis = 1-dB 10: Hysteresis = 2-dB 11: Hysteresis = 4-dB
D5–D1	R/W	00000	Left AGC Noise Threshold Control 00000: Left AGC Noise/Silence Detection disabled 00001: Left AGC noise threshold = –30-dB 00010: Left AGC noise threshold = –32-dB 00011: Left AGC noise threshold = –34-dB … 11101: Left AGC noise threshold = –86-dB 11110: Left AGC noise threshold = –88-dB 11111: Left AGC noise threshold = –90-dB
D0	R/W	0	Left AGC Clip Stepping Control 0: Left AGC clip stepping disabled 1: Left AGC clip stepping enabled

Page 0 / Register 29: Right AGC Control Register A

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Right AGC Enable 0: Right AGC is disabled 1: Right AGC is enabled
D6-D4	R/W	000	Right AGC Target Gain 000: Right AGC target gain = –5.5-dB 001: Right AGC target gain = –8-dB 010: Right AGC target gain = –10-dB 011: Right AGC target gain = –12-dB 100: Right AGC target gain = –14-dB 101: Right AGC target gain = –17-dB 110: Right AGC target gain = –20-dB 111: Right AGC target gain = –24-dB
D3–D2	R/W	00	Right AGC Attack Time These time constants will not be accurate when double rate audio mode is enabled. 00: Right AGC attack time = 8-msec 01: Right AGC attack time = 11-msec 10: Right AGC attack time = 16-msec 11: Right AGC attack time = 20-msec
D1–D0	R/W	00	Right AGC Decay Time These time constants will not be accurate when double rate audio mode is enabled. 00: Right AGC decay time = 100-msec 01: Right AGC decay time = 200-msec 10: Right AGC decay time = 400-msec 11: Right AGC decay time = 500-msec

Page 0 / Register 30: Right AGC Control Register B

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R/W	1111111	Right AGC Maximum Gain Allowed 0000000: Maximum gain = 0.0-dB 0000001: Maximum gain = 0.5-dB 0000010: Maximum gain = 1.0-dB … 1110110: Maximum gain = 59.0-dB 1110111–111111: Maximum gain = 59.5-dB
D0	R/W	0	Reserved. Write only '0' to this register bit.

Page 0 / Register 31: Right AGC Control Register C

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Noise Gate Hysteresis Level Control 00: Hysteresis is disabled 01: Hysteresis = 1-dB 10: Hysteresis = 2-dB 11: Hysteresis = 4-dB
D5–D1	R/W	00000	Right AGC Noise Threshold Control 00000: Right AGC Noise/Silence Detection disabled 00001: Right AGC noise threshold = –30-dB 00010: Right AGC noise threshold = –32-dB 00011: Right AGC noise threshold = –34-dB … 11101: Right AGC noise threshold = –86-dB 11110: Right AGC noise threshold = –88-dB 11111: Right AGC noise threshold = –90-dB
D0	R/W	0	Right AGC Clip Stepping Control 0: Right AGC clip stepping disabled 1: Right AGC clip stepping enabled

Page 0 / Register 32: Left AGC Gain Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	00000000	Left Channel Gain Applied by AGC Algorithm 1110 1000: Gain = –12.0-dB 1110 1001: Gain = –11.5-dB 1110 1010: Gain = –11.0-dB … 0000 0000: Gain = 0.0-dB 0000 0001: Gain = +0.5-dB … 0111 0110: Gain = +59.0-dB 0111 0111: Gain = +59.5-dB

Page 0 / Register 33: Right AGC Gain Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	00000000	Right Channel Gain Applied by AGC Algorithm 1110 1000: Gain = –12.0-dB 1110 1001: Gain = –11.5-dB 1110 1010: Gain = –11.0-dB … 0000 0000: Gain = 0.0-dB 0000 0001: Gain = +0.5-dB … 0111 0110: Gain = +59.0-dB 0111 0111: Gain = +59.5-dB

Page 0 / Register 34: Left AGC Noise Gate Debounce Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	00000	Left AGC Noise Detection Debounce Control These times[1] will not be accurate when double rate audio mode is enabled. 00000: Debounce = 0-msec 00001: Debounce = 0.5-msec 00010: Debounce = 1-msec 00011: Debounce = 2-msec 00100: Debounce = 4-msec 00101: Debounce = 8-msec 00110: Debounce = 16-msec 00111: Debounce = 32-msec 01000: Debounce = 64×1 = 64ms 01001: Debounce = 64×2 = 128ms 01010: Debounce = 64×3 = 192ms … 11110: Debounce = 64×23 = 1472ms 11111: Debounce = 64×24 = 1536ms
D2–D0	R/W	000	Left AGC Signal Detection Debounce Control These times[1] will not be accurate when double rate audio mode is enabled. 000: Debounce = 0-msec 001: Debounce = 0.5-msec 010: Debounce = 1-msec 011: Debounce = 2-msec 100: Debounce = 4-msec 101: Debounce = 8-msec 110: Debounce = 16-msec 111: Debounce = 32-msec

(1) Time constants are valid when DRA is not enabled. The values would change when DRA is enabled

Page 0 / Register 35: Right AGC Noise Gate Debounce Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	00000	Right AGC Noise Detection Debounce Control These times[1] will not be accurate when double rate audio mode is enabled. 00000: Debounce = 0-msec 00001: Debounce = 0.5-msec 00010: Debounce = 1-msec 00011: Debounce = 2-msec 00100: Debounce = 4-msec 00101: Debounce = 8-msec 00110: Debounce = 16-msec 00111: Debounce = 32-msec 01000: Debounce = 64×1 = 64ms 01001: Debounce = 64×2 = 128ms 01010: Debounce = 64×3 = 192ms … 11110: Debounce = 64×23 = 1472ms 11111: Debounce = 64×24 = 1536ms
D2–D0	R/W	00000	Right AGC Signal Detection Debounce Control These times[1] will not be accurate when double rate audio mode is enabled. 000: Debounce = 0-msec 001: Debounce = 0.5-msec 010: Debounce = 1-msec 011: Debounce = 2-msec 100: Debounce = 4-msec 101: Debounce = 8-msec 110: Debounce = 16-msec 111: Debounce = 32-msec

(1) Time constants are valid when DRA is not enabled. The values would change when DRA is enabled.

Page 0 / Register 36: ADC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left ADC PGA Status 0: Applied gain and programmed gain are not the same 1: Applied gain = programmed gain
D6	R	0	Left ADC Power Status 0: Left ADC is in a power down state 1: Left ADC is in a power up state
D5	R	0	Left AGC Signal Detection Status 0: Signal power is greater than noise threshold 1: Signal power is less than noise threshold
D4	R	0	Left AGC Saturation Flag 0: Left AGC is not saturated 1: Left AGC gain applied = maximum allowed gain for left AGC
D3	R	0	Right ADC PGA Status 0: Applied gain and programmed gain are not the same 1: Applied gain = programmed gain
D2	R	0	Right ADC Power Status 0: Right ADC is in a power down state 1: Right ADC is in a power up state
D1	R	0	Right AGC Signal Detection Status 0: Signal power is greater than noise threshold 1: Signal power is less than noise threshold
D0	R	0	Right AGC Saturation Flag 0: Right AGC is not saturated 1: Right AGC gain applied = maximum allowed gain for right AGC

Page 0 / Register 37: DAC Power and Output Driver Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Left DAC Power Control 0: Left DAC not powered up 1: Left DAC is powered up
D6	R/W	0	Right DAC Power Control 0: Right DAC not powered up 1: Right DAC is powered up
D5–D4	R/W	00	HPLCOM Output Driver Configuration Control 00: HPLCOM configured as differential of HPLOUT 01: HPLCOM configured as constant VCM output 10: HPLCOM configured as independent single-ended output 11: Reserved. Do not write this sequence to these register bits.
D3–D0	R	000	Reserved. Write only 0s to these register bits.

Page 0 / Register 38: High-Power Output Driver Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R	00	Reserved. Write only 0s to these register bits.
D5-D3	R/W	000	HPRCOM Output Driver Configuration Control 000: HPRCOM configured as differential of HPROUT 001: HPRCOM configured as constant VCM output 010: HPRCOM configured as independent single-ended output 011: HPRCOM configured as differential of HPLCOM 100: HPRCOM configured as external feedback with HPLCOM as constant VCM output 101–111: Reserved. Do not write these sequences to these register bits.
D2	R/W	0	Short Circuit Protection Control 0: Short-circuit protection on all high-power output drivers is disabled 1: Short-circuit protection on all high-power output drivers is enabled
D1	R/W	0	Short Circuit Protection Mode Control 0: If short-circuit protection enabled, it will limit the maximum current to the load 1: If short-circuit protection enabled, it will power down the output driver automatically when a short is detected
D0	R	0	Reserved. Write only '0' to this register bit.

Page 0 / Register 39: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	00000000	Reserved. Do not write to this register.

Page 0 / Register 40: High-Power Output Stage Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Output Common-Mode Voltage Control 00: Output common-mode voltage = 1.35 V 01: Output common-mode voltage = 1.5 V 10: Output common-mode voltage = 1.65 V 11: Output common-mode voltage = 1.8 V
D5–D2	R/W	0000	Reserved. Write only 0000 to these bits.
D1–D0	R/W	00	Output Volume Control Soft-Stepping 00: Output soft-stepping = one step per F_S 01: Output soft-stepping = one step per two F_S 10: Output soft-stepping disabled 11: Reserved. Do not write this sequence to these register bits.

Page 0 / Register 41: DAC Output Switching Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Left DAC Output Switching Control 00: Left DAC output selects DAC_L1 path 01: Left DAC output selects DAC_L3 path to left line output driver 10: Left DAC output selects DAC_L2 path to left high-power output drivers (1) 11: Reserved. Do not write this sequence to these register bits.
D5–D4	R/W	00	Right DAC Output Switching Control 00: Right DAC output selects DAC_R1 path 01: Right DAC output selects DAC_R3 path to right line output driver 10: Right DAC output selects DAC_R2 path to right high-power output drivers (1) 11: Reserved. Do not write this sequence to these register bits.
D3–D2	R/W	00	Reserved. Write only '0's to these bits.
D1–D0	R/W	00	DAC Digital Volume Control Functionality 00: Left and right DAC channels have independent volume controls 01: Left DAC volume follows the right channel control register 10: Right DAC volume follows the left channel control register 11: Left and right DAC channels have independent volume controls (same as 00)

(1) When using the DAC direct paths (DAC_L2 and DAC_R2), the signal will be gained up by a factor of –1 dB.

Page 0 / Register 42: Output Driver Pop Reduction Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	Output Driver Power-On Delay Control 0000: Driver power-on time = 0-µsec 0001: Driver power-on time = 10-µsec 0010: Driver power-on time = 100-µsec 0011: Driver power-on time = 1-msec 0100: Driver power-on time = 10-msec 0101: Driver power-on time = 50-msec 0110: Driver power-on time = 100-msec 0111: Driver power-on time = 200-msec 1000: Driver power-on time = 400-msec 1001: Driver power-on time = 800-msec 1010: Driver power-on time = 2-sec 1011: Driver power-on time = 4-sec 1100–1111: Reserved. Do not write these sequences to these register bits.
D3-D2	R/W	00	Driver Ramp-up Step Timing Control 00: Driver ramp-up step time = 0-msec 01: Driver ramp-up step time = 1-msec 10: Driver ramp-up step time = 2-msec 11: Driver ramp-up step time = 4-msec
D1	R/W	0	Weak Output Common-mode Voltage Control 0: Weakly driven output common-mode voltage is generated from bandgap reference 1: Weakly driven output common-mode voltage is generated from resistor divider off the AVDD supply
D0	R/W	0	Reserved. Write only '0' to this register bit.

Page 0 / Register 43: Left DAC Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Left DAC Digital Mute 0: The left DAC channel is not muted 1: The left DAC channel is muted
D6–D0	R/W	0000000	Left DAC Digital Volume Control Setting 0000000: Gain = 0.0-dB 0000001: Gain = –0.5-dB 0000010: Gain = –1.0-dB … 1111101: Gain = –62.5-dB 1111110: Gain = –63.0-dB 1111111: Gain = –63.5-dB

Page 0 / Register 44: Right DAC Digital Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	Right DAC Digital Mute 0: The right DAC channel is not muted 1: The right DAC channel is muted
D6–D0	R/W	0000000	Right DAC Digital Volume Control Setting 0000000: Gain = 0.0-dB 0000001: Gain = –0.5-dB 0000010: Gain = –1.0-dB … 1111101: Gain = –62.5-dB 1111110: Gain = –63.0-dB 1111111: Gain = –63.5-dB

Output Stage Volume Controls

A basic analog volume control with range from 0 dB to –78 dB and mute is replicated multiple times in the output stage network, connected to each of the analog signals that route to the output stage. In addition, to enable completely independent mixing operations to be performed for each output driver, each analog signal coming into the output stage may have up to seven separate volume controls. These volume controls all have approximately 0.5-dB step programmability over most of the gain range, with steps increasing slightly at the lowest attenuations. Table 5 lists the detailed gain versus programmed setting for this basic volume control.

Table 5. Output Stage Volume Control Settings and Gains

Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)	Gain Setting	Analog Gain (dB)
0 0.0		30	-15.0	60	-30.1	90	-45.2
1	-0.5	31	-15.5	61	-30.6	91	-45.8
2	-1.0	32	-16.0	62	-31.1	92	-46.2
3	-1.5	33	-16.5	63	-31.6	93	-46.7
4	-2.0	34	-17.0	64	-32.1	94	-47.4
5	-2.5	35	-17.5	65	-32.6	95	-47.9
6	-3.0	36	-18.0	66	-33.1	96	-48.2
7	-3.5	37	-18.6	67	-33.6	97	-48.7
8	-4.0	38	-19.1	68	-34.1	98	-49.3
9	-4.5	39	-19.6	69	-34.6	99	-50.0
10	-5.0	40	-20.1	70	-35.1	100	-50.3
11	-5.5	41	-20.6	71	-35.7	101	-51.0
12	-6.0	42	-21.1	72	-36.1	102	-51.4
13	-6.5	43	-21.6	73	-36.7	103	-51.8
14	-7.0	44	-22.1	74	-37.1	104	-52.2
15	-7.5	45	-22.6	75	-37.7	105	-52.7
16	-8.0	46	-23.1	76	-38.2	106	-53.7
17	-8.5	47	-23.6	77	-38.7	107	-54.2
18	-9.0	48	-24.1	78	-39.2	108	-55.3
19	-9.5	49	-24.6	79	-39.7	109	-56.7
20	-10.0	50	-25.1	80	-40.2	110	-58.3
21	-10.5	51	-25.6	81	-40.7	111	-60.2
22	-11.0	52	-26.1	82	-41.2	112	-62.7
23	-11.5	53	-26.6	83	-41.7	113	-64.3
24	-12.0	54	-27.1	84	-42.2	114	-66.2
25	-12.5	55	-27.6	85	-42.7	115	-68.7
26	-13.0	56	-28.1	86	-43.2	116	-72.2
27	-13.5	57	-28.6	87	-43.8	117	-78.3
28	-14.0	58	-29.1	88	-44.3	118–127	Mute
29	-14.5	59	-29.6	89	-44.8		

Page 0 / Register 45: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 46: PGA_L to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPLOUT 1: PGA_L is routed to HPLOUT
D6-D0	R/W	0000000	PGA_L to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 47: DAC_L1 to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPLOUT 1: DAC_L1 is routed to HPLOUT
D6-D0	R/W	0000000	DAC_L1 to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5

Page 0 / Register 48: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	00000000	Reserved. Do not write to this register.

Page 0 / Register 49: PGA_R to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPLOUT 1: PGA_R is routed to HPLOUT
D6-D0	R/W	0000000	PGA_R to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 50: DAC_R1 to HPLOUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPLOUT 1: DAC_R1 is routed to HPLOUT
D6-D0	R/W	0000000	DAC_R1 to HPLOUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 51: HPLOUT Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	HPLOUT Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPLOUT Mute 0: HPLOUT is muted 1: HPLOUT is not muted
D2	R/W	1	HPLOUT Power Down Drive Control 0: HPLOUT is weakly driven to a common-mode when powered down 1: HPLOUT is 3-stated with powered down
D1	R	1	HPLOUT Volume Control Status 0: Not all programmed gains to HPLOUT have been applied yet 1: All programmed gains to HPLOUT have been applied
D0	R/W	0	HPLOUT Power Control 0: HPLOUT is not fully powered up 1: HPLOUT is fully powered up

Page 0 / Register 52: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '00000000' to this register.

Page 0 / Register 53: PGA_L to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPLCOM 1: PGA_L is routed to HPLCOM
D6-D0	R/W	0000000	PGA_L to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 54: DAC_L1 to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPLCOM 1: DAC_L1 is routed to HPLCOM
D6-D0	R/W	0000000	DAC_L1 to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 55: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '0000000' to this register.

Page 0 / Register 56: PGA_R to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPLCOM 1: PGA_R is routed to HPLCOM
D6-D0	R/W	0000000	PGA_R to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 57: DAC_R1 to HPLCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPLCOM 1: DAC_R1 is routed to HPLCOM
D6-D0	R/W	0000000	DAC_R1 to HPLCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 58: HPLCOM Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	HPLCOM Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPLCOM Mute 0: HPLCOM is muted 1: HPLCOM is not muted
D2	R/W	1	HPLCOM Power Down Drive Control 0: HPLCOM is weakly driven to a common-mode when powered down 1: HPLCOM is 3-stated when powered down
D1	R	1	HPLCOM Volume Control Status 0: Not all programmed gains to HPLCOM have been applied yet 1: All programmed gains to HPLCOM have been applied
D0	R/W	0	HPLCOM Power Control 0: HPLCOM is not fully powered up 1: HPLCOM is fully powered up

Page 0 / Register 59: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '0000000' to this register.

Page 0 / Register 60: PGA_L to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPROUT 1: PGA_L is routed to HPROUT
D6-D0	R/W	0000000	PGA_L to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 61: DAC_L1 to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPROUT 1: DAC_L1 is routed to HPROUT
D6-D0	R/W	0000000	DAC_L1 to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 62: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '0000000' to this register.

Page 0 / Register 63: PGA_R to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPROUT 1: PGA_R is routed to HPROUT
D6-D0	R/W	0000000	PGA_R to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 64: DAC_R1 to HPROUT Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPROUT 1: DAC_R1 is routed to HPROUT
D6-D0	R/W	0000000	DAC_R1 to HPROUT Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 65: HPROUT Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	HPROUT Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPROUT Mute 0: HPROUT is muted 1: HPROUT is not muted
D2	R/W	1	HPROUT Power Down Drive Control 0: HPROUT is weakly driven to a common-mode when powered down 1: HPROUT is 3-stated when powered down
D1	R	1	HPROUT Volume Control Status 0: Not all programmed gains to HPROUT have been applied yet 1: All programmed gains to HPROUT have been applied
D0	R/W	0	HPROUT Power Control 0: HPROUT is not fully powered up 1: HPROUT is fully powered up

Page 0 / Register 66: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '0000000' to this register.

Page 0 / Register 67: PGA_L to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to HPRCOM 1: PGA_L is routed to HPRCOM
D6-D0	R/W	0000000	PGA_L to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 68: DAC_L1 to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to HPRCOM 1: DAC_L1 is routed to HPRCOM
D6-D0	R/W	0000000	DAC_L1 to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 69: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '0000000' to this register.

Page 0 / Register 70: PGA_R to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to HPRCOM 1: PGA_R is routed to HPRCOM
D6-D0	R/W	0000000	PGA_R to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 71: DAC_R1 to HPRCOM Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to HPRCOM 1: DAC_R1 is routed to HPRCOM
D6-D0	R/W	0000000	DAC_R1 to HPRCOM Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 72: HPRCOM Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	HPRCOM Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	HPRCOM Mute 0: HPRCOM is muted 1: HPRCOM is not muted
D2	R/W	1	HPRCOM Power Down Drive Control 0: HPRCOM is weakly driven to a common-mode when powered down 1: HPRCOM is 3-stated with powered down
D1	R	1	HPRCOM Volume Control Status 0: Not all programmed gains to HPRCOM have been applied yet 1: All programmed gains to HPRCOM have been applied
D0	R/W	0	HPRCOM Power Control 0: HPRCOM is not fully powered up 1: HPRCOM is fully powered up

Table 8.2. Page 0 / Register 73–78: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Write only '00000000' to these registers.

Page 0 / Register 79: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000010	Reserved. Write only '0000010' to this register.

Page 0 / Register 80: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '0000000' to this register.

Page 0 / Register 81: PGA_L to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to LEFT_LOP/M 1: PGA_L is routed to LEFT_LOP/M
D6-D0	R/W	0000000	PGA_L to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 82: DAC_L1 to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to LEFT_LOP/M 1: DAC_L1 is routed to LEFT_LOP/M
D6-D0	R/W	0000000	DAC_L1 to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 83: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '0000000' to this register.

Page 0 / Register 84: PGA_R to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to LEFT_LOP/M 1: PGA_R is routed to LEFT_LOP/M
D6-D0	R/W	0000000	PGA_R to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 85: DAC_R1 to LEFT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to LEFT_LOP/M 1: DAC_R1 is routed to LEFT_LOP/M
D6-D0	R/W	0000000	DAC_R1 to LEFT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 86: LEFT_LOP/M Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	LEFT_LOP/M Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	LEFT_LOP/M Mute 0: LEFT_LOP/M is muted 1: LEFT_LOP/M is not muted
D2	R/W	0	Reserved. Write only '0' to this register bit.
D1	R	1	LEFT_LOP/M Volume Control Status 0: Not all programmed gains to LEFT_LOP/M have been applied yet 1: All programmed gains to LEFT_LOP/M have been applied
D0	R/W	0	LEFT_LOP/M Power Control 0: LEFT_LOP/M is not fully powered up 1: LEFT_LOP/M is fully powered up

Page 0 / Register 87: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0	Reserved. Write only '0000000' to this register.

Page 0 / Register 88: PGA_L to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_L Output Routing Control 0: PGA_L is not routed to RIGHT_LOP/M 1: PGA_L is routed to RIGHT_LOP/M
D6-D0	R/W	0000000	PGA_L to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 89: DAC_L1 to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_L1 Output Routing Control 0: DAC_L1 is not routed to RIGHT_LOP/M 1: DAC_L1 is routed to RIGHT_LOP/M
D6-D0	R/W	0000000	DAC_L1 to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 90: Reserved Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000000	Reserved. Write only '00000000' to this register.

Page 0 / Register 91: PGA_R to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	PGA_R Output Routing Control 0: PGA_R is not routed to RIGHT_LOP/M 1: PGA_R is routed to RIGHT_LOP/M
D6-D0	R/W	0000000	PGA_R to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 92: DAC_R1 to RIGHT_LOP/M Volume Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	DAC_R1 Output Routing Control 0: DAC_R1 is not routed to RIGHT_LOP/M 1: DAC_R1 is routed to RIGHT_LOP/M
D6-D0	R/W	0000000	DAC_R1 to RIGHT_LOP/M Analog Volume Control For 7-bit register setting versus analog gain values, see Table 5.

Page 0 / Register 93: RIGHT_LOP/M Output Level Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D4	R/W	0000	RIGHT_LOP/M Output Level Control 0000: Output level control = 0-dB 0001: Output level control = 1-dB 0010: Output level control = 2-dB ... 1000: Output level control = 8-dB 1001: Output level control = 9-dB 1010–1111: Reserved. Do not write these sequences to these register bits.
D3	R/W	0	RIGHT_LOP/M Mute 0: RIGHT_LOP/M is muted 1: RIGHT_LOP/M is not muted
D2	R/W	0	Reserved. Write only '0' to this register bit.
D1	R	1	RIGHT_LOP/M Volume Control Status 0: Not all programmed gains to RIGHT_LOP/M have been applied yet 1: All programmed gains to RIGHT_LOP/M have been applied
D0	R/W	0	RIGHT_LOP/M Power Control 0: RIGHT_LOP/M is not fully powered up 1: RIGHT_LOP/M is fully powered up

Page 0 / Register 94: Module Power Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	Left DAC Power Status 0: Left DAC not fully powered up 1: Left DAC fully powered up
D6	R	0	Right DAC Power Status 0: Right DAC not fully powered up 1: Right DAC fully powered up
D5	R	0	Reserved. Write only '0' to this bit.
D4	R	0	LEFT_LOP/M Power Status 0: LEFT_LOP/M output driver powered down 1: LEFT_LOP/M output driver powered up
D3	R	0	RIGHT_LOP/M Power Status 0: RIGHT_LOP/M is not fully powered up 1: RIGHT_LOP/M is fully powered up
D2	R	0	HPLOUT Driver Power Status 0: HPLOUT Driver is not fully powered up 1: HPLOUT Driver is fully powered up
D1	R/W	0	HPROUT Driver Power Status 0: HPROUT Driver is not fully powered up 1: HPROUT Driver is fully powered up
D0	R	0	Reserved. Do not write to this register bit.

Page 0 / Register 95: Output Driver Short Circuit Detection Status Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short-circuit detected at HPLOUT 1: Short-circuit detected at HPLOUT
D6	R	0	HPROUT Short Circuit Detection Status 0: No short-circuit detected at HPROUT 1: Short-circuit detected at HPROUT
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short-circuit detected at HPLCOM 1: Short-circuit detected at HPLCOM
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short-circuit detected at HPRCOM 1: Short-circuit detected at HPRCOM
D3	R	0	HPLCOM Power Status 0: HPLCOM is not fully powered up 1: HPLCOM is fully powered up
D2	R	0	HPRCOM Power Status 0: HPRCOM is not fully powered up 1: HPRCOM is fully powered up
D1-D0	R	00	Reserved. Do not write to these register bits.

Page 0 / Register 96: Sticky Interrupt Flags Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short-circuit detected at HPLOUT driver 1: Short-circuit detected at HPLOUT driver
D6	R	0	HPROUT Short Circuit Detection Status 0: No short-circuit detected at HPROUT driver 1: Short-circuit detected at HPROUT driver
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short-circuit detected at HPLCOM driver 1: Short-circuit detected at HPLCOM driver
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short-circuit detected at HPRCOM driver 1: Short-circuit detected at HPRCOM driver
D3-D2	R	00	Reserved. Write only '00' to these bits.
D1	R	0	Left ADC AGC Noise Gate Status 0: Left ADC Signal Power Greater than Noise Threshold for Left AGC 1: Left ADC Signal Power Lower than Noise Threshold for Left AGC
D0	R	0	Right ADC AGC Noise Gate Status 0: Right ADC Signal Power Greater than Noise Threshold for Right AGC 1: Right ADC Signal Power Lower than Noise Threshold for Right AGC

Page 0 / Register 97: Real-time Interrupt Flags Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	HPLOUT Short Circuit Detection Status 0: No short-circuit detected at HPLOUT driver 1: Short-circuit detected at HPLOUT driver
D6	R	0	HPROUT Short Circuit Detection Status 0: No short-circuit detected at HPROUT driver 1: Short-circuit detected at HPROUT driver
D5	R	0	HPLCOM Short Circuit Detection Status 0: No short-circuit detected at HPLCOM driver 1: Short=circuit detected at HPLCOM driver
D4	R	0	HPRCOM Short Circuit Detection Status 0: No short-circuit detected at HPRCOM driver 1: Short-circuit detected at HPRCOM driver
D3-D2	R	00	Reserved. Write only '00' to these bits.
D1	R	0	Left ADC AGC Noise Gate Status 0: Left ADC Signal Power Greater than Noise Threshold for Left AGC 1: Left ADC Signal Power Lower than Noise Threshold for Left AGC
D0	R	0	Right ADC AGC Noise Gate Status 0: Right ADC Signal Power Greater than Noise Threshold for Right AGC 1: Right ADC Signal Power Lower than Noise Threshold for Right AGC

Page 0 / Register 98–100: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	00000000	Reserved. Write only '00000000' to these bits.

Page 0 / Register 101: Additional Clock Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	R/W	0000000	Reserved. Write only '0000000' to these bits.
D0	R/W	0	CODEC_CLKIN Source Selection 0: CODEC_CLKIN uses PLLDIV_OUT 1: CODEC_CLKIN uses CLKDIV_OUT

Page 0 / Register 102: Clock Generation Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D6	R/W	00	CLKDIV_IN Source Selection 00: CLKDIV_IN uses MCLK 01: Reserved. Do not use. 10: CLKDIV_IN uses BCLK 11: Reserved. Do not use.
D5-D4	R/W	00	PLLCLK_IN Source Selection 00: PLLCLK_IN uses MCLK 01: Reserved. Do not use. 10: PLLCLK _IN uses BCLK 11: Reserved. Do not use.
D3-D0	R/W	0010	Reserved. Write only '0010' to these bits.

Page 0 / Register 103–127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	00000000	Reserved. Do not write to these registers.

Page 1 / Register 0: Page Select Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D1	X	0000000	Reserved; write only 0s to these register bits.
D0	R/W	0	Page Select Bit Writing '0' to this bit sets Page-0 as the active page for following register accesses. Writing a '1' to this bit sets Page-1 as the active page for following register accesses. It is recommended that the user read this register bit back after each write, to ensure that the proper page is being accessed for future register read/writes. This register has the same functionality on page-0 and page-1.

Page 1 / Register 1: Left Channel Audio Effects Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x6B	Left Channel Audio Effects Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 2: Left Channel Audio Effects Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xE3	Left Channel Audio Effects Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 3: Left Channel Audio Effects Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x96	Left Channel Audio Effects Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 4: Left Channel Audio Effects Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x66	Left Channel Audio Effects Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 5: Left Channel Audio Effects Filter N2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x67	Left Channel Audio Effects Filter N2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 6: Left Channel Audio Effects Filter N2 Coefficient LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x5D	Left Channel Audio Effects Filter N2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 7: Left Channel Audio Effects Filter N3 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x6B	Left Channel Audio Effects Filter N3 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 8: Left Channel Audio Effects Filter N3 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xE3	Left Channel Audio Effects Filter N3 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 9: Left Channel Audio Effects Filter N4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x96	Left Channel Audio Effects Filter N4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 10: Left Channel Audio Effects Filter N4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x66	Left Channel Audio Effects Filter N4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 11: Left Channel Audio Effects Filter N5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x67	Left Channel Audio Effects Filter N5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 12: Left Channel Audio Effects Filter N5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x5D	Left Channel Audio Effects Filter N5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from -32768 to +32767.

Page 1 / Register 13: Left Channel Audio Effects Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x7D	Left Channel Audio Effects Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 14: Left Channel Audio Effects Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x83	Left Channel Audio Effects Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 15: Left Channel Audio Effects Filter D2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x84	Left Channel Audio Effects Filter D2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 16: Left Channel Audio Effects Filter D2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xEE	Left Channel Audio Effects Filter D2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 17: Left Channel Audio Effects Filter D4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x7D	Left Channel Audio Effects Filter D4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 18: Left Channel Audio Effects Filter D4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x83	Left Channel Audio Effects Filter D4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 19: Left Channel Audio Effects Filter D5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x84	Left Channel Audio Effects Filter D5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 20: Left Channel Audio Effects Filter D5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xEE	Left Channel Audio Effects Filter D5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 21: Left Channel De-emphasis Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x39	Left Channel De-emphasis Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 22: Left Channel De-emphasis Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x55	Left Channel De-emphasis Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 23: Left Channel De-emphasis Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xF3	Left Channel De-emphasis Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 24: Left Channel De-emphasis Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x2D	Left Channel De-emphasis Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 25: Left Channel De-emphasis Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x53	Left Channel De-emphasis Filter A0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 26: Left Channel De-emphasis Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x7E	Left Channel De-emphasis Filter A0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 27: Right Channel Audio Effects Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x6B	Right Channel Audio Effects Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 28: Right Channel Audio Effects Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xE3	Right Channel Audio Effects Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 29: Right Channel Audio Effects Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x96	Right Channel Audio Effects Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 30: Right Channel Audio Effects Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x66	Right Channel Audio Effects Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 31: Right Channel Audio Effects Filter N2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x67	Right Channel Audio Effects Filter N2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 32: Right Channel Audio Effects Filter N2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x5D	Right Channel Audio Effects Filter N2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 33: Right Channel Audio Effects Filter N3 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x6B	Right Channel Audio Effects Filter N3 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 34: Right Channel Audio Effects Filter N3 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xE3	Right Channel Audio Effects Filter N3 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 35: Right Channel Audio Effects Filter N4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x96	Right Channel Audio Effects Filter N4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 36: Right Channel Audio Effects Filter N4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x66	Right Channel Audio Effects Filter N4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 37: Right Channel Audio Effects Filter N5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x67	Right Channel Audio Effects Filter N5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 38: Right Channel Audio Effects Filter N5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x5D	Right Channel Audio Effects Filter N5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 39: Right Channel Audio Effects Filter D1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x7D	Right Channel Audio Effects Filter D1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 40: Right Channel Audio Effects Filter D1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x83	Right Channel Audio Effects Filter D1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a twos complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 41: Right Channel Audio Effects Filter D2 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x84	Right Channel Audio Effects Filter D2 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two’s complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 42: Right Channel Audio Effects Filter D2 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xEE	Right Channel Audio Effects Filter D2 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two’s complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 43: Right Channel Audio Effects Filter D4 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x7D	Right Channel Audio Effects Filter D4 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two’s complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 44: Right Channel Audio Effects Filter D4 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x83	Right Channel Audio Effects Filter D4 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two’s complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 45: Right Channel Audio Effects Filter D5 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x67	Right Channel Audio Effects Filter D5 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two’s complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 46: Right Channel Audio Effects Filter D5 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x5D	Right Channel Audio Effects Filter D5 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two’s complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 47: Right Channel De-emphasis Filter N0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x39	Right Channel De-emphasis Filter N0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 48: Right Channel De-emphasis Filter N0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x55	Right Channel De-emphasis Filter N0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 49: Right Channel De-emphasis Filter N1 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xF3	Right Channel De-emphasis Filter N1 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 50: Right Channel De-emphasis Filter N1 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x2D	Right Channel De-emphasis Filter N1 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 51: Right Channel De-emphasis Filter A0 Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x53	Right Channel De-emphasis Filter A0 Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 52: Right Channel De-emphasis Filter A0 Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x7E	Right Channel De-emphasis Filter A0 Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 53: 3-D Attenuation Coefficient MSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0x7F	3-D Attenuation Coefficient MSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 54: 3-D Attenuation Coefficient LSB Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0xFF	3-D Attenuation Coefficient LSB The 16-bit integer contained in the MSB and LSB registers for this coefficient are interpreted as a two's complement integer, with possible values ranging from –32768 to +32767.

Page 1 / Register 55–127: Reserved Registers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R	00000000	Reserved. Do not write to these registers.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2006) to Revision B	Page
• Corrected device pinout drawing.	3
• Added missing specifications for QFN package thermal impedance.	4

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/Ball Finish	MSL Peak Temp [(3)]
TLV320AIC31IRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV320AIC31IRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV320AIC31IRHBT	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TLV320AIC31IRHBTG4	ACTIVE	QFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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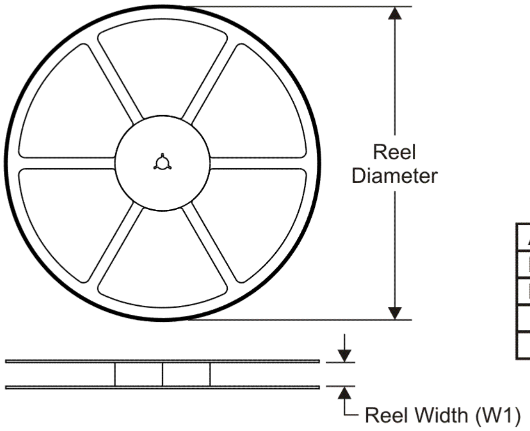
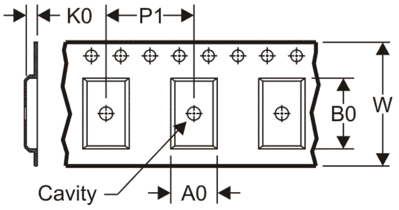
TAPE AND REEL INFORMATION

REEL DIMENSIONS

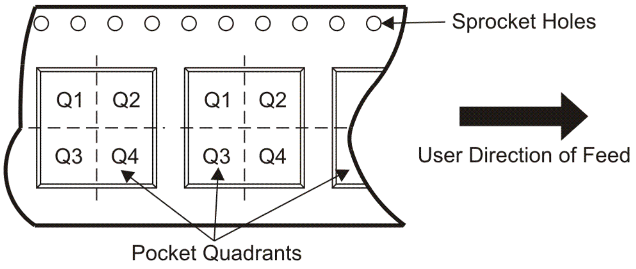

Reel Diameter
Reel Width (W1)

TAPE DIMENSIONS


K0
P1
B0
W
Cavity
A0

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

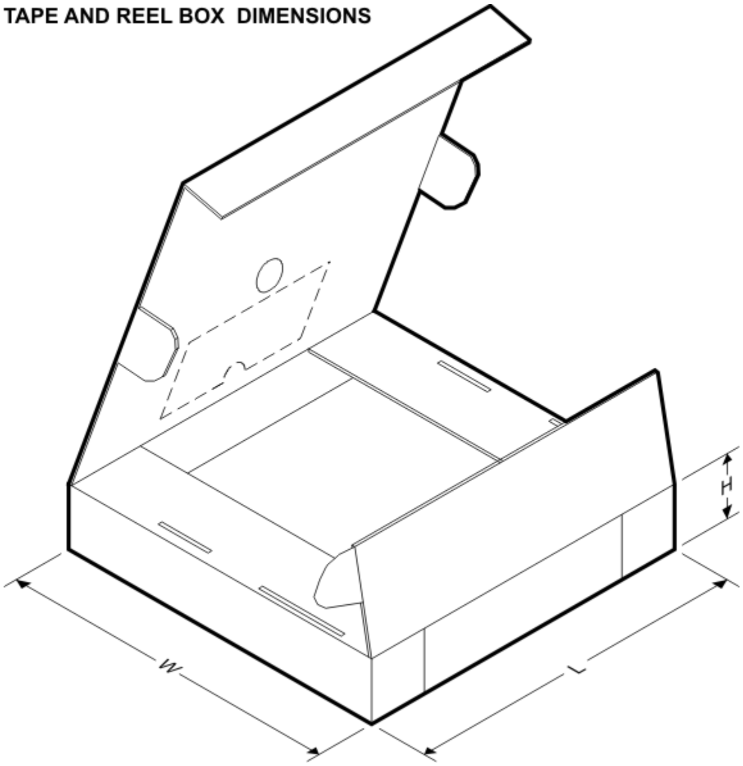
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Sprocket Holes
Q1
Q2
Q3
Q4
Q1
Q2
Q3
Q4
User Direction of Feed
Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC31IRHBR	QFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLV320AIC31IRHBT	QFN	RHB	32	250	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

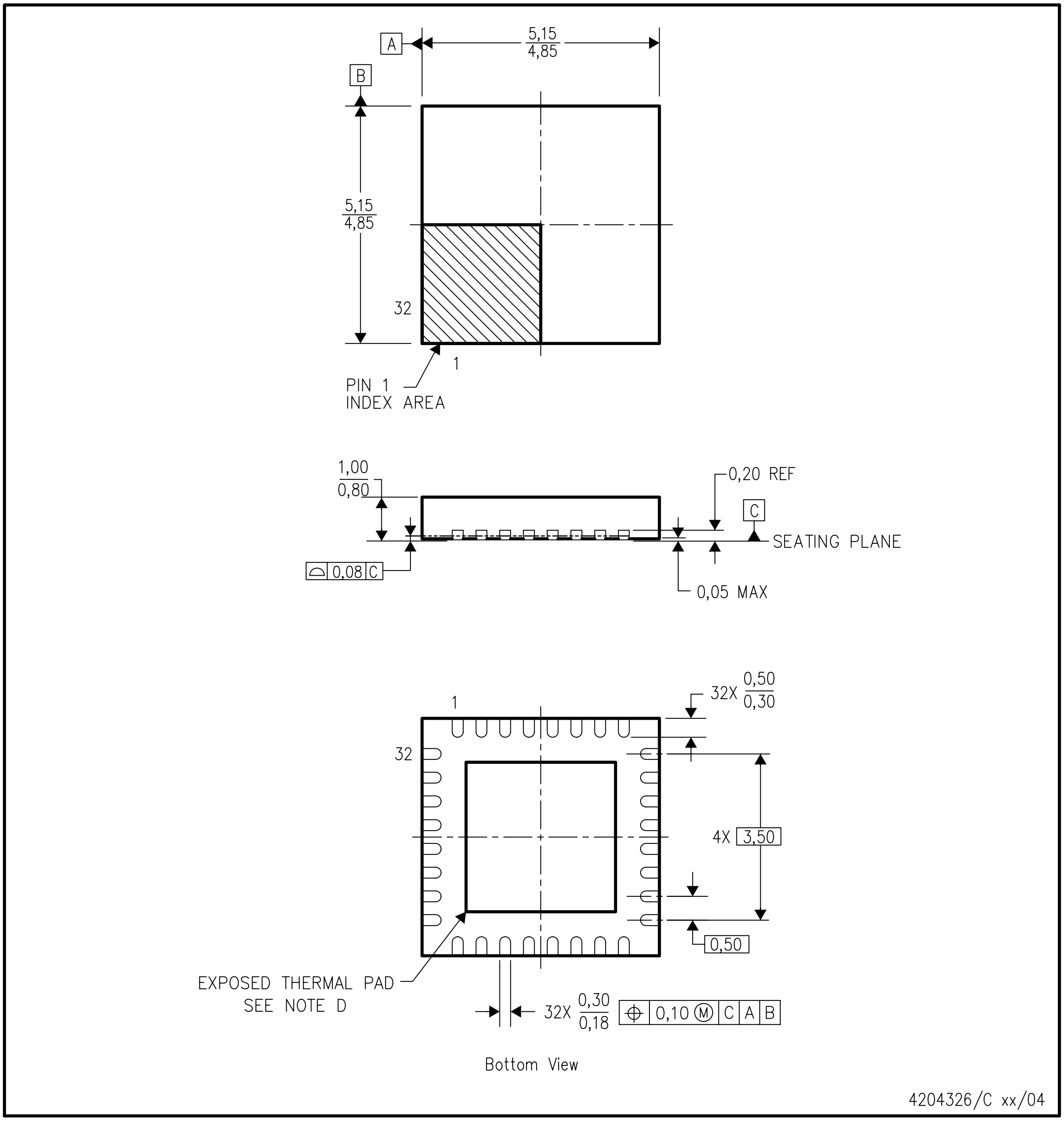
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC31IRHBR	QFN	RHB	32	3000	340.5	333.0	20.6
TLV320AIC31IRHBT	QFN	RHB	32	250	340.5	333.0	20.6

RHB (S–PQFP–N32) PLASTIC QUAD FLATPACK


A
5,15
4,85
B
5,15
4,85
32
1
PIN 1
INDEX AREA
1,00
0,80
0,20 REF
C
SEATING PLANE
0,08 C
0,05 MAX
1
32
32X 0,50
0,30
4X 3,50
0,50
EXPOSED THERMAL PAD
SEE NOTE D
32X 0,30
0,18
0,10 Ⓜ C A B
Bottom View
4204326/C xx/04

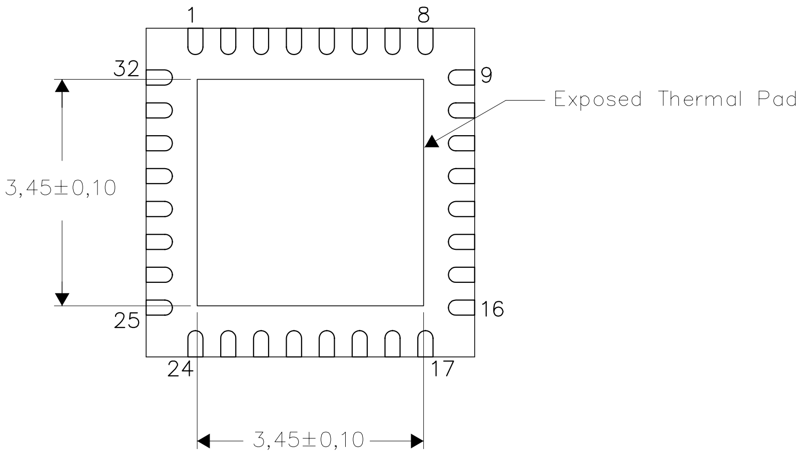
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) Package configuration.
- D The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
- E. Falls within JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

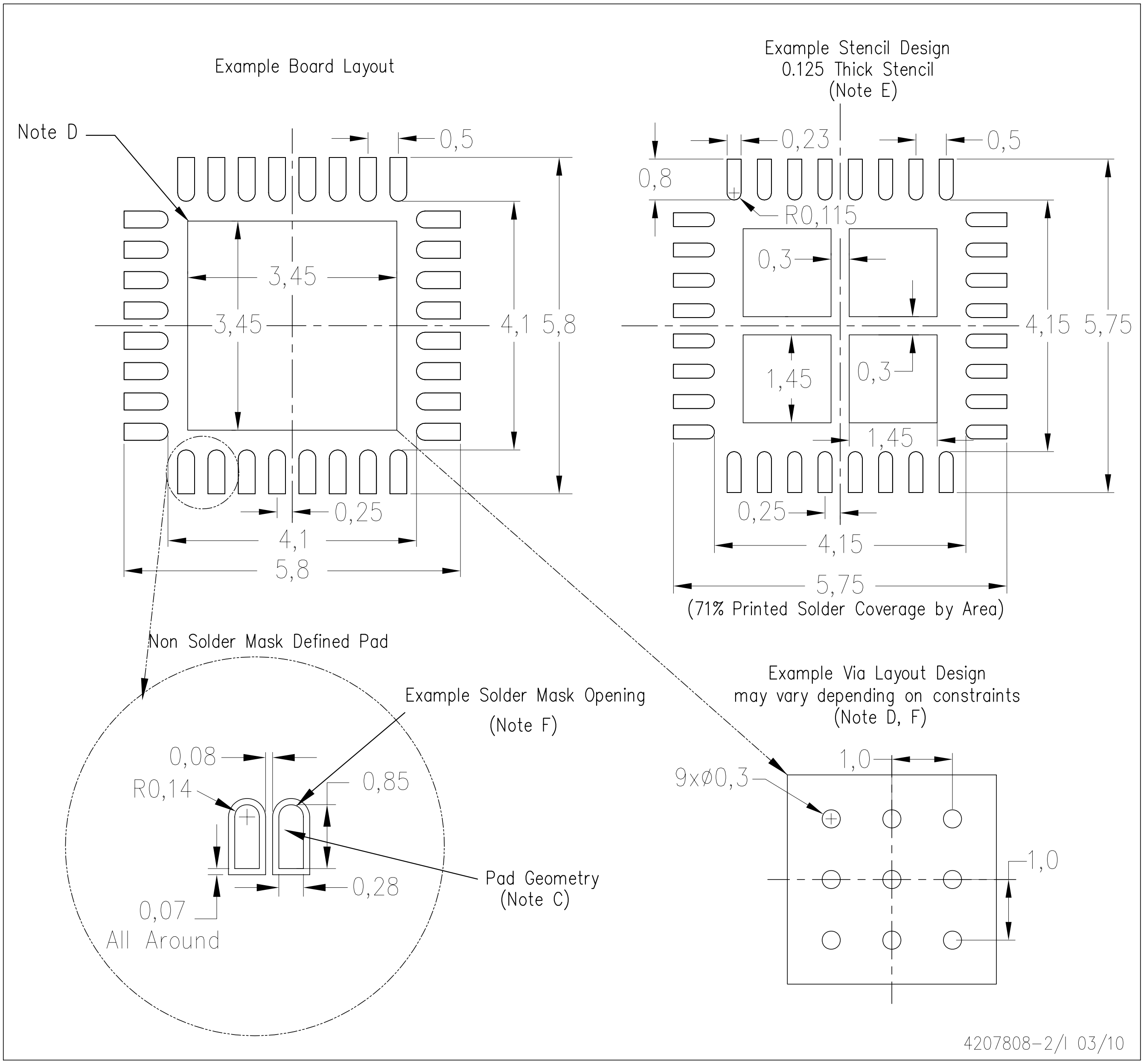


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S-PVQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD


Example Board Layout
Note D
0,5
3,45
3,45
4,1
5,8
0,25
4,1
5,8
Example Stencil Design
0.125 Thick Stencil
(Note E)
0,23
0,5
0,8
R0,115
0,3
0,3
1,45
1,45
4,15
5,75
0,25
4,15
5,75
(71% Printed Solder Coverage by Area)
Non Solder Mask Defined Pad
Example Solder Mask Opening
(Note F)
0,08
R0,14
0,85
0,28
0,07
All Around
Pad Geometry
(Note C)
Example Via Layout Design
may vary depending on constraints
(Note D, F)
1,0
9xø0,3
1,0
4207808-2/I 03/10

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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