# 含SMAART线接口的低功耗、数字温度传感器

查询样品: TMP104

## 特性

- 多重设备访问(MDA):
  - 全局读/写操作
- SMAART 线接口
- 分辨率: 8 位
- 准确度: 典型值为 ±0.5℃ (—10℃ 至 +100℃)
- 低静态电流:
  - 在 $I_Q$ 为 0.25 Hz的运行模式下为 3 μA
  - 1 μA 关断电流
- 电源电压范围: 1.4 V 至 3.6 V
- 数字输出
- 封装方式: 0.8-mm (±5%) × 1-mm (±5%) 4-焊球 WCSP (DSBGA)

## 应用

- 手机
- 笔记本电脑

## 说明

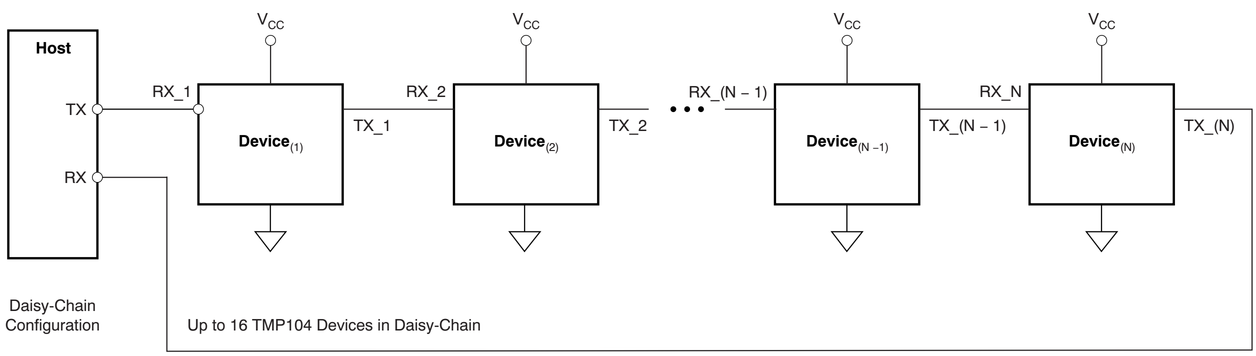
TMP104 是一款采用 4 焊球晶圆级芯片规模封装 (WCSP) 的数字输出温度传感器。 TMP104 对温度的读取辨别能力为 1℃。

TMP104 特有一个支持菊花链配置的 SMAART 线接口。 此外，该接口还支持多器件存取 (MDA) 命令，这将允许主机与总线上的多个器件同时进行通信，从而不必向总线上的每个 TMP104 分别发送命令。

最多可以把 16 个 TMP104 并联连接起来，并且主机可以很轻易地对它们进行读取操作。 对于那些必须监视多个温度测量区域而又空间受限、对功耗敏感的应用而言，TMP104 是特别理想的选择。

TMP104 的额定工作温度范围为－40℃ 至 +125℃。

### 典型应用



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION(1)

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | PACKAGE MARKING | ORDERING NUMBER |
|---|---|---|---|---|
| TMP104 | DSBGA-4 | YFF | T4 | TMP104YFFR |
| | | | | TMP104YFFT |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

## ABSOLUTE MAXIMUM RATINGS(1)

| | | TMP104 | UNIT |
|---|---|---|---|
| Supply voltage | | 3.6 | V |
| Input voltage | | –0.3 to (V+) + 0.3 | V |
| Operating temperature | | –55 to +150 | °C |
| Storage temperature | | –60 to +150 | °C |
| Junction temperature | | +150 | °C |
| ESD rating | Human body model (HBM) | 2000 | V |
| | Charged device model (CDM) | 1000 | V |
| | Machine model (MM) | 200 | V |

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TMP104 YFF 4 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 188.5 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 2.1 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 35.1 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 10.6 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 35.1 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | N/A | |

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

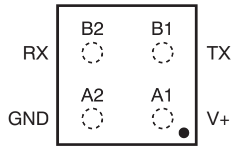
## ELECTRICAL CHARACTERISTICS

At $T_A$ = +25°C and V+ = +1.4 V to +3.6 V, unless otherwise noted.

| | PARAMETER | TEST CONDITIONS | TMP104 MIN | TMP104 TYP | TMP104 MAX | UNIT |
|---|---|---|---|---|---|---|
| **TEMPERATURE INPUT** | | | | | | |
| | Range | | –40 | | +125 | °C |
| | Accuracy (temperature error) | –10°C to +100°C, V+ = 1.8 V | | ±0.5 | ±2 | °C |
| | | –40°C to +125°C, V+ = 1.8 V | | ±1 | ±3 | °C |
| | | vs supply | | ±0.2 | ±0.5 | °C/V |
| | Resolution | | | 1.0 | | °C |
| **DIGITAL INPUT/OUTPUT** | | | | | | |
| $V_{IH}$ | Input logic levels | | 0.7 × (V+) | | V+ | V |
| $V_{IL}$ | | | –0.5 | | 0.3 × (V+) | V |
| $I_{IN}$ | Input current | 0 < $V_{IN}$ < (V+) + 0.3 V | | | 1 | μA |
| $V_{OL}$ | Output logic levels | V+ > 2 V, $I_{OL}$ = 1 mA | 0 | | 0.4 | V |
| | | V+ < 2 V, $I_{OL}$ = 1 mA | 0 | | 0.2 × (V+) | V |
| $V_{OH}$ | | V+ > 2 V, $I_{OH}$ = 1 mA | (V+) – 0.4 | | V+ | V |
| | | V+ < 2 V, $I_{OH}$ = 1 mA | 0.8 × (V+) | | V+ | V |
| | Resolution | | | 8 | | Bit |
| | Conversion time | | | 26 | 35 | ms |
| | Conversion modes | CR1 = 0, CR0 = 0 (default) | | 0.25 | | Conv/s |
| | | CR1 = 0, CR0 = 1 | | 1 | | Conv/s |
| | | CR1 = 1, CR0 = 0 | | 4 | | Conv/s |
| | | CR1 = 1, CR0 = 1 | | 8 | | Conv/s |
| | Timeout time | Interface | | 28 | | ms |
| | SMAART wire interface | Serial baud rate | 4.8 | | 114 | kbps |
| **POWER SUPPLY** | | | | | | |
| | Operating supply range | | +1.4 | | +3.6 | V |
| $I_Q$ | Quiescent current | Serial bus inactive, CR1 = 0, CR0 = 0 (default), V+ = 1.8 V | | 1.5 | 3 | μA |
| | | Serial bus active, CR1 = 0, CR0 = 0, V+ = 1.8 V | | 20 | | μA |
| $I_{SD}$ | Shutdown current | Serial bus inactive, V+ = 1.8 V | | 0.5 | 1 | μA |
| **TEMPERATURE** | | | | | | |
| | Specified range | | –40 | | +125 | °C |
| | Operating range | | –55 | | +150 | °C |

## PIN CONFIGURATION

**YFF PACKAGE**
**WCSP-4 (DSBGA-4)**
**(TOP VIEW)**




## PIN DESCRIPTIONS

| PIN | | |
|---|---|---|
| NO. | NAME | DESCRIPTION |
| A1 | V+ | Supply voltage |
| A2 | GND | Ground |
| B1 | TX | Serial data output pin (push-pull output) |
| B2 | RX | Serial data input pin |

## TYPICAL CHARACTERISTICS

At $T_A$ = +25°C and V+ = 1.8 V, unless otherwise noted.

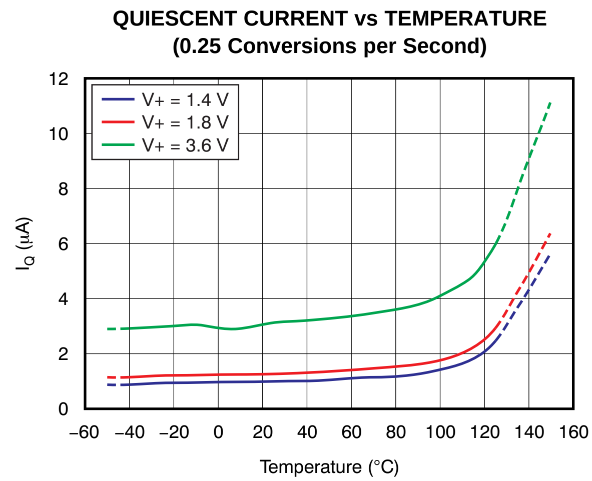



**Figure 1.**

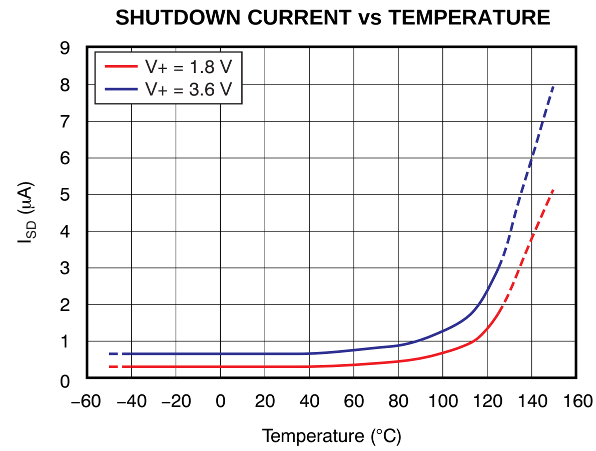



**Figure 2.**

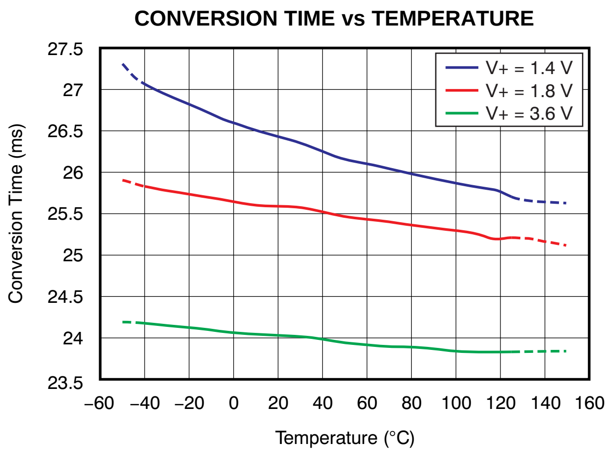



**Figure 3.**

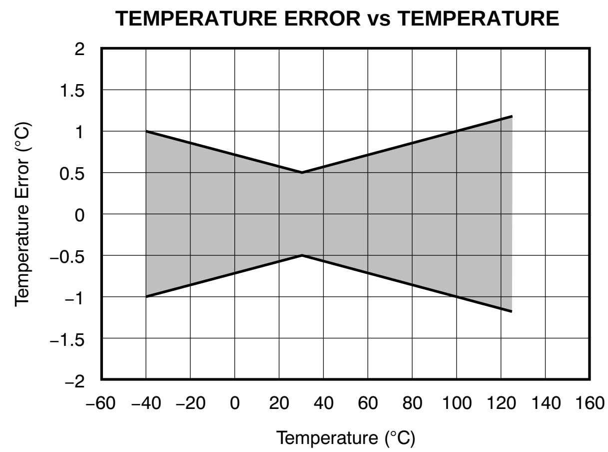



**Figure 4.**

# APPLICATION INFORMATION

## GENERAL DESCRIPTION

The TMP104 is a digital output temperature sensor in a wafer chip-scale package (WCSP) that is optimal for thermal management and thermal profiling. The TMP104 includes a SMAART wire interface that is capable of communicating in a daisy-chain with up to 16 devices on a single bus. The interface requires two pins from the host; the first device in the daisy-chain receives data from the host and the last device in the daisy-chain returns data to the host. In addition, the TMP104 has the capability of executing multiple device access (MDA) commands that allow multiple TMP104s to respond to a single global bus command. MDA commands reduce communication time and power in a bus that contains multiple TMP104 devices. The TMP104 is specified over a temperature range of –40°C to +125°C.

The TMP104 also has the capability of configuring the bus in a transparent mode, where the input from the host is sent directly to the next device in the chain without delay. Additionally, the TMP104 can disconnect the chain and create a serial communication controlled by each TMP104 on the bus, thereby allowing each device to have configurable addressing and interrupt capabilities. The input pin, RX, is a high-impedance node. The output pin, TX, has an internal push-pull output stage that can drive the host to GND or V+.

After an initialization sequence, each device on the bus is programmed with its own interface address that allows it to respond to its own address and also respond to general commands that permit the user to read or write to all of the devices on the bus without having to send its individual address and command to each individual device.

The temperature sensor in the TMP104 is the chip itself. Thermal paths run through the package bumps as well as the package. The lower thermal resistance of metal causes the bumps to provide the primary thermal path. To maintain accuracy in applications that require air or surface temperature measurement, care should be taken to isolate the package from ambient air temperature. A thermally-conductive adhesive can help to achieve accurate surface temperature measurement.

## COMMUNICATION PROTOCOL

Each communication of the SMAART wire protocol consists of 8-bit words, transferred least significant bit (LSB) first. Each 8-bit word begins with a *Start* bit that is logic low, and ends with a *Stop* bit that is logic high. By using a Start bit and Stop bit for each 8-bit word, the TMP104 can calibrate each word and maintain synchronous communication throughout the process. The host commences the communication by sending a Start bit followed by the calibration byte (55h), allowing the TMP104 to sync to the baud rate of the host, followed by the Stop bit. Then, another Start bit is sent, followed by the command register byte and a Stop bit. Finally, a third Start bit is sent followed by the data byte, where master sends data if the instruction is a write command, or the TMP104 breaks the chain and sends data if the instruction is a read command. The process finishes with a Stop bit. The sequence is shown in Table 1 and Figure 5.

**Table 1. Communication Format**

| Start bit | Calibration | Stop bit | Start bit | Command byte | Stop bit | Start bit | Data byte | Stop bit |
|---|---|---|---|---|---|---|---|---|

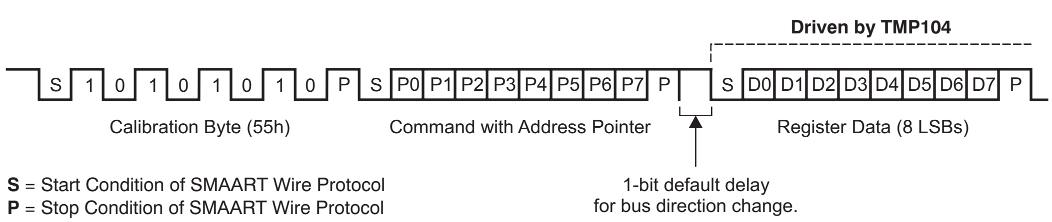



**Figure 5. Generic Communication BitStream**

The TMP104 has two dedicated pins for communication: TX and RX. Usually, these two pins are connected internally and the signal on the RX propagates to the TX; that is, the TMP104 works in a transparent mode. The TMP104 breaks this buffer configuration only when it must send data on the bus or during address assignment and alert procedures.

The TMP104 supports unique *address assignment* and *alert interrupt* procedures. There are general-call read and write commands that allow simultaneous reads or writes to all devices in the daisy-chain. The interface has built-in time outs (typically 28 ms) that return the interface to a known state if communication is disrupted.

## COMMAND REGISTER

Figure 6 shows the internal register structure of the TMP104. Communications between the registers are transferred through the interface in LSB-first order. The 8-bit Command Register, as shown in Table 2, is used to determine the type of instruction being addressed. These eight bits could either interpret a global instruction or an individual instruction, which is determined by the value of P7. When P7 = 0, the command byte interprets an individual instruction; when P7 = 1, the command byte interprets a global instruction.

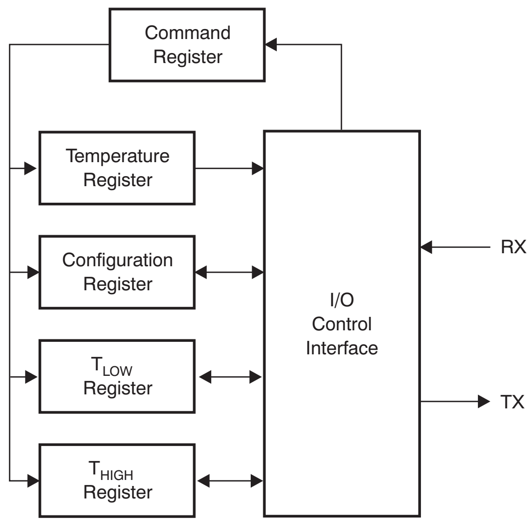



**Figure 6. Internal Register Structure**

**Table 2. Command Register Byte**

| P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |
|---|---|---|---|---|---|---|---|
| GLB | IN3/ID3 | IN2/ID2 | IN1/ID1 | IN0/ID0 | P1 | P0 | R/W |

## GLOBAL INITIALIZATION AND ADDRESS ASSIGNMENT SEQUENCE

At device power-up, every TMP104 in the daisy-chain is connected in transparent mode, as shown in Figure 7. The host must send the initialization command (P7-P0 = 10001100) in order for the bus to program its internal address depending on the number of devices on the bus.

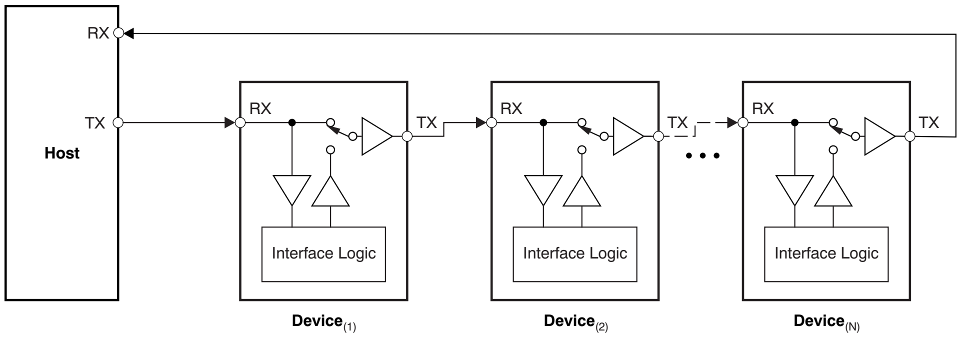



**Figure 7. TMP104 Daisy-Chain: Bus Status at Start of Global Initialization**

Each TMP104 in the chain interprets the initialization command byte and disconnects the chain, as shown in Figure 8. The host must then send the address assignment command, consisting of P7-P4 = 1001 and P3-P0 = 0000, where P3-P0 represents the address of the first device in the chain; this word is stored internally as its device ID. The first device increments the unit in the device address and then reconnects the bus, as shown in Figure 9. This address is then sent to the next device in the chain. Once all devices on the chain have received the respective addresses, the host receives the last programmed address on the chain + 1. The host can use this information to determine the total number of devices in the chain and the respective address of each device.

After the initialization sequence, every device can be addressed individually or through global commands. This global initialization sequence is a requirement and must be performed before any other communication.

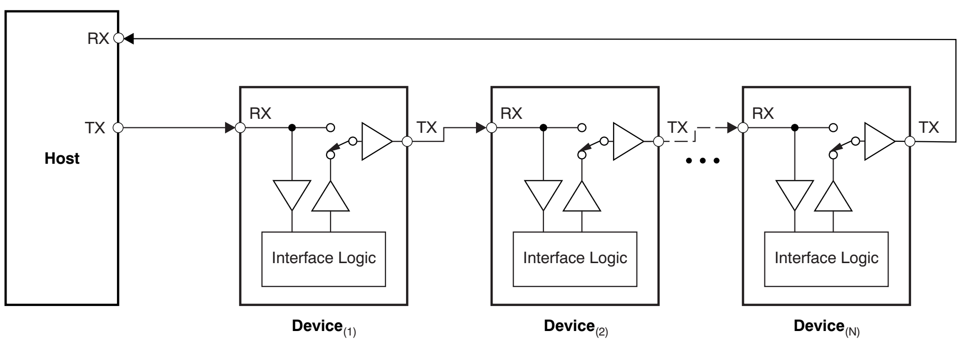



**Figure 8. TMP104 Daisy-Chain: Bus Status at Start of Address Assignment**

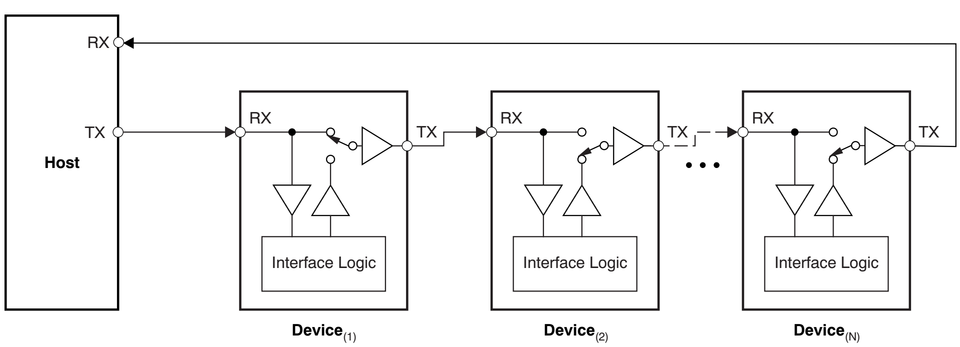



**Figure 9. TMP104 Daisy-Chain: Bus Status After First Device Address Assignment**

## GLOBAL READ AND WRITE

The host can initiate a global read or write command to all TMP104s in the daisy-chain by sending the read/write command, consisting of P7-P3 = 11110. P2-P1 indicate the data register pointer, as shown in Table 3, and P0 indicates read/write control. P0 = 0 indicates a global write command. The host must transfer one more byte of data for the register (indicated by bits P2-P1), and every TMP104 in the daisy-chain updates the appropriate register. P0 = 1 indicates a global read command. The TMP104 with the device ID of '0000' then breaks the bus connection, transmits the data from the register indicated by bits P2-P1, and then reconnects the bus. The TMP104 with the device ID of '0001' then repeats the same sequence, followed by the rest of the TMP104 devices in the daisy-chain.

**Table 3. Pointer Addresses**

| P0 | P0 | REGISTER |
|---|---|---|
| 0 | 0 | Temperature register (read-only) |
| 0 | 1 | Configuration register (read/write) |
| 1 | 0 | $T_{LOW}$ register (read/write) |
| 1 | 1 | $T_{HIGH}$ register (read/write) |

## GLOBAL CLEAR INTERRUPT

The host can initiate a global clear interrupt command (P7-P0 = 10101001) to all TMP104s in the daisy-chain. Upon receiving this command, the TMP104 disables future interrupts (D7 in the Configuration Register is set to '0'). If a TMP104 has previously broken the bus connection and sent an interrupt (logic low on the bus), it now stops holding the bus low. The device sends the baud rate calibration command and clear interrupt command to the next TMP104 in the chain, and then reconnects the bus. In the case of multiple devices having active interrupts, the clear interrupt command propagates through the daisy-chain, disables all interrupts, and reconnects the bus across all devices.

## GLOBAL SOFTWARE RESET

The host can initiate a global software reset command (P7-P0 = 10110100) to all TMP104s in the daisy-chain. Upon receiving this command, the TMP104 resets its internal registers except for the device ID, which is not reset, and reconnects the bus. If the bus is broken before the initiation of this command, all TMP104s before the broken bus point receive the command. If the host intends to initiate a global software reset across all TMP104s in the chain, this command must be transmitted multiple times until it echoes back to the host.

## INDIVIDUAL READ AND WRITE

The host can initiate an individual read/write command to a particular TMP104 in the daisy-chain by sending the read/write command. The read/write command consists of these parameters:

- P7 = 0
- P6-P3 = the device ID
- P2-P1 = the data register pointer; see Table 3
- P0 = indicates read/write control

P0 = 0 indicates an individual write command; the host must transfer one more byte of data for the register indicated by bits P2-P1. The TMP104 in the daisy-chain that corresponds to the device ID noted by bits P6-P3 then updates the appropriate register. P0 = 1 indicates an individual read command; as shown in Figure 10, the TMP104 in the daisy-chain that corresponds to the device ID pointed by bits P6-P3 then breaks the bus, transmits the data from the register pointed by bits P2-P1, and reconnects the bus.

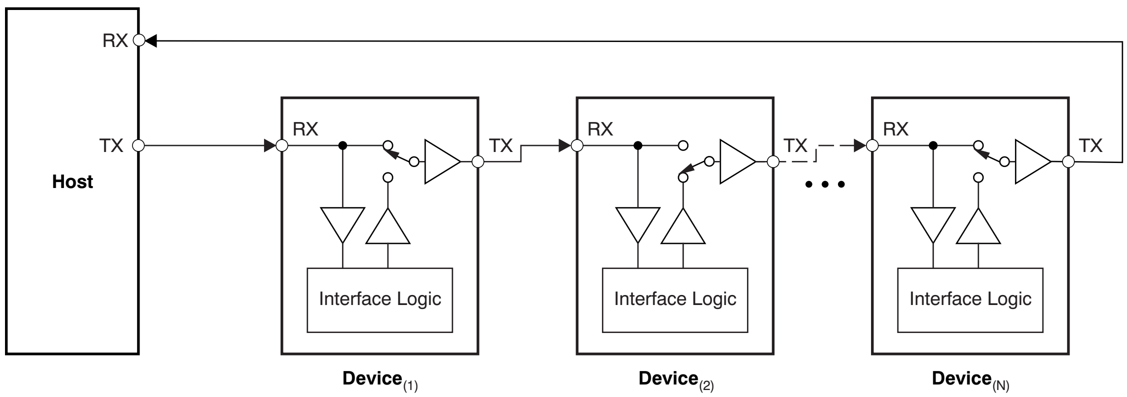



**Figure 10. TMP104 Daisy-Chain: Bus Status During Individual Read Operation of Second Device**

## TEMPERATURE REGISTER

The Temperature Register of the TMP104 is configured as an 8-bit, read-only register that stores the output of the most recent conversion. A single byte must be read to obtain data, and is described in Table 4. The data format for temperature is summarized in Table 5. One LSB equals 1°C.

**Table 4. Temperature Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |

Negative numbers are represented in binary twos complement format. Following power-up or reset, the Temperature Register reads 0°C until the first conversion is complete.

**Table 5. 8-Bit Temperature Data Format(1)**

| TEMPERATURE (°C) | DIGITAL OUTPUT | |
|---|---|---|
| | BINARY | HEX |
| 128 | 0111 1111 | 7F |
| 127 | 0111 1111 | 7F |
| 100 | 0110 0100 | 64 |
| 80 | 0101 0000 | 50 |
| 75 | 0100 1011 | 4B |
| 50 | 0011 0010 | 32 |
| 25 | 0001 1001 | 19 |
| 0 | 0000 0000 | 00 |
| –1 | 1111 1111 | FF |
| –25 | 1110 0111 | E7 |
| –55 | 1100 1001 | C9 |

(1) The resolution for the analog-to-digital converter (ADC) is 1°C/count, where *count* is equal to the digital output of the ADC.

For positive temperatures (for example, +50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code, left-justified format. Denote a positive number with most significant bit (MSB) = 0.

Example: (+50°C)/(1°C/count) = 50 = 32h = 0011 0010

For negative temperatures (for example, –25°C):

Generate the twos complement of a negative number by complementing the absolute value binary number and adding 1. Denote a negative number with MSB = 1.

Example: (|–25°C|)/(1°C/count) = 25 = 19h = 0001 1001

Twos complement format: 1110 0110 + 1 = 1110 0111

## CONFIGURATION REGISTER

The Configuration Register is an 8-bit read/write register used to store bits that control the operational modes of the temperature sensor. Read/write operations are performed LSB first. The format and power-up/reset value of the Configuration Register is shown in Table 6.

**Table 6. Configuration and Power-Up/Reset Format**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| INT_EN | CR1 | CR0 | FH | FL | LC | M1 | M0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

### Temperature Watchdog Function (FH, FL)

The TMP104 contains a watchdog function that monitors device temperature and compares the result to the values stored in the temperature limit registers ($T_{HIGH}$ and $T_{LOW}$) in order to determine if the device temperature is within these set limits. If the temperature of the TMP104 becomes greater than the value in the $T_{HIGH}$ register, then the flag-high bit (FH) in the Configuration Register is set to '1'. If the temperature falls below value in the $T_{LOW}$ register, then the flag-low bit (FL) is set to '1'. If both flag bits remain '0', then the temperature is within the temperature *window* set by the temperature limit registers, as shown in Figure 11.

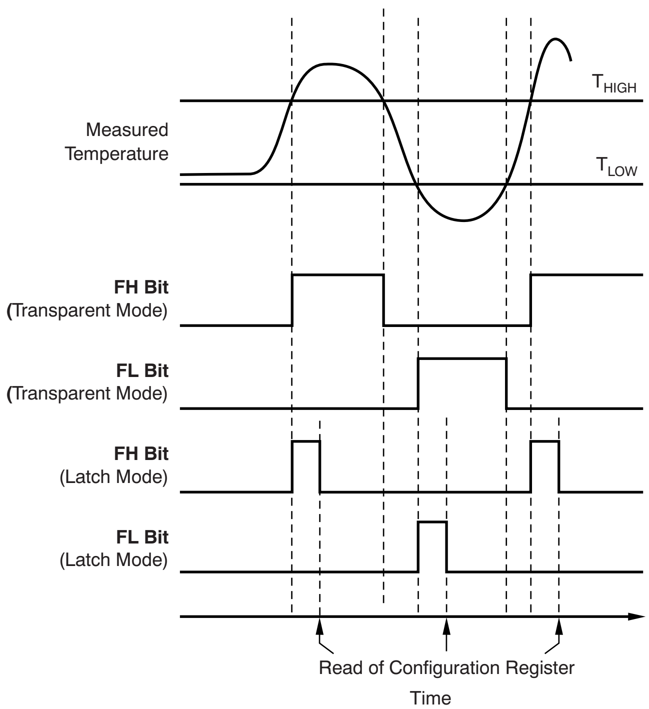



**Figure 11. Temperature Flag Functional Diagram**

The latch bit (LC) in the Configuration Register is used to latch the value of the flag bits (FH and FL) until the master issues a read command to the Configuration Register. The flag bits are set to '0' if a read command is received by the TMP104, or if LC = 0 and the temperature is within the temperature limits. The power-on default values for these bits are FH = 0, FL = 0, and LC = 0.

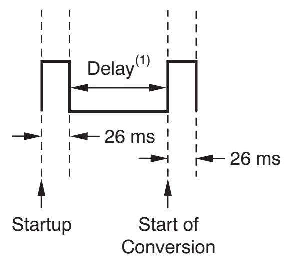
### Conversion Rate (CR1, CR0)

The conversion rate bits (CR1 and CR0), located in the Configuration Register, configure the TMP104 for conversion rates of 8 Hz, 4 Hz, 1 Hz, or 0.25 Hz (default). The TMP104 has a typical conversion time of 26 ms. To achieve different conversion rates, the TMP104 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0. Table 7 shows the settings for CR1 and CR0.

**Table 7. Conversion Rate Settings**

| CR1 | CR0 | CONVERSION RATE |
|---|---|---|
| 0 | 0 | 0.25 Hz (default) |
| 0 | 1 | 1 Hz |
| 1 | 0 | 4 Hz |
| 1 | 1 | 8 Hz |

After power-up or general-call reset, the TMP104 immediately starts a conversion, as shown in Figure 12. The first result is available after 26 ms (typical). The active quiescent current during conversion is 40 μA (typical at +25°C, V+ = 1.8 V). The quiescent current during delay is 1.0 μA (typical at +25°C, V+ = 1.8 V).




(1) Delay is set by CR1 and CR0.

**Figure 12. Conversion Start**

### Conversion Modes

#### *Shutdown Mode (M1 = 0, M0 = 0)*

Shutdown mode saves maximum power by shutting down all device circuitry other than the serial interface, reducing current consumption to typically less than 0.5 μA. Shutdown mode is enabled when bits M1 and M0 (in the Configuration Register) read '00'. The device shuts down when the current conversion is completed.

#### *One-Shot Mode (M1 = 0, M0 = 1)*

The TMP104 features a One-Shot Temperature Measurement mode. When the device is in Shutdown mode, writing '01' to bits M1 and M0 starts a single temperature conversion. During the conversion, bits M1 and M0 read '01'. The device returns to the shutdown state at the completion of the single conversion. After the conversion, bits M1 and M0 read '00'. This feature is useful for reducing power consumption in the TMP104 when continuous temperature monitoring is not required.

As a result of the short conversion time, the TMP104 can achieve a higher conversion rate. A single conversion typically takes 26 ms and an individual read can take place in less than 300 μs. When using One-Shot mode, 30 or more conversions per second are possible.

#### *Continuous Conversion Mode (M1 = 1)*

When the TMP104 is in Continuous Conversion mode (M1 = 1), continuous conversions are performed at a rate determined by the conversion rate bits, CR1 and CR0 (in the Configuration Register). The TMP104 performs a single conversion, and then powers down and waits for the appropriate delay set by CR1 and CR0. See Table 7 for CR1 and CR0 settings.

### Interrupt Functionality (INT_EN)

The TMP104 interrupts the host by disconnecting the bus and issuing an interrupt request by holding the bus low if all of these conditions are met, as shown in Figure 13:

- INT_EN in the Configuration Register is set to '1';
- The temperature result is higher than the value in the $T_{HIGH}$ register or lower than the value in the $T_{LOW}$ register (as indicated by a '1' in either FL or FH);
- The bus is logic high and idle for more than 28 ms.

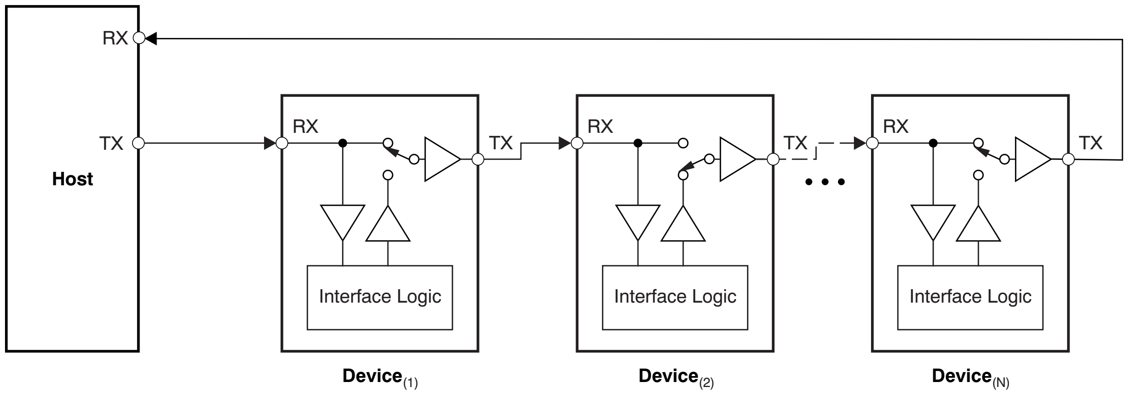



**Figure 13. TMP104 Daisy-Chain:
Bus Status During an Interrupt Request (Logic Low) from Second Device**

The interrupt on the bus is latched regardless of the status of LC. Writing a '1' to INT_EN automatically sets the LC bit. The TMP104 holds the bus low until one of the following events happen:

- Global Interrupt Clear command received;
- Global Software Reset command received;
- A power-on reset event occurs.

Each of these events clears INT_EN; the TMP104 does not issue future interrupts until the host writes '1' to bit D7 in the Configuration Register to re-enable future interrupts.

In a system with enabled interrupts, it is possible for a TMP104 on the bus to issue an interrupt at the same time that the host starts a communication sequence. To avoid this scenario, it is recommended that the host should check the status on the receiving side of the bus after transmitting the calibration byte. If it is '1', then the host can continue with the communication. If it is '0', one of the TMP104 devices on the bus is issuing an alert and the host must transmit a Global Interrupt Clear command.

## TEMPERATURE LIMIT REGISTERS

The $T_{HIGH}$ and $T_{LOW}$ registers are used to store the temperature limit thresholds for the TMP104 watchdog function. At the end of each temperature measurement, the TMP104 compares the temperature results to each of these limits. If the temperature result is greater than the $T_{HIGH}$ limit, then the FH bit in the Configuration Register is set to '1'. If the temperature result is less than the $T_{LOW}$ limit, then the FL bit in the Configuration Register is set to '1'; see Figure 11.

Table 8 and Table 9 describe the format for the $T_{HIGH}$ and $T_{LOW}$ registers. Power-up reset values for $T_{HIGH}$ and $T_{LOW}$ are: $T_{HIGH}$ = +60°C and $T_{LOW}$ = –10°C. The format of the data for $T_{HIGH}$ and $T_{LOW}$ is the same as for the Temperature Register.

**Table 8. $T_{HIGH}$ Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| H7 | H6 | H5 | H4 | H3 | H2 | H1 | H0 |

**Table 9. $T_{LOW}$ Register**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| L7 | L6 | L5 | L4 | L3 | L2 | L1 | L0 |

## TIMEOUT FUNCTION

A timeout mechanism is implemented on the TMP104 to allow for re-synchronization of the SMAART wire interface if synchronization between the host and the TMP104 is lost for 28 ms (typical). If the timeout period expires between the calibration byte and the command byte, or between the command byte and any data byte, or between any data bytes, the TMP104 resets the SMAART wire interface circuitry so that it expects the baud rate calibration command to restart. Every time a byte is transmitted on the SMAART wire interface, this timeout period restarts.

## NOISE

The TMP104 is a very low-power device and generates very low noise on the supply bus. Applying a bypass capacitor to the V+ pin of the TMP104 can further reduce any noise the TMP104 might propagate to other components. $C_F$ in Figure 14 should be greater than 0.1 μF.

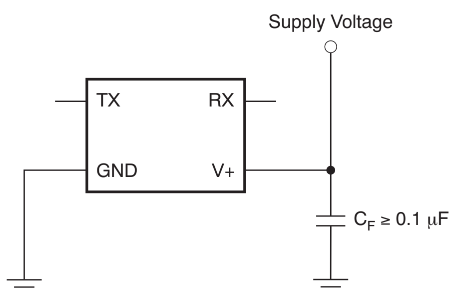



**Figure 14. Noise Reduction**

## SMAART WIRE INTERFACE TIMING SPECIFICATIONS

Figure 15 illustrates the key timing and jitter considerations for the SMAART wire interface. Table 10 contains the timing specifications for ensured, reliable operation. During a transaction, the baud rate must remain within ±1% of its initialization byte value; however, the baud rate can change from transaction to transaction. There is an allowed delay between each byte transfer of less than 28 ms, which is the bus inactivity timeout check for the TMP104 SMAART wire interface.

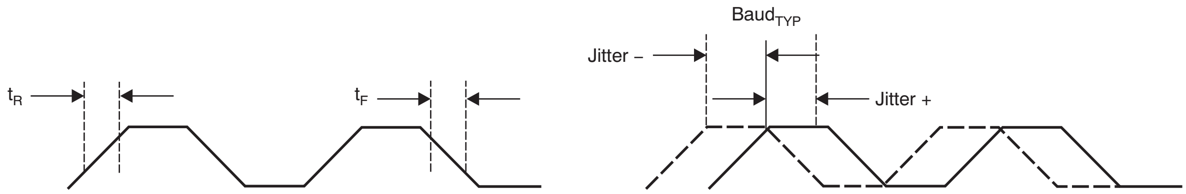



**Figure 15. SMAART Wire Timing Diagram**

**Table 10. Timing Diagram Definitions**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Baud | | 4.8 k | 114 k | Bits/s |
| $t_R$ | Clock/data rise time | | 0.5 | %Baud |
| $t_F$ | Clock/data fall time | | 0.5 | %Baud |
| Jitter | | | ±1 | %Baud |

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/ Ball Finish | MSL Peak Temp (3) | Samples (Requires Login) |
|---|---|---|---|---|---|---|---|---|---|
| TMP104YFFR | ACTIVE | DSBGA | YFF | 4 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |
| TMP104YFFT | ACTIVE | DSBGA | YFF | 4 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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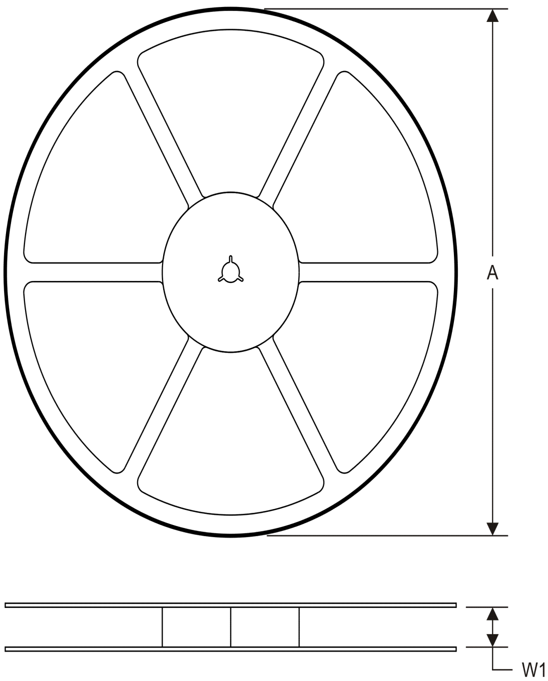
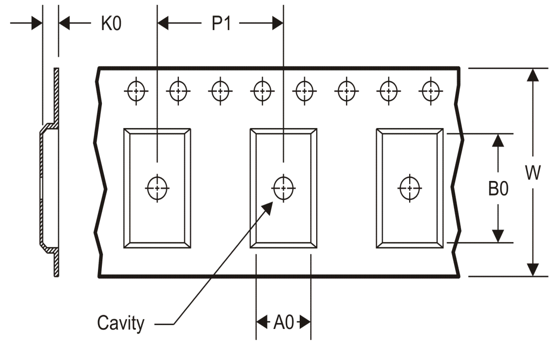
## TAPE AND REEL INFORMATION

### REEL DIMENSIONS




### TAPE DIMENSIONS



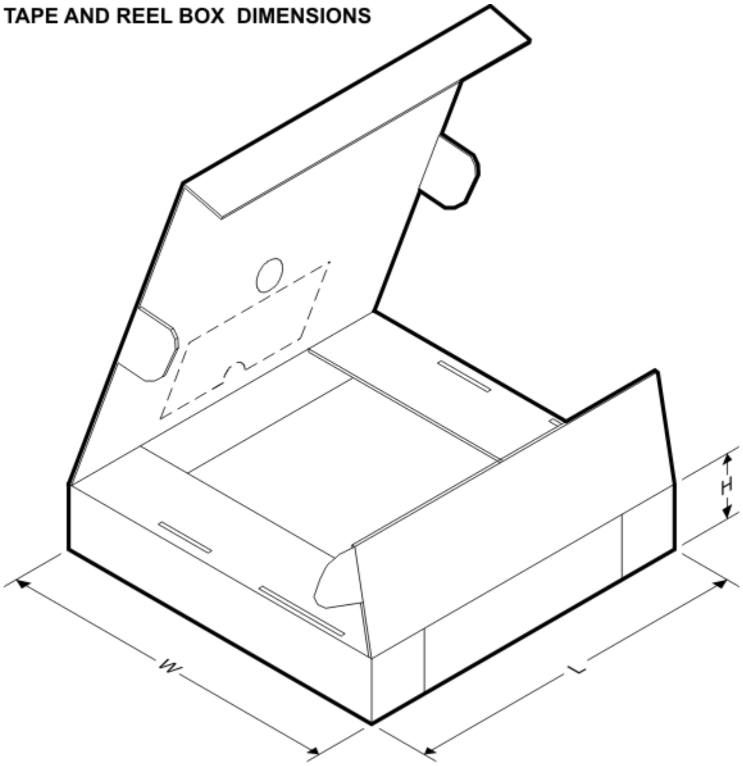

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

### TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMP104YFFR | DSBGA | YFF | 4 | 3000 | 180.0 | 8.4 | 0.86 | 1.06 | 0.69 | 4.0 | 8.0 | Q1 |
| TMP104YFFT | DSBGA | YFF | 4 | 250 | 180.0 | 8.4 | 0.86 | 1.06 | 0.69 | 4.0 | 8.0 | Q1 |

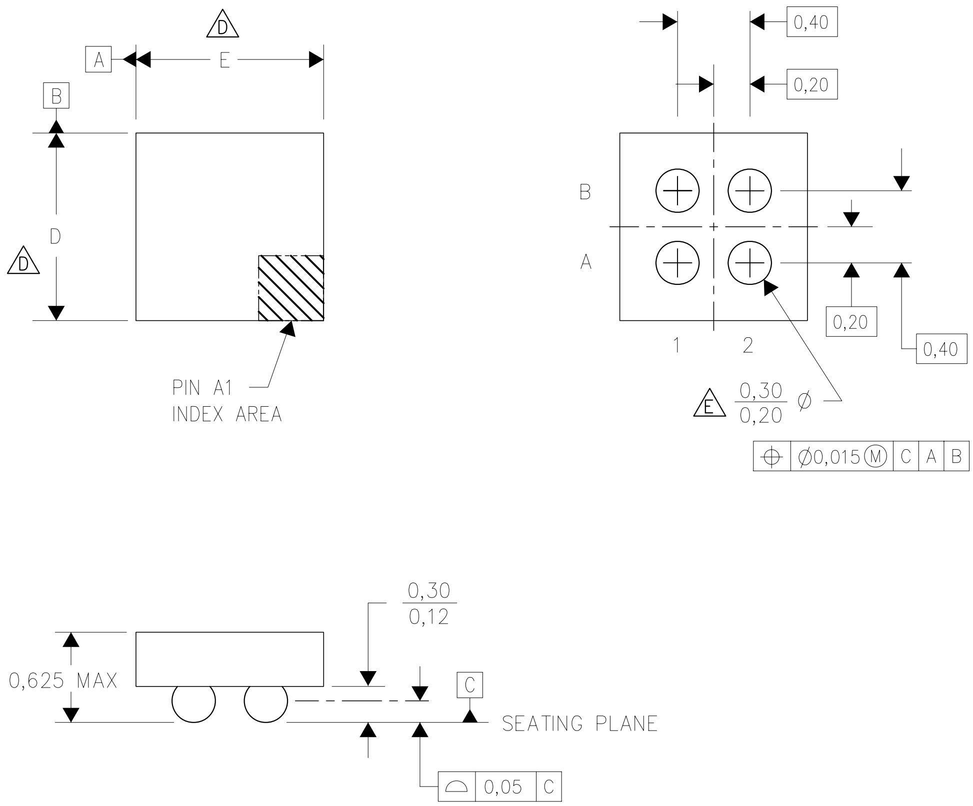
## TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMP104YFFR | DSBGA | YFF | 4 | 3000 | 210.0 | 185.0 | 35.0 |
| TMP104YFFT | DSBGA | YFF | 4 | 250 | 210.0 | 185.0 | 35.0 |

YFF (S-XBGA-N4) DIE-SIZE BALL GRID ARRAY

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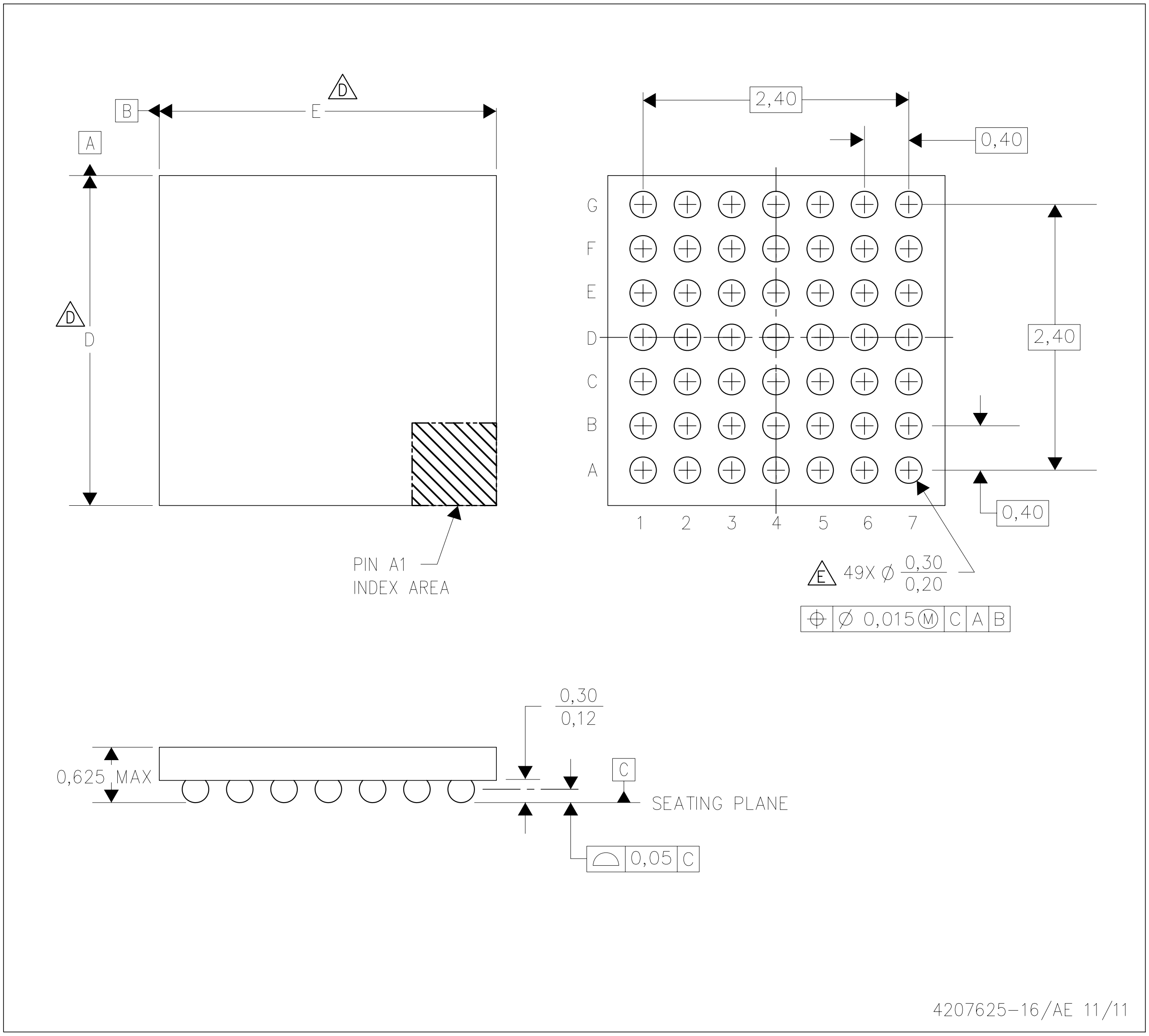
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. The package size (Dimension D and E) of a particular device is specified in the device Product Data Sheet version of this drawing, in case it cannot be found in the product data sheet please contact a local TI representative.
E. Reference Product Data Sheet for array population.
2 x 2 matrix pattern is shown for illustration only.
F. This package contains Pb-free balls.

NanoFree is a trademark of Texas Instruments

YFF (R-XBGA-N49) DIE-SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
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