TRUE RMS RF POWER DETECTOR

Check for Samples: TRF1600

FEATURES

- RF True RMS Power Detector
- RMS to DC Conversion Up to 2 GHz
- Waveform and Modulation Independent (CW, GSM, WCDMA, TDMA, HSUPA)
- Linear-In-dB Output
- Input Dynamic Range of 28 dB (–29 dBm to –1 dBm)
- External Input Pin
- 6.7-mA Typical Operating Current
- 5-μA Maximum Shutdown Current
- Operating Temperature Range: –20°C to 85°C
- Small 2-mm x 2-mm QFN 6 Pin Package

APPLICATIONS

- Cellular Handsets (GSM, CDMA, TDMA)
- Power Amplifier Control Loops
- Transmitter Power Measurement and Control

DESCRIPTION

The TRF1600 is a true RMS power detector with a 28-dB dynamic input range and a linear-to-dB DC output. It is intended for use in wireless handheld devices such as cell phones and PDAs to measure and control PA output power accurately independent of the modulation scheme.

The device is designed to operate off of a lithium-ion battery (2.7 V to 5.5 V, 6 V tolerant) or a regulated supply. A low input signal at the enable pin puts the device in shut-down mode and supply current consumption is reduced to <5 μA. When asserted high the device enters active mode and outputs a DC voltage proportional to the RMS value of the input power expressed in dBm.

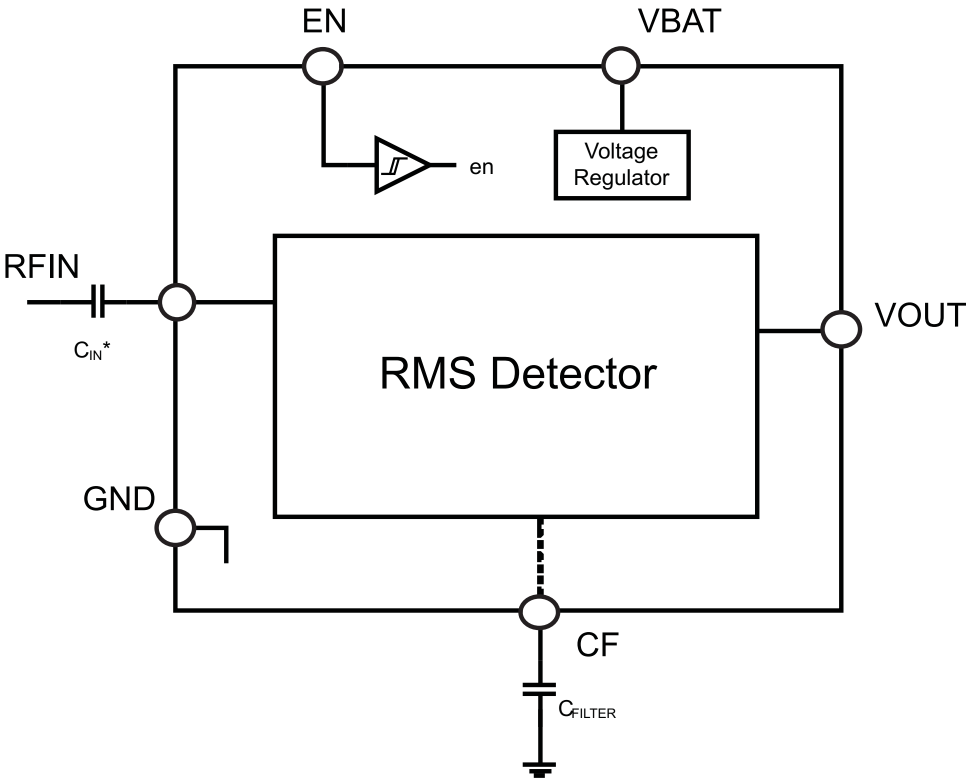
Table 1. ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER
–20°C to 85°C	DRV	TRF1600DRVR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

BLOCK DIAGRAM



*C_{IN} may be omitted if the DC level of the RF input signal is at ground.

PINOUT

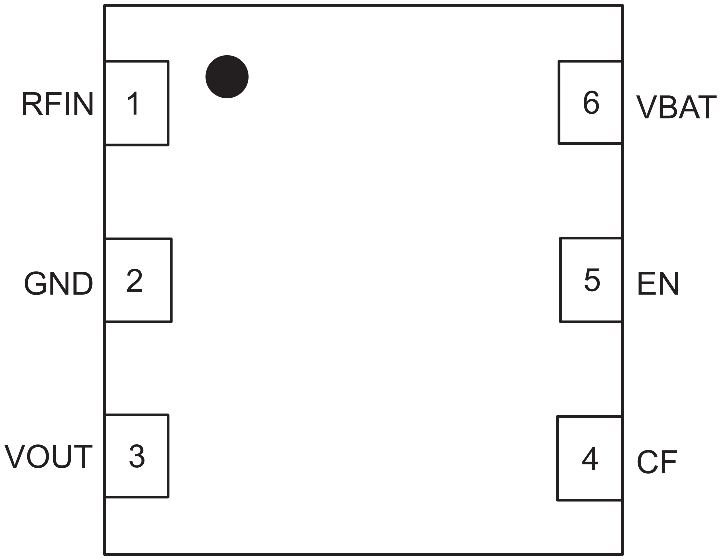


Table 2. TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
RFIN	1	I	RF input
GND	2		Ground
VOUT	3	O	Output of the device
CF	4	I	Filter capacitor. Pin needs to be connected to an off-chip filter capacitor in the application.
EN	5	I	Enable pin/Vprog
VBAT	6		Input supply pin to the device

ABSOLUTE MAXIMUM RATINGS(1)

All voltages values are with respect to GND. Over operating free-air temperature range (unless otherwise noted).

			VALUE	UNIT
	Unregulated input battery voltage		-0.5 to 6.0	V
	EN		-0.5 to 3.6	V
	VOUT		-0.5 to 3.6	V
	PRFIN (max RF input power)		6	dBm
θ_{JA}	Thermal resistance, junction to ambient		140	°C/W
P_D	Continuous power dissipation		50	mW
	ESD integrity	HBM (human body model)	2k	V
		CMD (charged device model)	500	
		IEC Contact – V_{CC} pin(2)	8k	
		IEC Air – V_{CC} pin(2)	15k	
T_A	Operating ambient temperature		–40 to 125	°C
T_J	Operating junction temperature		125	°C
T_S	Storage temperature		–40 to 125	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) IEC ESD tests performed on V_{CC} pin with five shunt capacitors ranging from 10 pF to 10 µF. This is meant to evaluate the performance of the device when it is powered directly from a battery with these capacitors used as bypass capacitors on the same PC board.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{BAT}	Unregulated input battery voltage	2.7		5.5	V
f_{IN}	Input frequency range	800		2000	MHz
	EN pin voltage	0		3.3	V
P_D	Continuous power dissipation			35	mW
T_A	Operating ambient temperature	–20		85	°C
	C_{FILTER}	0		3000	pF

ELECTRICAL CHARACTERISTICS

V_{BAT} = 3.0 ±5%, T_A = –20 to 85ºC, C_{FILTER} = 820 pF ±10%, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{BAT}	Battery voltage		2.7		5.5	V
$I_{BAT,\ ACTIVE}$	Supply current	EN = HIGH		6.7	8.5	mA
$I_{BAT,\ IDLE}$	Supply current, idle	EN = LOW RF input power present			10	µA
$I_{BAT,\ S/D}$	Supply current, shutdown	EN = LOW No RF input power present			5	µA
INPUT						
f_{IN}	Input frequency		800		2000	MHz
$P_{RFIN800}$	Input power, 800 MHz	Referred to 50-Ω Zin	–34		–1	dBm
$P_{RFIN2000}$	Input power, 2 GHz	Referred to 50-Ω Zin	–29		–1	dBm
OUTPUT						
$V_{OUT\ Max}$	Output voltage maximum	–1 dBm, 800 MHz	1.2	1.55	1.7	V
$V_{OUT\ Max}$	Output voltage maximum	–1 dBm, 2 GHz	1	1.32	1.55	V
$V_{OUT\ No\ RF}$	Output voltage no RF	No RF present	0	160	300	mV
$V_{OUT\ Range}$	Output voltage range	Over specified dynamic range		1.27		V

ELECTRICAL CHARACTERISTICS (continued)

V_{BAT} = 3.0 ±5%, T_A = –20 to 85ºC, C_{FILTER} = 820 pF ±10%, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OUT,GAIN}$	Output voltage gain		30	35	40	mV/dB
	10-dB log conformance error over temperature(1)	See Appendix A.1	–1		1	dB
	1-dB log conformance error	Ideal 1-dB power step	–0.3		0.3	dB
	Straight line 5-dB step error(2)	See Appendix A.2		0.06		dB
	Output variation due to modulation at same input power	Anywhere in dynamic range. (AM modulation 100% modulation depth with a 1-MHz tone)		0.1	0.35	dB
TC_{VOUT}	Response temperature coefficient(1)	P_{RFIN} = –4 dBm See Appendix A.3		2.2		mdB/°C
ΔTC_{VOUT}	Response temperature sensitivity spread - 1σ(1)	P_{RFIN} = –4 dBm See Appendix A.3		4.1		mdB/°C
ΔV_{OUT_TEMP}	Output voltage repeatability over temperature(1)			0.04	0.11	dB
PSRR	Power supply rejection ratio	V_{BAT} = 2.7 V to 5.5 V	30			dB
$V_{OUT,\ NOISE}$	Output referred noise	Integrated over bandwidth 1 kHz – 6.5 kHz		100	200	μV_{RMS}
$R_{OUT,\ EN1}$	Output impedance	EN = HIGH		9	50	Ω
$I_{OUT,\ EN0}$	Output leakage	EN = LOW			3	µA
t_{SAMPLE}	Sampling time (time to valid output)	EN = HIGH P_{RFIN} = MAX V_{OUT} 10% to 90%			13	µs
t_{WAKEUP}	Wakeup time	EN LOW to HIGH No RF input V_{OUT} to 90%			13	µs
LOGIC LEVEL INPUTS (EN)						
V_{IL}	Input low level				0.6	V
V_{IH}	Input high level		1.1			V
I_{IH}, I_{IH}	Input bias current		–1		1	µA

(1) Parameters require temperature testing. Limits based on 3σ statistics characterized on a limited number of samples. Limits not guaranteed in production.

(2) Limits based on 3σ statistics characterized on a limited number of samples. Limits not guaranteed in production.

TYPICAL PERFORMANCE CHARACTERISITICS

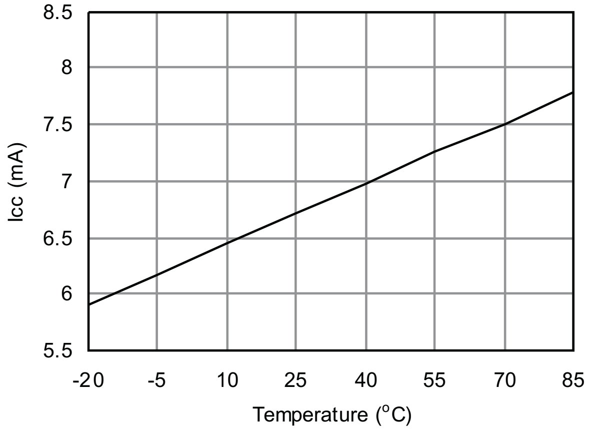

CURRENT CONSUMPTION
vs
TEMPERATURE

Figure 1.

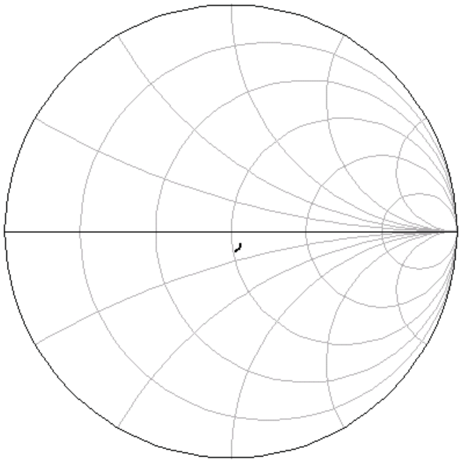

RF INPUT REFLECTION COEFFICIENT
(800 MHz TO 2 GHz)

Figure 2.

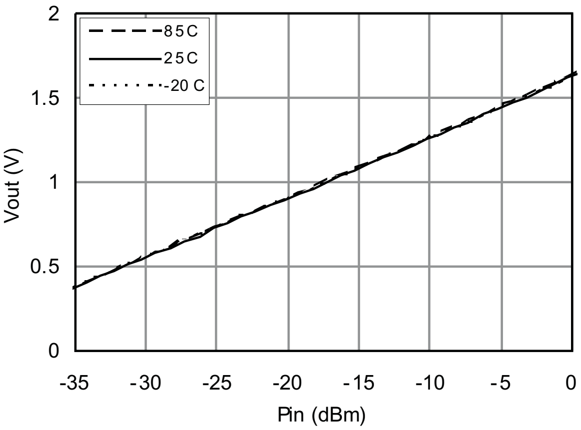

OUTPUT VOLTAGE
vs
INPUT POWER AT 800 MHz

Figure 3.

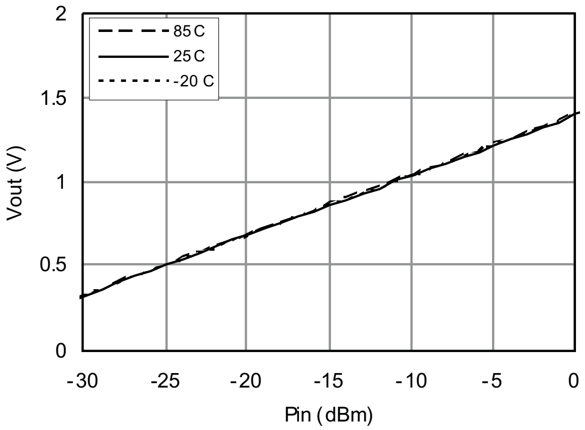

OUTPUT VOLTAGE
vs
INPUT POWER AT 2 GHz

Figure 4.

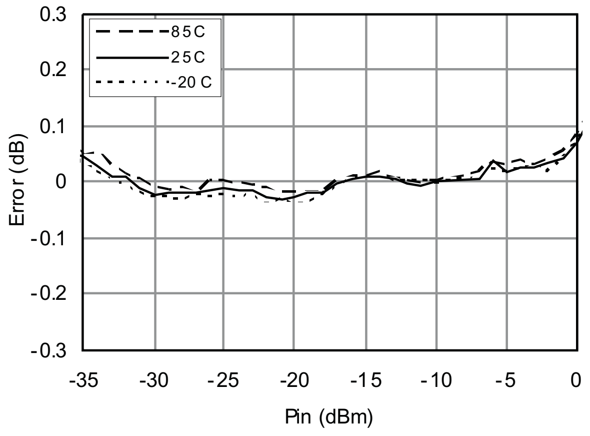

1-dB LOG CONFORMANCE ERROR AT 800 MHz

Figure 5.

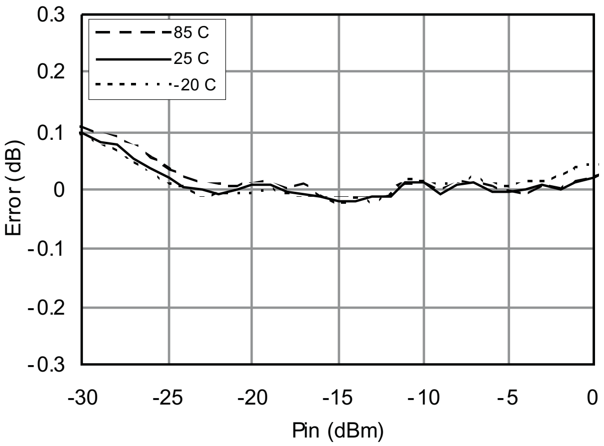

1-dB LOG CONFORMANCE ERROR AT 2 GHz

Figure 6.

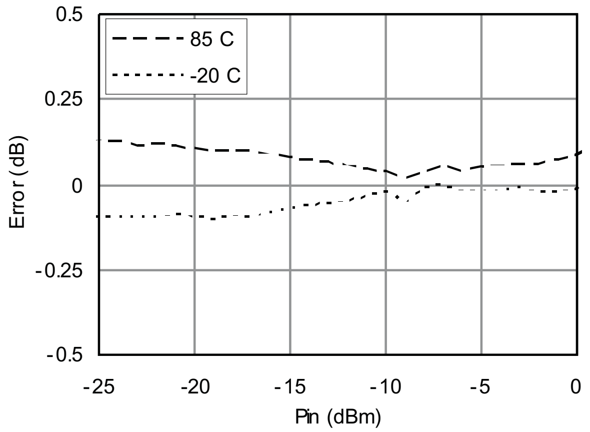

10-dB LOG CONFORMANCE ERROR AT 800 MHz

Figure 7.

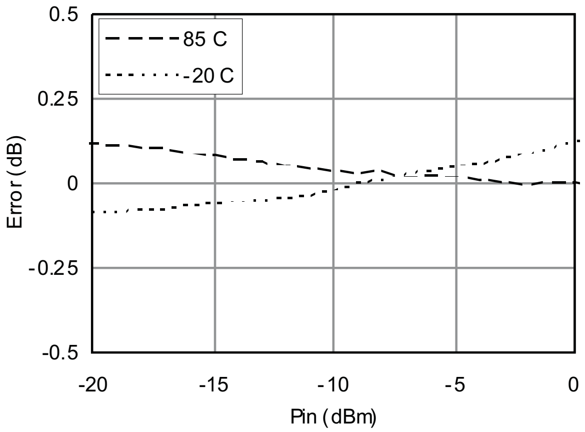

10-dB LOG CONFORMANCE ERROR AT 2 GHz

Figure 8.

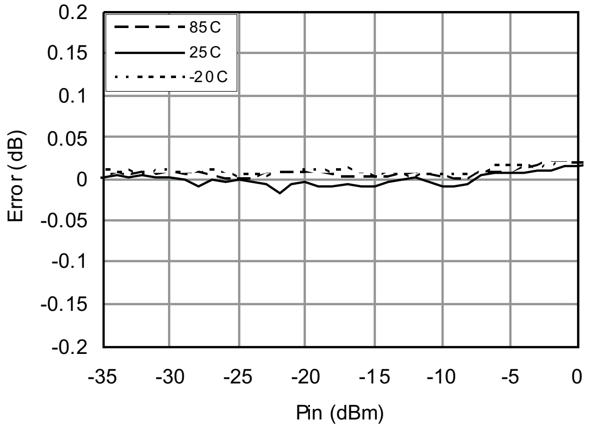

DEVIATION DUE TO MODULATION
(Reference Measurement Channel 12.2,
3GPP TS 34.121-1 V8.7.0, Table C2.1.1, 800 MHz)

Figure 9.

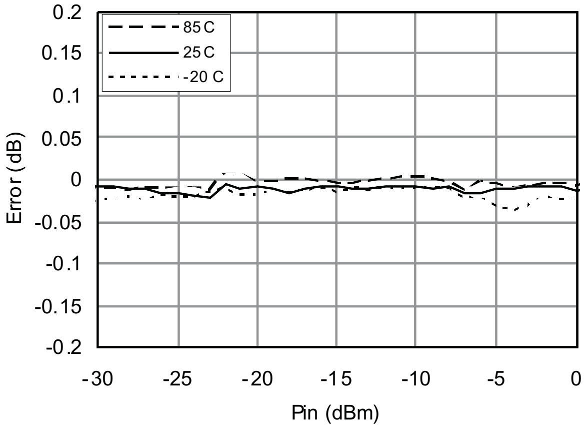

DEVIATION DUE TO MODULATION
(Reference Measurement Channel 12.2,
3GPP TS 34.121-1 V8.7.0, Table C2.1.1, 2 GHz

Figure 10.

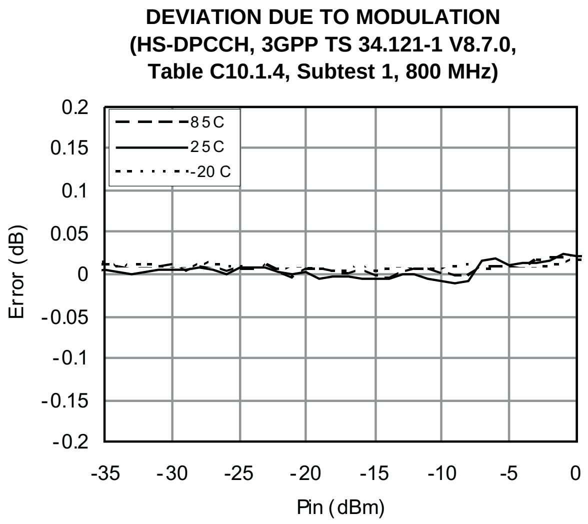

DEVIATION DUE TO MODULATION (HS-DPCCH, 3GPP TS 34.121-1 V8.7.0, Table C10.1.4, Subtest 1, 800 MHz)

Figure 11.

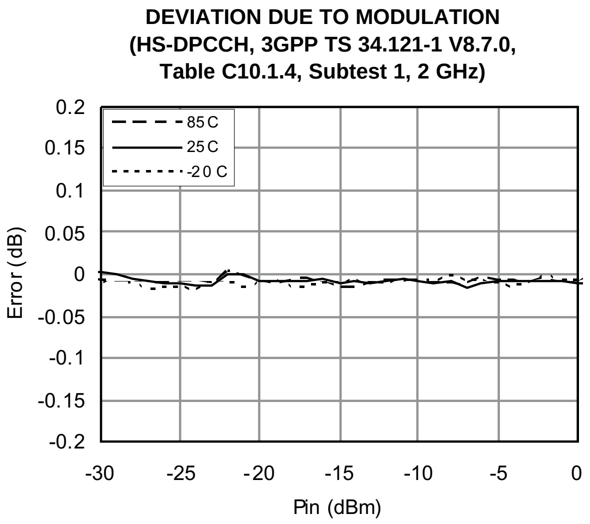

DEVIATION DUE TO MODULATION (HS-DPCCH, 3GPP TS 34.121-1 V8.7.0, Table C10.1.4, Subtest 1, 2 GHz)

Figure 12.

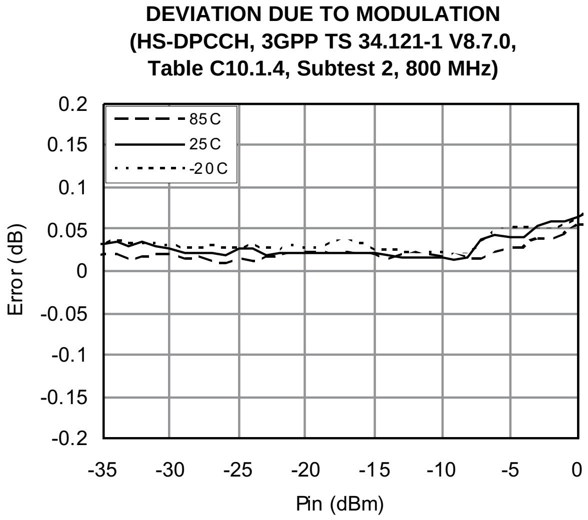

DEVIATION DUE TO MODULATION (HS-DPCCH, 3GPP TS 34.121-1 V8.7.0, Table C10.1.4, Subtest 2, 800 MHz)

Figure 13.

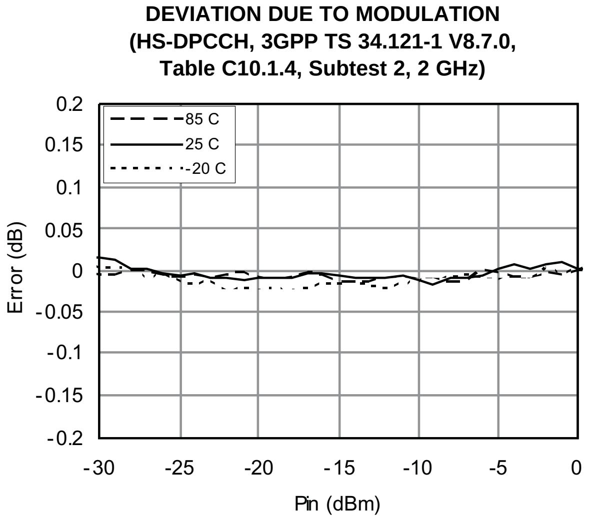

DEVIATION DUE TO MODULATION (HS-DPCCH, 3GPP TS 34.121-1 V8.7.0, Table C10.1.4, Subtest 2, 2 GHz)

Figure 14.

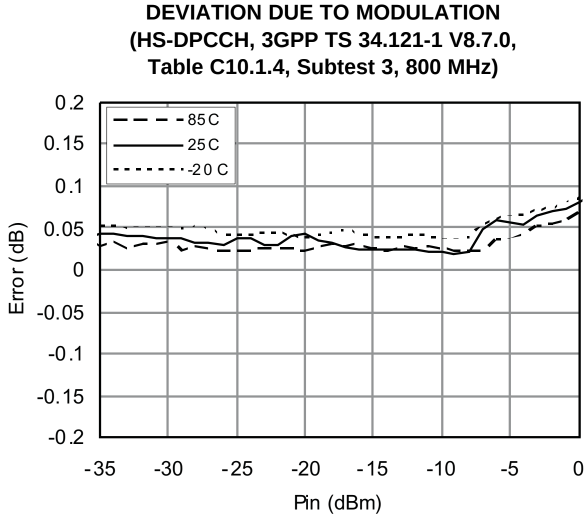

DEVIATION DUE TO MODULATION (HS-DPCCH, 3GPP TS 34.121-1 V8.7.0, Table C10.1.4, Subtest 3, 800 MHz)

Figure 15.

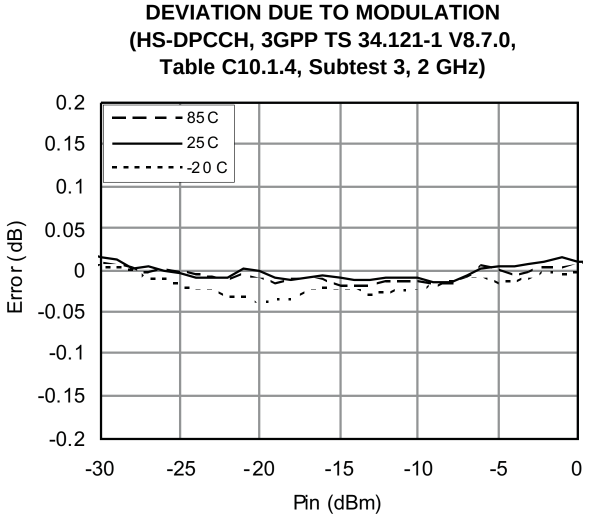

DEVIATION DUE TO MODULATION (HS-DPCCH, 3GPP TS 34.121-1 V8.7.0, Table C10.1.4, Subtest 3, 2 GHz)

Figure 16.

DEVIATION DUE TO MODULATION (HS-DPCCH, 3GPP TS 34.121-1 V8.7.0, Table C10.1.4, Subtest 4, 800 MHz)

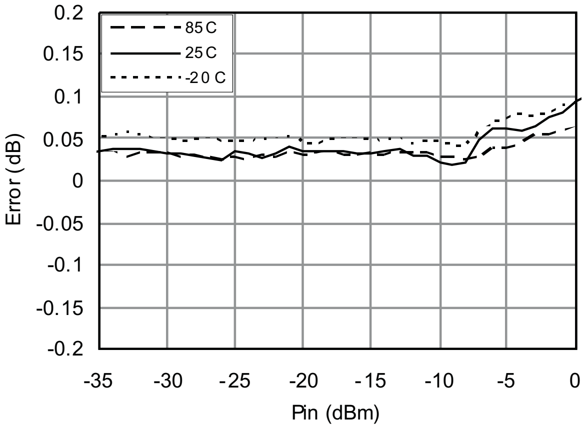


Figure 17.

DEVIATION DUE TO MODULATION (HS-DPCCH, 3GPP TS 34.121-1 V8.7.0, Table C10.1.4, Subtest 4, 2 GHz)

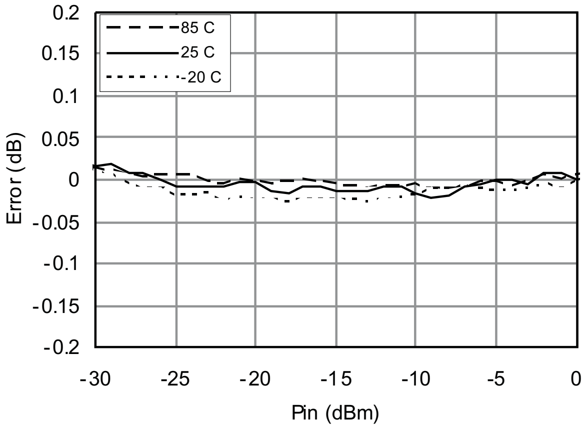


Figure 18.

DEVIATION DUE TO MODULATION (HS-DPCCH and E-DCH, 3GPP TS 34.121-1 V8.7.0, Table C11.1.3, Subtest 1, 800 MHz)

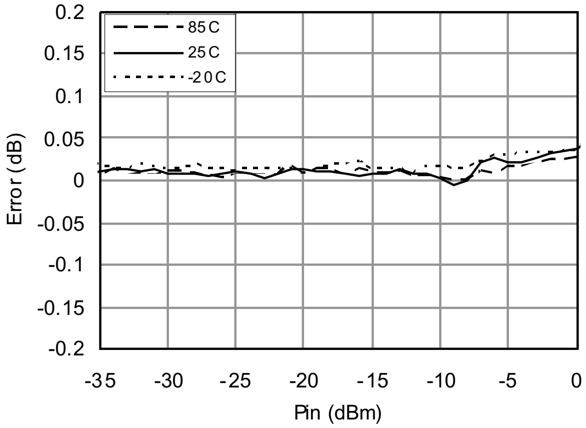


Figure 19.

DEVIATION DUE TO MODULATION (HS-DPCCH and E-DCH, 3GPP TS 34.121-1 V8.7.0, Table C11.1.3, Subtest 1, 2 GHz)

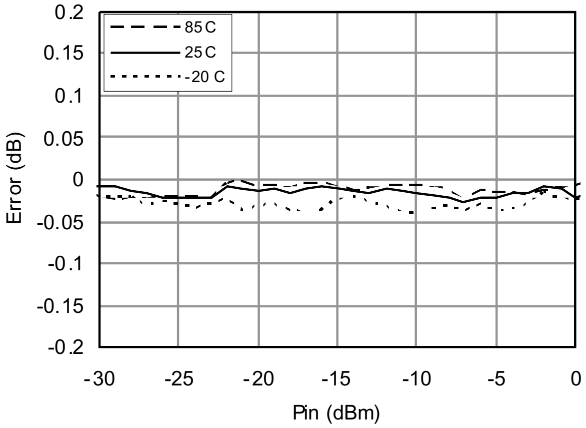


Figure 20.

DEVIATION DUE TO MODULATION (HS-DPCCH and E-DCH, 3GPP TS 34.121-1 V8.7.0, Table C11.1.3, Subtest 2, 800 MHz)

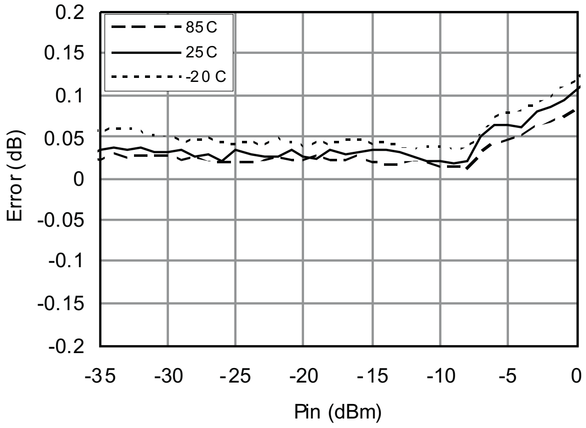


Figure 21.

DEVIATION DUE TO MODULATION (HS-DPCCH and E-DCH, 3GPP TS 34.121-1 V8.7.0, Table C11.1.3, Subtest 2, 2 GHz)

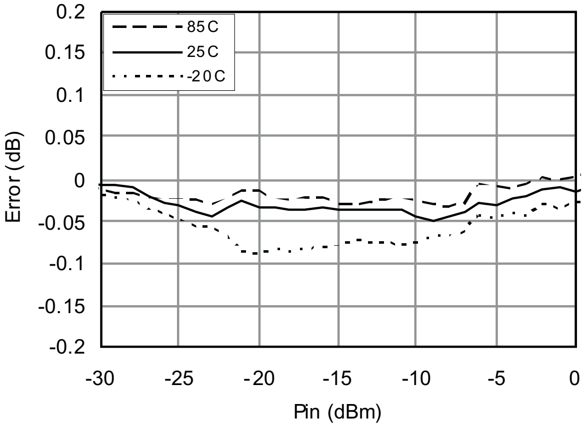


Figure 22.

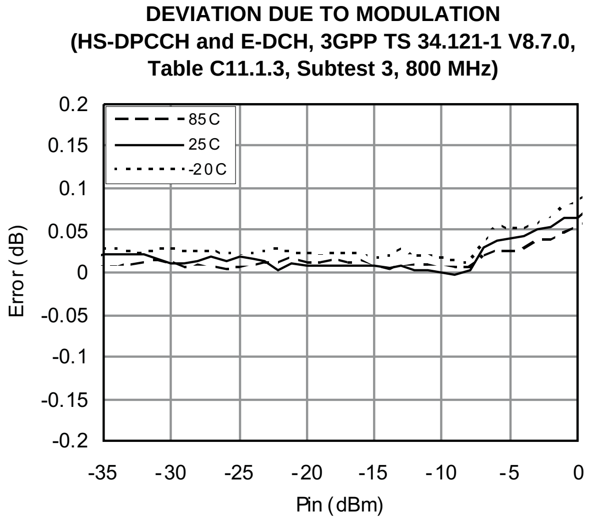


Figure 23.

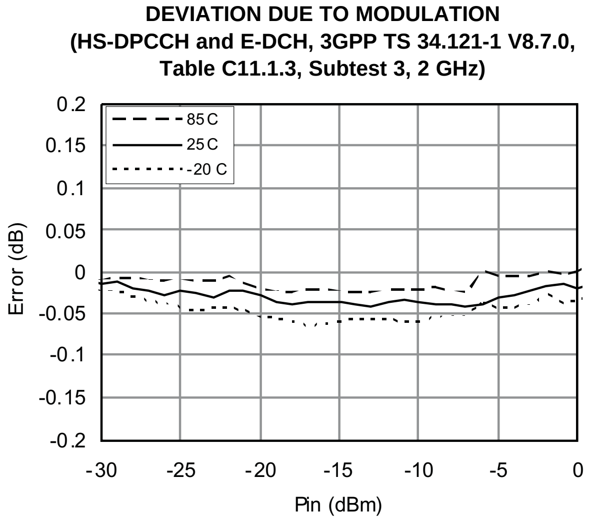


Figure 24.

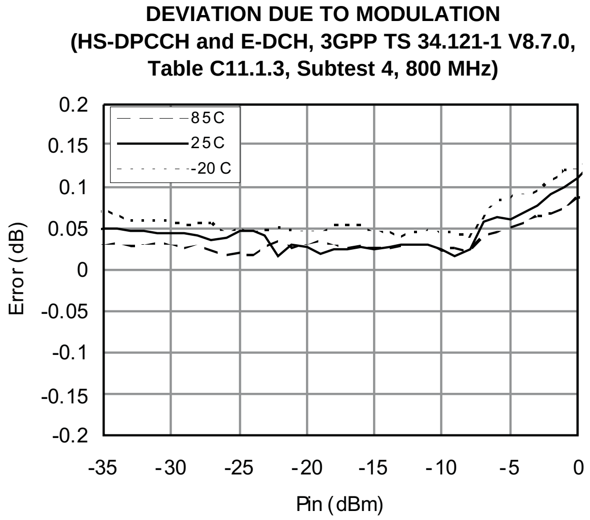


Figure 25.

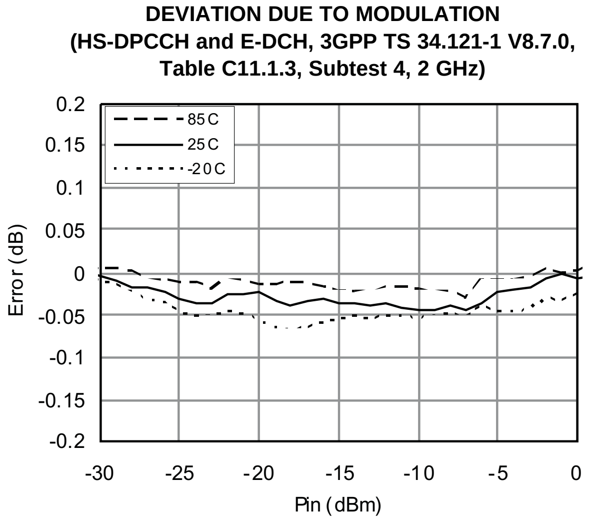


Figure 26.

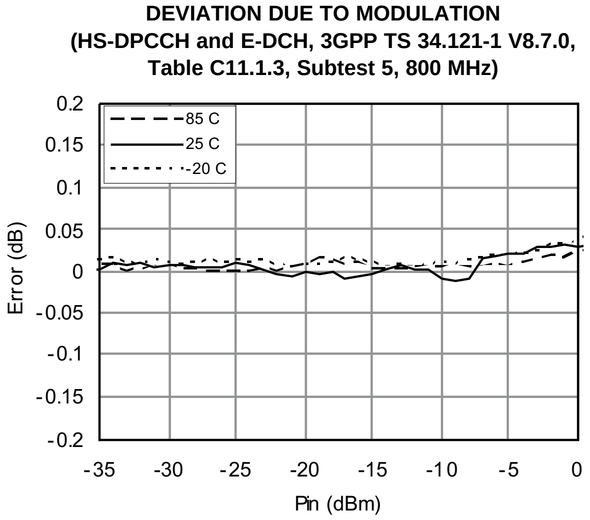


Figure 27.

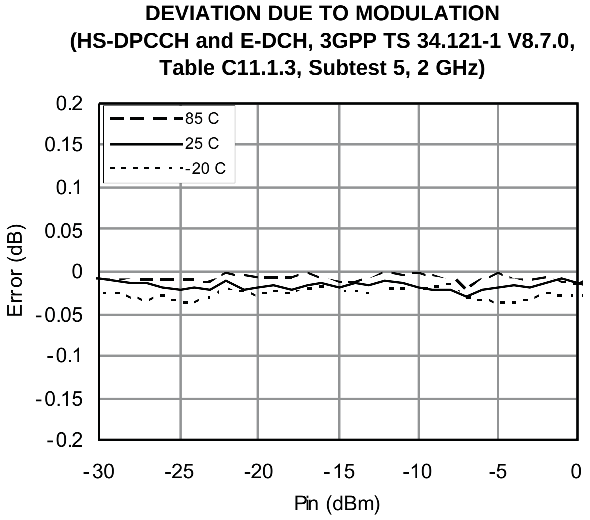


Figure 28.

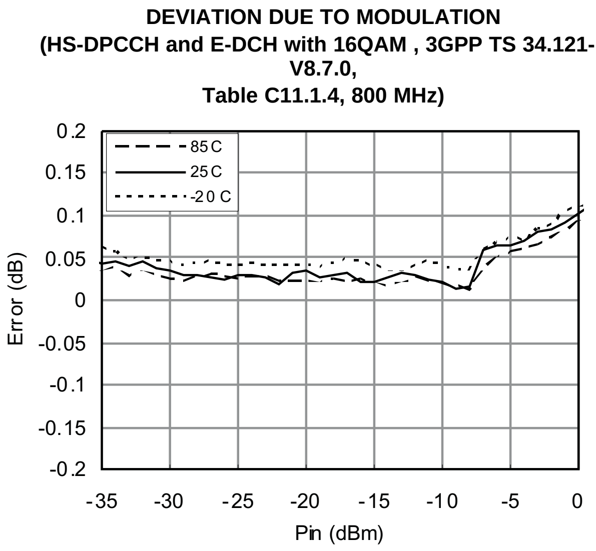


Figure 29.

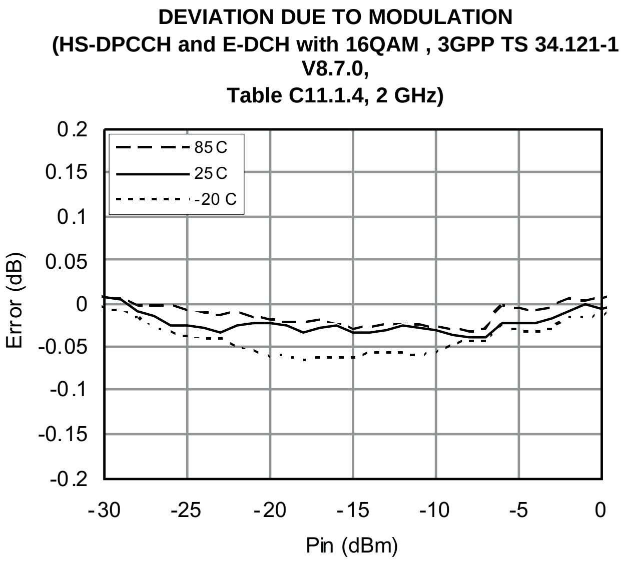
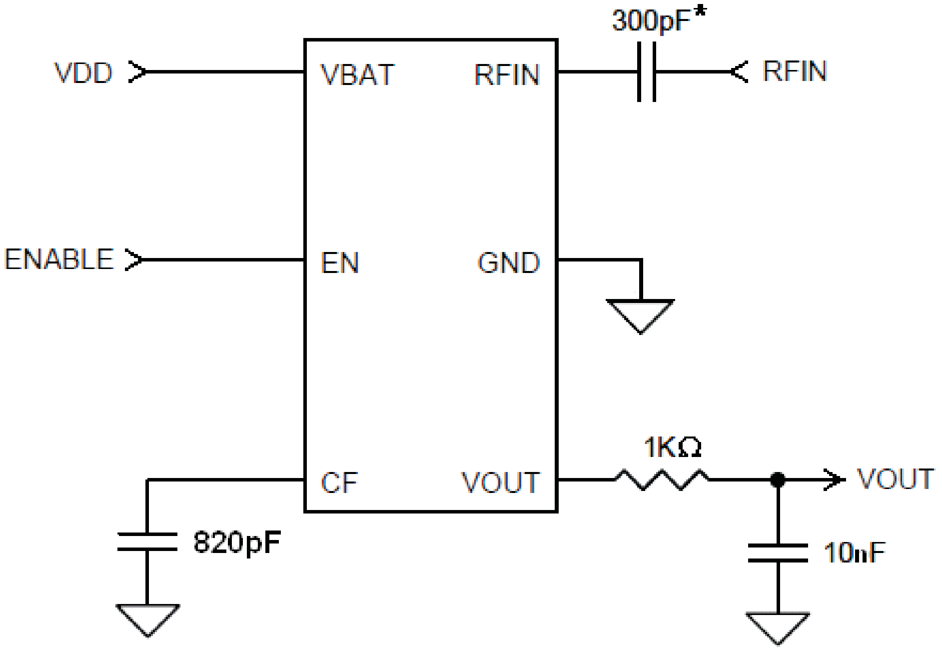


Figure 30.



*The input coupling capacitor on the RF input pin may be omitted if the DC voltage on this pin is at ground.

Figure 31. Application Circuit

APPENDIX A: MEASUREMENT PROCEDURES

10-dB Log Conformance Error Over Temperature

The 10-dB log conformance error over temperature is a measure of the change in slope of the rms detector output over temperature. The measurement is performed by taking an ideal 10-dB step in input power with a CW signal at room temperature and measuring the change in output voltage. The measurement is then repeated at a different temperature and the 10-dB log conformance error over temperature is given in dB by Equation 1.

$$10\text{-}dB\ log\ conformance\ error = 10 \bullet \left(\frac{\Delta V_{OUT}\,(T)}{\Delta V_{OUT}\,(25°C)} - 1 \right) \tag{1}$$

This measurement is taken on a statistical sample of parts. The 3σ limits from these samples are within the limits provided in the Electrical Characteristics table.

Straight Line 5-dB Step Error

The straight line 5-dB step error is a measure of the maximum error that results from fitting a straight line between two points of a 5-dB step as shown in Figure 32. The straight line shown in bold represents a perfect 5-dB step, while the curved line represents the detector output (the curvature in this figure is exaggerated for explanation purposes). The maximum difference output voltage between these two curves is the straight line 5-dB step error.

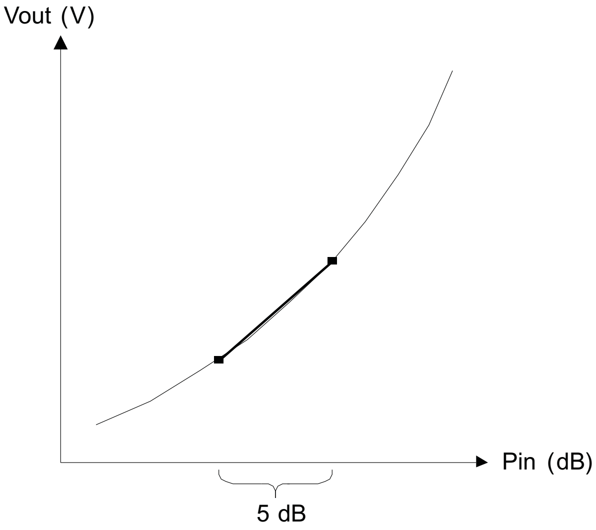


Figure 32. Straight Line 5-dB Step Error

Response Temperature Coefficient & Response Temperature Sensitivity Spread - 1σ

The response temperature coefficient is a measure of the change in detector output voltage for a given RF input power. The measurement is performed by measuring the detector output voltage over temperature for a set CW RF input power. The response temperature gain coefficient expressed in mdB/°C is given by Equation 2.

$$Response\ temperature\ gain\ coefficient = 1000 \bullet \frac{\Delta V_{OUT}}{V_{OUT,GAIN} \bullet \Delta T} \tag{2}$$

Where $V_{OUT,GAIN}$ is the output voltage gain expressed in V/dB. This measurement is taken on a statistical sample of parts. The mean of these samples are provided in the Electrical Characteristics table.

The response temperature sensitivity spread - 1σ, ΔTC_{VOUT}, is the 1σ variation in TC_{VOUT}.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TRF1600DRVR	PREVIEW	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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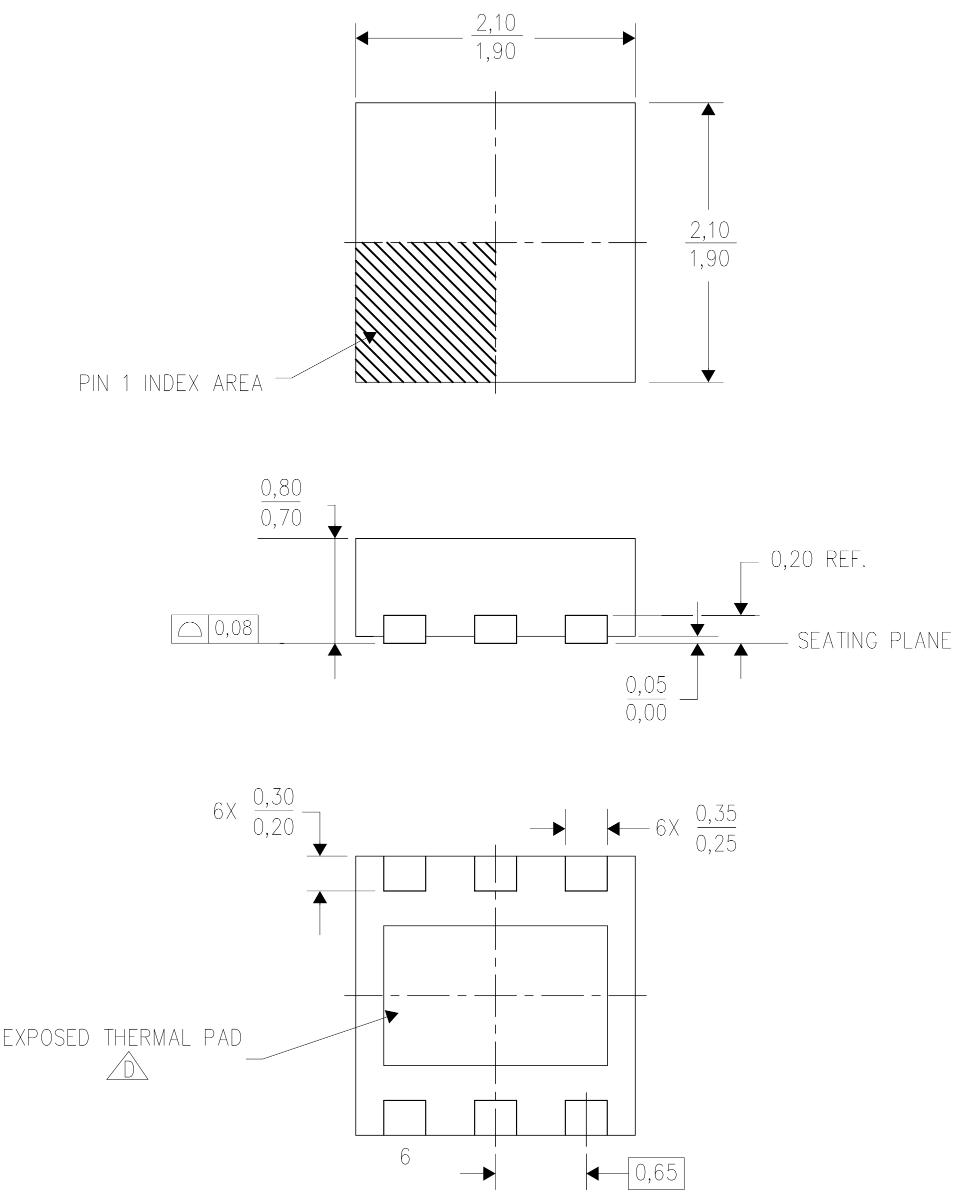
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4206925/E 10/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Small Outline No–Lead (SON) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

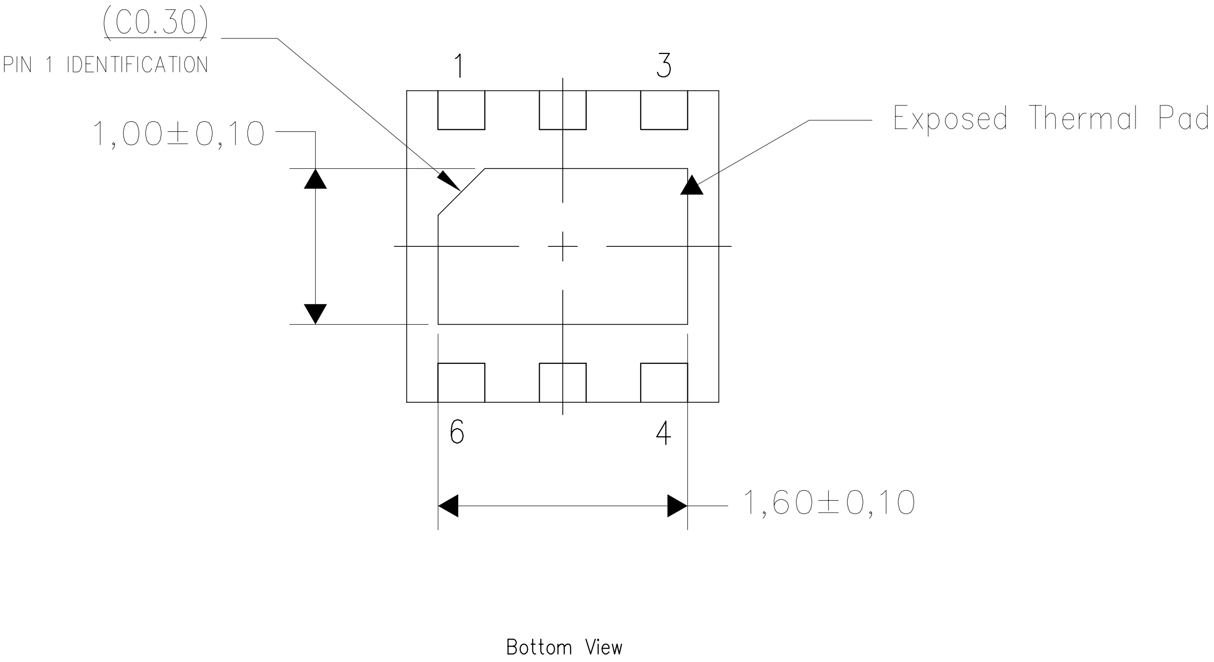
DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

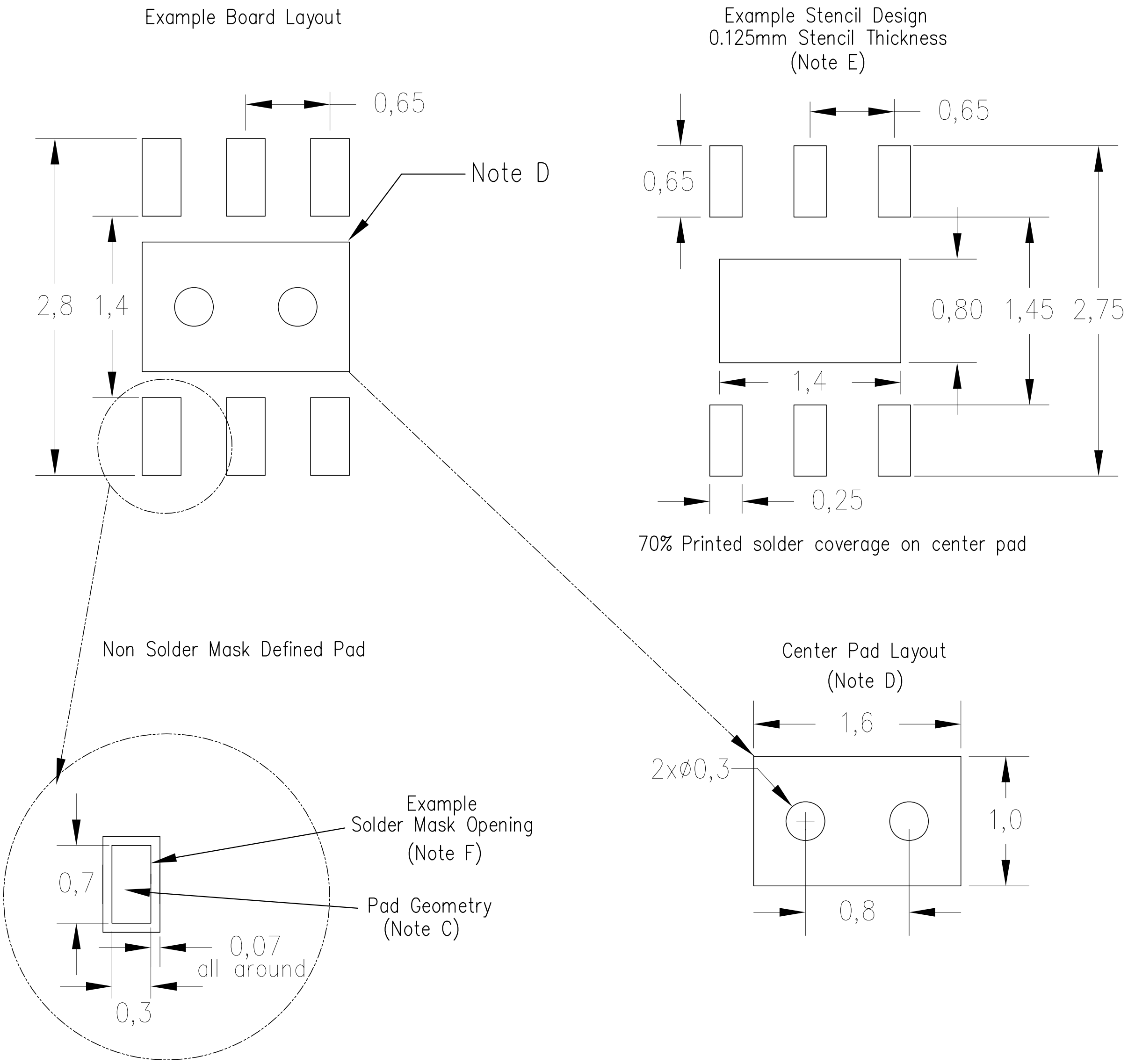


Exposed Thermal Pad Dimensions

4206926–2/L 11/11

NOTE: A. All linear dimensions are in millimeters

DRV (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



4207812/F 04/11

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC–7351 is recommended for alternate designs.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.

F. Customers should contact their board fabrication site for solder mask tolerances.

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