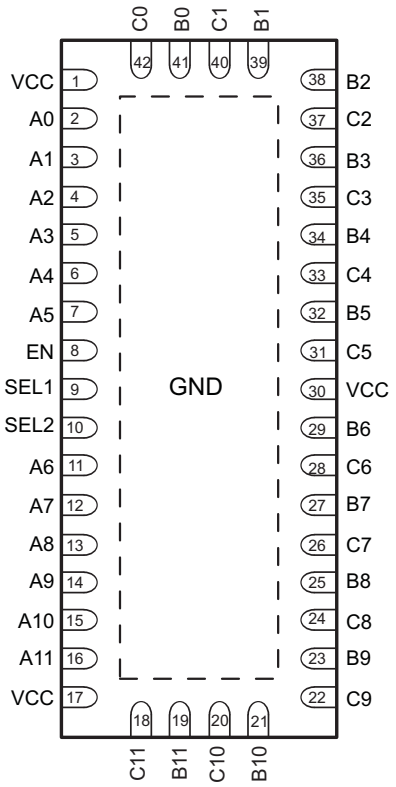
适用于 DDR3 应用的 12 通道、1:2 多路复用器 / 多路解复用器开关

查询样品: TS3DDR3812

特性

- 符合 **DDR3 SDRAM** 标准 **(JESD79-3D)**
- **1.675 GHz** 的高带宽
- 低传播延迟（t_{pd} **= 40 ps** 典型值）
- 低位与位间时滞（$t_{sk(o)}$ **= 6 ps** 最大值）
- 低而平坦的导通阻抗
  （r_{ON} **= 8 Ω** 典型值）
- 低输入 / 输出电容
  （C_{ON} **= 5.6 pF** 典型值）
- 低串扰 （在 **250 MHz** 典型值下，$_{X}$**TALK = –43 dB**）
- V_{CC} 工作范围：**3 V** 至 **3.6 V**
- 数据 **I/O** 端口上的轨至轨开关
  （**0** 至V_{CC}）
- 分离开关控制逻辑支持上限及下限 **6** 通道
- 专用启用逻辑支持 **Hi-Z** 模式
- I_{OFF} 保护可在断电状态 （V_{CC} **= 0 V**）下防止漏电
- 每个 **JESD22** 的 **ESD** 性能测试
  - **2000 V** 人体模式
    （**A114B**、**Class II**）
  - **1000 V** 带电器件模式 **(C101)**
- **42** 引脚 **RUA** 封装 （**9 × 3.5** 毫米、**0.5** 毫米间距）

图 **1. RUA** 封装
（俯视图）



应用

- **DDR3** 信号开关
- **DIMM** 模块
- 笔记本 / 台式机
- 服务器

说明

TS3DDR3812 是一款专门针对 DDR3 应用而设计的 12 通道、1:2 多路复用器 / 多路解复用器开关。 该产品采用 3 至 3.6 V 电源供电，支持低而平坦的导通阻抗以及低 I/O 电容，可实现 1.675 GHz 的典型带宽。

通道 A_0 通过 A_{11} 分为两个 6 位组，可通过两组称之为 SEL1 与 SEL2 的数字输入进行独立控制。 这些选择输入可控制每个 6 位 DDR3 信号源的开关位置，使它们能够准确发送至两个终点中的一个。 此外， 本开关还可用于将单个设备与两个 6 位 DDR3 信号源中的一个连接起来。 对于 12 位 DDR3 信号源的开关，只需外部连接 SEL1 与 SEL2，便可通过 GPIO 输入控制所有 12 个通道。 EN 输入可在不使用时使整个芯片处于高阻抗 (Hi-Z) 状态。

这些特性使 TS3DDR3812 理想适用于存储器、模拟 / 数字视频、LAN 以及其它高速信号开关应用。

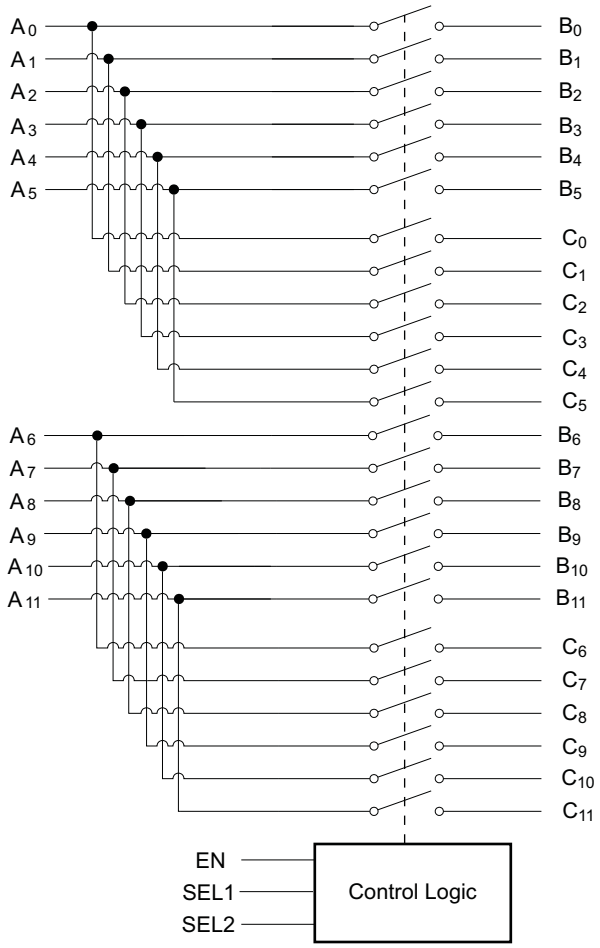
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN - RUA	Tape and Reel	TS3DDR3812RUAR	SL812

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Figure 2. LOGIC DIAGRAM



FUNCTION TABLE

EN	SEL1	SEL2	FUNCTION
L	X	X	A_0 to A_{11}, B_0 to B_{11}, and C_0 to C_{11} are Hi-Z
H	L	L	A_0 to A_5 = B_0 to B_5 and A_6 to A_{11} = B_6 to B_{11}
H	L	H	A_0 to A_5 = B_0 to B_5 and A_6 to A_{11} = C_6 to C_{11}
H	H	L	A_0 to A_5 = C_0 to C_5 and A_6 to A_{11} = B_6 to B_{11}
H	H	H	A_0 to A_5 = C_0 to C_5 and A_6 to A_{11} = C_6 to C_{11}

TERMINAL FUNCTIONS

PIN		DESCRIPTION
NAME	NUMBER	
V_{CC}	1,17, 30	Supply Voltage
GND	ThermalPad	Ground
EN	8	Enable Input
SEL1	9	Select Input
SEL2	10	Select Input
A_0, A_1, A_2, A_3, A_4, A_5, A_6, A_7, A_8, A_9, A_{10}, A_{11}	2, 3, 4, 5, 6, 7, 11, 12, 13, 14, 15, 16	Data I/Os
B_0, B_1, B_2, B_3, B_4, B_5, B_6, B_7, B_8, B_9, B_{10}, B_{11}	41, 39, 38, 36, 34, 32, 29, 27, 25, 23, 21, 19	Data I/Os
C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}	42, 40, 37, 35, 33, 31, 28, 26, 24, 22, 20, 18	Data I/Os

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
$V_{I/O}$	Analog voltage range(2)(3)(4)	A, B, C	–0.5	7	V
V_{IN}	Digital input voltage range(2)(3)	SEL1, SEL2	–0.5	7	V
$I_{I/OK}$	Analog port diode current	$V_{I/O}$ < 0		–50	mA
I_{IK}	Digital input clamp current	V_{IN} < 0		–50	mA
$I_{I/O}$	On-state switch current(5)	A, B, C	–128	128	mA
I_{DD}, I_{GND}	Continuous current through V_{DD} or GND		–100	100	mA
θ_{JA}	Package thermal impedance(6)	RUA package		31.8	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		3	3.6	V
V_{IH}	High-level control input voltage	SEL1, SEL2	2	5.5	V
V_{IL}	Low-level control input voltage	SEL1, SEL2	0	0.8	V
V_{IN}	Input voltage	SEL1, SEL2	0	5.5	V
$V_{I/O}$	Input/Output voltage		0	V_{CC}	V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS(1)	MIN	TYP(2)	MAX	UNIT
V_{IK}	Digital input clamp voltage	SEL1, SEL2	V_{CC} = 3.6 V, I_{IN} = –18 mA	–1.2	–0.8		V
R_{ON}	ON-state resistance	A, B, C	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = -40 mA		8	12	Ω
$R_{ON(flat)}$(3)	ON-state resistance flatness	A, B, C	V_{CC} = 3 V, $V_{I/O}$ = 1.5 V and V_{CC}, $I_{I/O}$ = –40 mA		1.5		Ω
ΔR_{ON}(4)	On-state resistance match between channels	A, B, C	V_{CC} = 3 V, 1.5 V ≤ $V_{I/O}$ ≤ V_{CC}, $I_{I/O}$ = –40 mA		0.4	1	Ω
I_{IH}	Digital input high leakage current	SEL1, SEL2	V_{CC} = 3.6 V , V_{IN} = V_{DD}			±1	µA
I_{IL}	Digital input low leakage current	SEL1, SEL2	V_{CC} = 3.6 V, V_{IN} = GND			±1	µA
I_{OFF}	Leakage under power off conditions	All outputs	V_{CC} = 0 V, $V_{I/O}$ = 0 to 3.6 V, V_{IN} = 0 to 5.5 V			±1	µA
C_{IN}	Digital input capacitance	SEL1, SEL2	f = 1 MHz, V_{IN} = 0 V		2.6	3.2	pF
C_{OFF}	Switch OFF capacitance	A, B, C	f = 1 MHz, $V_{I/O}$ = 0 V, Output is open, Switch is OFF		2		pF
C_{ON}	Switch ON capacitance	A, B, C	f = 1 MHz, $V_{I/O}$ = 0 V, Output is open, Switch is ON		5.6		pF
I_{CC}	V_{CC} supply current		V_{CC} = 3.6 V, $I_{I/O}$ = 0, V_{IN} = V_{DD} or GND		300	400	µA

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs
(2) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C
(3) $R_{ON(FLAT)}$ is the difference of R_{ON} in a given channel at specified voltages.
(4) ΔR_{ON} is the difference of R_{ON} from center port (A_5, A_6) to any other ports.

SWITCHING CHARACTERISTICS

Over recommended operation free-air temperature range, V_{CC} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 4 pF (unless otherwise noted) (see Figure 8 and Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	A or B,C	B,C or A		40		ps
t_{PZH}, t_{PZL}	SEL1	A_{0-5} or B_{0-5}, C_{0-5}	2		7	ns
	SEL2	A_{6-11} or B_{6-11}, C_{6-11}	2		7	ns
t_{PHZ}, t_{PLZ}	SEL1	A_{0-5} or B_{0-5}, C_{0-5}	2		5	ns
	SEL2	A_{6-11} or B_{6-11}, C_{6-11}	2		5	ns
$t_{sk(o)}$(3)	A or B,C	B, C or A		6	30	ps
$t_{sk(p)}$(4)	A or B, C	B, C or A		6	30	ps

(1) All typical values are at V_{CC} = 3.3V (unless otherwise noted), T_A = 25°C.
(2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port (A_5, A_6) and any other channel.
(4) Skew between opposite transitions of the same output $|t_{PHL} - t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP(1)	UNIT
X_{TALK}	R_L = 50 Ω, f = 250 MHz (see Figure 12)	–43	dB
O_{IRR}	R_L = 50 Ω, f = 250 MHz (see Figure 13)	–42	dB
BW	R_L = 50 Ω, Switch ON (see Figure 11)	1.675	GHz

(1) All Typical Values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.

OPERATING CHARACTERISTICS

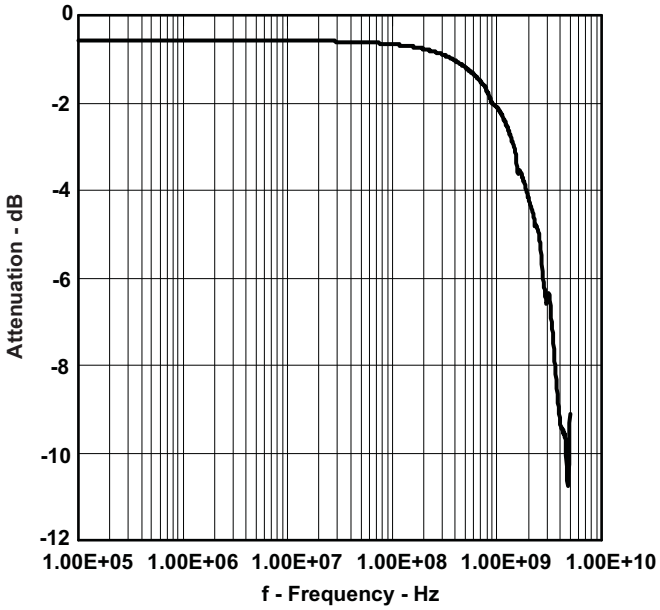


Figure 3. Gain vs Frequency

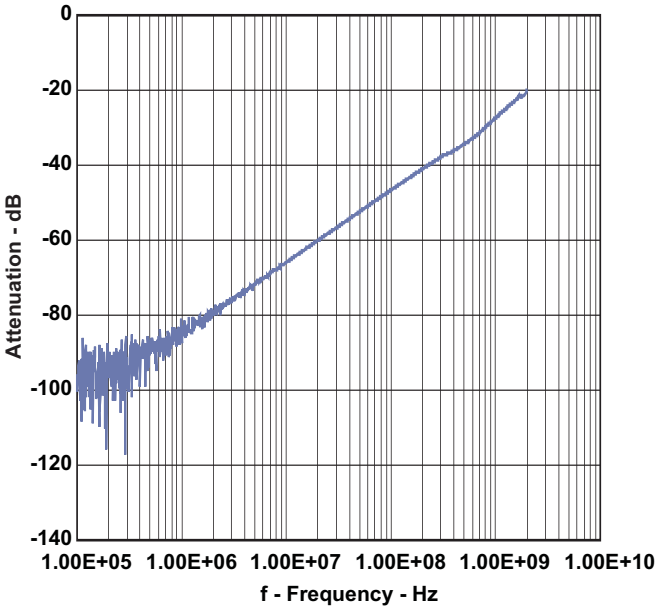


Figure 4. Off Isolation vs Frequency

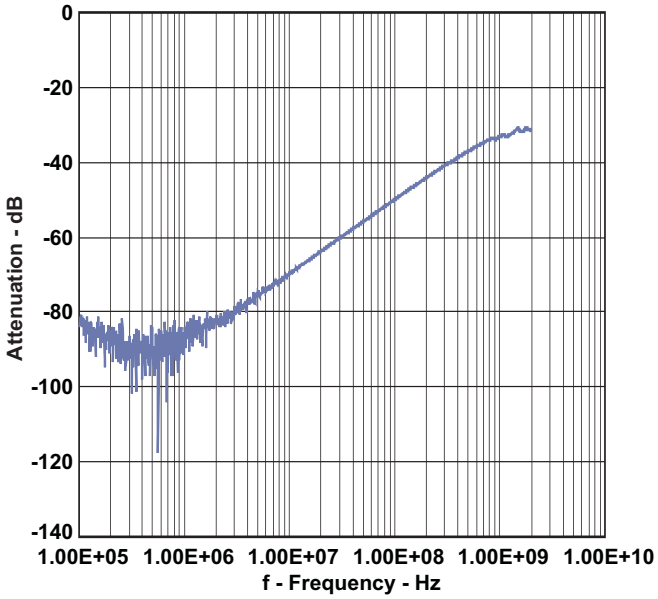


Figure 5. Crosstalk vs Frequency

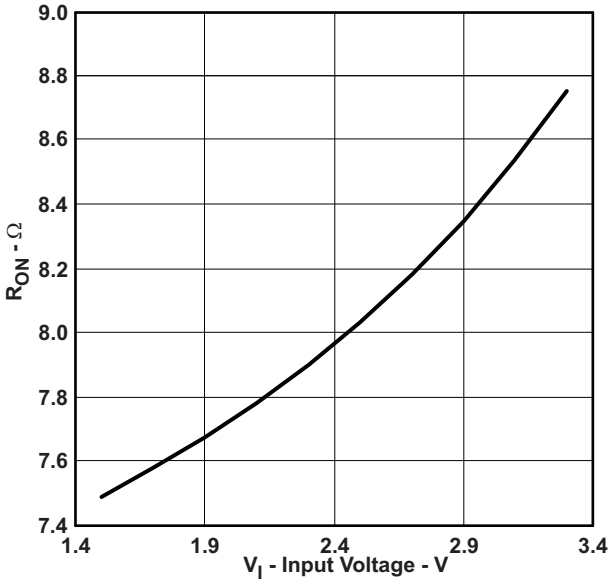
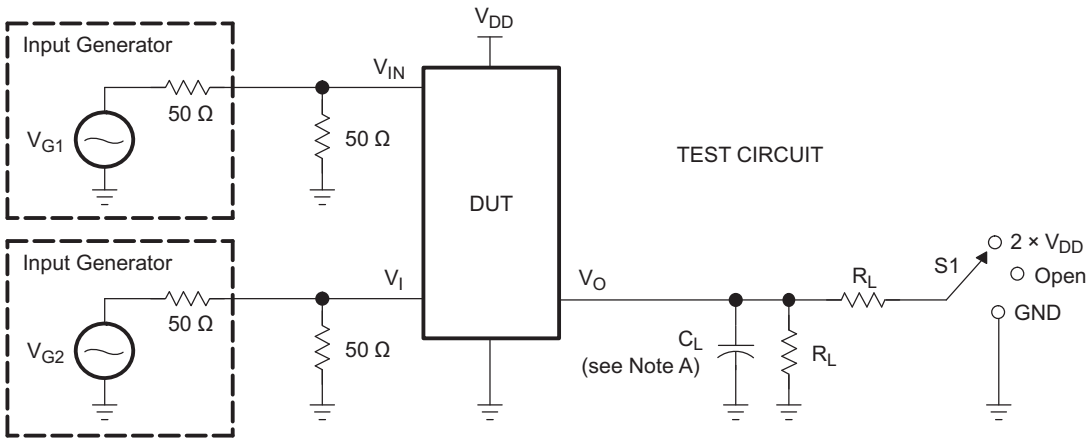


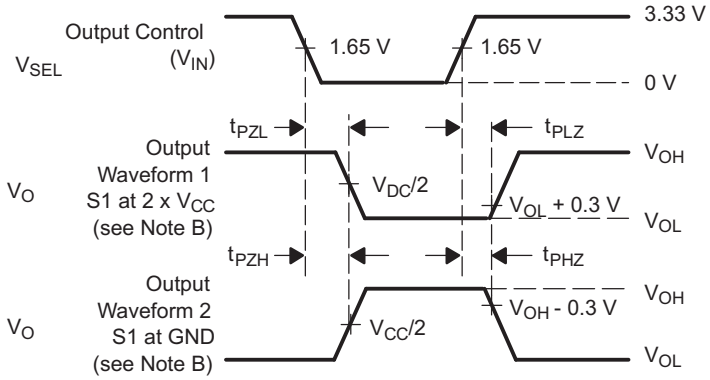
Figure 6. R_{ON} vs V_{IN}

PARAMETER MEASUREMENT INFORMATION

Figure 7. Enable and Disable Times



TEST	V_{DD}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ± 0.3 V	2 × V_{DD}	200 Ω	GND	4 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ± 0.3 V	GND	200 Ω	V_{DD}	4 pF	0.3 V



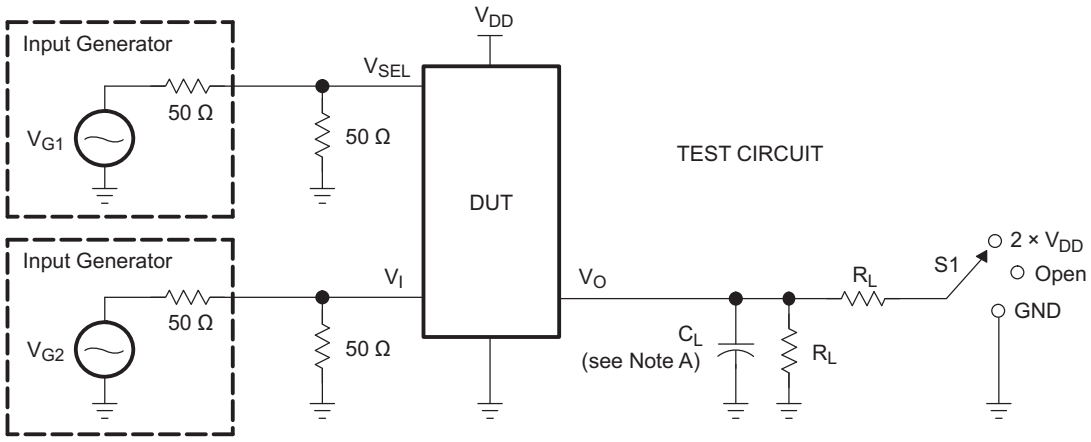
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics:PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

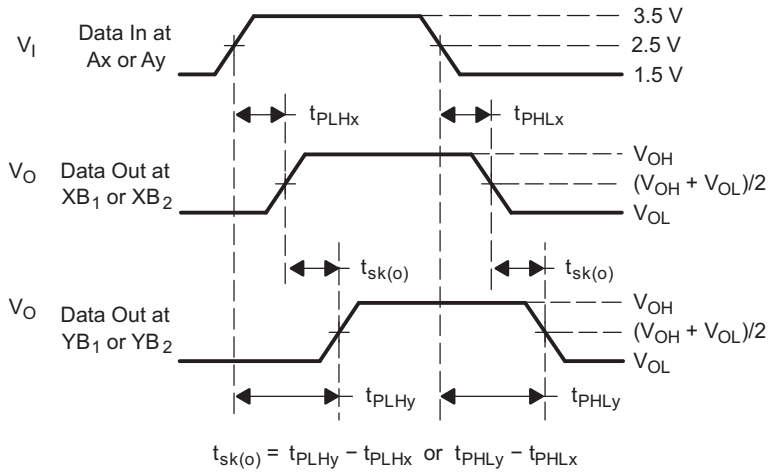
Figure 8. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

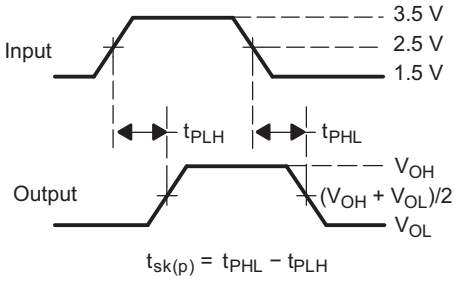
Figure 9. Skew



TEST	V_{CC}	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{CC} or GND	4 pF
$t_{sk(p)}$	3.3 V ± 0.3V	Open	200 Ω	V_{CC} or GND	4 pF



VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)



VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 10. Test Circuit andf Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

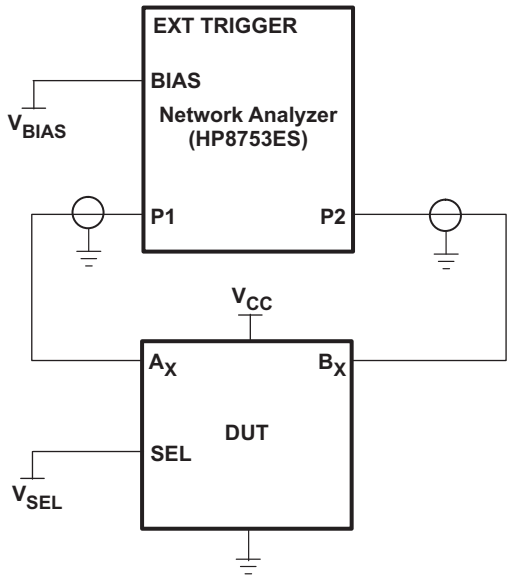


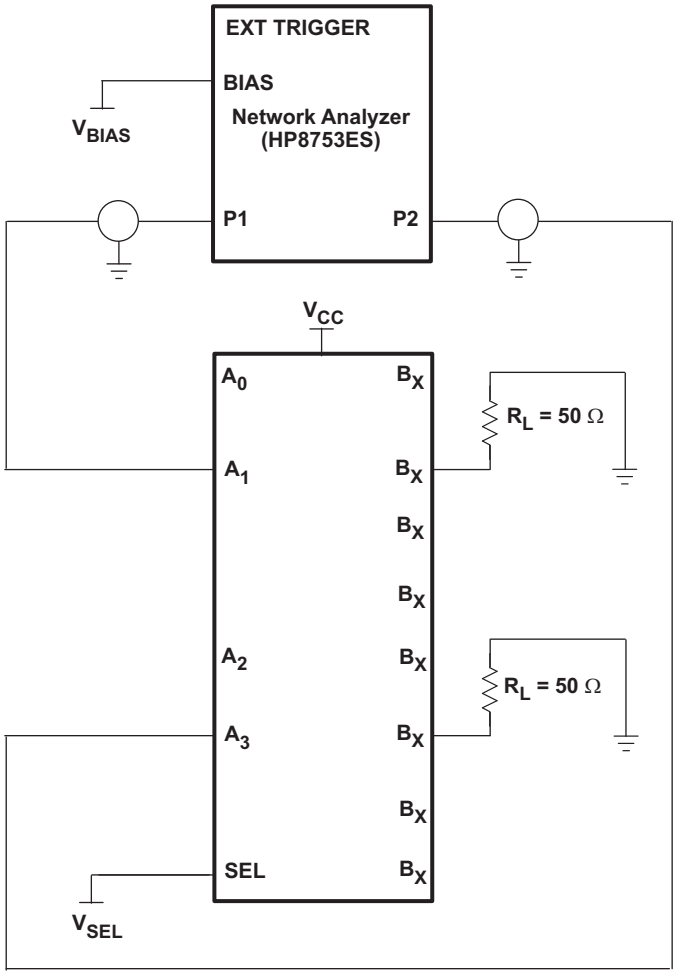
Figure 11. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at B0. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.
B. A 50 W termination resistor is needed to match the loading of the network analyzer.

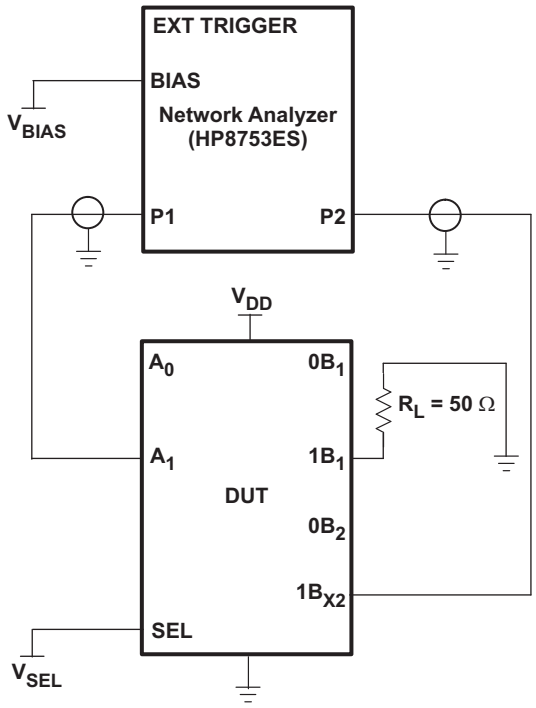
Figure 12. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.
B. A 50 W termination resistor is needed to match the loading of the network analyzer.

Figure 13. Test Circuit for OFF Isolation (O_{IRR})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = GND and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PACKAGING INFORMATION

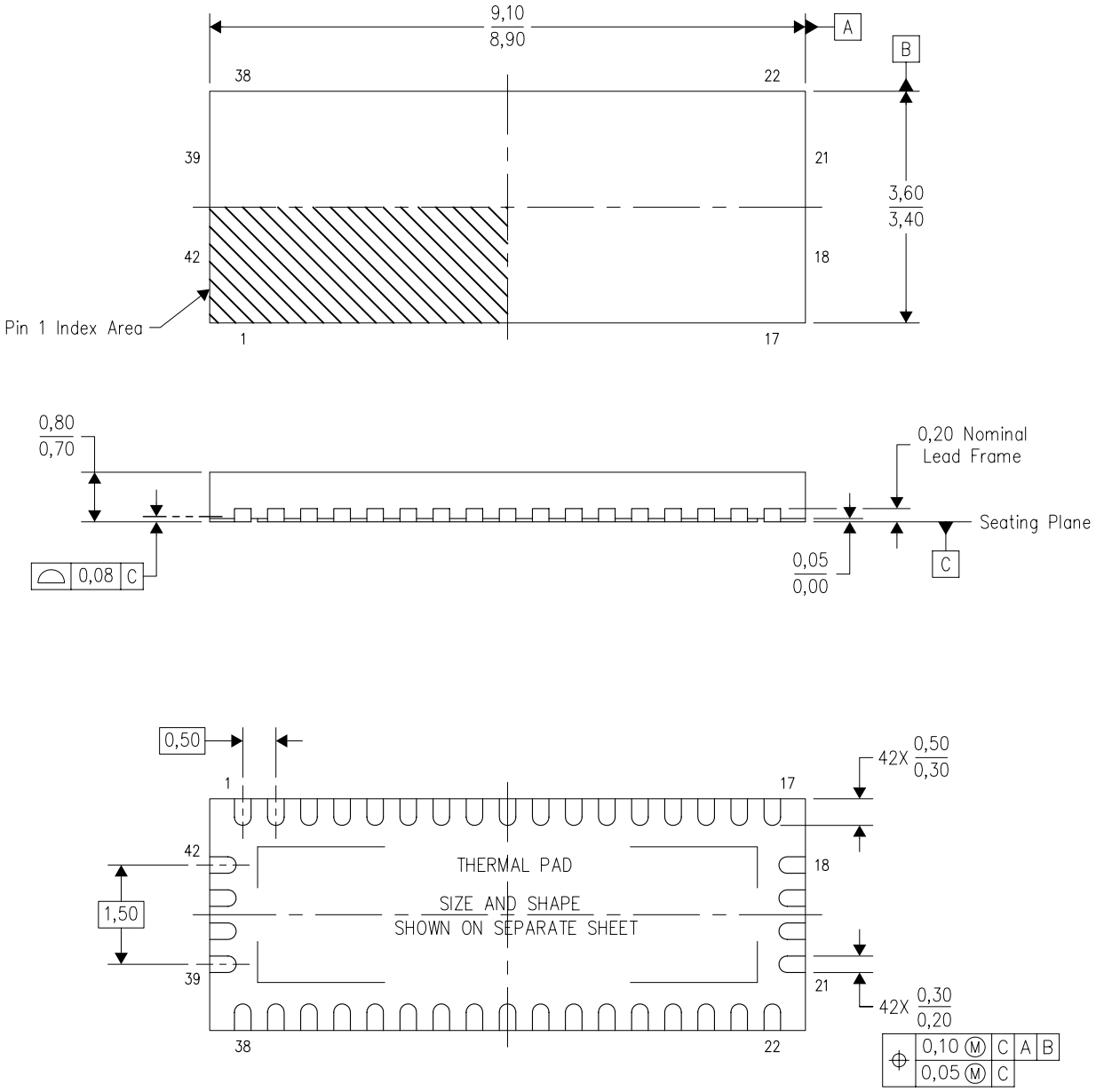
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TS3DDR3812RUAR	ACTIVE	WQFN	RUA	42	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

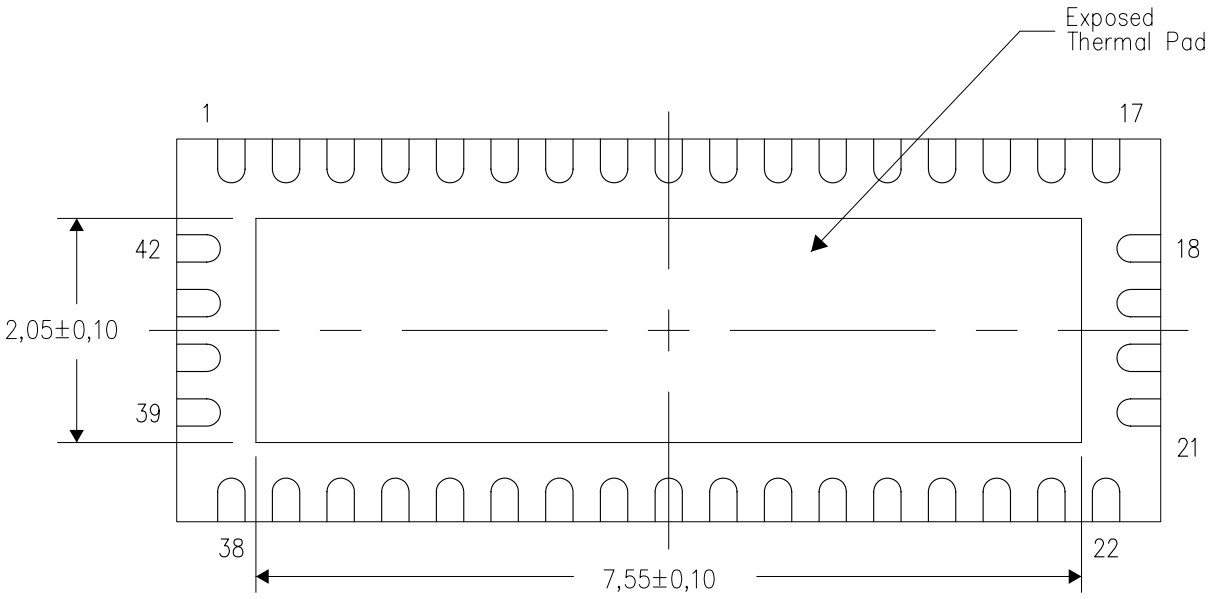
RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



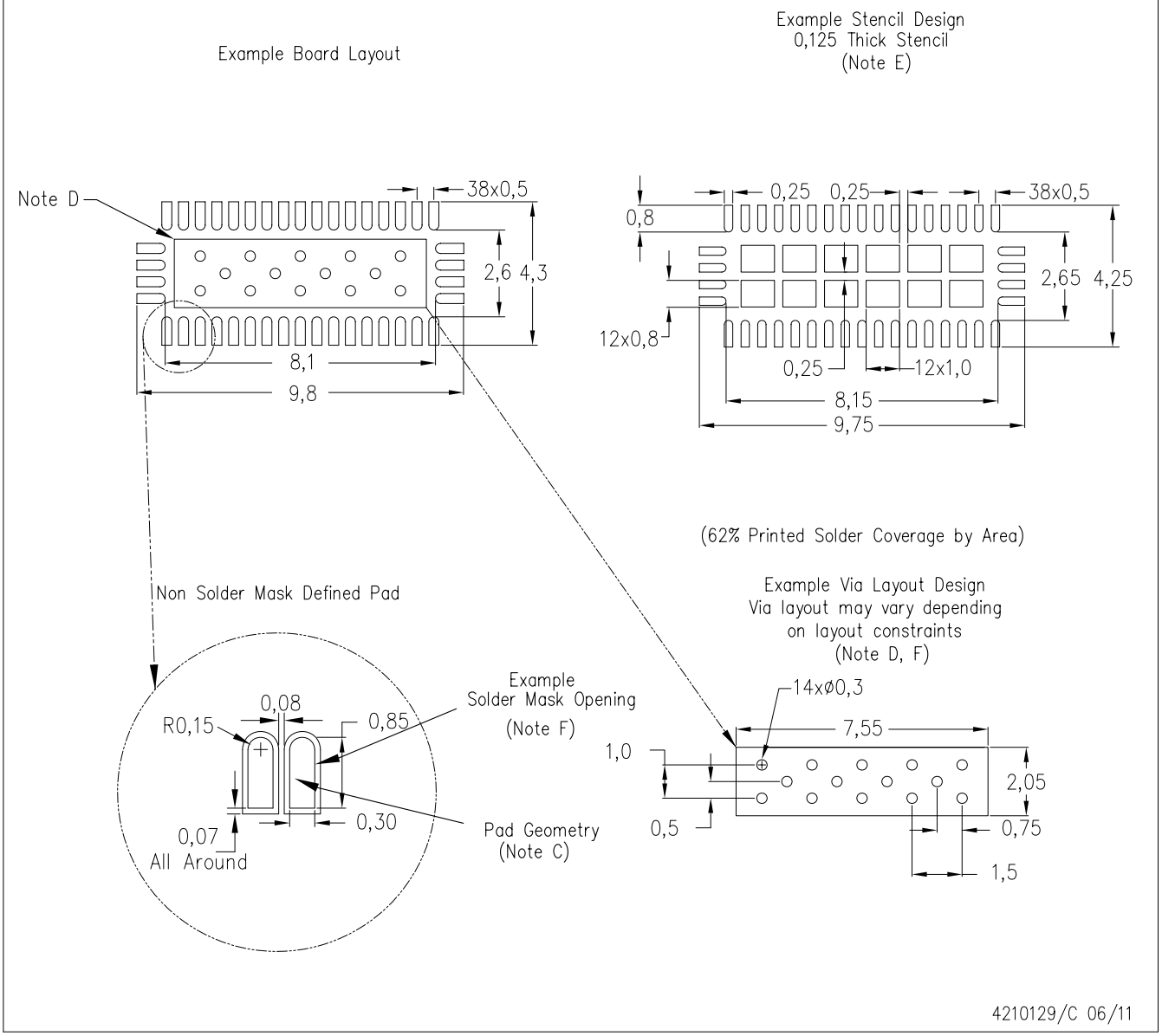
Bottom View

Exposed Thermal Pad Dimensions

4208352/D 06/11

NOTE: All linear dimensions are in millimeters

RUA (R–PWQFN–N42) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

重要声明

德州仪器(TI) 及其下属子公司有权在不事先通知的情况下, 随时对所提供的产品和服务进行更正、修改、增强、改进或其它更改，并有权随时中止提供任何产品和服务。客户在下订单前应获取最新的相关信息，并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的硬件产品的性能符合TI 标准保修的适用规范。仅在TI 保证的范围内，且TI 认为有必要时才会使用测试或其它质量控制技术。除非政府做出了硬性规定，否则没有必要对每种产品的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用TI 组件的产品和应用自行负责。为尽量减小与客户产品和应用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何TI 专利权、版权、屏蔽作品权或其它与使用了TI 产品或服务的组合设备、机器、流程相关的TI 知识产权中授予的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从TI 获得使用这些产品或服务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是TI 的专利权或其它知识产权方面的许可。

对于TI 的产品手册或数据表，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况下才允许进行复制。在复制信息的过程中对内容的篡改属于非法的、欺诈性商业行为。TI 对此类篡改过的文件不承担任何责任。

在转售TI 产品或服务时，如果存在对产品或服务参数的虚假陈述，则会失去相关TI 产品或服务的明示或暗示授权，且这是非法的、欺诈性商业行为。TI 对此类虚假陈述不承担任何责任。

TI 产品未获得用于关键的安全应用中的授权，例如生命支持应用（在该类应用中一旦TI 产品故障将预计造成重大的人员伤亡），除非各方官员已经达成了专门管控此类使用的协议。购买者的购买行为即表示，他们具备有关其应用安全以及规章衍生所需的所有专业技术和知识，并且认可和同意，尽管任何应用相关信息或支持仍可能由TI 提供，但他们将独力负责满足在关键安全应用中使用其产 品及TI 产品所需的所有法律、法规和安全相关要求。此外，购买者必须全额赔偿因在此类关键安全应用中使用TI 产品而对TI 及其 代表造成的损失。

TI 产品并非设计或专门用于军事/航空应用，以及环境方面的产品，除非TI 特别注明该产品属于“军用”或“增强型塑料”产品。只 有TI 指定的军用产品才满足军用规格。购买者认可并同意，对TI 未指定军用的产品进行军事方面的应用，风险由购买者单独承担，并且独力负责在此类相关使用中满足所有法律和法规要求。

TI 产品并非设计或专门用于汽车应用以及环境方面的产品，除非TI 特别注明该产品符合ISO/TS 16949 要求。购买者认可并同意，如果他们在汽车应用中使用任何未被指定的产品，TI 对未能满足应用所需要求不承担任何责任。

可访问以下URL 地址以获取有关其它TI 产品和应用解决方案的信息：

产品		应用	
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	http://www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	http://www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	http://www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	http://www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	http://www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	http://www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	http:///www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	http://www.ti.com.cn/microcontrollers	无线通信	www.ti.com.cn/wireless
RFID 系统	http://www.ti.com.cn/rfidsys		
RF/IF 和 ZigBee® 解决方案	www.ti.com.cn/radiofre		
	TI E2E 工程师社区	http://e2e.ti.com/cn/	

邮寄地址： 上海市浦东新区世纪大道 1568 号，中建大厦 32 楼 邮政编码： 200122