0.65-Ω DUAL SPDT ANALOG SWITCHES WITH NEGATIVE SIGNALING CAPABILITY

Check for Samples: TS5A22362, TS5A22364

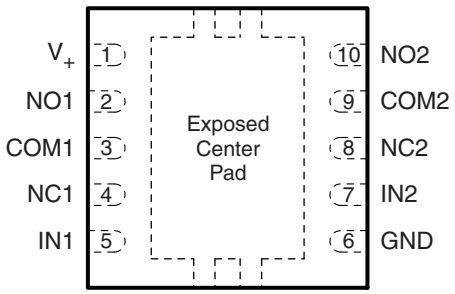
FEATURES

- **Specified Break-Before-Make Switching**
- **Negative Signaling Capability: Maximum Swing From –2.75 V to 2.75 V (V_+ = 2.75 V)**
- **Internal Shunt Switch Prevents Audible Click-and-Pop When Switching Between Two Sources (TS5A22364)**
- **Low ON-State Resistance (0.65 Ω Typical)**
- **Low Charge Injection**
- **Excellent ON-State Resistance Matching**
- **2.3-V to 5.5-V Power Supply (V_+)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2500-V Human-Body Model (A114-B, Class II)**
  - **1500-V Charged-Device Model (C101)**
  - **200-V Machine Model (A115-A)**

APPLICATIONS

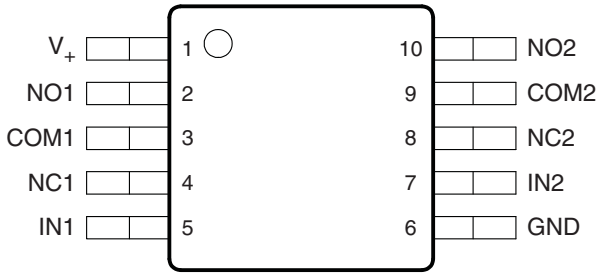
- **Cell Phones**
- **PDAs**
- **Portable Instrumentation**
- **Audio Routing**

DRC PACKAGE
(TOP VIEW)

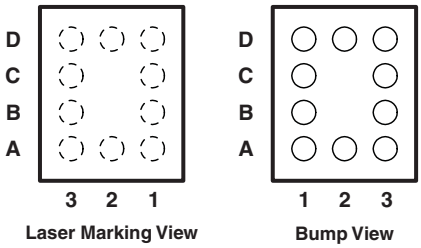


The exposed center pad, if used, must be connected as a secondary GND or left electrically open.

DGS PACKAGE
(TOP VIEW)



YZP PACKAGE



YZP PACKAGE TERMINAL ASSIGNMENTS

D	IN1	GND	IN2
C	NC1		NC2
B	COM1		COM2
A	NO1	V_+	NO2
	3	**2**	**1**

DESCRIPTION/ORDERING INFORMATION

The TS5A22362 and TS5A22364 are single-pole double-throw (SPDT) analog switches designed to operate from 2.3 V to 5.5 V. The devices feature negative signal capability that allows signals below ground to pass through the switch without distortion. Additionally, the TS5A22364 includes an internal shunt switch, which automatically discharges any capacitance at the NC or NO terminals when they are unconnected to COM. This reduces the audible click/pop noise when switching between two sources. The break-before-make feature prevents signal distortion during the transferring of a signal from one path to another. Low ON-state resistance, excellent channel-to-channel ON-state resistance matching, and minimal total harmonic distortion (THD) performance are ideal for audio applications.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	NanoFree™ – WCSP (DSBGA) YZP (Pb-free)	Tape and reel	TS5A22362YZPR	392
			TS5A22364YZPR	382
	MSOP (VSSOP) – DGS	Tape and reel	TS5A22362DGSR	39R
			TS5A22364DGSR	38R
	SON – DRC	Tape and reel	TS5A22362DRCR	ZVG
			TS5A22364DRCR	ZVF

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(3) YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

SUMMARY OF CHARACTERISTICS

V_+ = 2.7 V, T_A = 25°C

Configuration	2:1 Multiplexer/Demultiplexer (2 × SPDT)
Number of channels	2
ON-state resistance (r_{on})	0.65 Ω
ON-state resistance match (Δr_{on})	0.023 Ω
ON-state resistance flatness ($r_{on(flat)}$)	0.18 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	80 ns/70 ns
Break-before-make time (t_{BBM})	7 ns
Charge injection (Q_C)	150 pC
Bandwidth (BW)	17 MHz
OFF isolation (O_{ISO})	–66 dB at 100 kHz
Crosstalk (X_{TALK})	–75 dB at 100 kHz
Total harmonic distortion (THD)	0.01%
Leakage current ($I_{NO(OFF)}$, $I_{NC(OFF)}$)	50 nA
Package options	10-pin WCSP (YZP), 10-pin VSSOP (DGS), and 10-pin SON (DRC)

FUNCTION TABLE

IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON

APPLICATION BLOCK DIAGRAMS

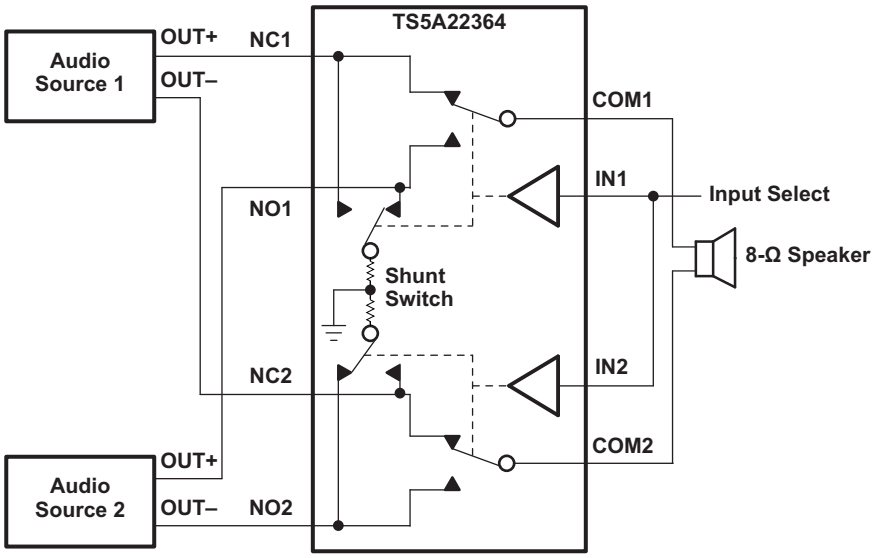


Figure 1. TS5A22364 Application Block Diagram

Shunt Switch (TS5A22364)

The 50-Ω shunt switches on the TS5A22364 automatically discharge any capacitance at the NC or NO terminals when they are unconnected to COM. This reduces audible click-and-pop sounds that occur when switching between audio sources. Audible clicks and pops are caused when a step DC voltage is switched into the speaker. By automatically discharging the side that is not connected, any residual DC voltage is removed, thereby reducing the clicks and pops.

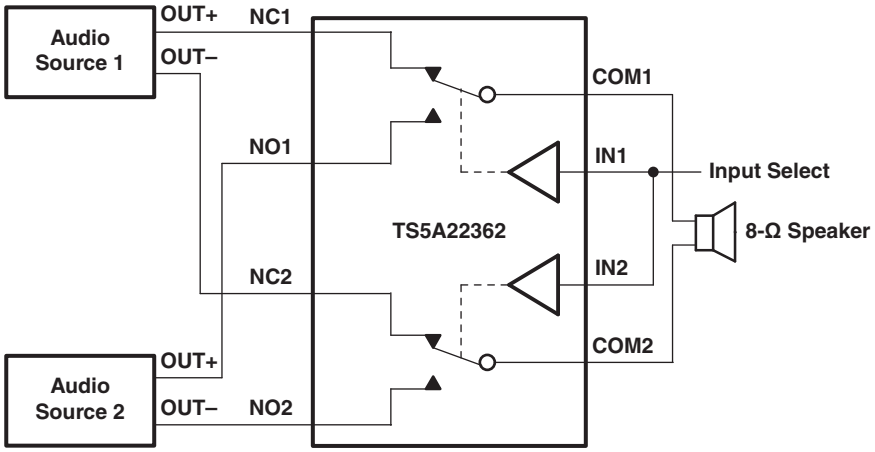


Figure 2. TS5A22362 Application Block Diagram

Negative Signaling Capacity

The TS5A22362 and TS5A22364 dual SPDT switches feature negative signal capability that allows signals below ground to pass through without distortion. These analog switches operate from a single +2.3-V to +5.5-V supply. The input/output signal swing of the device is dependant of the supply voltage V_+: the devices pass signals as high as V_+ and as low as $V_+ – 5.5$ V, including signals below ground with minimal distortion.

Table 1 shows the input/output signal swing the user can get with different supply voltages.

Table 1. INPUT/OUTPUT SIGNAL SWING

SUPPLY VOLTAGE, V+	MINIMUM (V_{NC}, V_{NO}, V_{COM}) = V_+ – 5.5	MAXIMUM (V_{NC}, V_{NO}, V_{COM}) = V_+
5.5 V	0 V	5.5 V
4.2 V	–1.3 V	4.2 V
3.3 V	–2.2 V	3.3 V
3 V	–2.5 V	3 V
2.5 V	–3 V	2.5 V

ABSOLUTE MINIMUM AND MAXIMUM RATINGS(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_+	Supply voltage range(3)		–0.5	6	V
V_{NC} V_{NO} V_{COM}	Analog voltage range(3) (4) (5)		V_+ – 6	V_+ + 0.5	V
$I_{I/OK}$	Analog port diode current	V_{NC}, V_{NO}, V_{COM} < 0 or V_{NC}, V_{NO}, V_{COM} > V_+	–50	50	mA
I_{NC} I_{NO} I_{COM}	ON-state switch current	V_{NC}, V_{NO}, V_{COM} = 0 to V_+	–150	150	mA
	ON-state peak switch current(6)		–300	300	
V_I	Digital input voltage range		–0.5	6.5	V
I_{IK}	Digital input clamp current(3) (4)	V_I < 0	–50	50	mA
I_+ I_{GND}	Continuous current through V_+or GND		–100	100	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle

THERMAL IMPEDANCE RATINGS

				UNIT
θ_{JA}	Package thermal impedance(1)	DGS package	56.5	°C/W
		DRC package	165.36	
		YZP package	93	

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY(1)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					V_+ – 5.5		V_+	V
ON-state resistance	r_{on}	V_{NC} or V_{NO} = V_+, 1.5 V, V_+ – 5.5 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	2.7 V		0.65	0.94	Ω
				Full				1.04	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	2.7 V		0.023	0.11	Ω
				Full				0.15	
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} or V_{NO} = V_+, 1.5 V, V_+ – 5.5 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	2.7 V		0.18	0.46	Ω
				Full				0.5	
Shunt switch resistance (TS5A22364 only)	r_{SH}	I_{NO} or I_{NC} = 10 mA		Full	2.7 V		25	50	Ω
NC, NO OFF leakage current (TS5A22362 Only)	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} = 2.25 V, V_+ – 5.5 V, V_{COM} = V_+ – 5.5 V, 2.25 V, V_{NO} = Open, COM to NO, or V_{NO} = 2.25 V, V_+ – 5.5 V, V_{COM} = V_+ – 5.5 V, 2.25 V, V_{NC} = Open, COM to NC	See Figure 17	25°C	2.7	–50		50	nA
				Full		–375		375	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = Open, V_{COM} = V_+, V_+ – 5.5 V,	See Figure 18	25°C	2.7 V	–50		50	nA
				Full		–375		375	
Digital Control Inputs (IN)(2)									
Input logic high	V_{IH}			Full		1.4		5.5	V
Input logic low	V_{IL}			Full				0.6	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+ or 0		25°C	2.7 V	–250		250	nA
				Full		–250		250	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 2.5-V SUPPLY (1) (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	2.5 V		44	80	ns
				Full	2.3 V to 2.7 V			80	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	2.5 V		22	70	ns
				Full	2.3 V to 2.7 V			70	
Break-before-make time	t_{BBM}	See Figure 21 for TS5A22362 See Figure 22 for TS5A22364		25°C	2.5 V	1	7		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 26	25°C	2.5 V		150		pC
NC, NO OFF capacitance (TS5A22362 only)	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or GND,	See Figure 19	25°C	2.5 V		70		pF
NC, NO, COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, Switch ON, f = 10 MHz	See Figure 19	25°C	2.5 V		370		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 19	25°C	2.5 V		2.6		pF
Bandwidth	BW	R_L = 50 Ω, –3 dB	See Figure 21	25°C	2.5 V		17		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω	f = 100 kHz, See Figure 24	25°C	2.5 V		–66		dB
Crosstalk	X_{TALK}	R_L = 50 Ω	f = 100 kHz, See Figure 25	25°C	2.5 V		–75		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 27	25°C	2.5 V		0.01		%
Supply									
Positive supply current	I_+	V_I = V+ or GND		25°C	2.7 V		0.2	1.1	μA
				Full				1.3	
Positive supply current	I_+	V_I = V+ – 5.5 V		Full	2.7 V			3.3	μA

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY(1)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					V_+ – 5.5		V_+	V
ON-state resistance	r_{on}	V_{NC} or V_{NO} ≤ V_+, 1.5 V, V_+ – 5.5 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	3 V		0.61	0.87	Ω
				Full				0.97	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.5 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	3 V		0.024	0.13	Ω
				Full				0.13	
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} or V_{NO} ≤ V_+, 1.5 V, V_+ – 5.5 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	3 V		0.12	0.46	Ω
				Full				0.5	
Shunt switch resistance (TS5A22364 only)	r_{SH}	I_{NO} or I_{NC} = 10 mA		Full	3 V		25	37	Ω
NC, NO OFF leakage current (TS5A22362 only)	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} = 3 V, V_+ – 5.5 V V_{COM} = V_+ – 5.5 V, 3 V V_{NO} = Open COM to NO or V_{NO} = 3 V, V_+ – 5.5 V, V_{COM} = V_+ – 5.5 V, 3 V V_{NC} = Open COM to NC	See Figure 17	25°C	3.6 V	–50		50	nA
				Full		–375		375	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = Open, V_{COM} = V_+,V_+ – 5.5 V,	COM to NO or NC, See Figure 18	25°C	3.6 V	–50		50	nA
				Full		–375		375	
Digital Control Inputs (IN)(2)									
Input logic high	V_{IH}			Full		1.4		5.5	V
Input logic low	V_{IL}			Full				0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+ or 0		25°C	3.6 V	–250		250	nA
				Full		–250		250	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 3.3-V SUPPLY (1) (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	3.3 V		34	80	ns
				Full	3 V to 3.6 V			80	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	3.3 V		19	70	ns
				Full	3 V to 3.6 V			70	
Break-before-make time	t_{BBM}	See Figure 21 for TS5A22362 See Figure 22 for TS5A22364		25°C	3.3 V	1	7		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 26	25°C	3.3 V		150		pC
NC, NO OFF capacitance (TS5A22362 only)	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or V_+ – 5.5 V,	See Figure 19	25°C	3.3 V		70		pF
NC, NO, COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND, f = 10 MHz	See Figure 19	25°C	3.3 V		370		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 19	25°C	3.3 V		2.6		pF
Bandwidth	BW	R_L = 50 Ω, –3 dB	Switch ON, See Figure 21	25°C	3.3 V		17.5		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω,	f = 100 kHz, See Figure 24	25°C	3.3 V		–68		dB
Crosstalk	X_{TALK}	R_L = 50 Ω,	f = 100 kHz, See Figure 25	25°C	3.3 V		–76		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 27	25°C	3.3 V		0.008		%
Supply									
Positive supply current	I_+	V_I = V+ or GND		25°C	3.6 V		0.1	1.2	µA
				Full				1.3	
		V_I = V+ –5.5 V		Full	3.6 V			3.4	µA

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY(1)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
Analog signal range	V_{COM}, V_{NO}, V_{NC}					V_+ – 5.5		V_+	V
ON-state resistance	r_{on}	V_{NC} or V_{NO} = V_+, 1.6 V, V_+ = –5.5 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	4.5 V		0.52	0.74	Ω
				Full				0.83	
ON-state resistance match between channels	Δr_{on}	V_{NC} or V_{NO} = 1.6 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	4.5 V		0.04	0.23	Ω
				Full				0.30	
ON-state resistance flatness	$r_{on(flat)}$	V_{NC} or V_{NO} = V_+, 1.6 V, V_+ = –5.5 V, I_{COM} = –100 mA,	COM to NO or NC, See Figure 16	25°C	4.5 V		0.076	0.46	Ω
				Full				0.5	
Shunt switch resistance (TS5A22364 only)	r_{SH}	I_{NO} or I_{NC} = 10 mA		Full	4.5 V		16	36	Ω
NC, NO OFF leakage current	$I_{NC(OFF)}$, $I_{NO(OFF)}$	V_{NC} = 4.5 V, V_+ – 5.5 V V_{COM} = V_+ – 5.5 V, 4.5 V V_{NO} = Open COM to NO or V_{NO} = 4.5 V, V_+ – 5.5 V, V_{COM} = V_+ – 5.5 V, 4.5 V V_{NC} = Open COM to NC	See Figure 17	25°C	5.5 V	–50		50	nA
				Full		–375		375	
COM ON leakage current	$I_{COM(ON)}$	V_{NC} and V_{NO} = Open, V_{COM} = V_+, V_+ – 5.5 V,	See Figure 18	25°C	5.5 V	–50		50	nA
				Full		–375		375	
Digital Control Inputs (IN)(2)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full				0.8	V
Input leakage current	I_{IH}, I_{IL}	V_{IN} = V_+ or 0		25°C	5.5 V	–250		250	nA
				Full		–250		250	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum

(2) All unused digital inputs of the device must be held at V_+ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS FOR 5-V SUPPLY (1) (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	5 V		27	80	ns
				Full	4.5 V to 5.5 V			80	
Turn-off time	t_{OFF}	V_{COM} = V_+, R_L = 300 Ω,	C_L = 35 pF, See Figure 20	25°C	5 V		13	70	ns
				Full	4.5 V to 5.5 V			70	
Break-before-make time	t_{BBM}	V_{NC} = V_{NO} = V_+/2 R_L = 300 Ω,	C_L = 35 pF, See Figure 21	25°C	5 V	1	3.5		ns
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 26	25°C	5 V		10		pC
NC, NO OFF capacitance (TS5A22362 only)	$C_{NC(OFF)}$, $C_{NO(OFF)}$	V_{NC} or V_{NO} = V_+ or V_+ – 5.5 V,	See Figure 19	25°C	5 V		70		pF
NC, NO, COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_+ or GND,	See Figure 19	25°C	5 V		370		pF
Digital input capacitance	C_I	V_I = V_+ or GND	See Figure 19	25°C	5 V		2.6		pF
Bandwidth	BW	R_L = 50 Ω,	See Figure 21	25°C	5 V		18.3		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω,	f = 100 kHz, See Figure 24	25°C	5 V		–70		dB
Crosstalk	X_{TALK}	R_L = 50 Ω,	f = 100 kHz, See Figure 25	25°C	5 V		–78		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 27	25°C	5 V		0.009		%
Supply									
Positive supply current	I_+	V_I = V_+ or GND		25°C	5.5 V		0.2	1.3	µA
				Full				3.5	
		V_I = V_+ – 5.5 V		Full				5	

TYPICAL PERFORMANCE

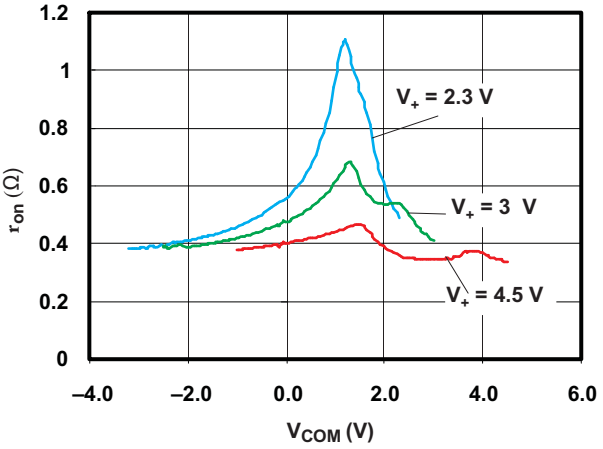


Figure 3. r_{on} vs V_{COM}

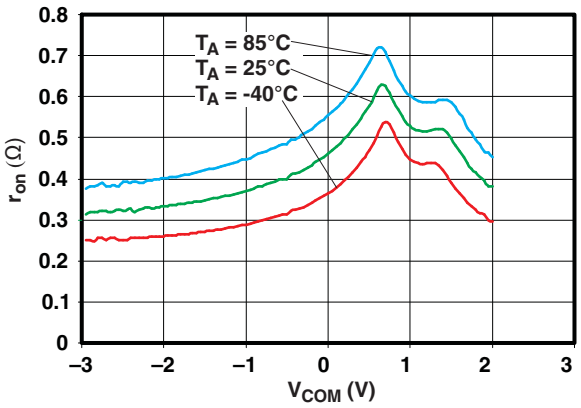


Figure 4. r_{on} vs V_{COM} (V_+ = 2.7 V)

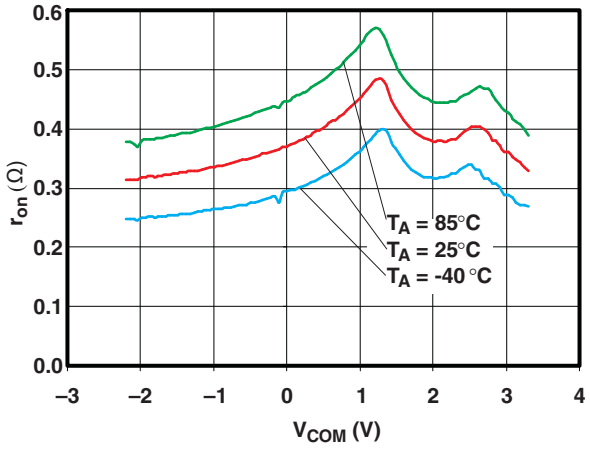


Figure 5. r_{on} vs V_{COM} (V_+ = 3.3 V)

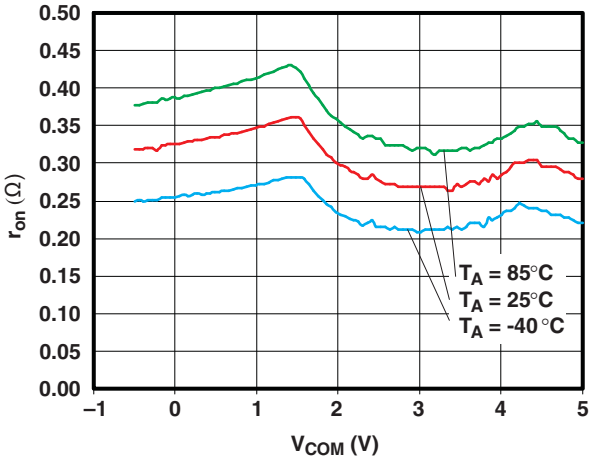


Figure 6. r_{on} vs V_{COM} (V_+ = 5 V)

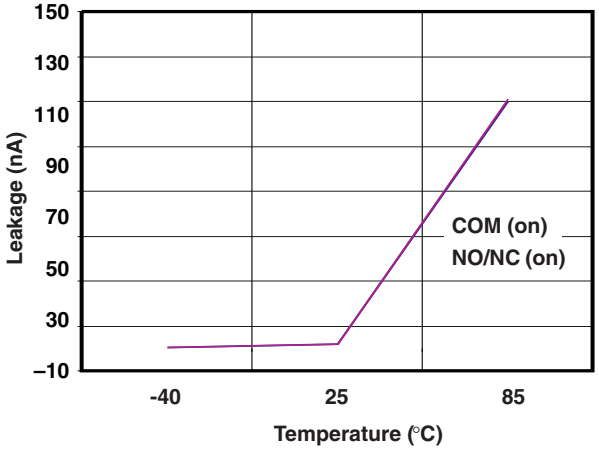


Figure 7. Leakage Current vs Temperature

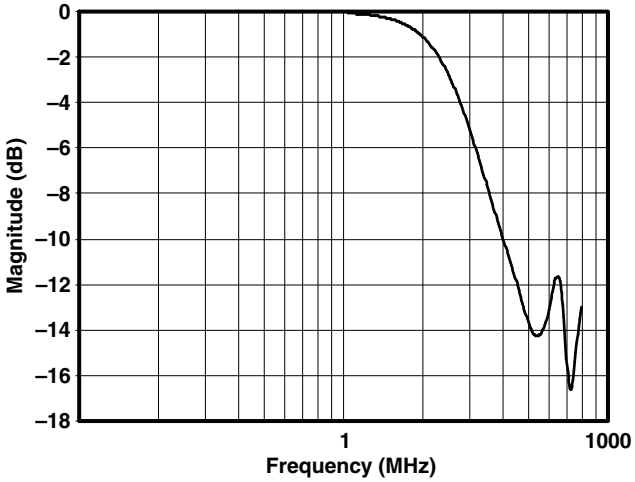


Figure 8. Insertion Loss

TYPICAL PERFORMANCE (continued)

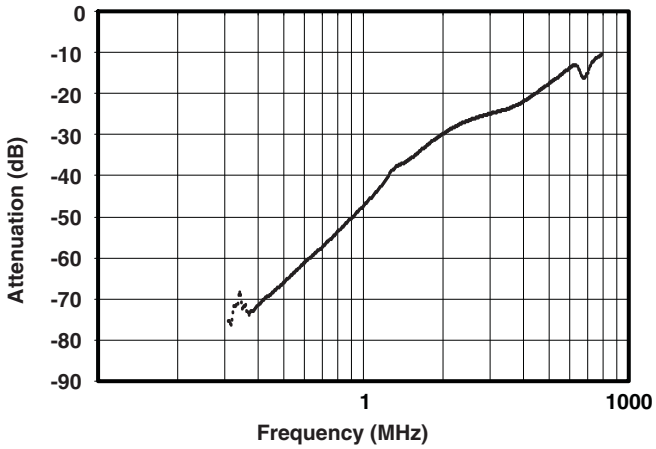


Figure 9. OFF Isolation vs Frequency

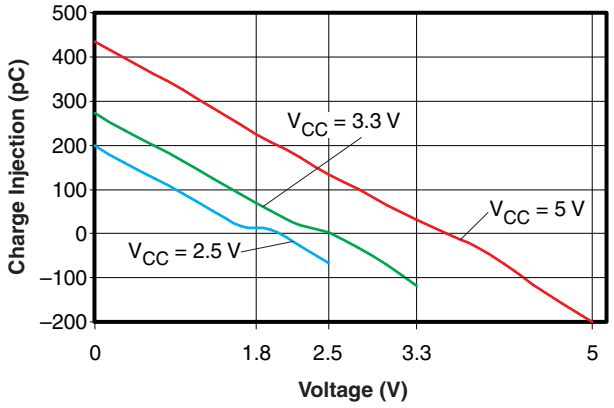


Figure 10. Charge Injection (Q_C) vs V_{COM}

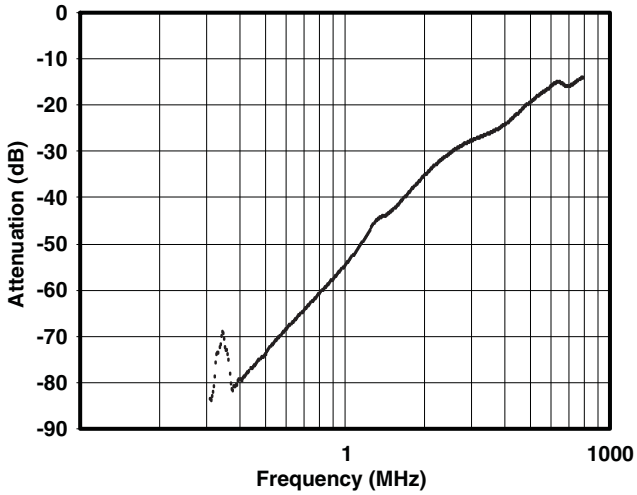


Figure 11. Crosstalk (V_+ = 3.3 V)

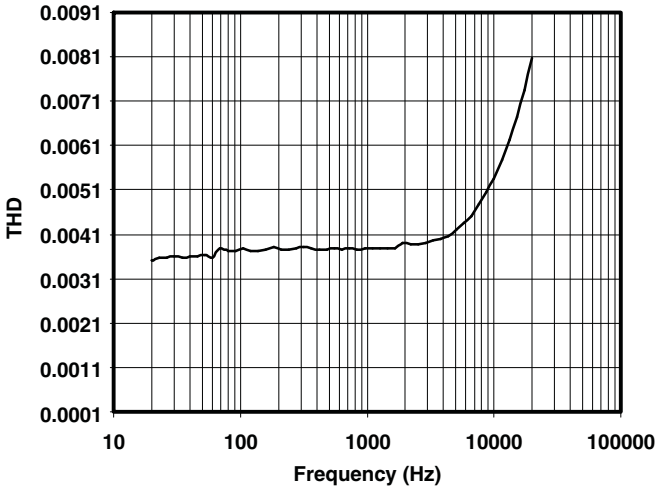


Figure 12. Total Harmonic Distortion vs Frequency

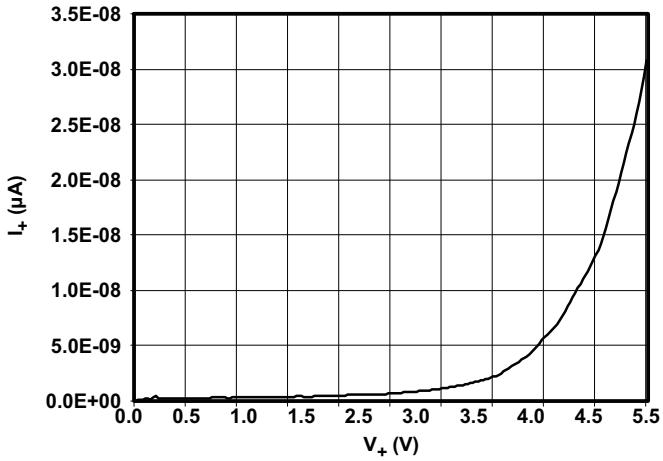


Figure 13. Power-Supply Current vs V_+

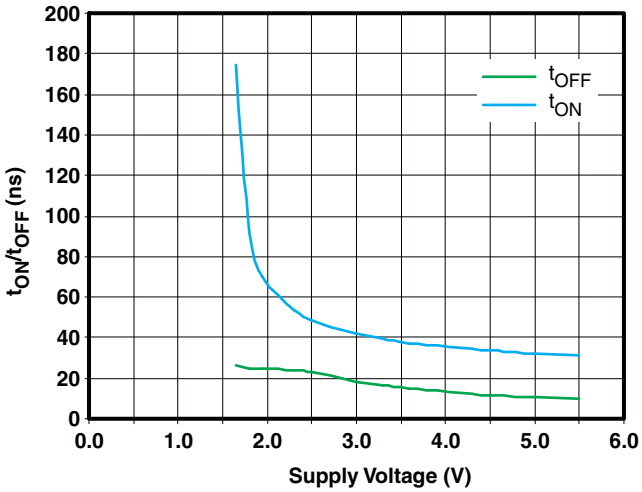


Figure 14. t_{ON} and t_{OFF} vs Supply Voltage

TYPICAL PERFORMANCE (continued)

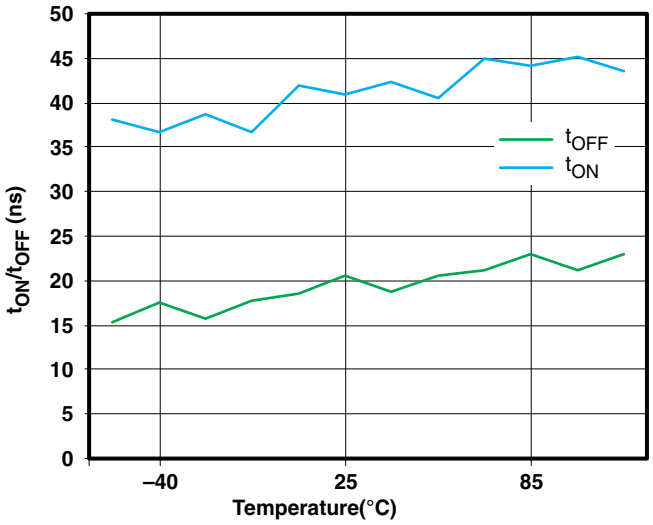


Figure 15. t_{ON} and t_{OFF} vs Temperature (2.5-V Supply)

PARAMETER MEASUREMENT INFORMATION

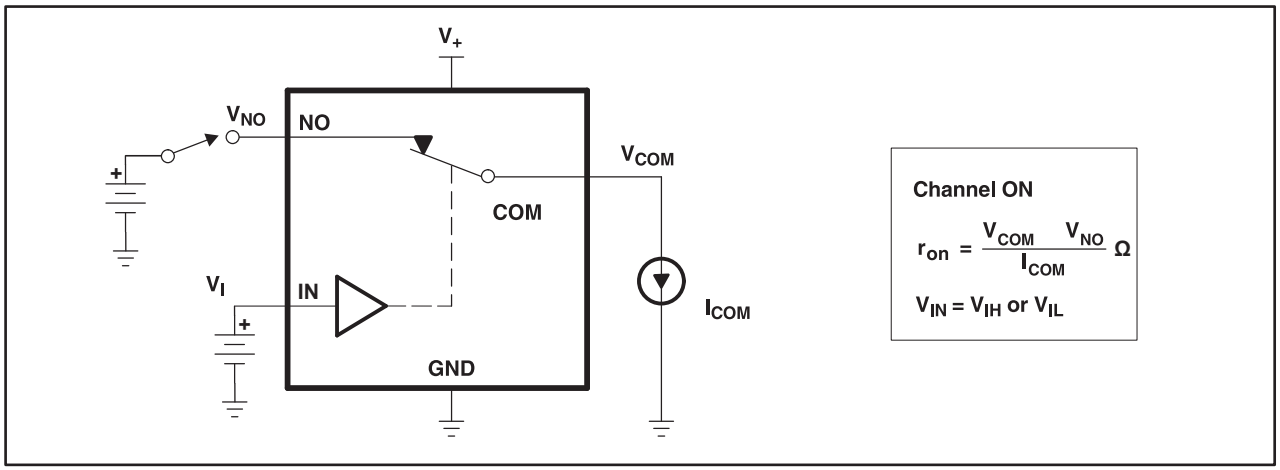


Figure 16. ON-State Resistance (r_{ON})

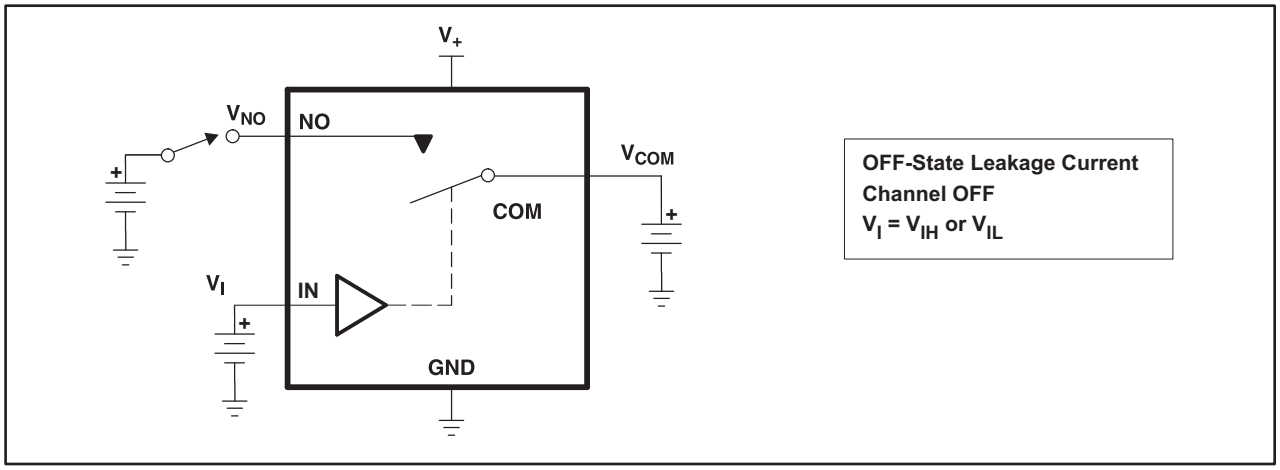


Figure 17. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$)

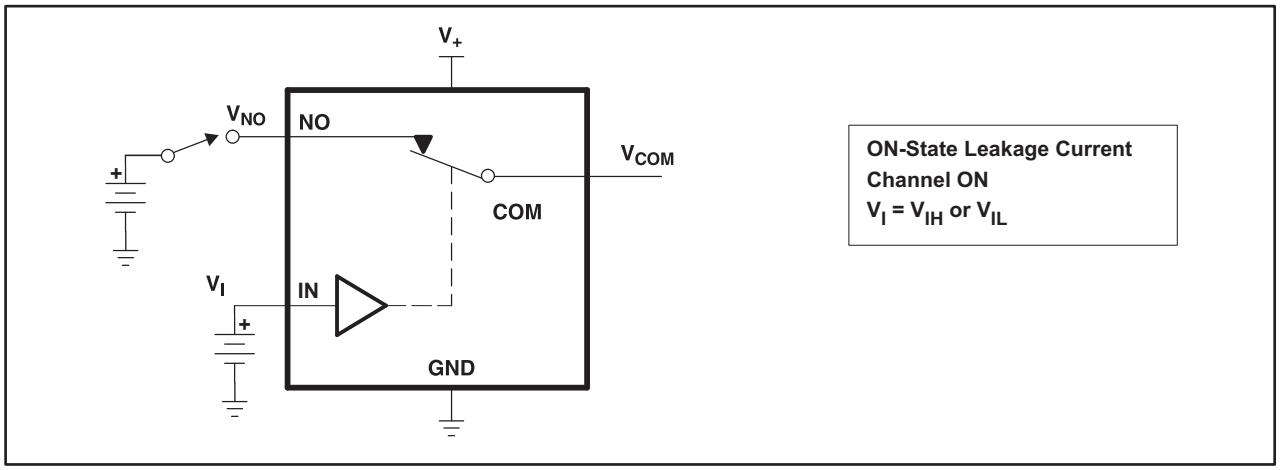


Figure 18. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

PARAMETER MEASUREMENT INFORMATION (continued)

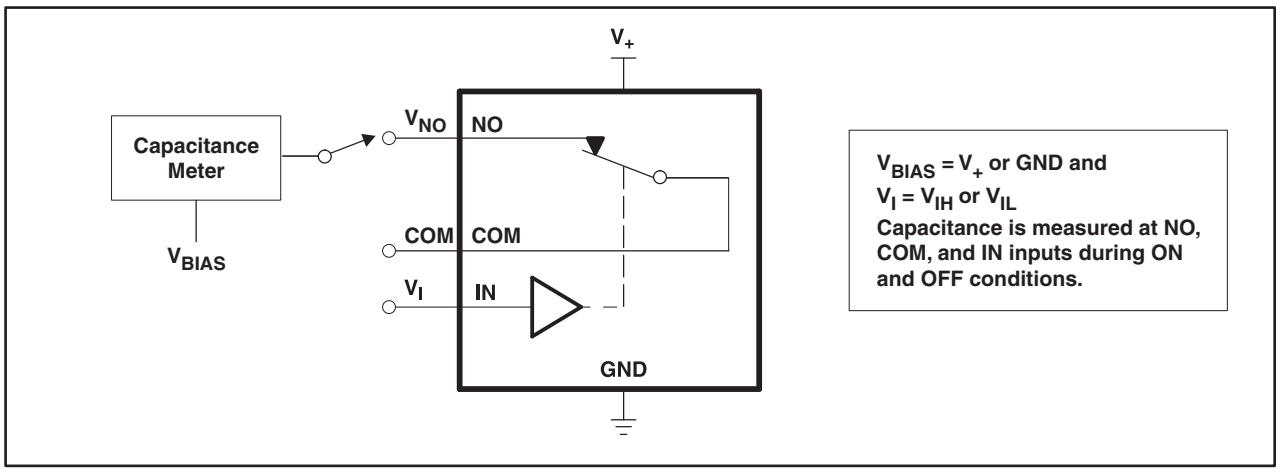
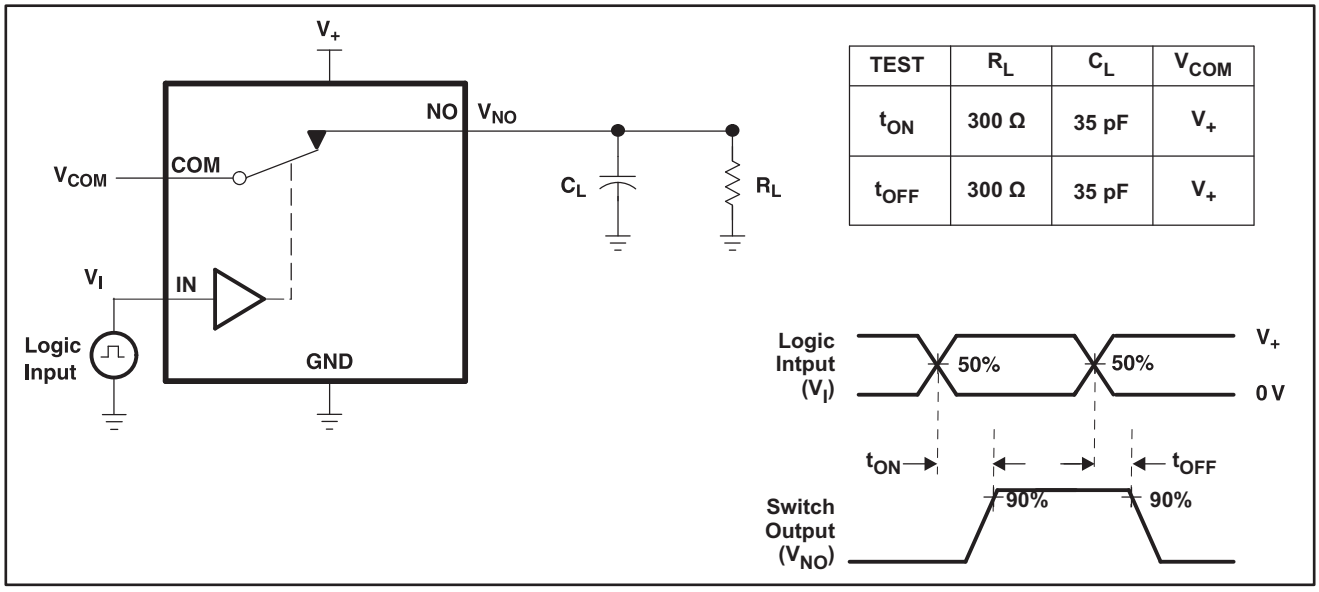


Figure 19. Capacitance
(C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.



TEST	R_L	C_L	V_{COM}
t_{ON}	300 Ω	35 pF	V_+
t_{OFF}	300 Ω	35 pF	V_+

Figure 20. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

C. C_L includes probe and jig capacitance.

D. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

PARAMETER MEASUREMENT INFORMATION (continued)

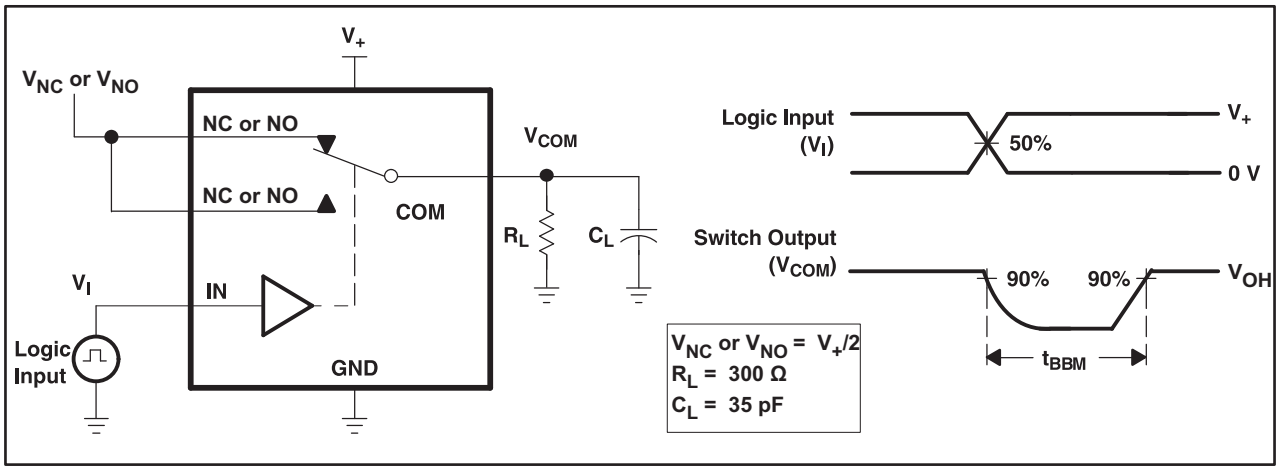


Figure 21. Break-Before-Make Time (t_{BBM}) (TS5A22362 Only)

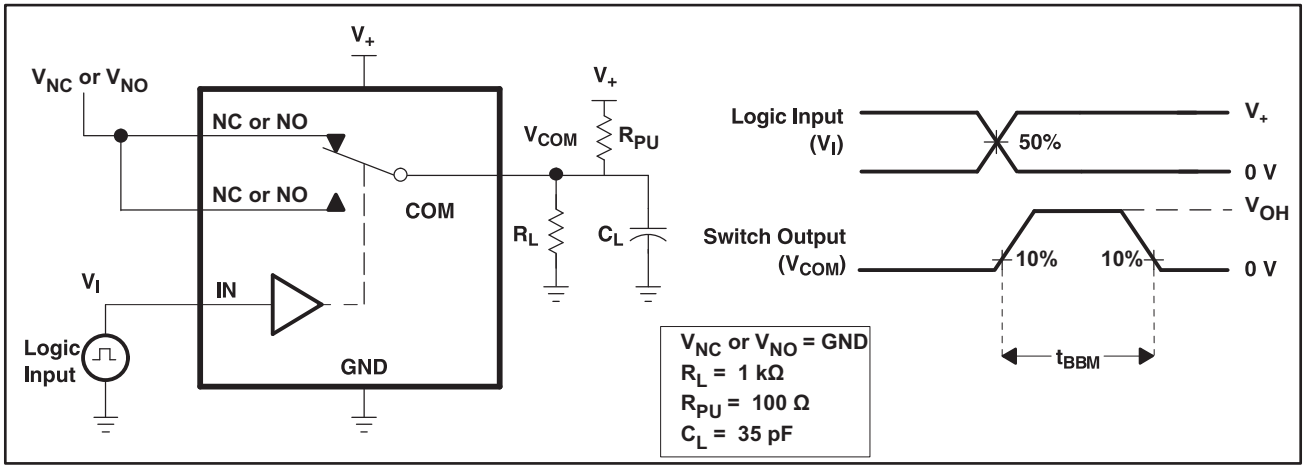


Figure 22. Break-Before-Make Time (t_{BBM}) (TS5A22364 Only)

E. C_L includes probe and jig capacitance.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

PARAMETER MEASUREMENT INFORMATION (continued)

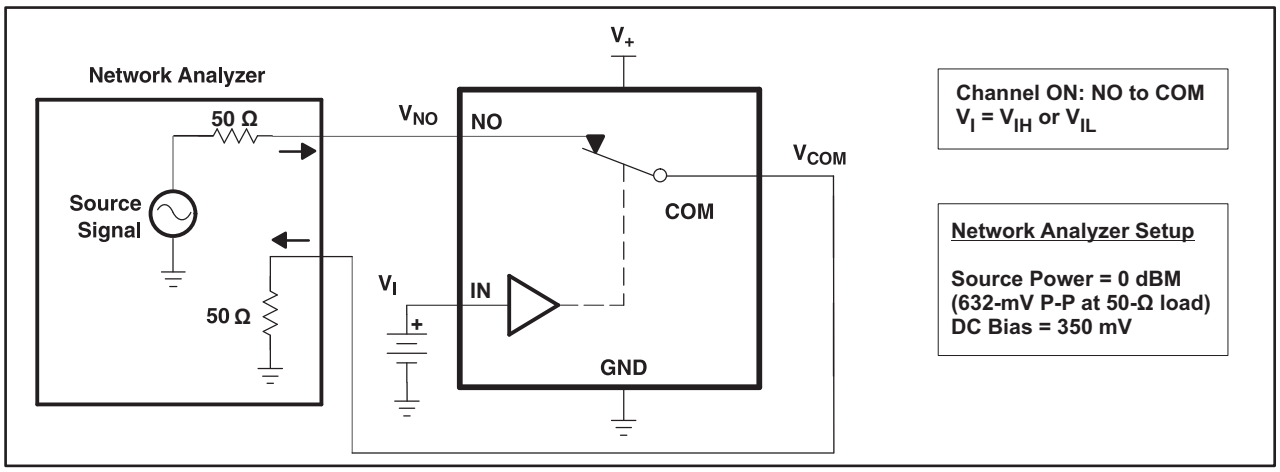


Figure 23. Bandwidth (BW)

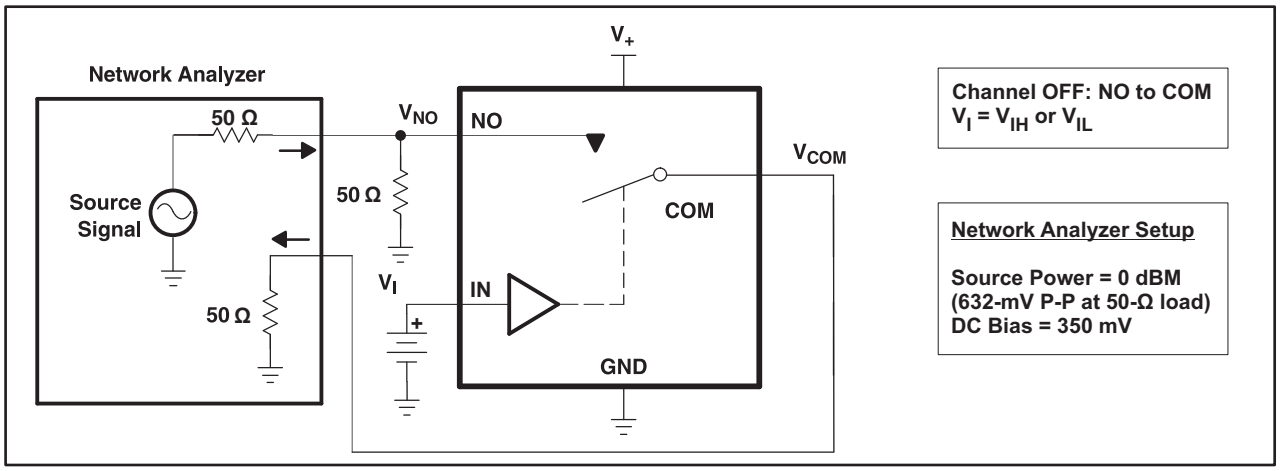


Figure 24. OFF Isolation (O_{ISO})

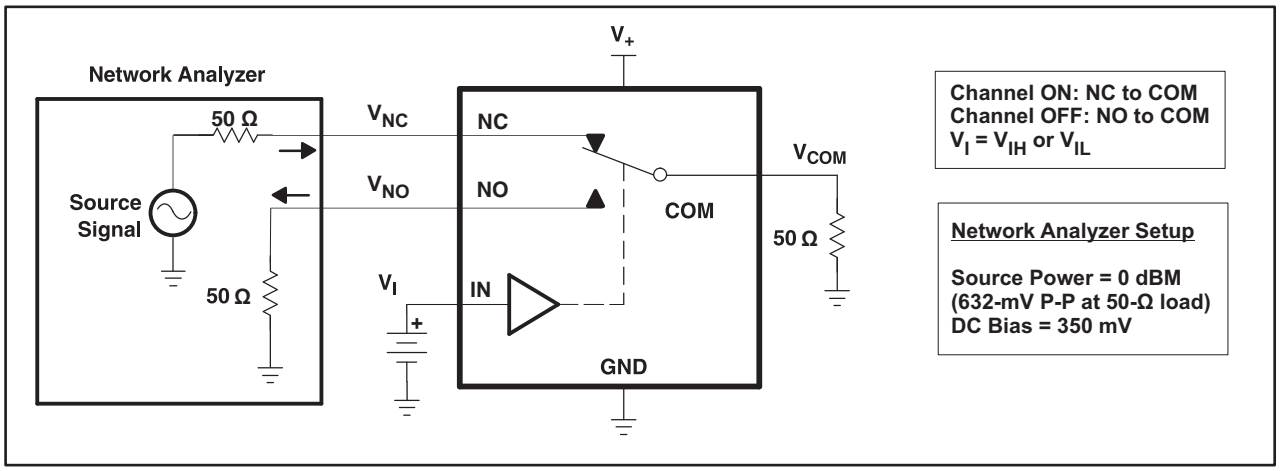


Figure 25. Crosstalk (X_{TALK})

G. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

H. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION (continued)

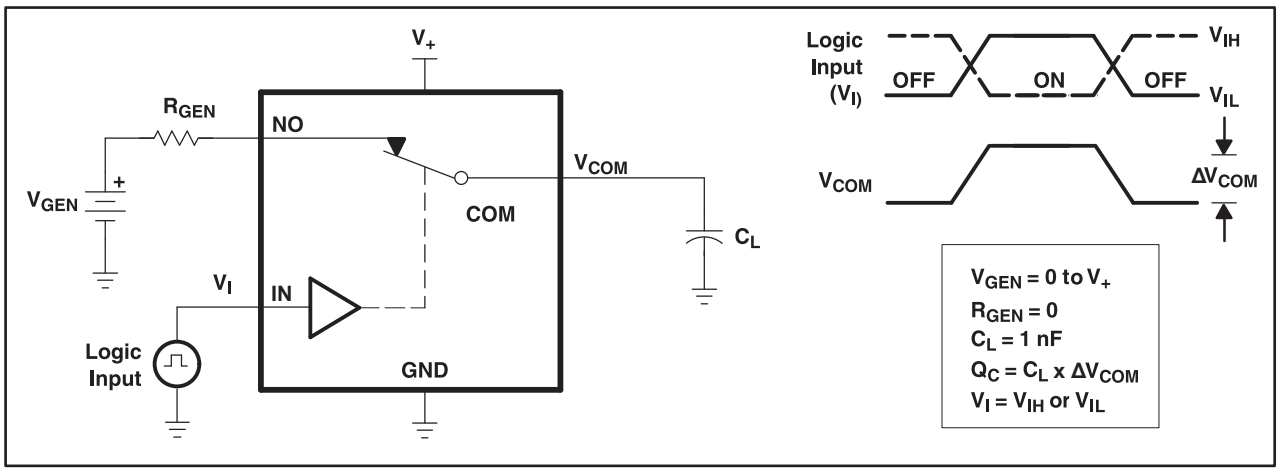


Figure 26. Charge Injection (Q_C)

I. C_L includes probe and jig capacitance.

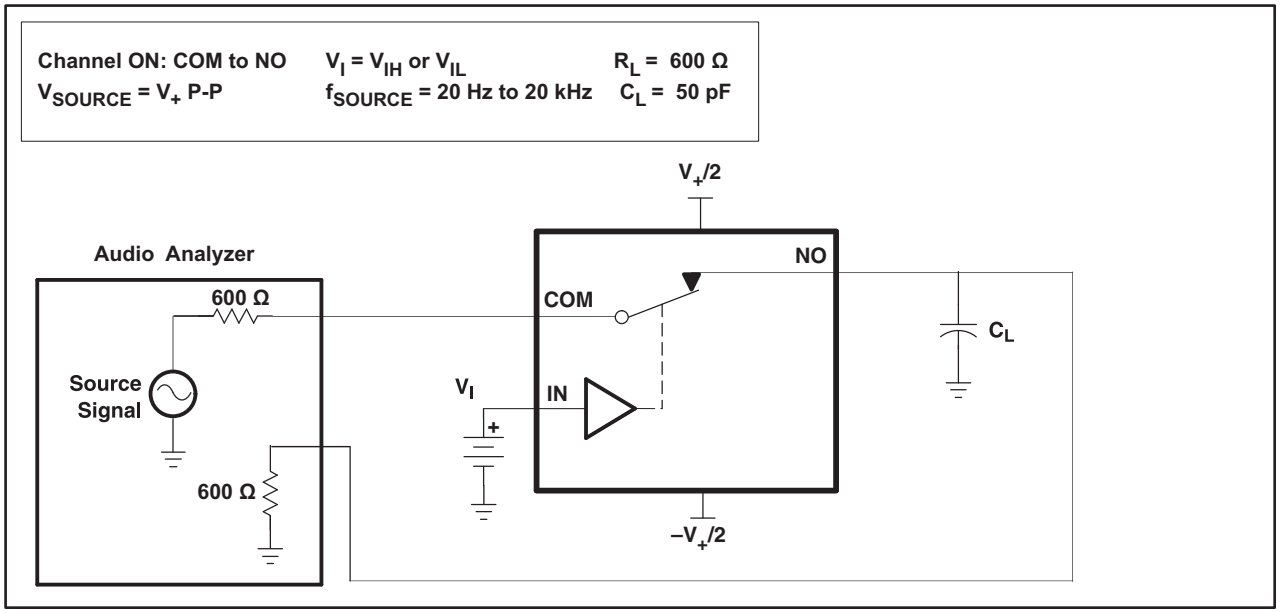


Figure 27. Total Harmonic Distortion (THD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS5A22362DGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS5A22362DGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS5A22362DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS5A22362DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS5A22362YZPR	ACTIVE	DSBGA	YZP	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM
TS5A22364DGSR	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS5A22364DGSRG4	ACTIVE	MSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TS5A22364DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TS5A22364YZPR	ACTIVE	DSBGA	YZP	10	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

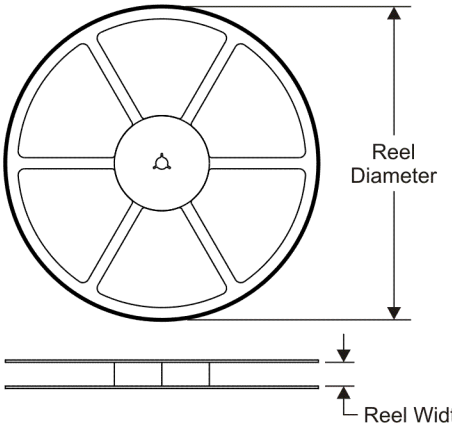
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

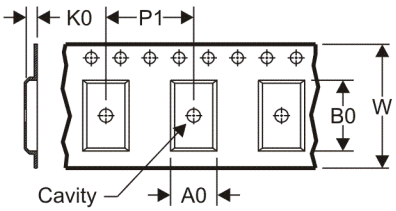
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

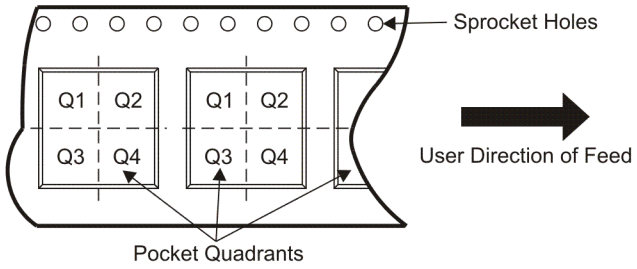


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

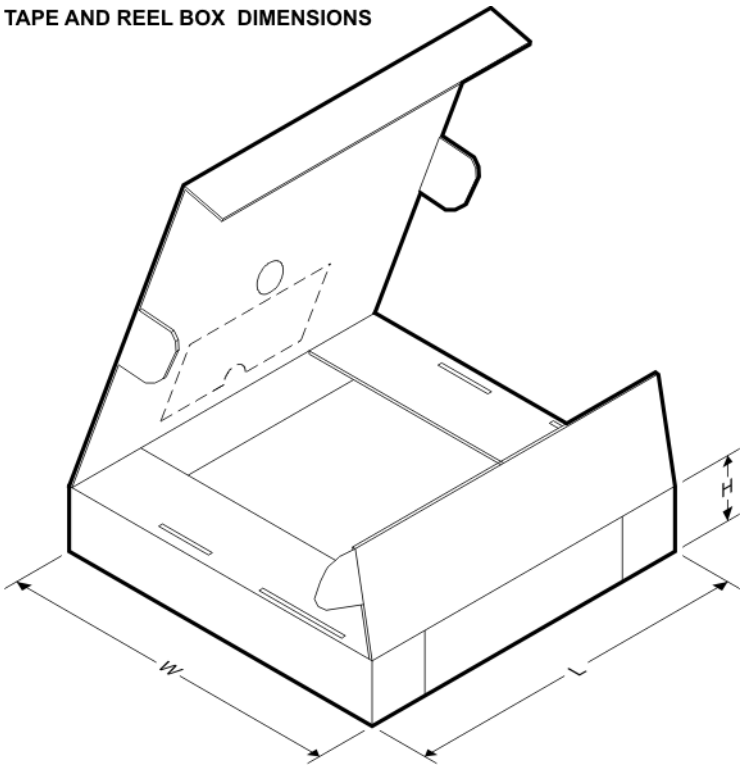
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A22362DGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A22362DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS5A22362YZPR	DSBGA	YZP	10	3000	180.0	8.4	1.5	2.03	0.7	4.0	8.0	Q2
TS5A22364DGSR	MSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TS5A22364DRCR	SON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TS5A22364YZPR	DSBGA	YZP	10	3000	180.0	8.4	1.5	2.03	0.7	4.0	8.0	Q2

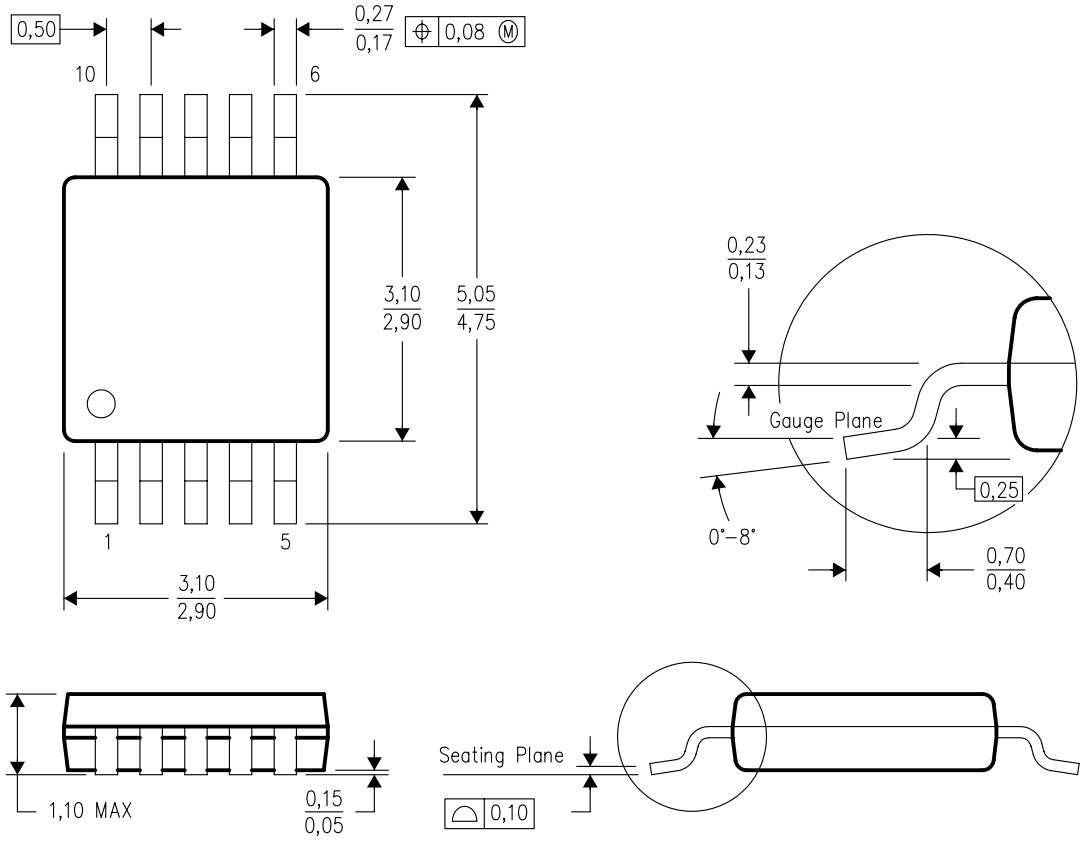
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A22362DGSR	MSOP	DGS	10	2500	358.0	335.0	35.0
TS5A22362DRCR	SON	DRC	10	3000	346.0	346.0	29.0
TS5A22362YZPR	DSBGA	YZP	10	3000	220.0	220.0	34.0
TS5A22364DGSR	MSOP	DGS	10	2500	358.0	335.0	35.0
TS5A22364DRCR	SON	DRC	10	3000	346.0	346.0	29.0
TS5A22364YZPR	DSBGA	YZP	10	3000	220.0	220.0	34.0

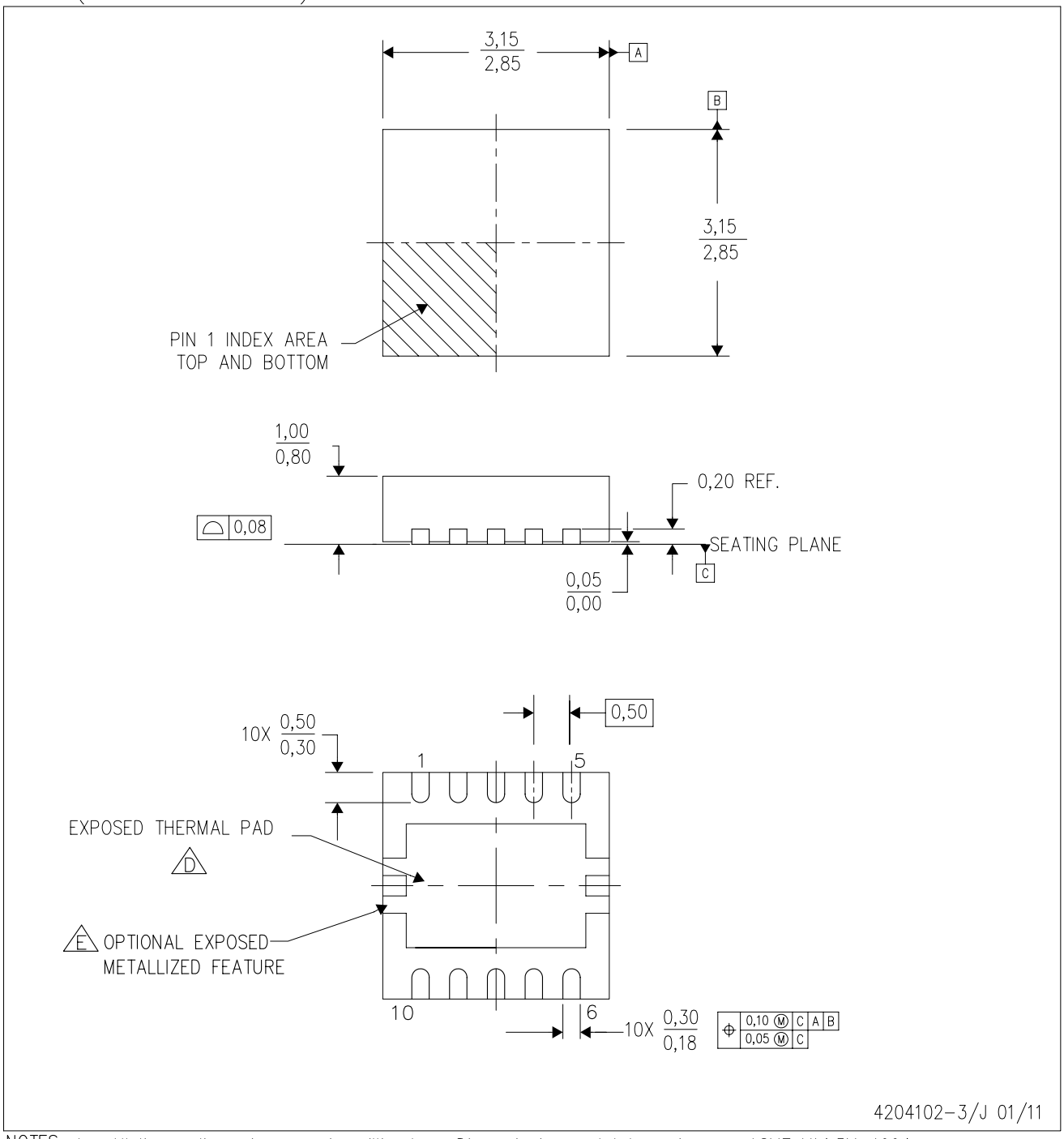
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

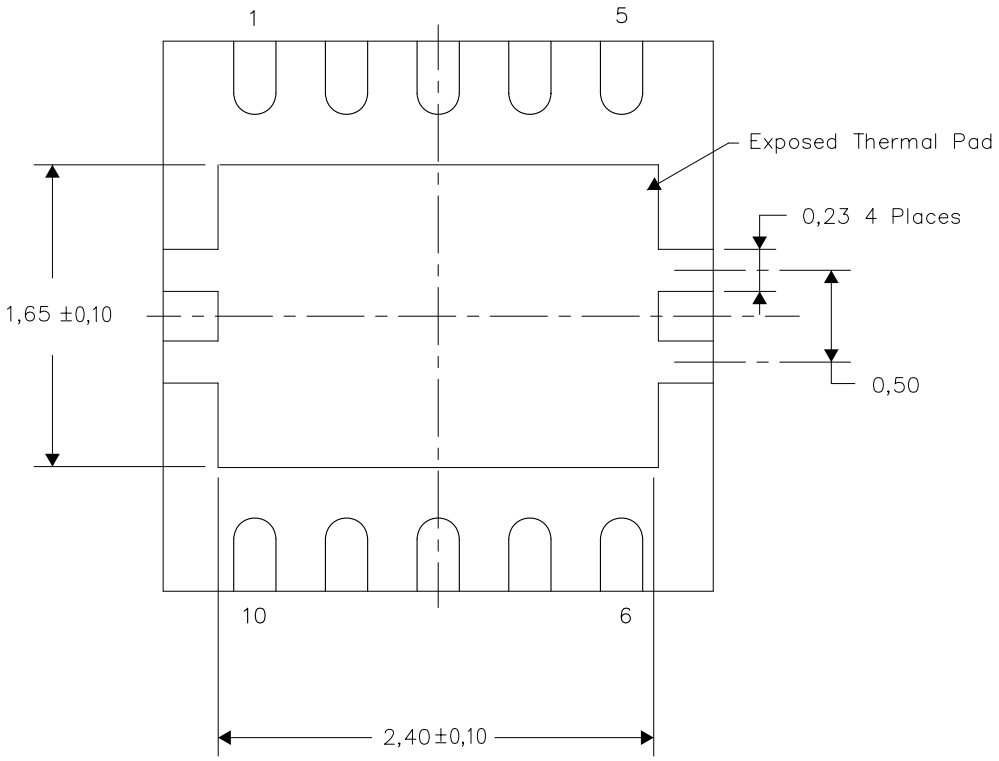
DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



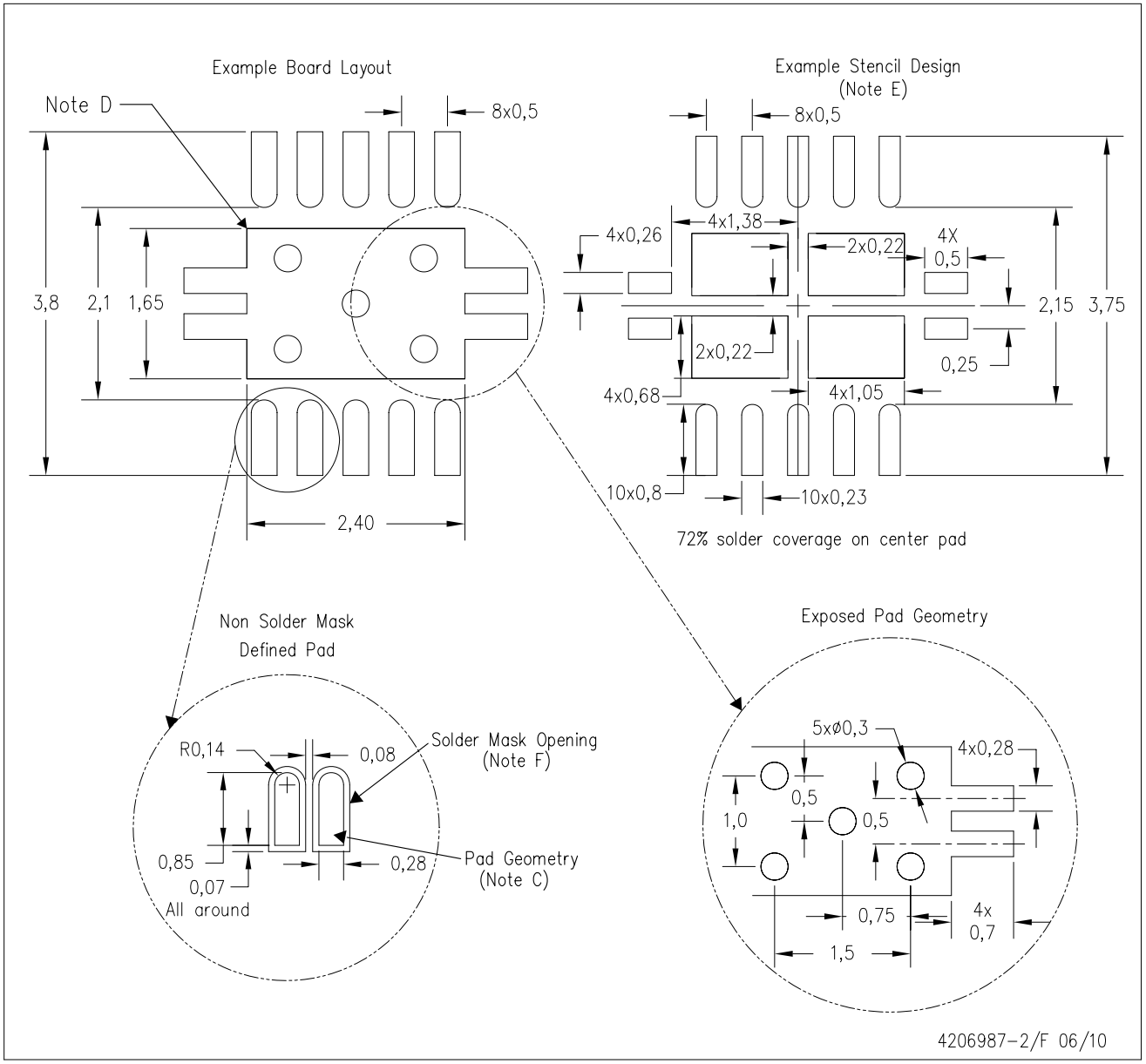
Bottom View

Exposed Thermal Pad Dimensions

4206565–3/L 02/11

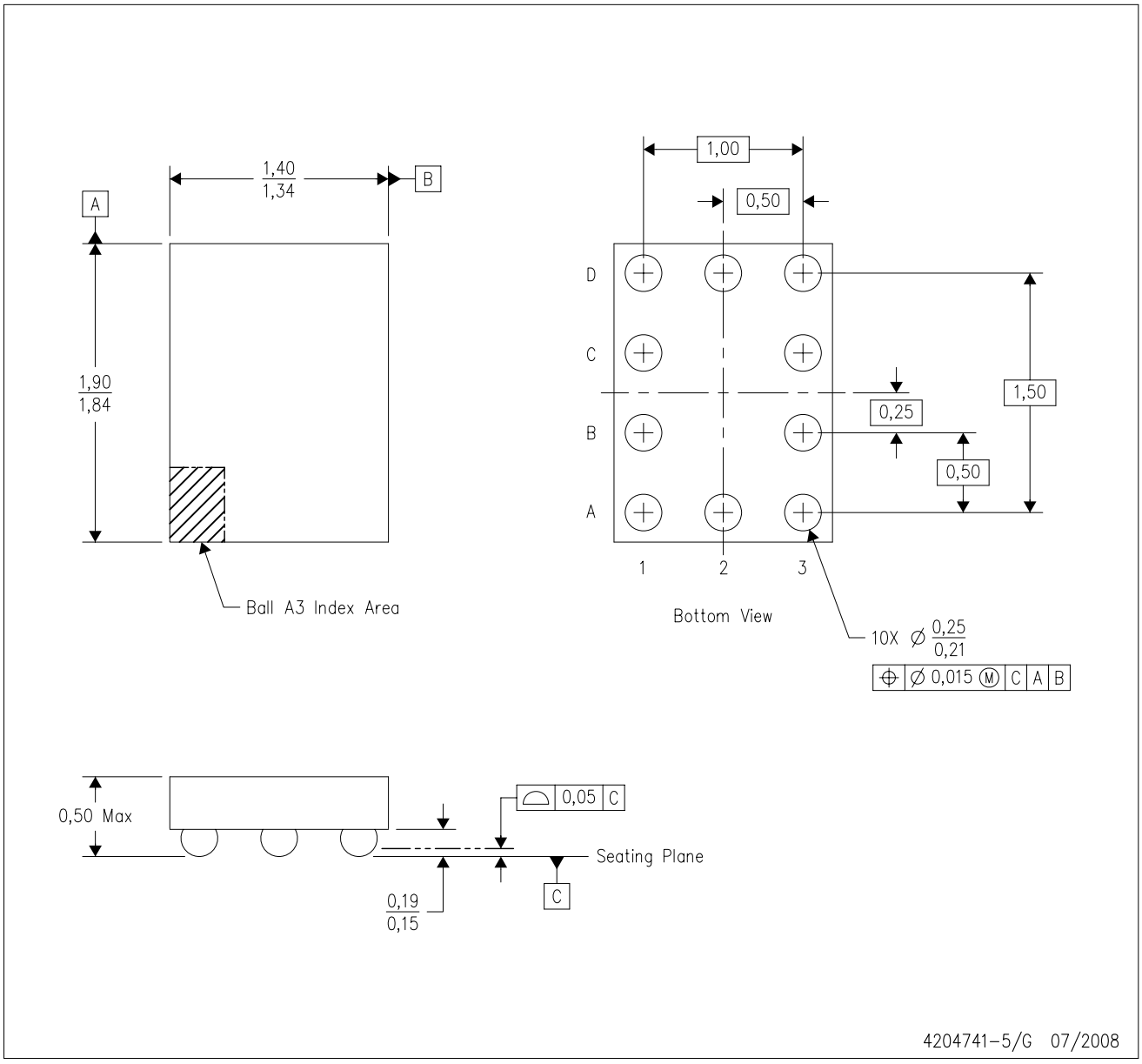
NOTE: A. All linear dimensions are in millimeters

DRC (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

YZP (R–XBGA–N10) (CUSTOM) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is a lead–free solder ball design.

NanoFree is a trademark of Texas Instruments.

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