

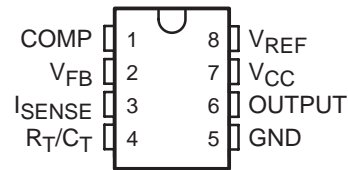
UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

SGLS134C – SEPTEMBER 2002 – REVISED FEBRUARY 2006

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Optimized for Off-line and DC-to-DC Converters**
- **Low Start Up Current (<0.5 mA)**
- **Trimmed Oscillator Discharge Current**
- **Automatic Feed Forward Compensation**
- **Pulse-by-Pulse Current Limiting**
- **Enhanced Load Response Characteristics**
- **Under-Voltage Lockout With Hysteresis**
- **Double Pulse Suppression**
- **High Current Totem Pole Output**
- **Internally Trimmed Bandgap Reference**
- **500 kHz Operation**
- **Low R_O Error Amp**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

D PACKAGE
(TOP VIEW)



description

The UC1842A/3A/4A/5A family of control ICs is a pin-for-pin compatible improved version of the UC3842/3/4/5 family. Providing the necessary features to control current mode switched mode power supplies, this family has the following improved features. Start up current is guaranteed to be less than 0.5 mA. Oscillator discharge is trimmed to 8.3 mA. During under voltage lockout, the output stage can sink at least 10 mA at less than 1.2 V for V_{CC} over 5 V.

The difference between members of this family are shown in the table below.

PART NUMBER	UVLO ON	UVLO OFF	MAXIMUM DUTY CYCLE
UC1842A	16 V	10 V	<100%
UC1843A	8.5 V	7.9 V	<100%
UC1844A	16 V	10 V	<50%
UC1845A	8.5 V	7.9 V	<50%

ORDERING INFORMATION‡

T _A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	SOP – D	Tape and reel	UC1842AMDREP	1842AME
–55°C to 125°C	SOP – D	Tape and reel	UC1843AMDREP	1843AME
–55°C to 125°C	SOP – D	Tape and reel	UC1844AMDREP	1844AME
–55°C to 125°C	SOP – D	Tape and reel	UC1845AMDREP	1845AME

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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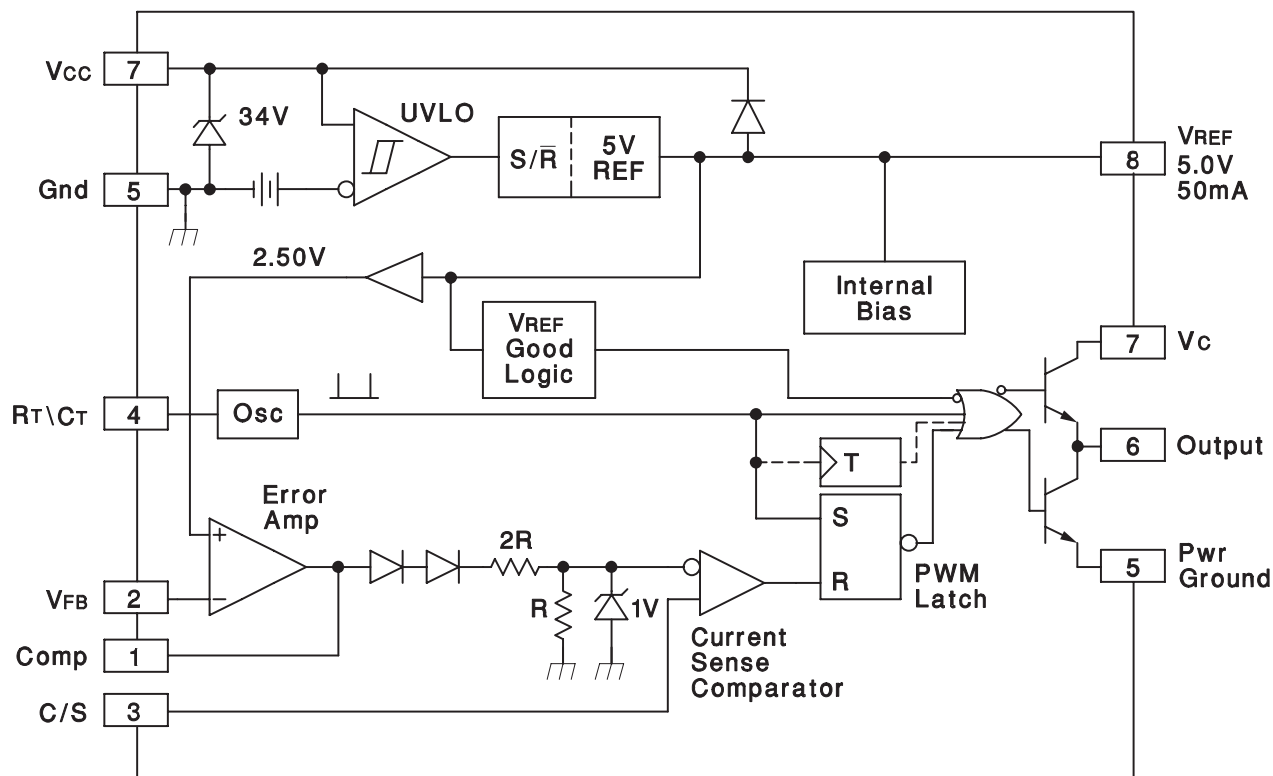
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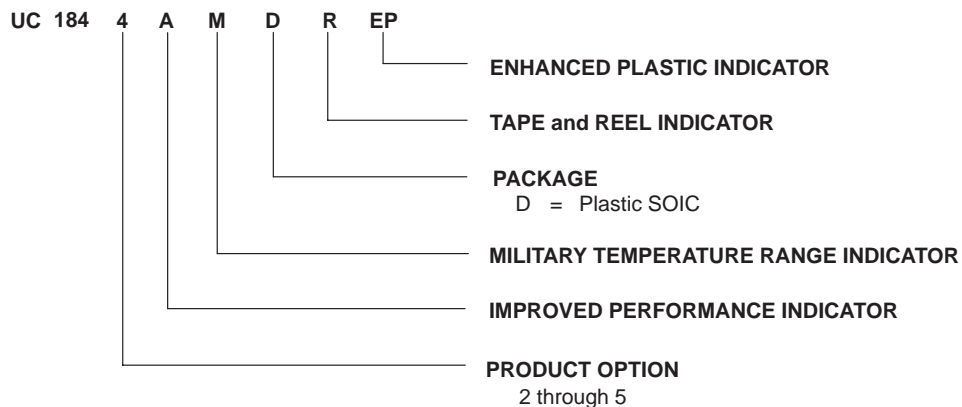
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block diagram



NOTES: 1. Toggle flip flop used only in 1844A and 1845A.

Ordering Information



UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

SGLS134C – SEPTEMBER 2002 – REVISED FEBRUARY 2006

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)^{†‡}

V_{CC} voltage (low impedance source)	30 V
V_{CC} voltage (I_{CC} mA)	self limiting
Output current, I_O	±1 A
Output energy (capacitive load)	5 μ J
Analog Inputs (pins 2, 3)	-0.3 V to 6.3 V
Error Amp Output Sink current	10 mA
Power Dissipation at $T_A < 25^\circ\text{C}$	1 W
Package thermal impedance, θ_{JA} (see Note 1):	97°C/W
Storage temperature range, T_{stg}	-65°C to 150°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] Unless otherwise indicated, voltages are reference to ground and currents are positive into and negative out of the specified terminals.

NOTE 1: Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

electrical characteristics, $T_A = -55^\circ\text{C}$ to 125°C for the UC184xAM-EP, $V_{CC} = 15\text{ V}$ (see Note 1), $R_T = 10\text{ k}\Omega$, $C_T = 3.3\text{ nF}$, and $T_A = T_J$ (unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Reference Section						
Output voltage	$T_J = 25^\circ\text{C}$, $I_O = 1\text{ mA}$	4.95	5	5.05	V	
Line regulation voltage	$V_{IN} = 12\text{ V}$ to 25 V		6	20	mV	
Load regulation voltage	$I_O = 1\text{ mA}$ to 20 mA		6	25	mV	
Temperature stability	See Notes NO TAG and NO TAG		0.2	0.4	mV/°C	
Total output variation voltage	Line, Load, Temp.	4.9		5.1	V	
Output noise voltage	$f = 10\text{ Hz}$ to 10 kHz , See Note NO TAG		50		μ V	
Long term stability	1000 hours, See Note 2		5	25	mV	
Output short-circuit current		-30	-100	-180	mA	
Oscillator Section						
Initial accuracy	See Note NO TAG	47	52	57	kHz	
Voltage stability	$V_{CC} = 12\text{ V}$ to 25 V		0.2%	1%		
Temperature stability	$T_A = \text{MIN}$ to MAX , See Note 2		5%			
Amplitude peak-to-peak	V pin 4, See Note 2		1.7		V	
Discharge current	V pin 4 = 2 V, See Note 3	$T_J = 25^\circ\text{C}$	7.8	8.3	8.8	mA
		$T_J = \text{Full range}$	7.5		8.8	

- NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.
 2. Not production tested.
 3. This parameter is measured with $R_T = 10\text{ k}\Omega$ to V_{REF} . This contributes approximately 300 μ A of current to the measurement. The total current flowing into the R_T/C pin will be approximately 300 μ A higher than the measured value.

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SGLS134C – SEPTEMBER 2002 – REVISED FEBRUARY 2006

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PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier Section						
Input voltage	COMP = 2.5 V		2.45	2.5	2.55	V
Input bias current				-0.3	-1	μA
Open loop voltage gain (A_{VOL})	$V_O = 2\text{ V}$ to 4 V		65	90		dB
Unity gain bandwidth	See Note 2	$T_J = 25^\circ\text{C}$	0.7	1		MHz
PSRR	$V_{CC} = 12\text{ V}$ to 25 V		60	70		dB
Output sink current	FB = 2.7 V, COMP = 1.1 V		2	6		mA
Output source current	FB = 2.3 V, COMP = 5 V		-0.5	-0.8		mA
V_{OUT} high	FB = 2.3 V, $R_L = 15\text{ k}\Omega$ to GND		5	6		V
V_{OUT} low	FB = 2.7 V, $R_L = 15\text{ k}\Omega$ to V_{REF}			0.7	1.1	V
Current Sense Section						
Gain	See Note 3 and Note 4		2.85	3	3.15	V/V
Maximum input signal	COMP = 5 V, See Note 3		0.9	1	1.1	V
PSRR	$V_{CC} = 12\text{ V}$ to 25 V , See Note 3			70		dB
Input bias current				-2	-10	μA
Delay to output	$I_{SENSE} = 0\text{ V}$ to 2 V , See Note 2			150	300	ns
Output Section (OUT)						
Low-level output voltage	$I_{OUT} = 20\text{ mA}$			0.1	0.4	V
	$I_{OUT} = 200\text{ mA}$			15	2.2	
High-level output voltage	$I_{OUT} = -20\text{ mA}$		13	13.5		V
	$I_{OUT} = -200\text{ mA}$		12	13.5		
Rise time	$C_L = 1\text{ nF}$, See Note 2	$T_J = 25^\circ\text{C}$		50	150	ns
Fall time	$C_L = 1\text{ nF}$, See Note 2	$T_J = 25^\circ\text{C}$		50	150	ns
UVLO saturation	$V_{CC} = 5\text{ V}$, $I_{OUT} = 10\text{ mA}$			0.7	1.2	V
Undervoltage Lockout Section						
Start threshold	UC1842A, UC1844A		15	16	17	V
	UC1843A, UC1845A		7.8	8.4	9	
Minimum operation voltage after turn on	UC1842A, UC1844A		9	10	11	V
	UC1843A, UC1845A		7	7.6	8.2	

- NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.
 2. Not production tested.
 3. Parameter measured at trip point of latch with V_{FB} at 0 V.
 4. Gain is defined by: $A = \frac{\Delta V_{COMP}}{\Delta V_{SENSE}}$; $0 \leq V_{SENSE} \leq 0.8\text{ V}$.

UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

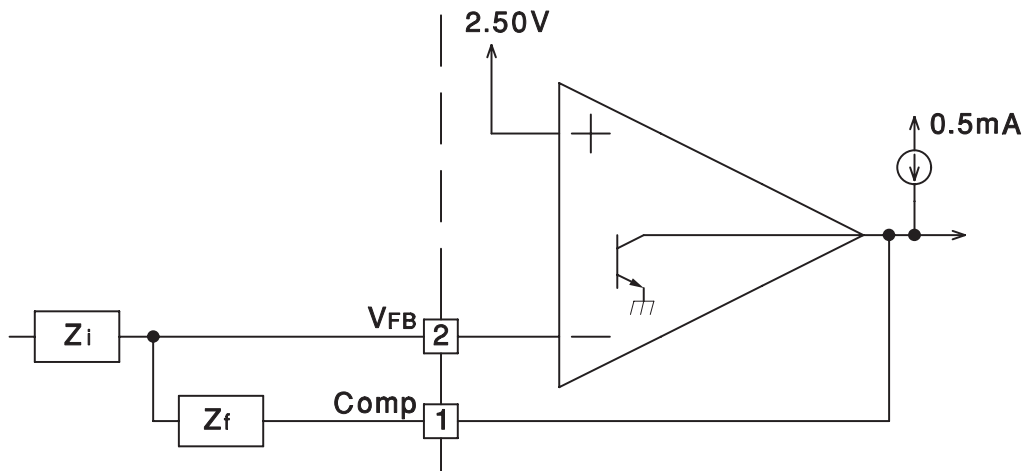
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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM Section					
Maximum duty cycle	UC1842A, UC1843A	94%	96%	100%	
	UC1844A, UC1845A	47%	48%	50%	
Minimum duty cycle				0%	
Total Standby Current					
Start-up current			0.3	0.5	mA
Operating supply current	FB = 0 V, SENSE = 0 V		11	17	mA
V_{CC} internal zener voltage	$I_{CC} = 25\text{ mA}$	30	34		V

NOTES: 1. Adjust V_{CC} above the start threshold before setting at 15 V.

PARAMETER MEASUREMENT INFORMATION



Error Amp can source and sink up to 0.5 mA and sink up to 2 mA.

Figure 1. Error Amp Configuration

UC1842A-EP, UC1843A-EP, UC1844A-EP, UC1845A-EP CURRENT-MODE PWM CONTROLLER

SGLS134C – SEPTEMBER 2002 – REVISED FEBRUARY 2006

PARAMETER MEASUREMENT INFORMATION

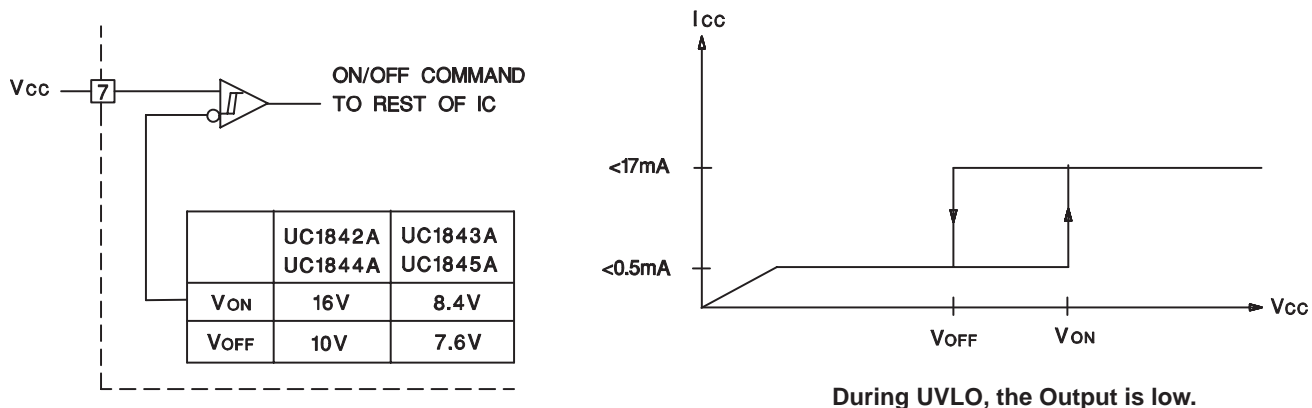
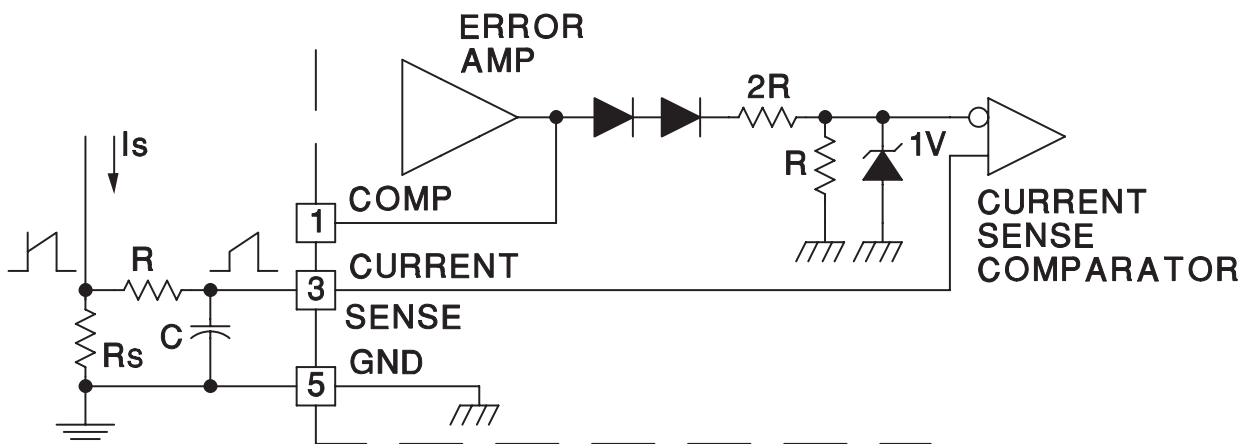


Figure 2. Under Voltage Lockout



Peak Current (I_s) is determined by the following formula:

$$I_{smax} = \frac{1V}{R_S}$$

A small RC filter may be required to suppress switch transients.

Figure 3. Current Sense Circuit

PARAMETER MEASUREMENT INFORMATION

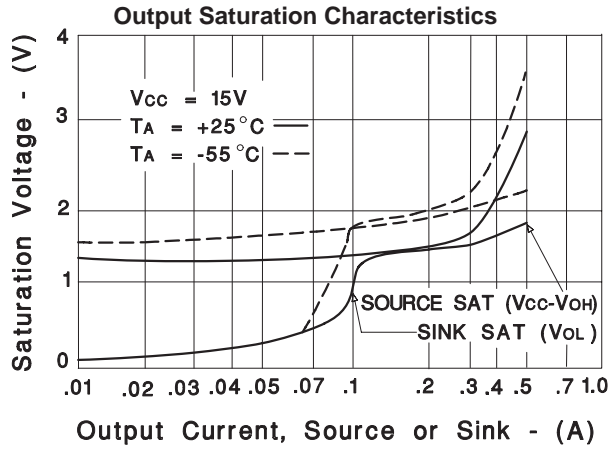


Figure 4

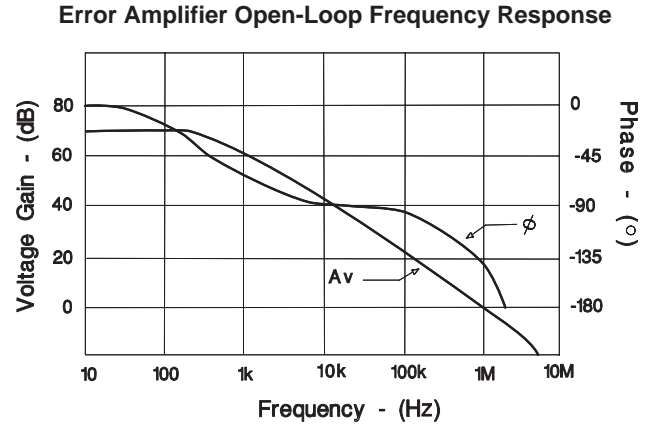


Figure 5

APPLICATION INFORMATION

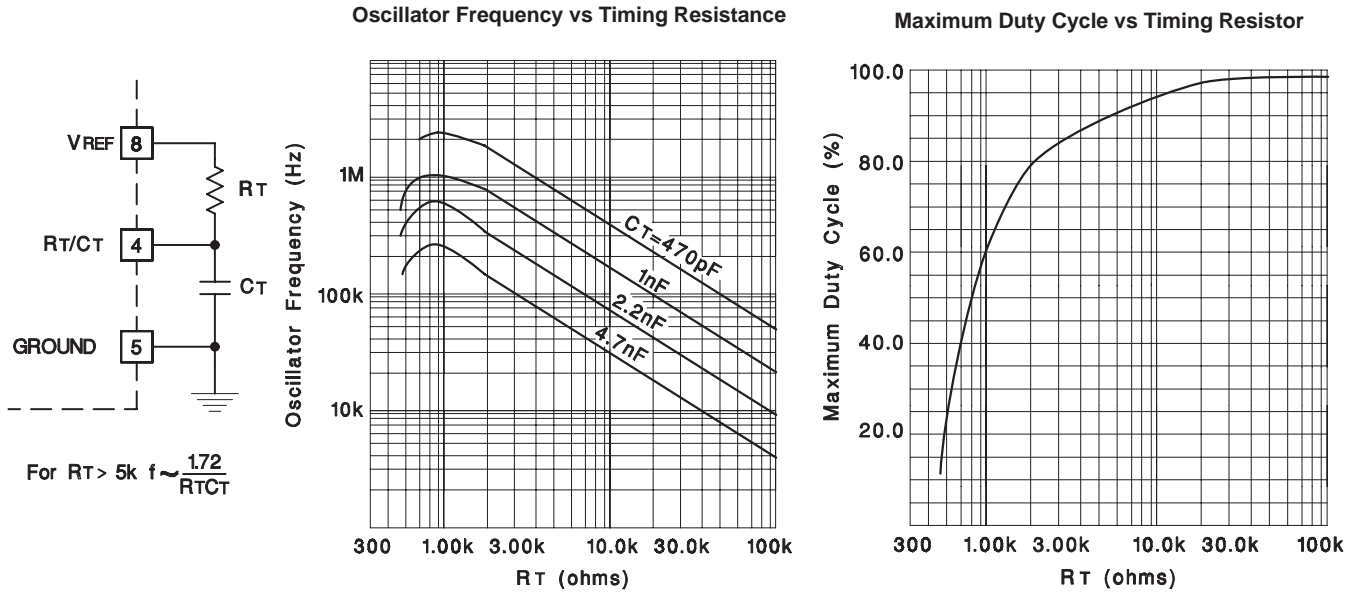
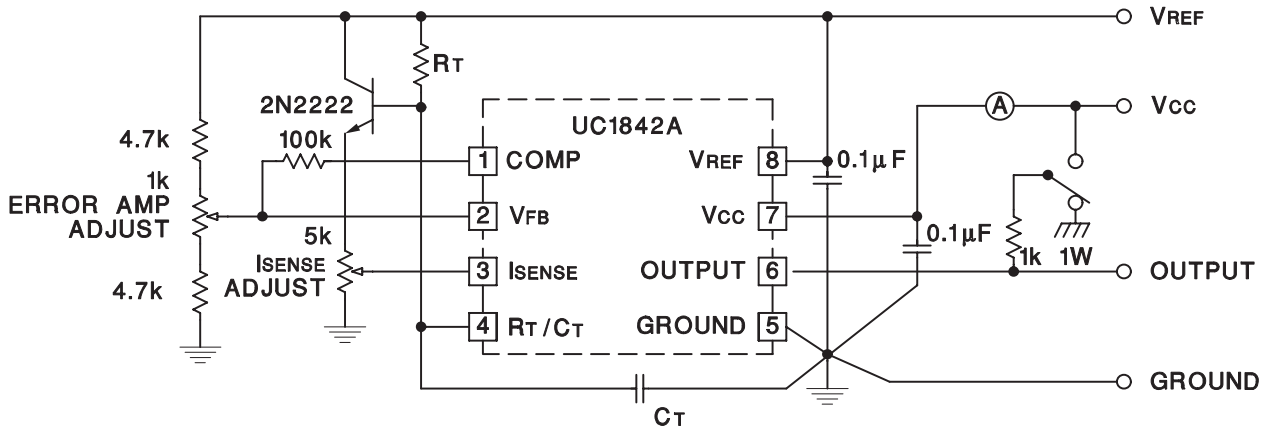


Figure 6. Oscillator

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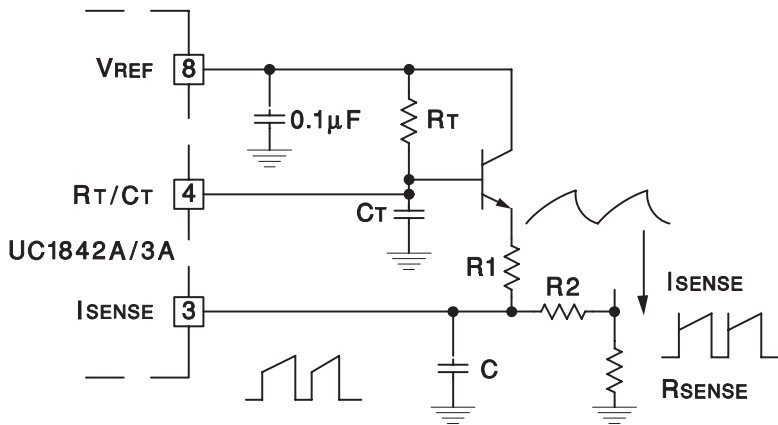
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APPLICATION INFORMATION



High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5k potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

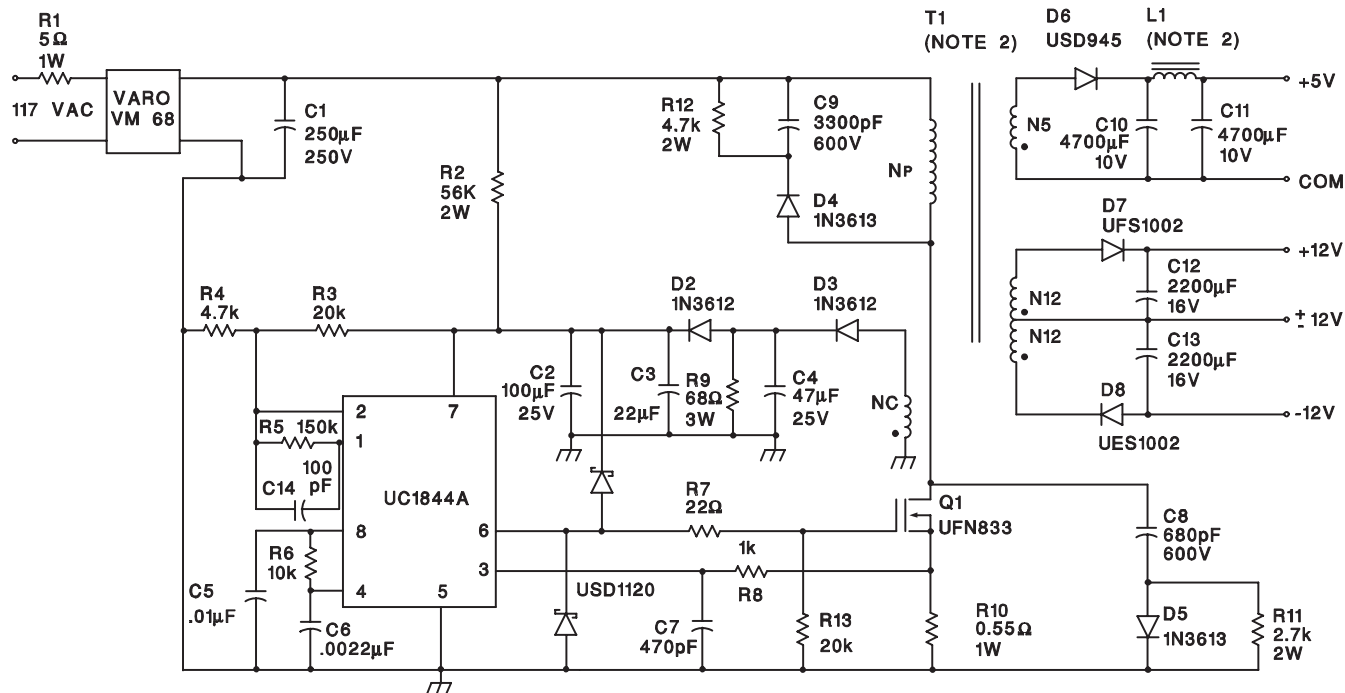
Figure 7. Open-Loop Laboratory Text Fixture



A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%. Note that capacitor, C, forms a filter with R2 to suppress the leading edge switch spikes.

Figure 8. Slope Compression

APPLICATION INFORMATION



Power Supply Specifications

1. Input Voltage 95VAC to 130VAC (50 Hz/60 Hz)
2. Line Isolation 3750 V
3. Switching Frequency 40 kHz
4. Efficiency, Full Load 70%
5. Output Voltage:
 - A. +5V, $\pm 5\%$; 1A to 4A Load
 - B. +12V, $\pm 3\%$; 0.1A to 0.3A Load Ripple voltage: 100 mV P-P Max
 - C. -12V, $\pm 3\%$; 0.1A to 0.3A Load Ripple voltage: 100 mV P-P Max

Figure 9. Off-Line Flyback Regulator

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
UC1842AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
UC1843AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
UC1843AMDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
UC1844AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
UC1845AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
UC1845AMDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
V62/03625-01YE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
V62/03625-02YE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
V62/03625-03YE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart
V62/03625-04YE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Add to cart

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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- Catalog: [UC1842A](#), [UC1843A](#), [UC1844A](#), [UC1845A](#)
- Space: [UC1842A-SP](#), [UC1843A-SP](#), [UC1844A-SP](#), [UC1845A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC1842AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	4.0	12.0	Q1
UC1843AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	4.0	12.0	Q1
UC1844AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	4.0	12.0	Q1
UC1845AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

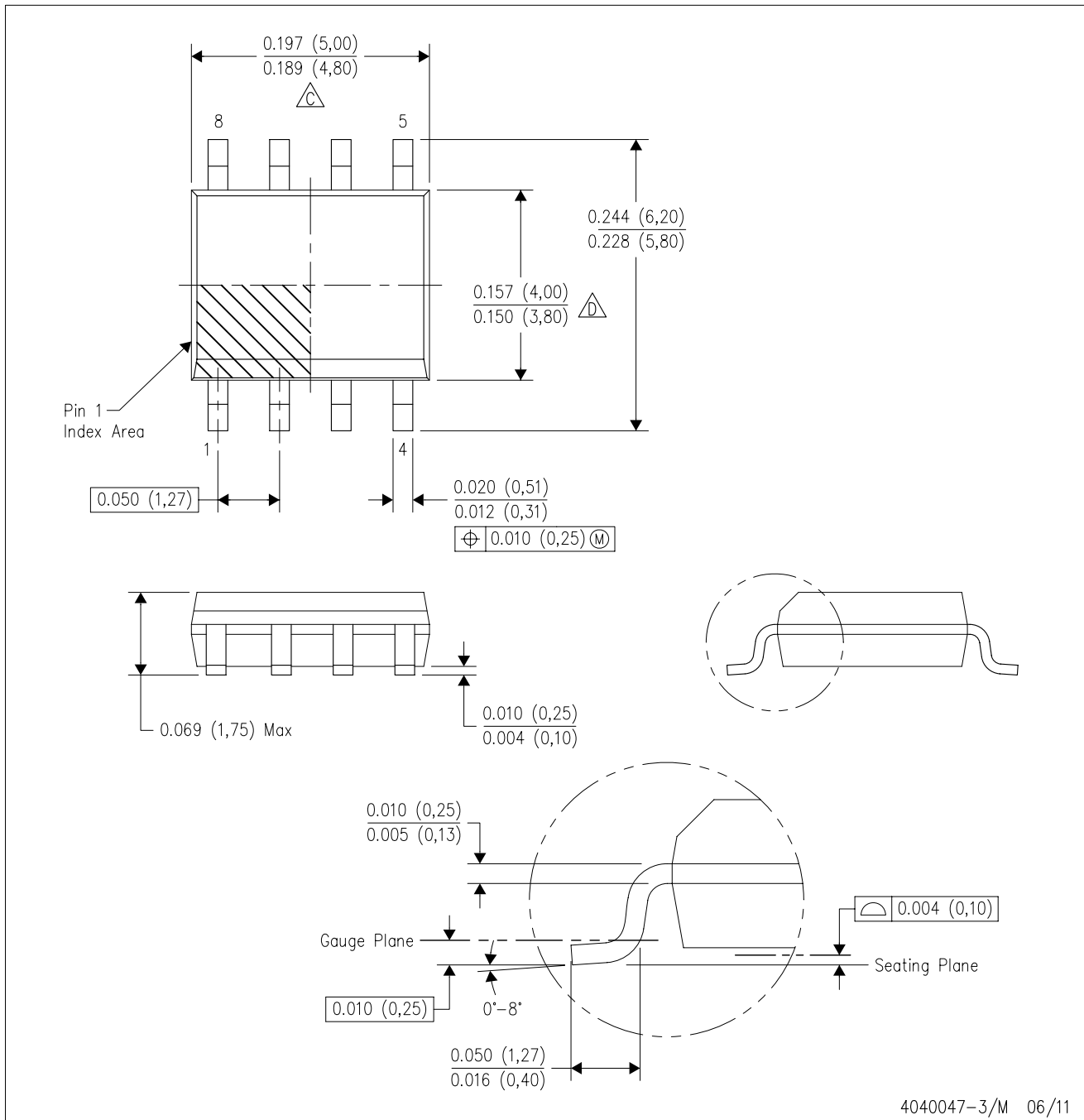


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC1842AMDREP	SOIC	D	8	2500	367.0	367.0	35.0
UC1843AMDREP	SOIC	D	8	2500	367.0	367.0	35.0
UC1844AMDREP	SOIC	D	8	2500	367.0	367.0	35.0
UC1845AMDREP	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

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