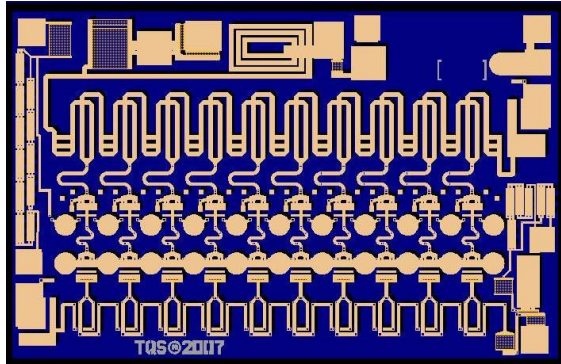
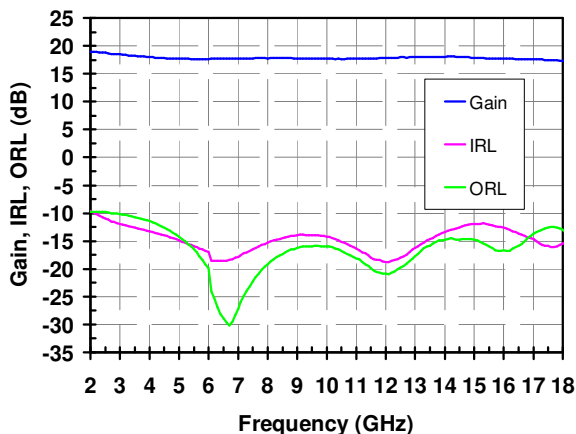
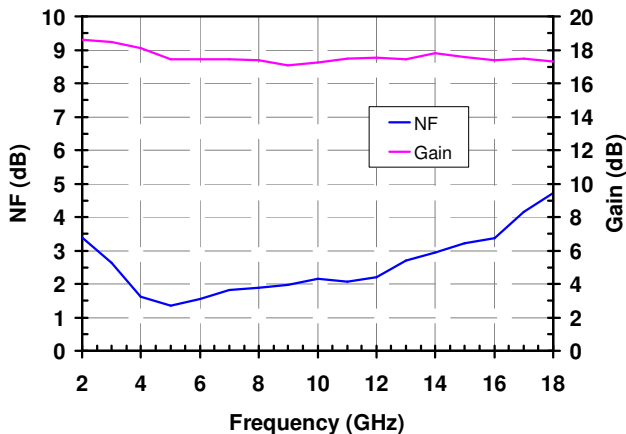


2-18 GHz Low Noise Amplifier with AGC



Measured Performance

Bias conditions: $V_d = 5\text{ V}$, $I_d = 75\text{ mA}$, $V_{g1} = -0.6\text{ V}$,
 $V_{g2} = +1.3\text{ V}$ Typical



Key Features

- Frequency Range: 2 - 18 GHz
- Midband NF: 2 dB
- Gain: 17 dB
- >30 dB adjustable gain with V_{g2}
- TOI: 29 dBm Typical
- 22 dBm Nominal P_{sat} , 18 dBm Nominal P_{1dB}
- ESD Protection circuitry on V_{g1} & V_{g2}
- Bias: $V_d = 5\text{ V}$, $I_d = 75\text{ mA}$, $V_{g1} = -0.6\text{ V}$, $V_{g2} = +1.3\text{ V}$, Typical
- Technology: 3MI 0.15 μm Power pHEMT
- Chip Dimensions: 2.09 x 1.35 x 0.1 mm

Primary Applications

- Wideband Gain Block / LNA
- X-Ku Point to Point Radio
- Electronic Warfare Applications

Product Description

The TriQuint TGA2525 is a compact LNA Gain Block MMIC with adjustable gain control (AGC). The LNA operates from 2-18 GHz and is designed using TriQuint's proven standard 0.15 μm Power pHEMT production process.

The TGA2525 provides a nominal 18 dBm of output power at 1 dB gain compression with a small signal gain of 17 dB. Greater than 30 dB adjustable gain can be achieved using V_{g2} pin. Typical noise figure is 2 dB at 8 GHz. Special circuitry on both V_{g1} and V_{g2} pins provides ESD protection.

The TGA2525 is suitable for a variety of wideband systems such as point to point radios, radar warning receivers and electronic counter measures.

The TGA2525 is 100% DC and RF tested on-wafer to ensure performance compliance. The TGA2525 has a protective surface passivation layer providing environmental robustness.

Lead-Free & RoHS compliant.

Evaluation Boards are available upon request.

Datasheet subject to change without notice.

Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	10 V	
Vd	Drain Voltage	7 V	2/
Vg1	Gate #1 Voltage Range	-2 to 0 V	
Vg2	Gate #2 Voltage Range	-2 to +3 V	
Id	Drain Current	144 mA	2/
Ig1	Gate #1 Current Range	-24 to 24 mA	3/
Ig2	Gate #2 Current Range	-24 to 24 mA	
Pin	Input Continuous Wave Power	22 dBm	2/

- 1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.
- 2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.
- 3/ ESD protection diodes on both Vg1 and Vg2 will conduct current for voltages approaching turn-on voltages. Diode turn-on voltage levels will decrease with decreasing temperature.

Table II
Recommended Operating Conditions

Symbol	Parameter 1/	Value
Vd	Drain Voltage	5 V
Id	Drain Current	75 mA
Id_Drive	Drain Current under RF Drive	130 mA
Vg1	Gate #1 Voltage	-0.6 V
Vg2	Gate #2 Voltage	1.3 V

- 1/ See assembly diagram for bias instructions.

Table III
RF Characterization Table

Bias: Vd = 5 V, Id = 75 mA, Vg1 = -0.6 V, Vg2 = +1.3 V typical

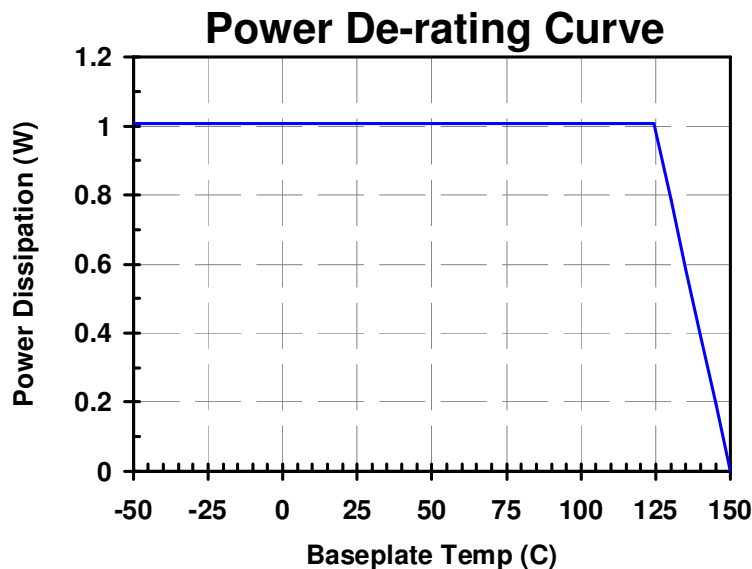
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOMINAL	MAX	UNITS
Gain	Small Signal Gain	f = 2 - 14 GHz f = 14 - 18 GHz	14 14	17 17	- -	dB
IRL	Input Return Loss	f = 2 GHz f = 3 - 14 GHz f = 14 - 18 GHz	8.5 10 10	15 15 12	- - -	dB
ORL	Output Return Loss	f = 2 - 3 GHz f = 4 - 18 GHz	9 10	15 15	- -	dB
Psat	Saturated Output Power	f = 2 - 14 GHz f = 14 - 18 GHz	- -	22 20	- -	dBm
P1dB	Output Power @ 1dB Compression	f = 2 GHz f = 4, 8 GHz f = 10, 14 GHz f = 18 GHz	14 15 13 11	18 17 17 15	- - - -	dBm
TOI	Output TOI	f = 2 - 14 GHz f = 14 - 18 GHz	- -	29 25	- -	dBm
NF	Noise Figure	f = 2 - 14 GHz f = 14 - 18 GHz	- -	2 4	4 6	dB
S21/T	S21 Temperature Dependence	f = 2 - 18 GHz	-	-0.008	-	dB / °C

Table IV
Power Dissipation and Thermal Properties

Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 70 °C	Pd = 1.01 W Tchannel = 96 °C Tm = 9.7 E+8 Hrs	1/ 2/
Thermal Resistance, θ_{jc}	Vd = 5 V Id = 75 mA Pd = 0.375 W	θ_{jc} = 41.4 (°C/W) Tchannel = 86 °C Tm = 4.3 E+9 Hrs	
Thermal Resistance, θ_{jc} Under RF Drive	Vd = 5 V Id = 120 mA Pout = 22 dBm Pd = 0.45 W	θ_{jc} = 41.4 (°C/W) Tchannel = 89 °C Tm = 2.7 E+9 Hrs	
Mounting Temperature	30 Seconds	320 °C	
Storage Temperature		-65 to 150 °C	

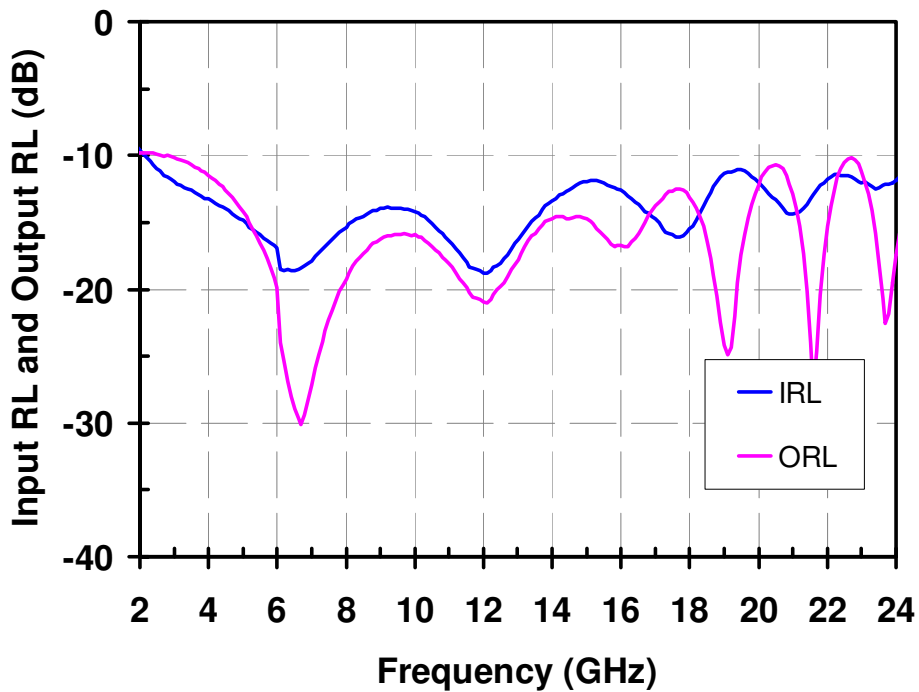
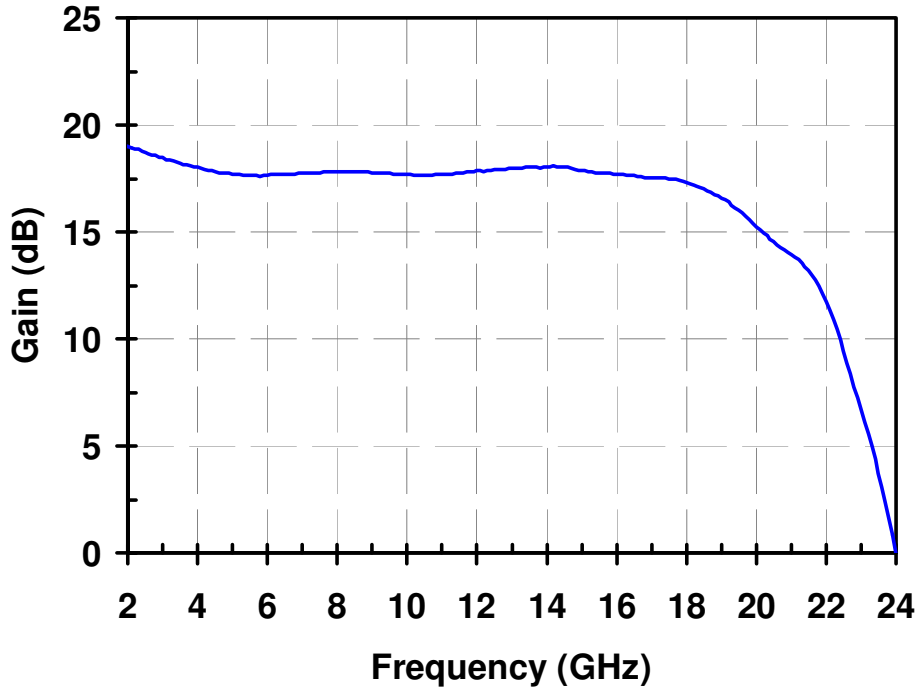
- 1/ For a median life of 1E+6 hours, Power Dissipation is limited to

$$Pd(max) = (150\text{ °C} - Tbase\text{ °C})/\theta_{jc}.$$
- 2/ Channel operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.



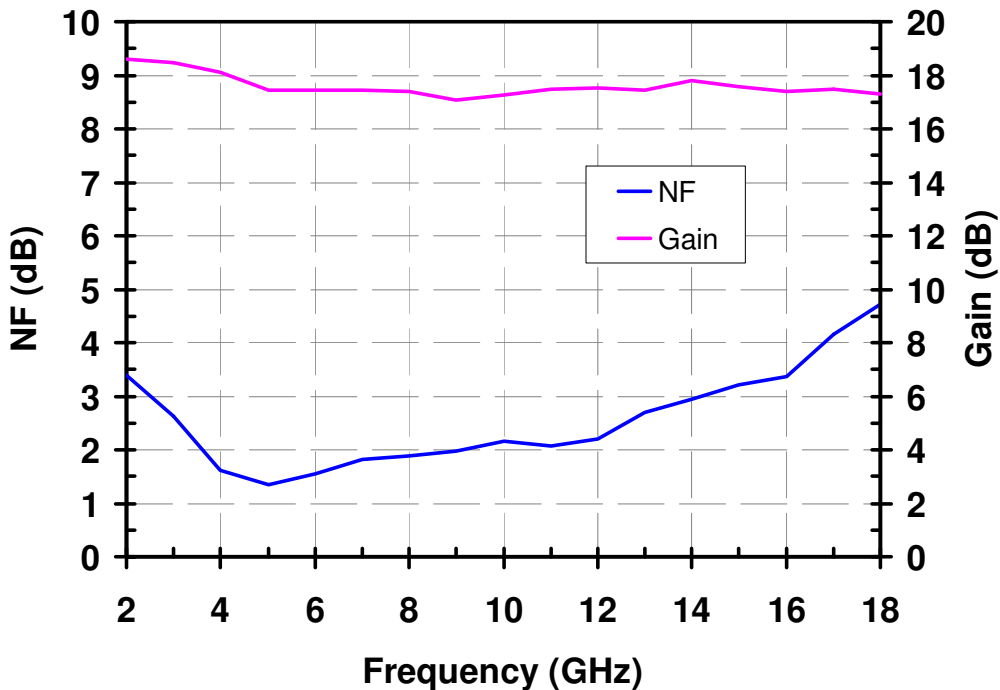
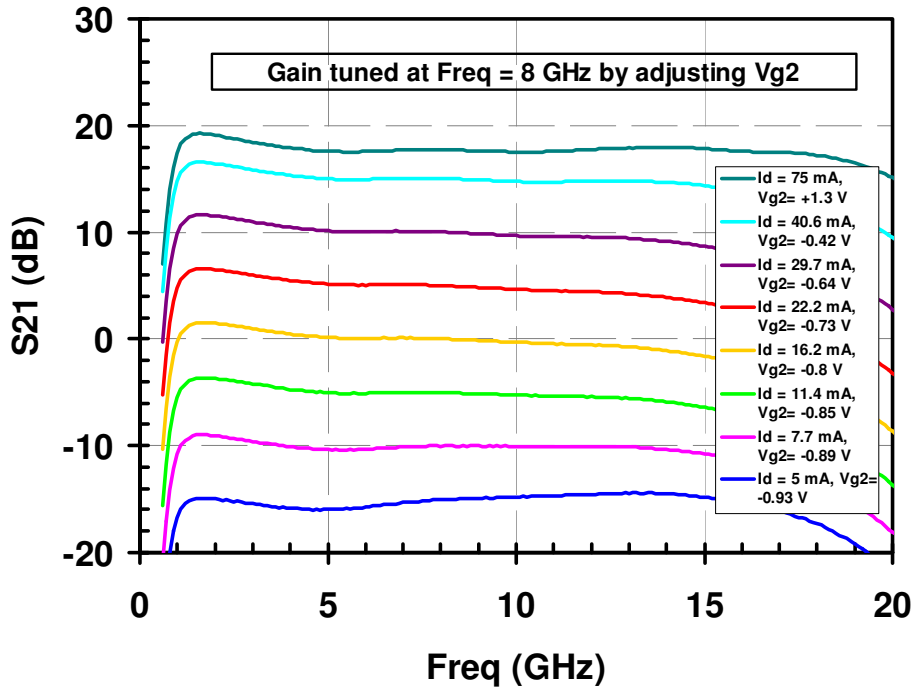
Measured Data

Bias conditions: $V_d = 5\text{ V}$, $I_d = 75\text{ mA}$, $V_{g1} = -0.6\text{ V}$, $V_{g2} = +1.3\text{ V}$ Typical



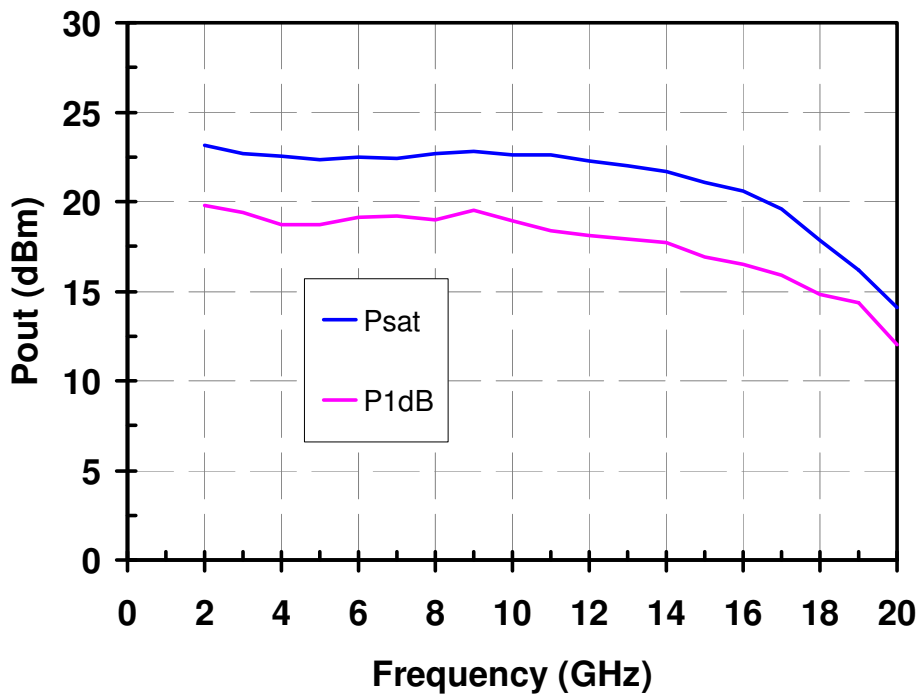
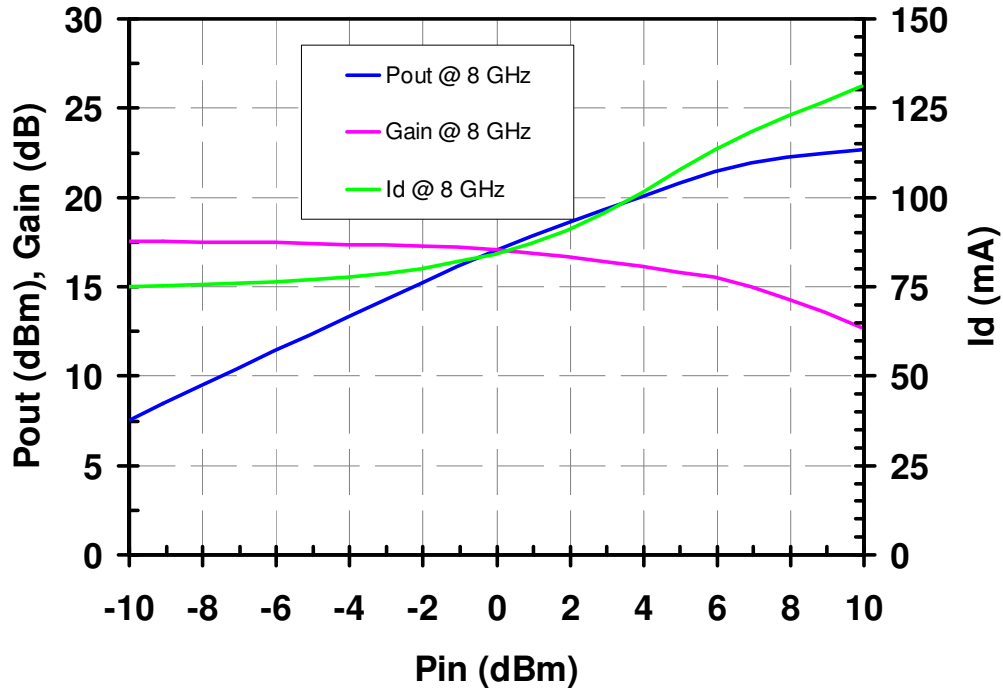
Measured Data

Bias conditions: $V_d = 5\text{ V}$, $I_d = 75\text{ mA}$, $V_{g1} = -0.6\text{ V}$, $V_{g2} = +1.3\text{ V}$ Typical



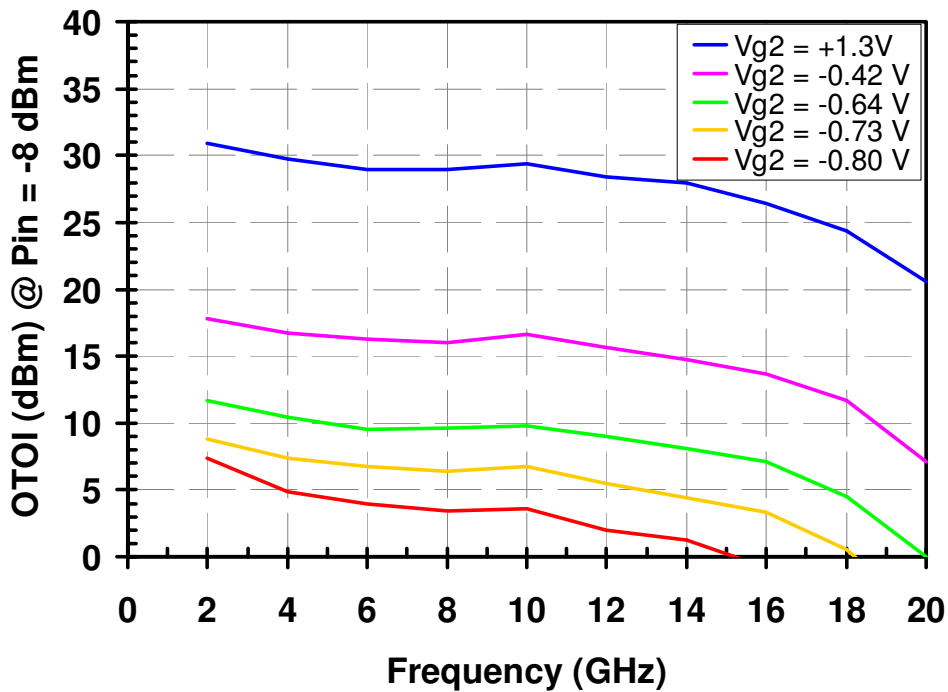
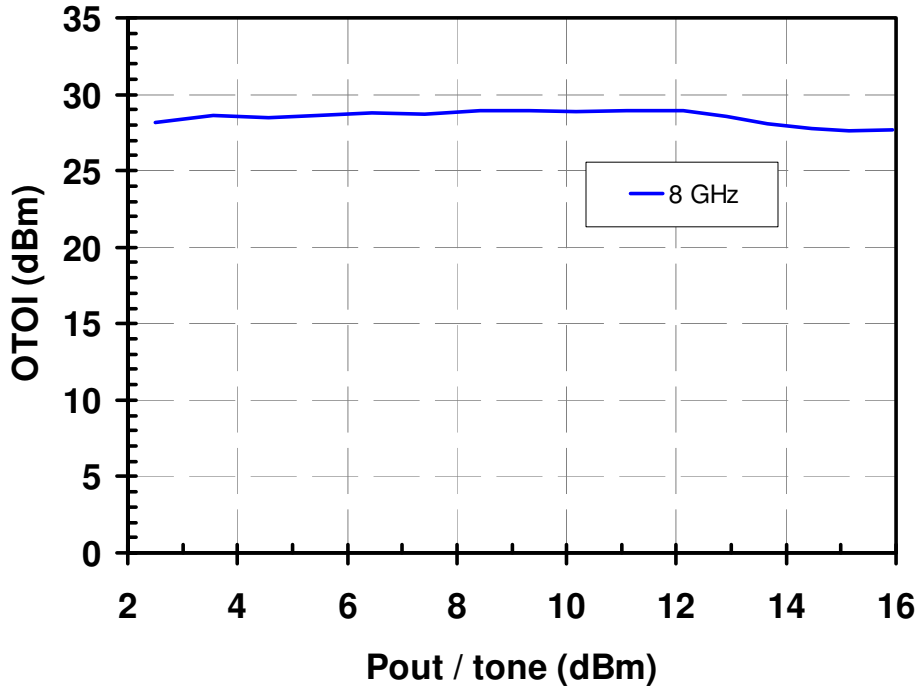
Measured Data

Bias conditions: $V_d = 5\text{ V}$, $I_d = 75\text{ mA}$, $V_{g1} = -0.6\text{ V}$, $V_{g2} = +1.3\text{ V}$ Typical

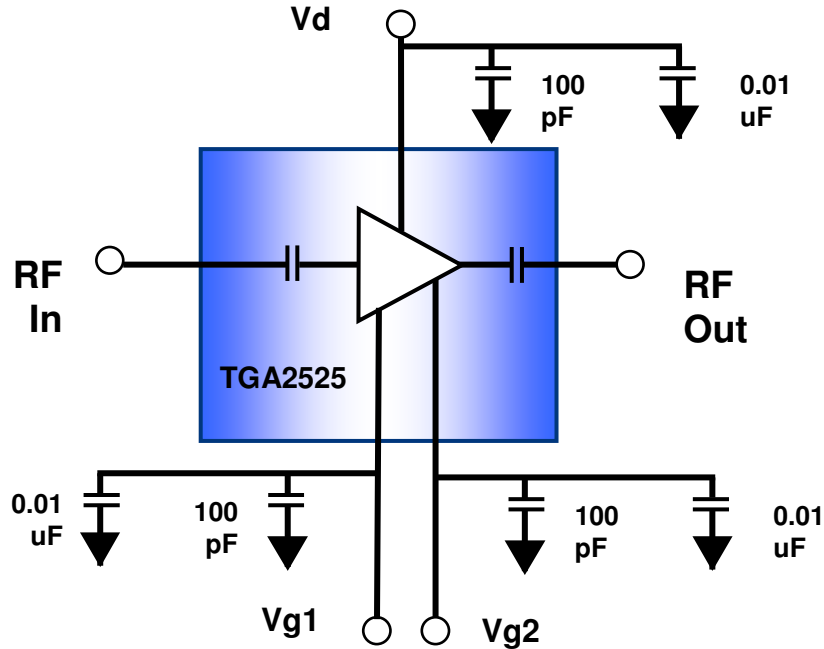


Measured Data

Bias conditions: $V_d = 5\text{ V}$, $I_d = 75\text{ mA}$, $V_{g1} = -0.6\text{ V}$, $V_{g2} = +1.3\text{ V}$ Typical



Electrical Schematic



Bias Procedures

Bias-up Procedure

Vg1 set to -1.5 V

Vd set to +5 V

Vg2 set to +1 V

Adjust Vg1 more positive until Id is 75 mA. This will be ~ Vg1 = -0.6 V

Apply RF signal to input

Adjust Vg2 to obtain desired gain.

Bias-down Procedure

Reduce Vg2 to +1 V

Turn off RF supply

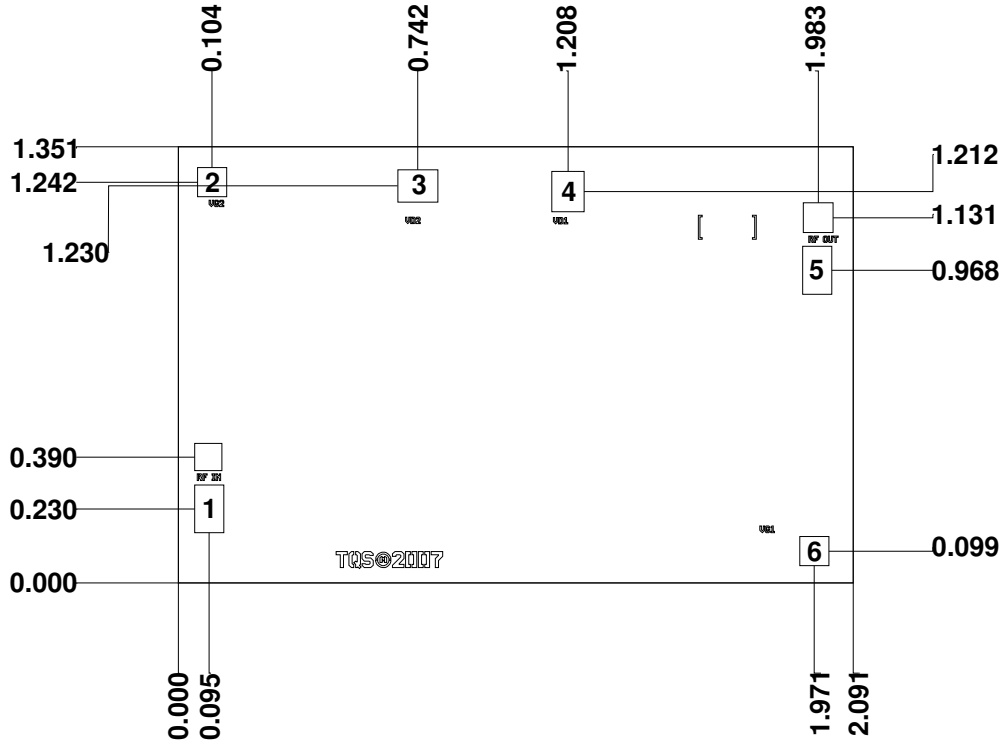
Reduce Vg1 to -1.5V. Ensure Id ~ 0 mA

Vg2 to 0 V

Turn Vd to 0 V

Turn Vg1 to 0 V

Mechanical Drawing

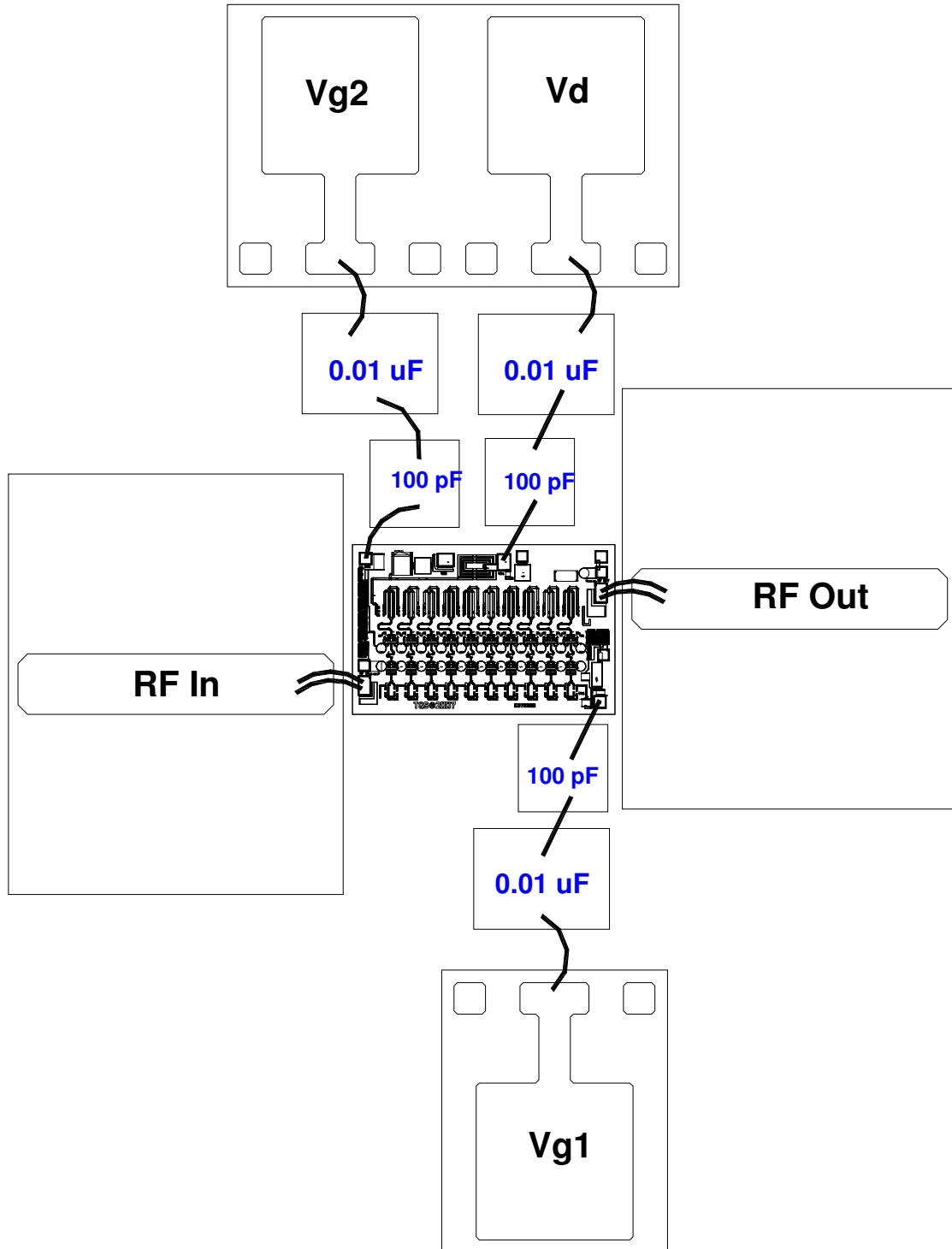


Units: millimeters
 Thickness: 0.10
 Die x,y size tolerance: +/- 0.050
 Chip edge to bond pad dimensions are shown to center of pad
 Ground is backside of die

Bond Pad #1	RF In	0.090 x 0.148	Bond Pad #4	Vd1	0.100 x 0.125
Bond Pad #2	Vg2	0.090 x 0.090	Bond Pad #5	RF Out	0.090 x 0.148
Bond Pad #3	Vd2 (Not used)	0.125 x 0.100	Bond Pad #6	Vg1	0.090 x 0.090

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Recommended Assembly Diagram



GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Assembly Notes

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment (i.e. epoxy) can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.

Reflow process assembly notes:

- Use AuSn (80/20) solder and limit exposure to temperatures above 300°C to 3-4 minutes, maximum.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- Do not use any kind of flux.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Devices with small pad sizes should be bonded with 0.0007-inch wire.

Ordering Information

Part	ECCN	Package Style
TGA2525	EAR99	GaAs MMIC Die

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.