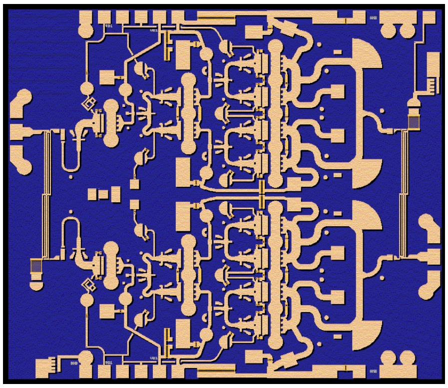
**TriQuint SEMICONDUCTOR**

# TGA4022

# K Band High Power Amplifier



## Key Features

- Frequency Range: 18 - 23 GHz
- 26 dB Nominal Gain
- 32.5 dBm Nominal P1dB
- 15dB Nominal Return Loss
- Bias 7.0 V, 840 mA
- 0.25 um 2MI pHEMT Technology
- Chip Dimensions 3.65 x 3.14 x 0.10 mm
  (0.144 x 0.124 x 0.004 in)

## Primary Applications

- Point-to-Point Radio
- Point-to-Multipoint Communications
- K-Band Sat-Com

## Product Description

The TriQuint TGA4022 is a compact High Power Amplifier MMIC for K-band applications. The part is designed using TriQuint's proven standard 0.25 um power pHEMT production process.

The TGA4022 nominally provides 32.5dBm of Output Power @ 1dB Gain Compression from 18 - 23GHz. The MMIC also provides 26dB Gain and 15dB typical Return Loss.

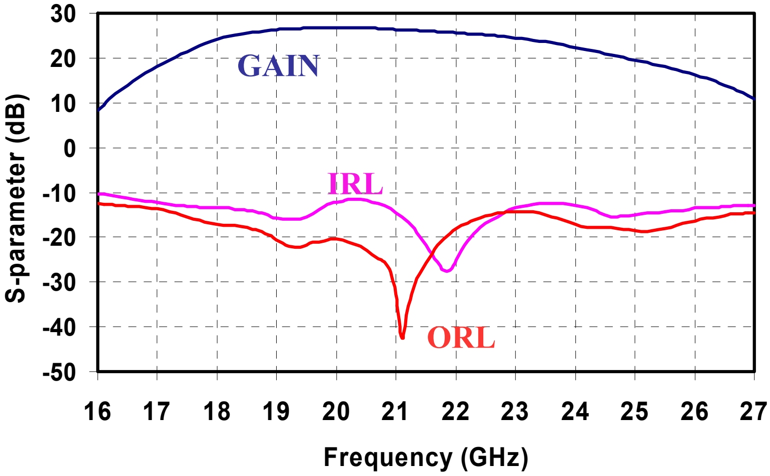
The part is ideally suited for markets such as Point-to-Point Radio, Point-to-Multipoint Communications, and K-Band Satellite Communications both commercial and military.

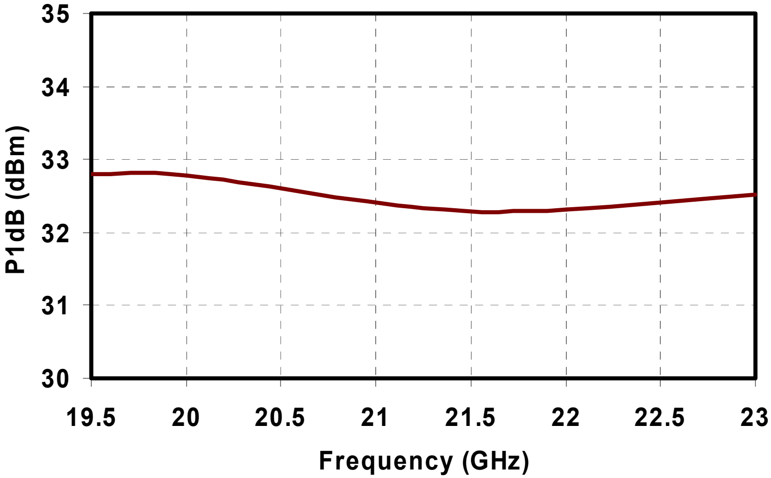
The TGA4022 is 100% DC and RF tested on-wafer to ensure performance compliance.

Lead-Free & RoHS compliant.

## Measured Fixtured Data

**Bias Conditions: Vd =7.0 V, Id =840 mA**





*Datasheet subject to change without notice.*

## TABLE I
## MAXIMUM RATINGS 1/

| SYMBOL | PARAMETER | VALUE | NOTES |
|---|---|---|---|
| Vd | Drain Voltage | 8 V | 2/ |
| Vg | Gate Voltage Range | -1 TO + 0 V | |
| Id | Drain Current | 1.5 A | 2/ 3/ |
| $\lvert Ig \rvert$ | Gate Current | 56 mA | 3/ |
| $P_{IN}$ | Input Continuous Wave Power | 26 dBm | |
| $P_D$ | Power Dissipation | 12 W | 2/ 4/ |
| $T_{CH}$ | Operating Channel Temperature | 200 °C | 5/ 6/ |
| | Mounting Temperature (30 Seconds) | 320 °C | |
| $T_{STG}$ | Storage Temperature | -65 to 150 °C | |

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed $P_D$.

3/ Total current for the entire MMIC.

4/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is 2.3E4 hrs.

5/ Junction operating temperature will directly affect the device median time to failure (Tm). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

6/ These ratings apply to each individual FET.

## TABLE II
## DC PROBE TESTS
(Ta = 25 °C, Nominal)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| $I_{DSS,Q1}$ | Saturated Drain Current | 120 | 180 | 240 | mA |
| $G_{M,Q1}$ | Transconductance | 162 | 240 | 318 | mS |
| $V_{BVGS}$ | Breakdown Voltage Gate_Source | -30 | -15 | -12 | V |
| $V_{BVGD}$ | Breakdown Voltage Gate_Drain | -30 | -16 | -12 | V |
| $V_P$ | Pinch-off Voltage | -1.35 | -1 | -0.65 | V |

Q1 is 600 um FET

## TABLE III
## ELECTRICAL CHARACTERISTICS
(Ta = 25 $^0$C Nominal)

| PARAMETER | TYPICAL | UNITS |
|---|---|---|
| Frequency Range | 18 - 23 | GHz |
| Drain Voltage, Vd | 7.0 | V |
| Drain Current, Id | 840 | mA |
| Small Signal Gain, S21 | 26 | dB |
| Input Return Loss, S11 | 15 | dB |
| Output Return Loss, S22 | 20 | dB |
| Pout @ 1dB Gain Compression, P1dB | 32.5 | dBm |

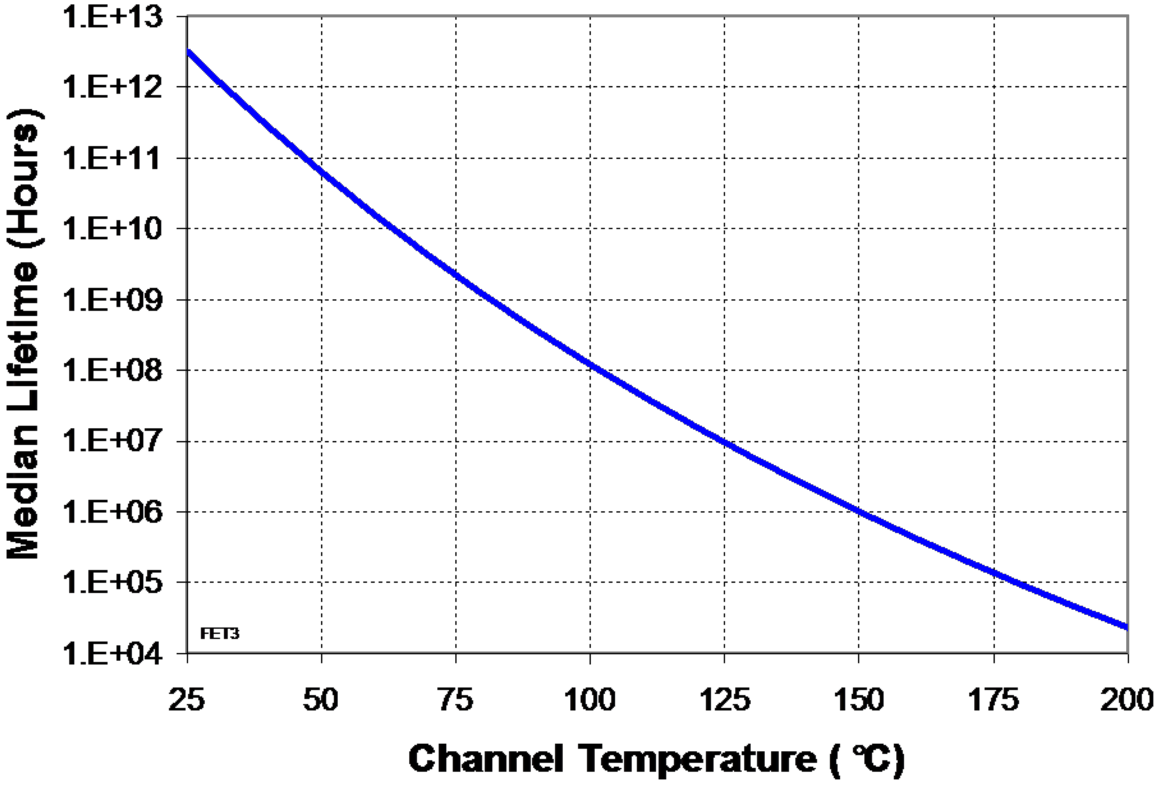
Note: Temperature coefficient on Gain -0.036 dB/$^0$C

## TABLE IV
## THERMAL INFORMATION

| PARAMETER | TEST CONDITIONS | $T_{CH}$ (°C) | $\theta_{JC}$ (°C/W) | Tm (HRS) |
|---|---|---|---|---|
| $\theta_{JC}$ Thermal Resistance (channel to backside of Carrier) | Vd = 7 V<br>Id = 1 A<br>Pdiss = 7 W | 146 | 10.8 | 1.5 E+6 |

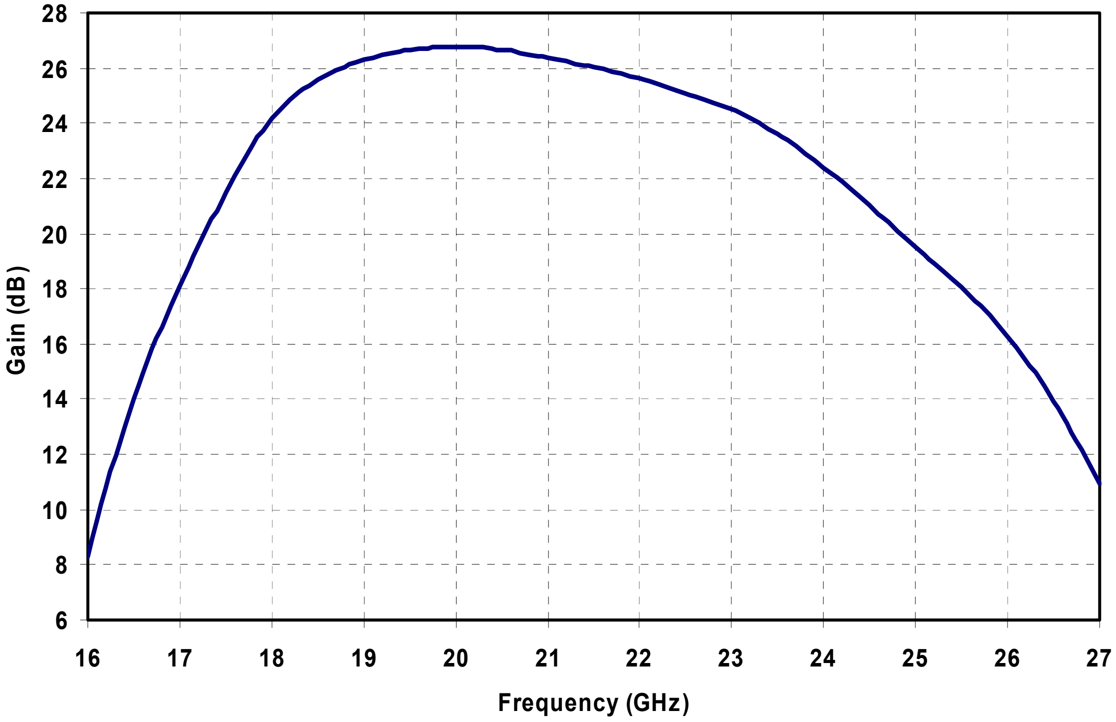
Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70 °C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

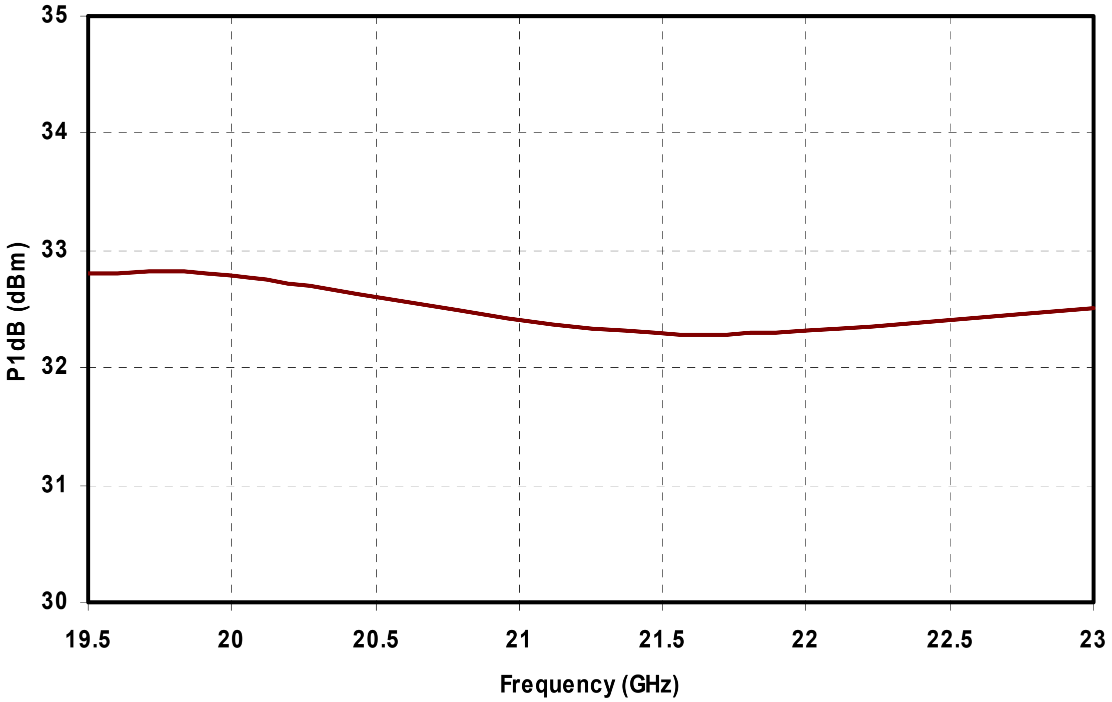
Median Lifetime (Tm) vs. Channel Temperature



# Preliminary Measured Data

**Bias Conditions: Vd = 7.0 V, Id = 840 mA, Room Temperature**





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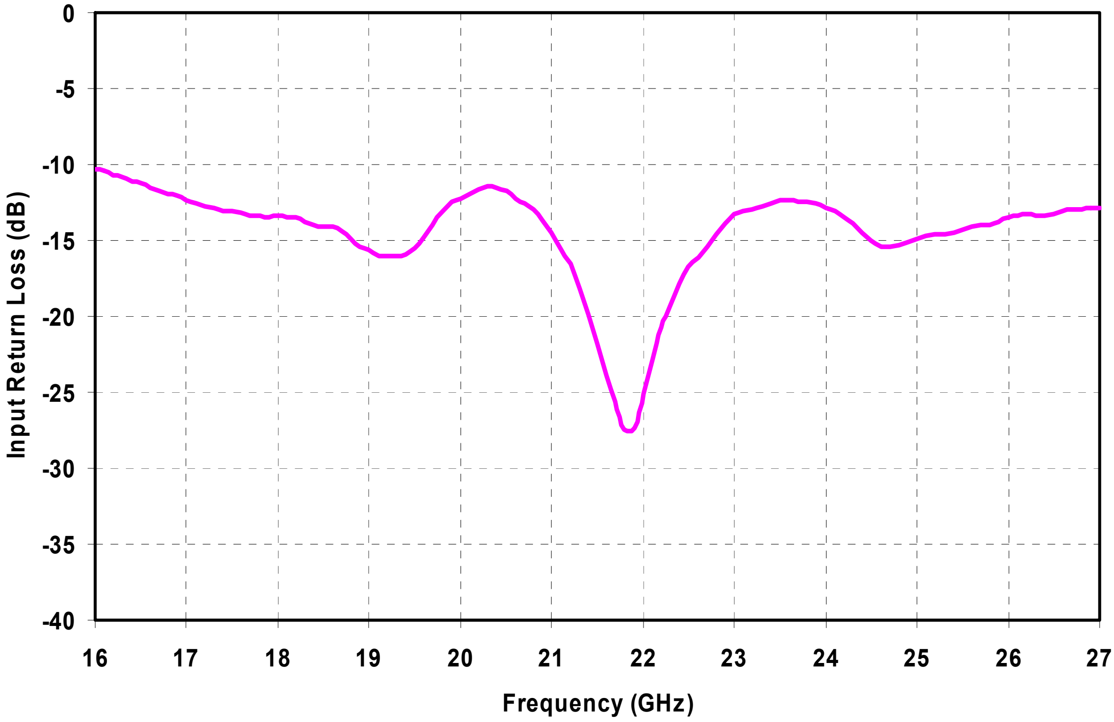

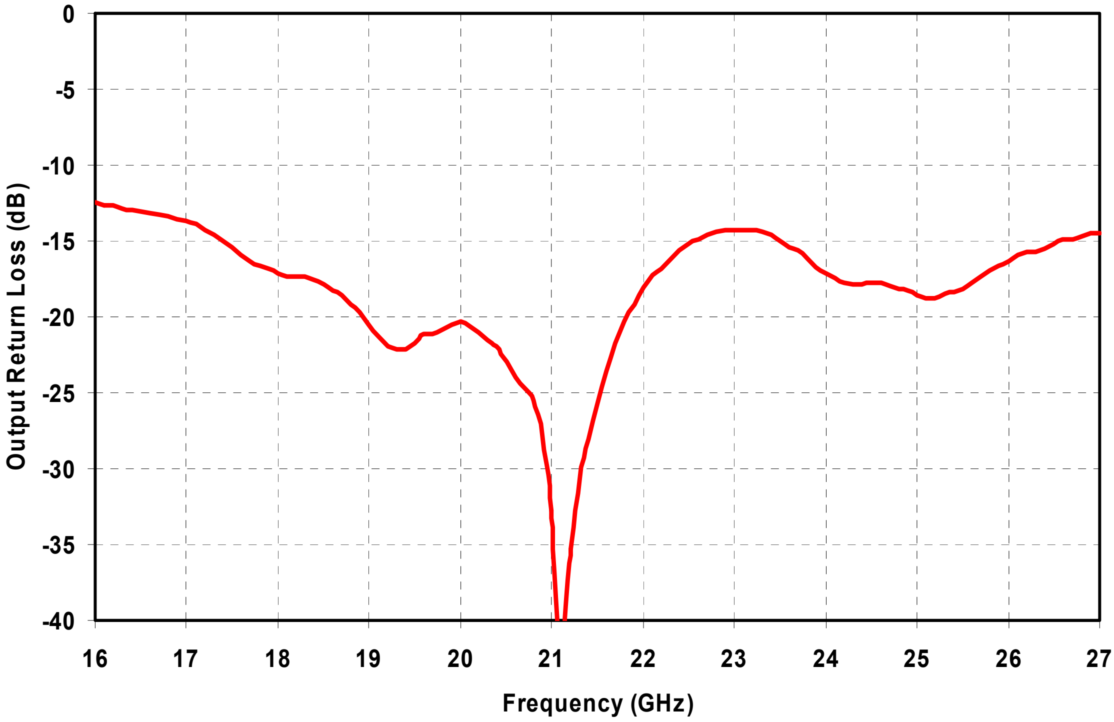

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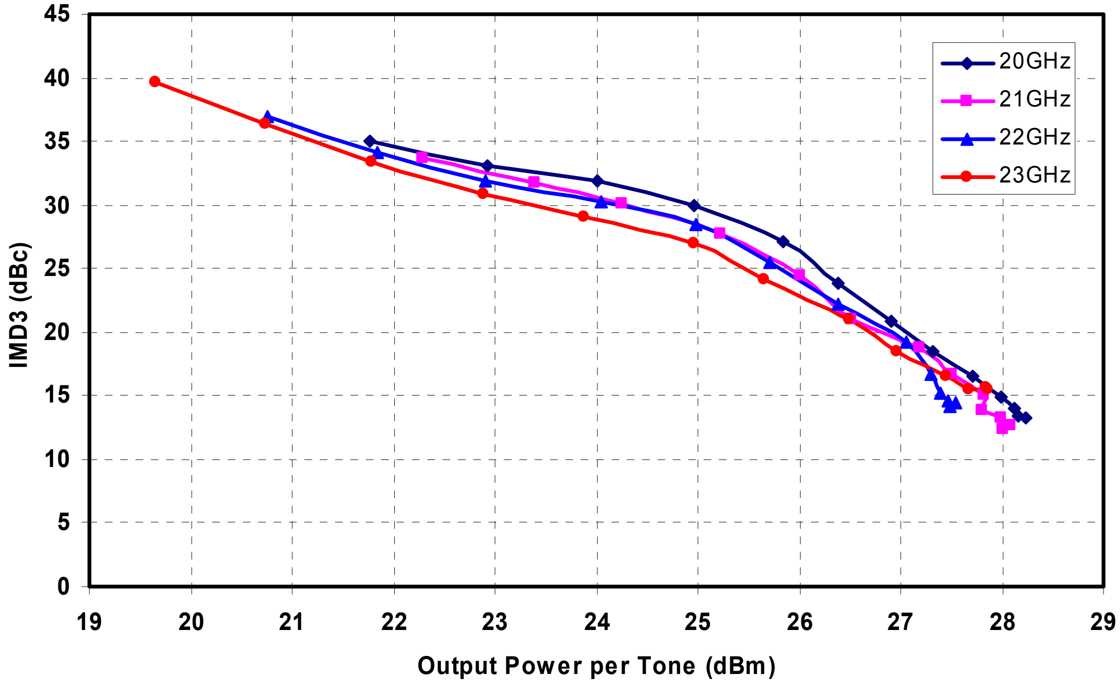
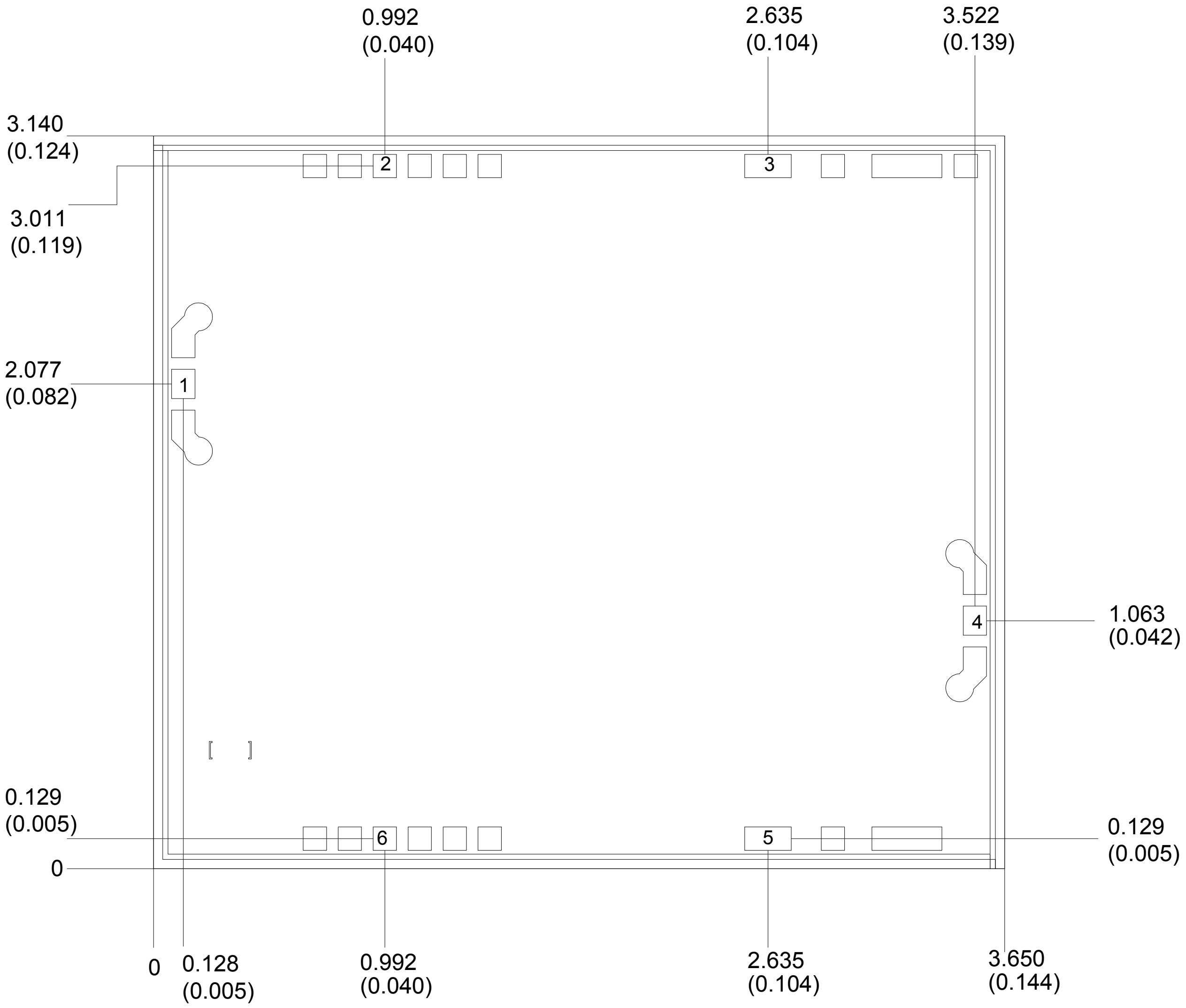


## Mechanical Drawing



Units: Millimeters (inches)

Thickness: 0.100 (0.004)

Chip size to bond pad dimensions are shown to center of bond pad

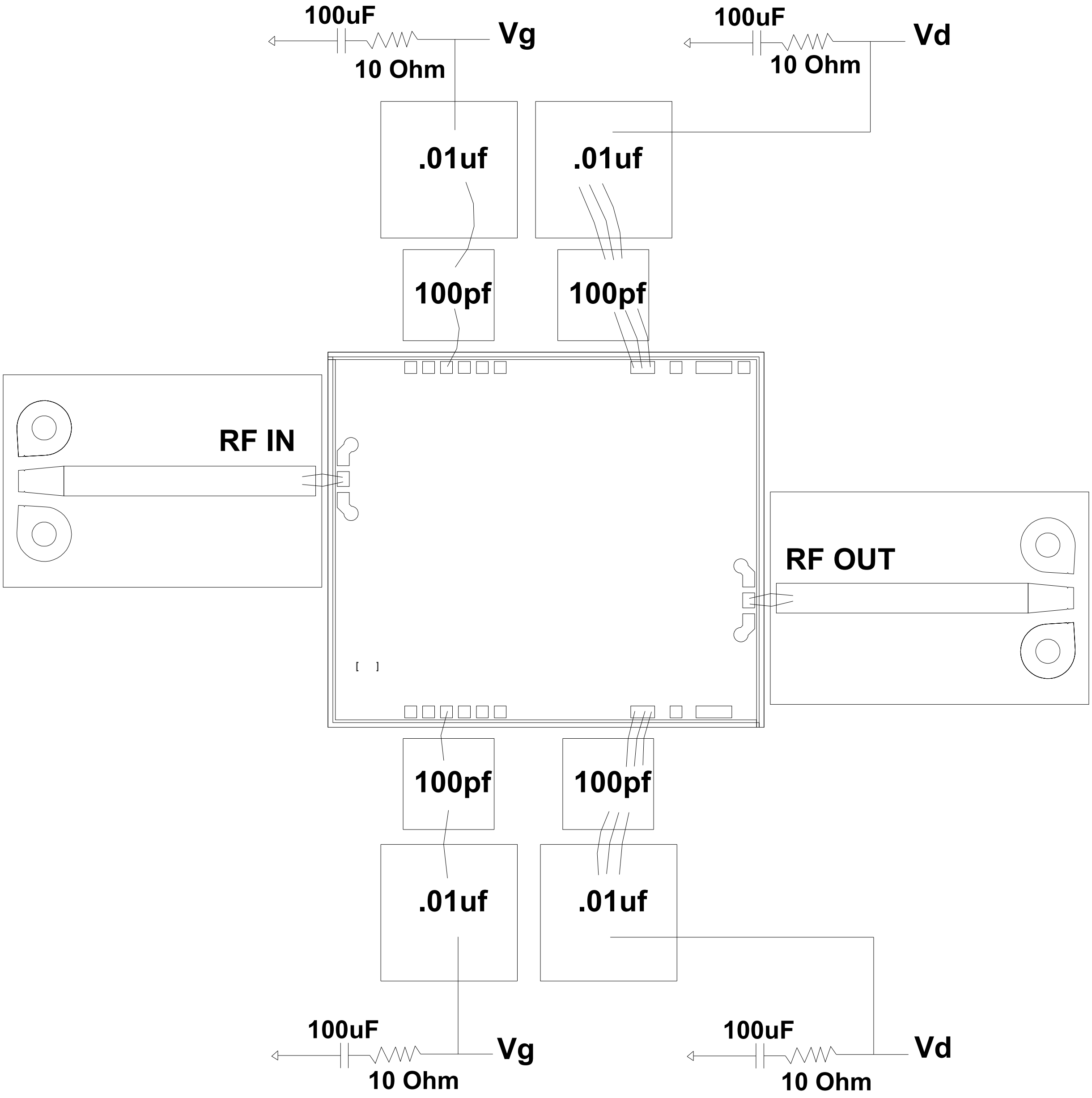
Chip size tolerance: +/- 0.051 (0.002)

RF Ground is backside of MMIC

| | | | |
|---|---|---|---|
| Bond pad #1: | (RF In) | 0.100 X 0.125 | (0.004 X 0.005) |
| Bond pad #2, #6: | (Vg) | 0.100 X 0.100 | (0.004 X 0.004) |
| Bond pad #3, #5: | (Vd) | 0.200 X 0.100 | (0.008 X 0.004) |
| Bond pad #4: | (RF Out) | 0.100 X 0.125 | (0.004 X 0.005) |

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***

## Recommended Chip Assembly Diagram



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## Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above $300^0$C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is $200^0$C.

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