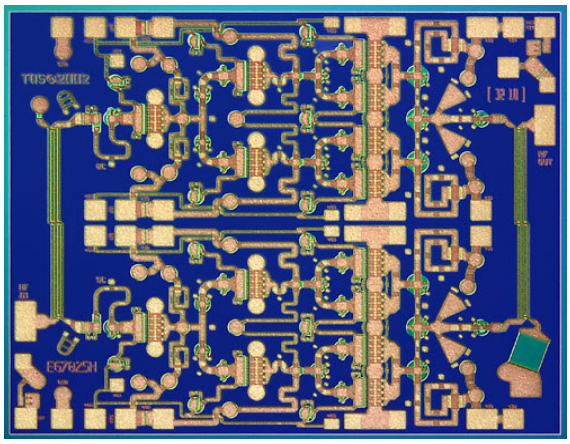
27 - 31 GHz 2W Balanced Power Amplifier TGA4513

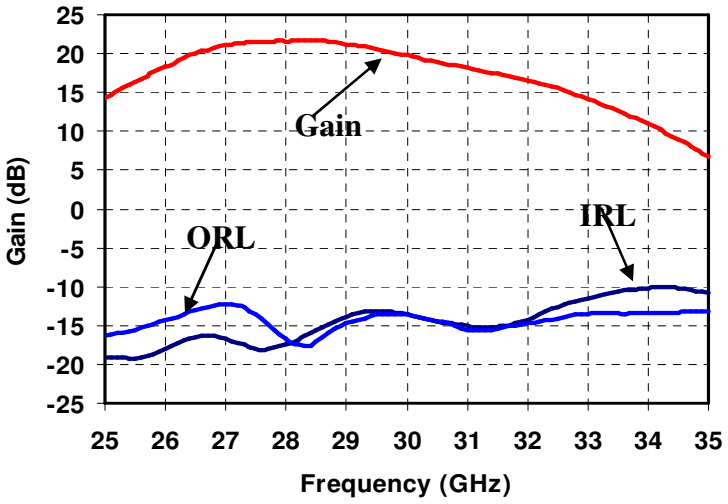


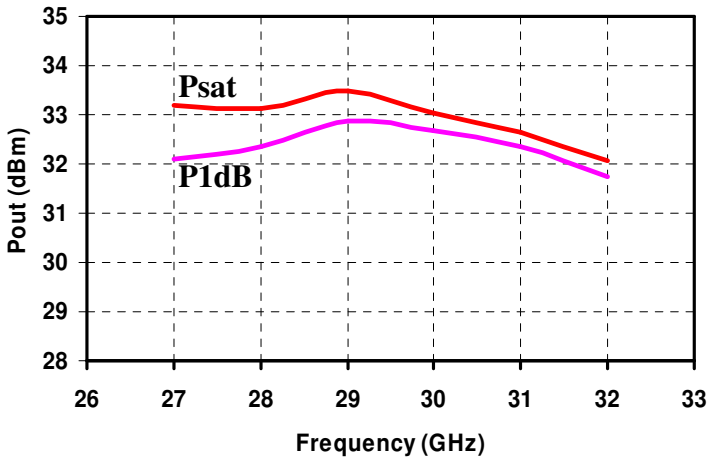
Key Features

- 27 - 31 GHz Bandwidth
- > 32 dBm P1dB
- 33 dBm Psat
- 20 dB Nominal Gain
- IMR3 is 37 dBc @ 18 dBm SCL
- 14 dB Nominal Return Loss
- Bias: 6 V, 840 mA
- 0.25 um 3MI MMW pHEMT Technology
- Chip Dimensions: 2.8 x 2.2 x 0.1 mm (0.110 x 0.087 x 0.004) in

Measured Data

Bias Conditions: Vd = 6 V, Id = 840 mA





Primary Applications

- Satellite Ground Terminal
- Point to Point Radio
- Point to Multi Point Radio
- LMDS

Note: This device is early in the characterization process prior to finalizing all electrical specifications. Specifications are subject to change without notice.

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	VALUE	NOTES
V^+	Positive Supply Voltage	7 V	2/
V^-	Negative Supply Voltage Range	-3 TO 0 V	
I^+	Positive Supply Current	1.86 A	2/
$\|I_G\|$	Gate Supply Current	18 mA	3/
P_{IN}	Input Continuous Wave Power	22 dBm	
P_D	Power Dissipation	7.18 W	2/ 4/
T_{CH}	Operating Channel Temperature	150 ^{0}C	5/ 6/
T_M	Mounting Temperature (30 Seconds)	320 ^{0}C	
T_{STG}	Storage Temperature	-65 to 150 ^{0}C	

1/ These ratings represent the maximum operable values for this device.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.

3/ Total current for the entire MMIC.

4/ When operated at this bias condition with a base plate temperature of 70 ^{o}C, the median life is 1.0E+6 hrs.

5/ Junction iperating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

6/ These ratings apply to each individual FET.

TABLE II
DC PROBE TESTS
(T_A = 25 °C Nominal)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	VALUE
I_{DSS1}	Saturated Drain Current	60	282	V
G_{M1}	Transconductance	132	318	mS
V_{BVGS1}	Breakdown Voltage gate-source	-30	-8	V
V_{BVGD1}	Breakdown Voltage gate-drain	-30	-11	V
$V_{P1,8}$	Pinch-off Voltage	-1.5	-0.5	V

TABLE III
ELECTRICAL CHARACTERISTICS
(Ta = 25 ^{0}C, Nominal)

PARAMETER	TYPICAL	UNITS
Drain Operating	6	V
Quiescent Current	840	mA
Small Signal Gain, S21	20	dB
Input Return Loss, S11	14	dB
Output Return Loss, S22	14	dB
Reverse Isolation, S12	-40	dB
Output Power @ 1 dB Compression Gain, P1dB	> 32	dBm
Power @ saturated, Psat	33	dBm
IMR3 @ 18 dBm SCL	37	dBc

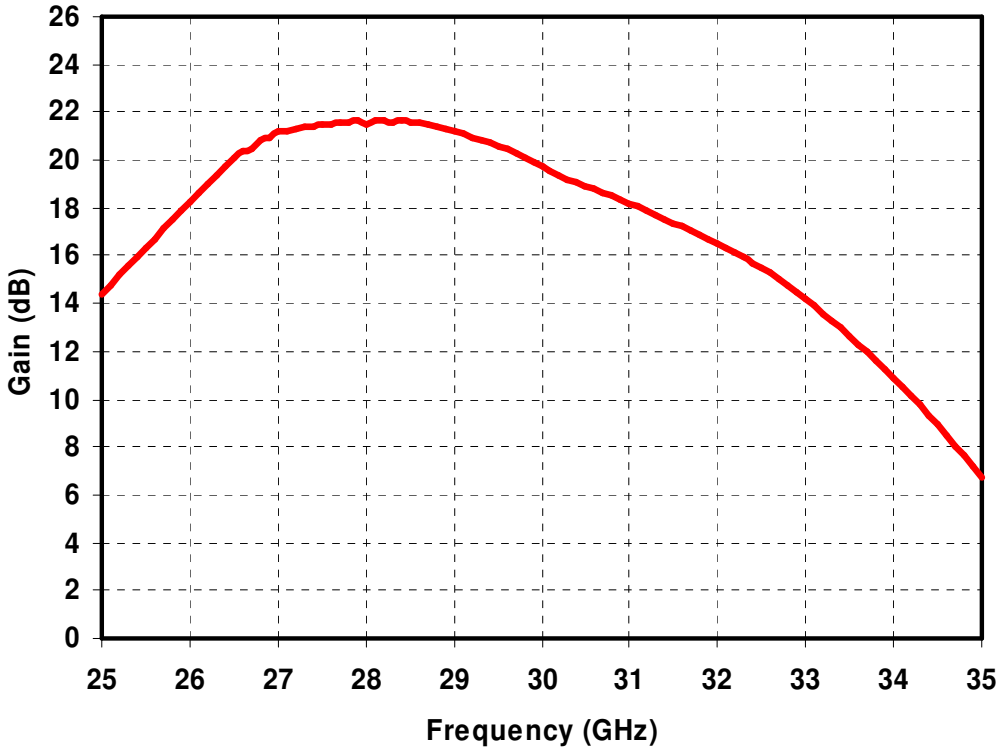
TABLE IV
THERMAL INFORMATION

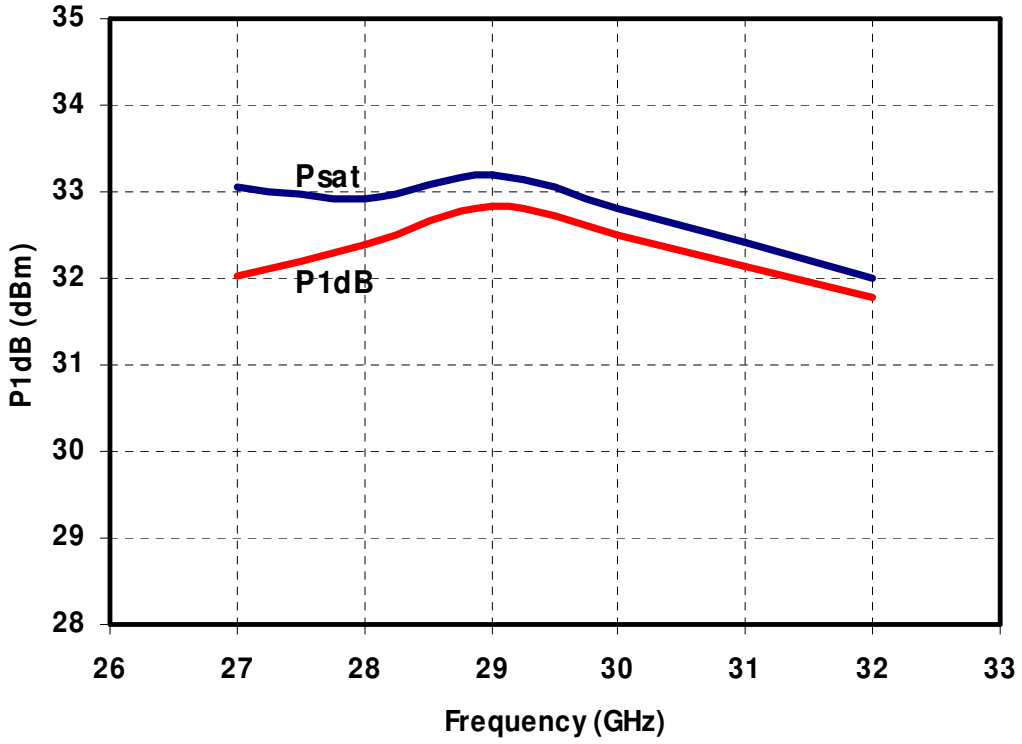
Parameter	Test Conditions	T_{CH} (°C)	θ_{JC} (°C/W)	T_M (hrs)
θ_{JC} Thermal Resistance (Channel Case)	V_D = 6 V I_D = 0.84 A (Quiescent) P_{DISS} = 5.04 W Tbase = 70 °C	130.1	11.92	5.9 E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

Measured Data

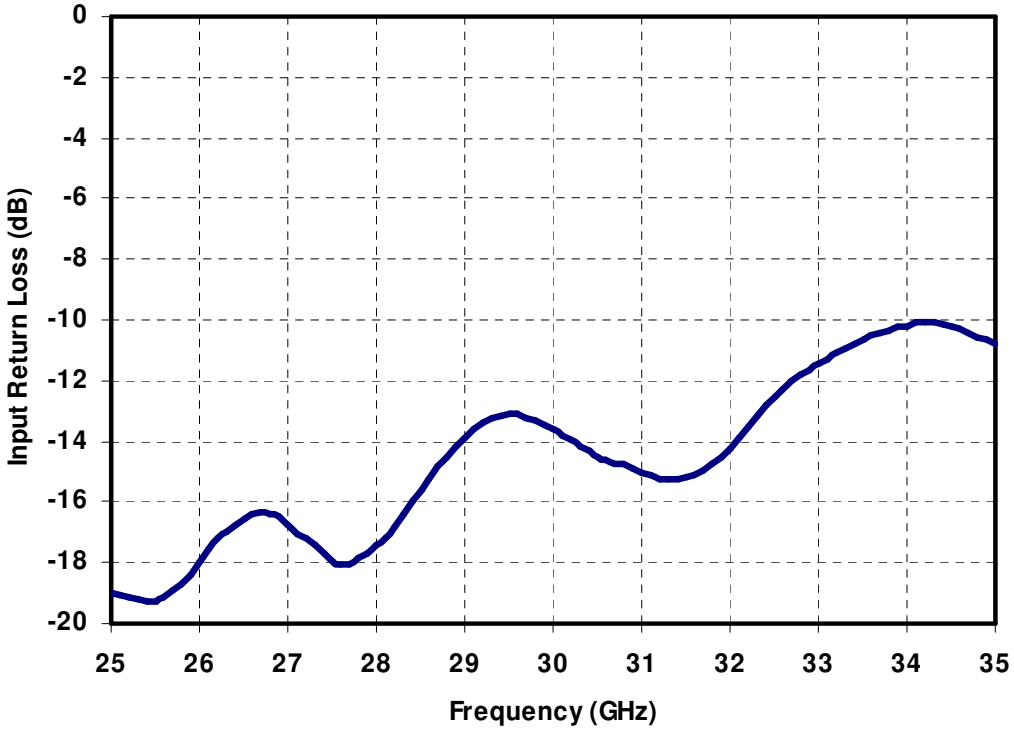
Bias Conditions: Vd = 6 V, Id = 840 mA

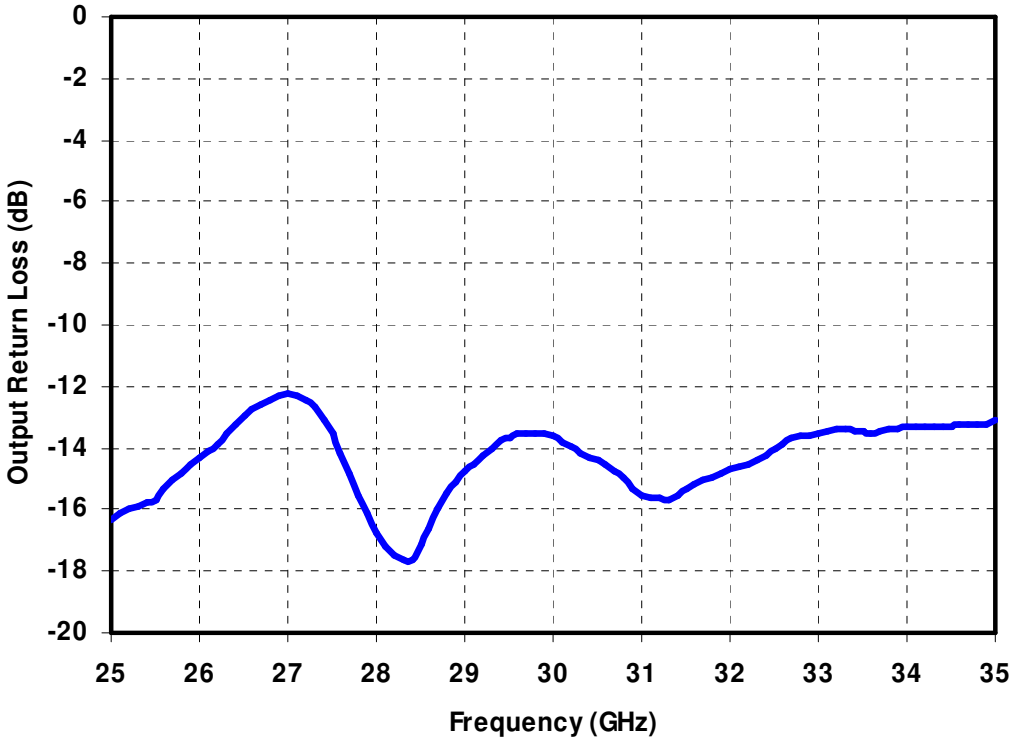




Measured Data

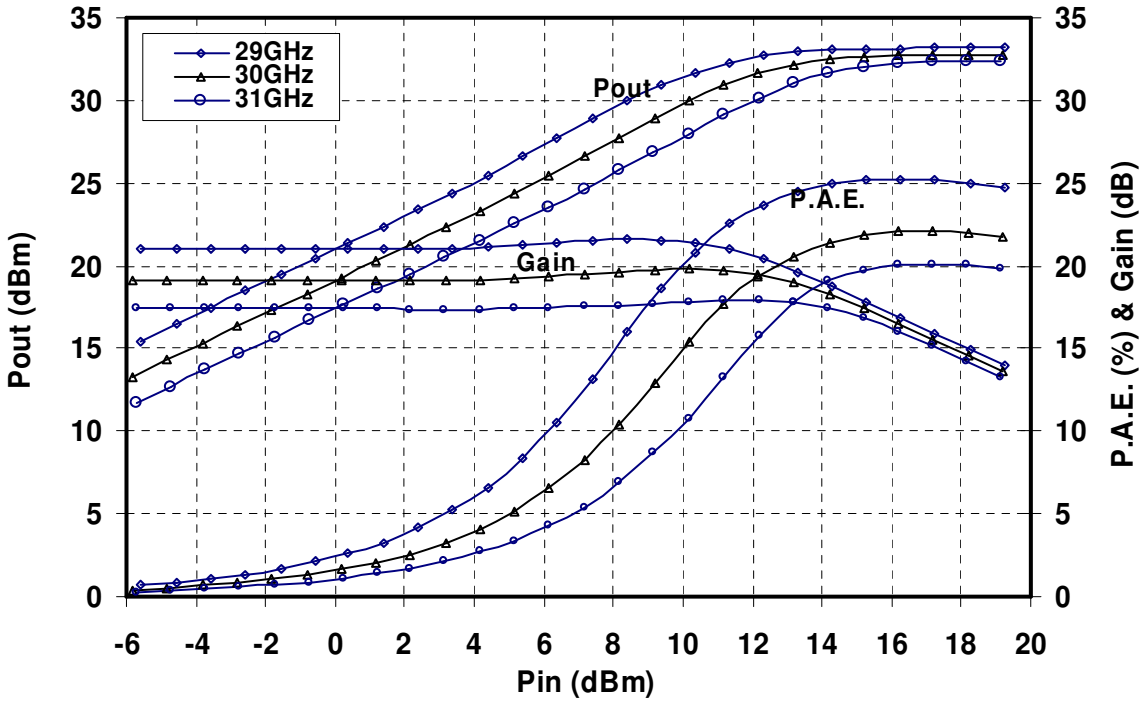
Bias Conditions: Vd = 6 V, Id = 840 mA

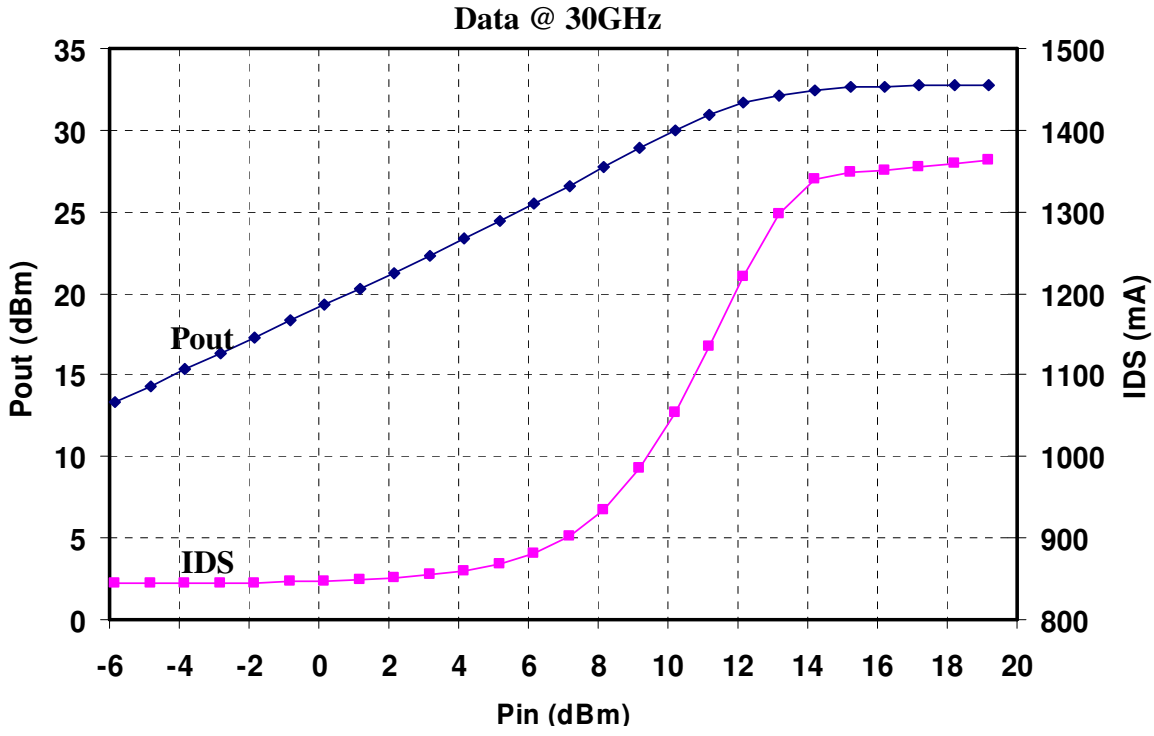




Measured Data

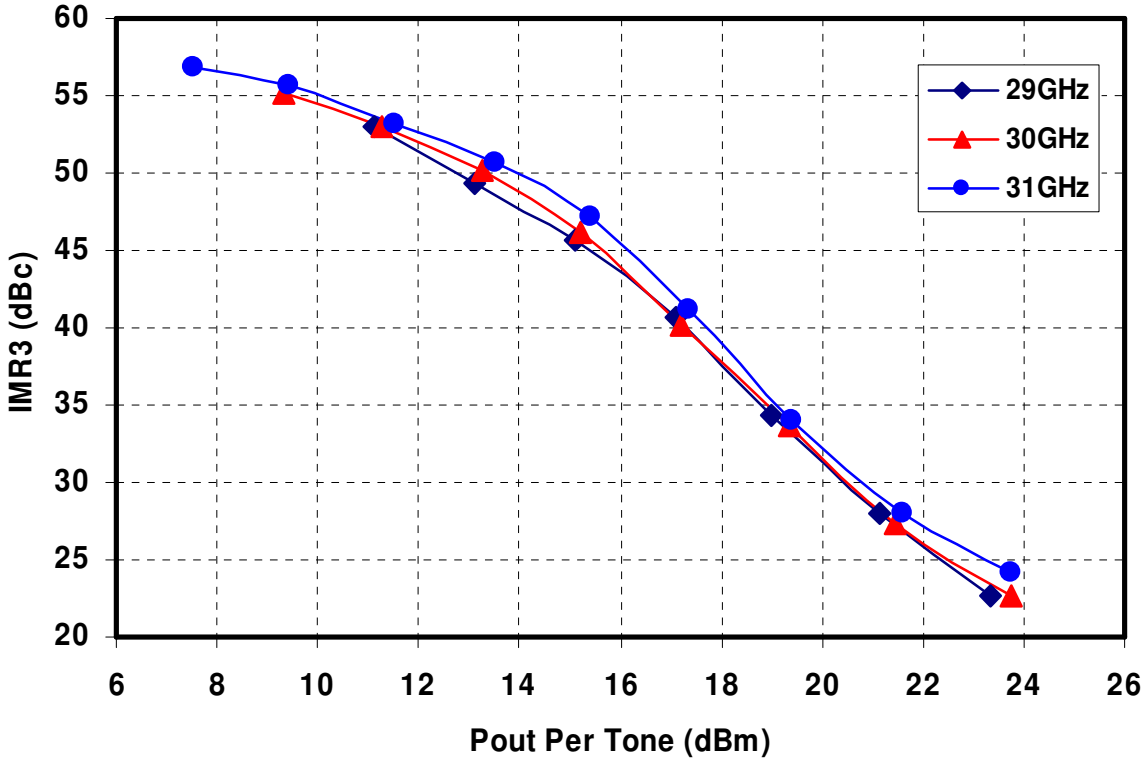
Bias Conditions: Vd = 6 V, Id = 840 mA



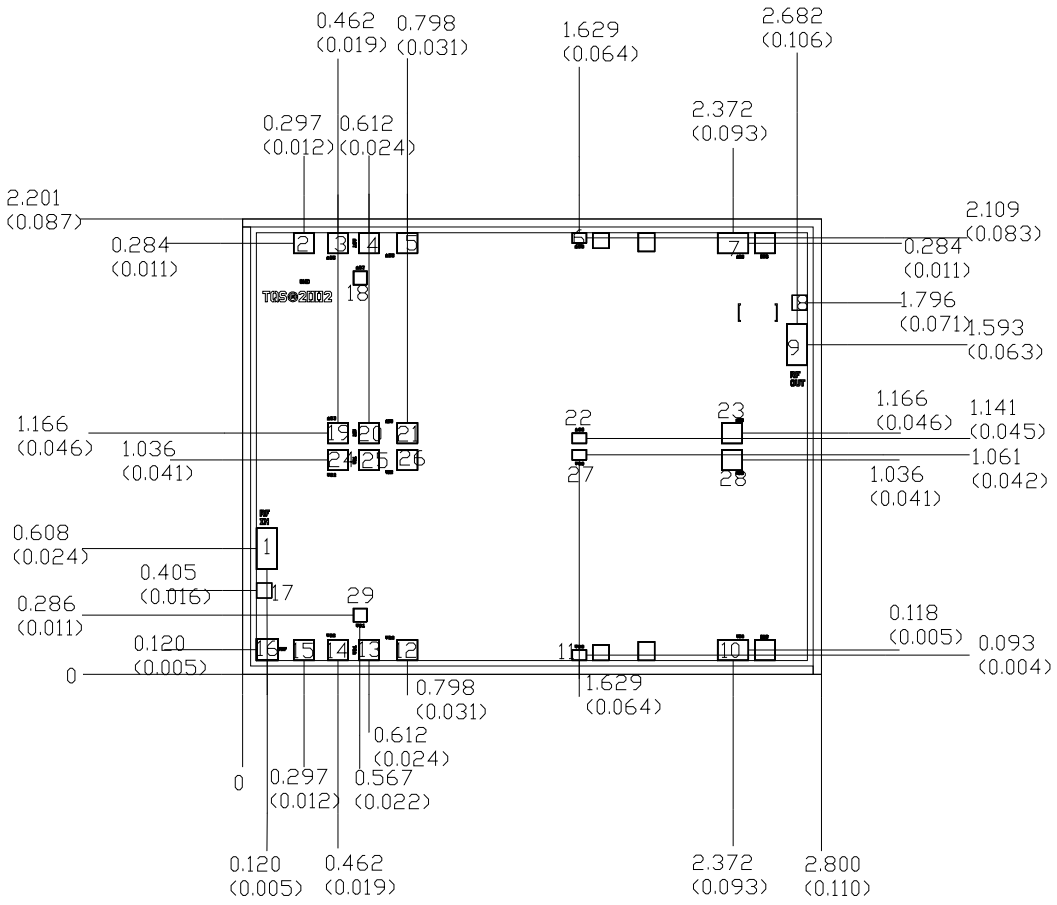


Measured Data

Bias Conditions: Vd = 6 V, Id = 840 mA, Δf = 10 MHz



Mechanical Drawing

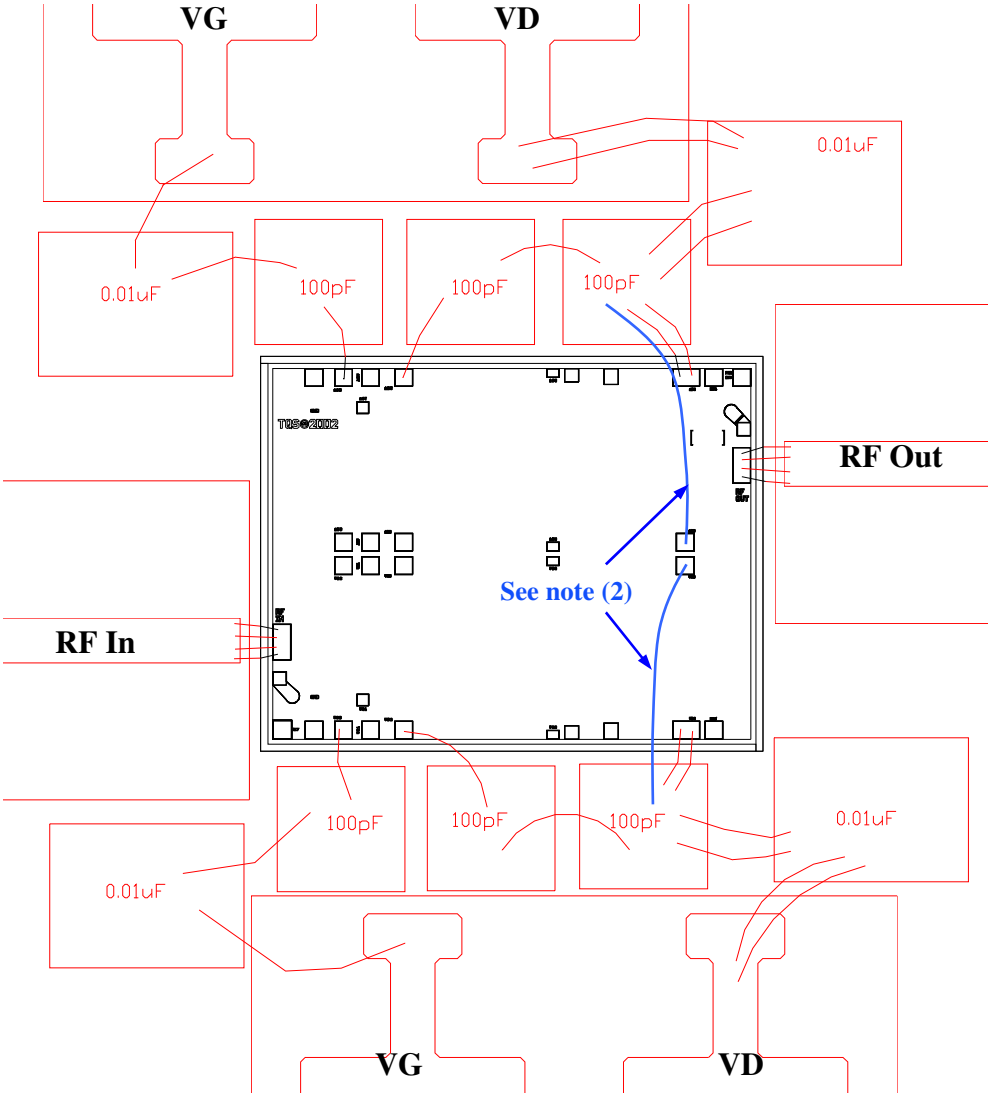


Units: millimeters (inches)
Thickness: 0.100 (0.004)
Chip edge to bond pad dimensions are shown to center of bond pad
Chip size tolerance: +/- 0.051 (0.002)
GND is back side of MMIC

Bond pad #1	RF In	0.100 x 0.200	(0.004 x 0.008)
Bond pad #2, 15, 16	N/C	0.100 x 0.100	(0.004 x 0.004)
Bond pad #3, 14, 19, 24	VG2	0.100 x 0.100	(0.004 x 0.004)
Bond pad #4, 13, 20, 25	VD1	0.100 x 0.100	(0.004 x 0.004)
Bond pad # 5, 12, 21, 26	VD2	0.100 x 0.100	(0.004 x 0.004)
Bond pad # 6, 11, 22, 27	VG3	0.070 x 0.050	(0.003 x 0.002)
Bond pad # 7, 10	VD3	0.150 x 0.100	(0.006 x 0.004)
Bond pad # 8, 17	N/C	0.075 x 0.075	(0.003 x 0.003)
Bond pad # 9	RF Out	0.100 x 0.200	(0.004 x 0.008)
Bond pad # 18, 29	VG1	0.065 x 0.065	(0.003 x 0.003)
Bond pad # 23, 28	VD3	0.100 x 0.100	(0.004 x 0.004)

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Chip Assembly Diagram(1)



Note
(1): Minimum 1 uF bypass Capacitors are required on both drain and gate power supplies.
(2): Alternate configuration without these bondwires: the maximum positive supply current is reduced to 1.3A.

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Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200°C.

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